1. **Hamming code 7-bit circuit**
    - **Verilog Code, IO file declaration and Testbench**

Hamming_Code_7bit.v

C:/Users/user/Desktop/Kaushal_DSD_LAB/GATE_LEVEL_MODELLING/HAMMING_CODE_

```
13  module Hamming_Code_7bit(D,Error,O,EN);
14  input [7:1] D;
15  input EN;
16  output [7:1] O;
17  output Error;
18  wire [4:1] P;
19  wire [7:0] Y;
20  // Detecting error bit
21  xor X_1(P[1],D[1],D[3],D[5],D[7]);
22  xor X_2(P[2],D[2],D[3],D[6],D[7]);
23  xor X_3(P[4],D[4],D[5],D[6],D[7]);
24  // CORRECTION CIRCUIT
25  Decoder_3x8 DEC(Y,P,EN);
26  buf BO_1(Error,~Y[0]);
27  xor XO_1(O[1],Y[1],D[1]);
28  xor XO_2(O[2],Y[2],D[2]);
29  xor XO_3(O[3],Y[3],D[3]);
30  xor XO_4(O[4],Y[4],D[4]);
31  xor XO_5(O[5],Y[5],D[5]);
32  xor XO_6(O[6],Y[6],D[6]);
33  xor XO_7(O[7],Y[7],D[7]);
34  endmodule
35  module Decoder_3x8(Y,I,EN);
36  input [3:0] I;
37  input EN;
38  output [7:0] Y;
39  and a_0(Y[0],~I[3],~I[1],~I[0],EN);
40  and a_1(Y[1],~I[3],~I[1],I[0],EN);
41  and a_2(Y[2],~I[3],I[1],~I[0],EN);
42  and a_3(Y[3],~I[3],I[1],I[0],EN);
43  and a_4(Y[4],I[3],~I[1],~I[0],EN);
44  and a_5(Y[5],I[3],~I[1],I[0],EN);
45  and a_6(Y[6],I[3],I[1],~I[0],EN);
46  and a_7(Y[7],I[3],I[1],I[0],EN);
```

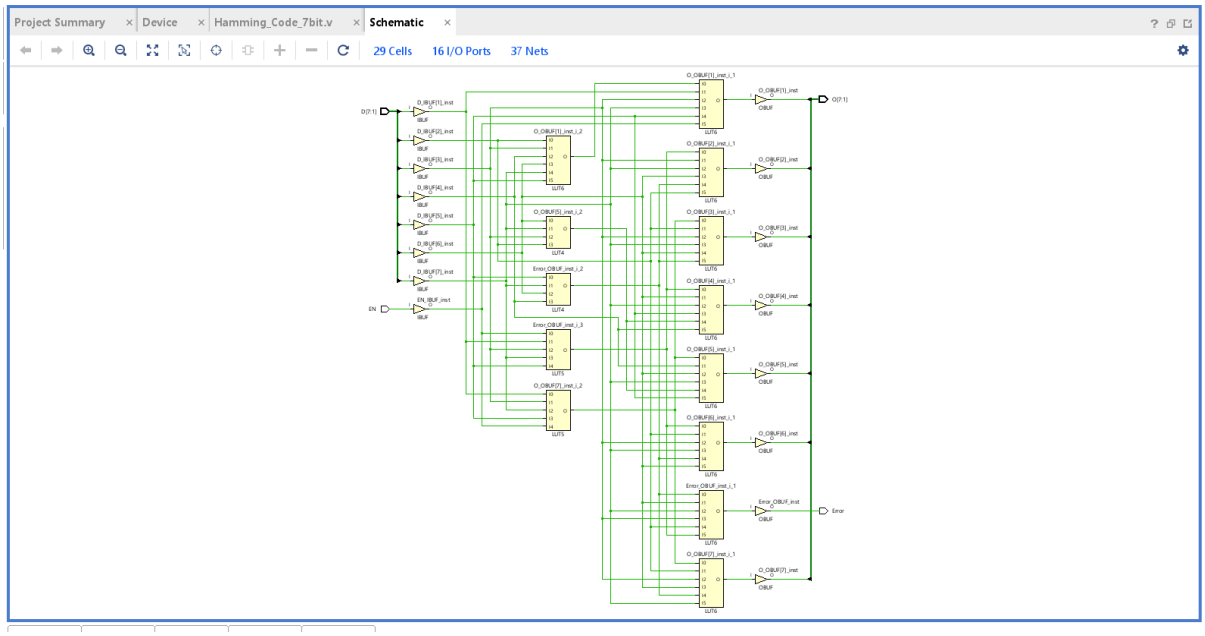
IO_HammingCode

File Edit View

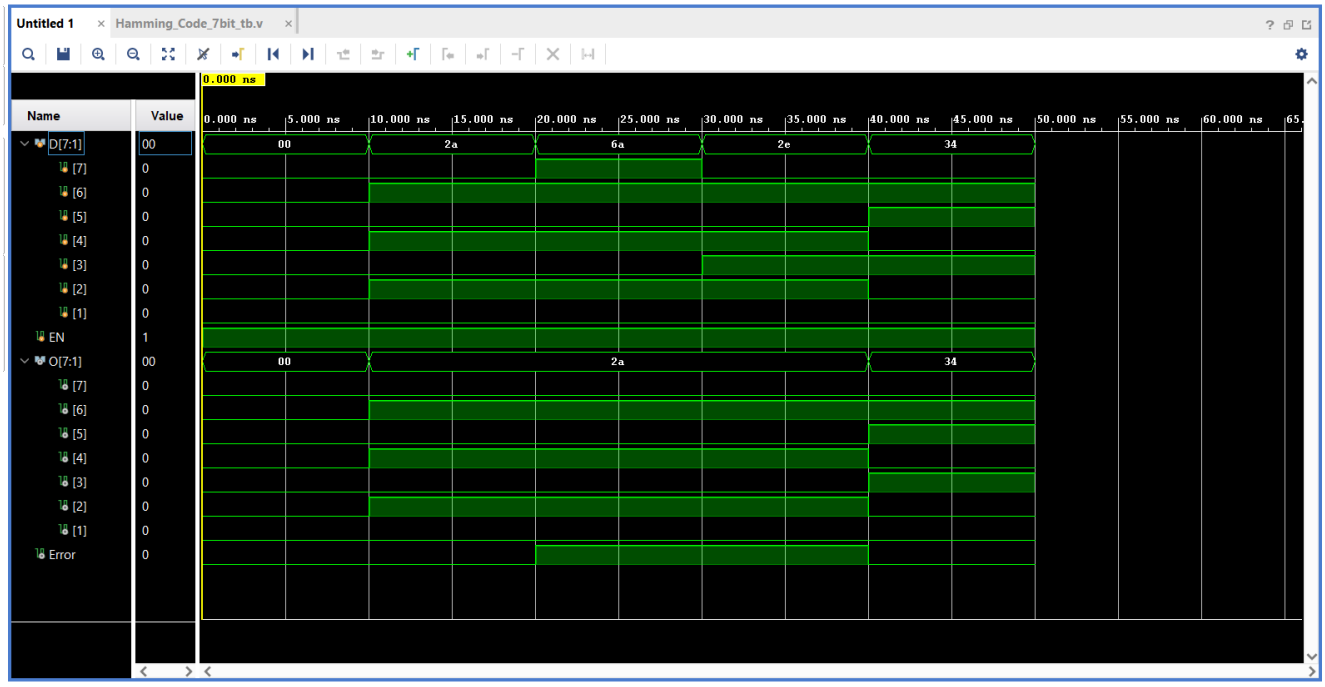
```
set_property IOSTANDARD LVCMOS18 [get_ports EN]
set_property IOSTANDARD LVCMOS18 [get_ports Error]
set_property IOSTANDARD LVCMOS18 [get_ports {D[7]}]
set_property IOSTANDARD LVCMOS18 [get_ports {D[6]}]
set_property IOSTANDARD LVCMOS18 [get_ports {D[5]}]
set_property IOSTANDARD LVCMOS18 [get_ports {D[4]}]
set_property IOSTANDARD LVCMOS18 [get_ports {D[3]}]
set_property IOSTANDARD LVCMOS18 [get_ports {D[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {D[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[7]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[6]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[5]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[4]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[3]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {O[1]}]
set_property PACKAGE_PIN V10 [get_ports EN]
set_property PACKAGE_PIN V11 [get_ports Error]
set_property PACKAGE_PIN J15 [get_ports {D[1]}]
set_property PACKAGE_PIN L16 [get_ports {D[2]}]
set_property PACKAGE_PIN M13 [get_ports {D[3]}]
set_property PACKAGE_PIN R15 [get_ports {D[4]}]
set_property PACKAGE_PIN R17 [get_ports {D[5]}]
set_property PACKAGE_PIN T18 [get_ports {D[6]}]
set_property PACKAGE_PIN U18 [get_ports {D[7]}]
set_property PACKAGE_PIN H17 [get_ports {O[1]}]
set_property PACKAGE_PIN K15 [get_ports {O[2]}]
set_property PACKAGE_PIN J13 [get_ports {O[3]}]
set_property PACKAGE_PIN N14 [get_ports {O[4]}]
set_property PACKAGE_PIN R18 [get_ports {O[5]}]
set_property PACKAGE_PIN V17 [get_ports {O[6]}]
set_property PACKAGE_PIN U17 [get_ports {O[7]}]
```

```
12
13  module Hamming_Code_7bit_tb();
14  reg [7:1] D;
15  reg EN;
16  wire [7:1] O;
17  wire Error;
18
19  Hamming_Code_7bit HM_1(D,Error,O,EN);
20
21  initial
22  begin
23  D = 7'b0000000;
24  EN = 1;
25
26      #10 D = 7'b0101010;
27      #10 D = 7'b1101010;
28      #10 D = 7'b0101110;
29      #10 D = 7'b0110100;
30  end
31
32  initial $monitor ($time, " D = %b, EN = %b, O = %b, Error = %b",D,EN,O,Error);
33  initial #50 $stop;
34
35  endmodule
36
```

- **Synthesis schematic**



Simulation



- **FPGA Implementation**