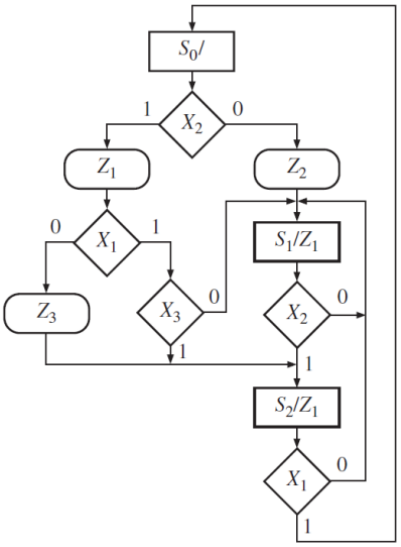
數位系統設計 (Digital System Design)

Homework 3

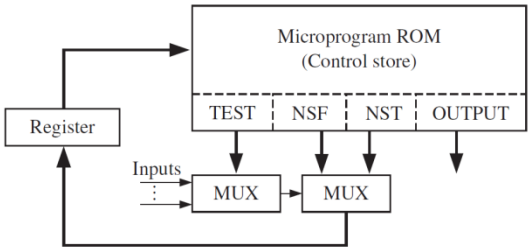
A. Realize the SM chart shown in Figure 1 using a microprogramming structure. The multiplexer inputs are selected as shown in the table beside the SM chart.



TEST	
00	1
01	X_1
10	X_2
11	X_3

Figure 1: An SM chart.

(a) Realize the SM chart using the two-address microprogramming structure. A typical block diagram for microprogramming with a single qualifier per state and two next-state addresses (SQTA) is shown below:



TEST	
00	1
01	X_1
10	X_2
11	X_3

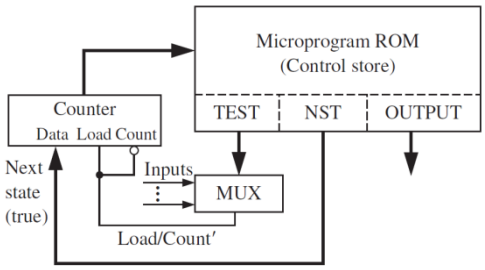
i. Convert the SM chart to the proper form by adding a minimum number of states to the given chart.

ii. Define the format of the two-address control word clearly and write the microprogram, i.e., the ROM table, required to implement the circuit.

iii. What is the size of the ROM (number of words × number of bits per word) required for the two-address microprogramming?

iv. What is the size of the ROM if no microprogram is used but the traditional ROM method (LUT method) is used to implement the original SM chart?

(b) Realize the SM chart using the one-address microprogramming structure. A typical block diagram for microprogramming with a single qualifier per state and one next-state addresses (SQSA) is shown below:



TEST	
00	1
01	X_1
10	X_2
11	X_3

i. Convert the SM chart to the proper form by adding a minimum number of extra states to the chart derived in (a). Make a suitable state assignment.

ii. Define the format of the one-address control word clearly and write the microprogram, i.e., the ROM table, required to implement the circuit.

iii. What is the size of the ROM (number of words × number of bits per word) required for the one-address microprogramming?

(c) Please write the **Verilog circuit module** for the two-address microprogrammed controller derived in (a). The circuit module should be named as *HW3_SQTA_microprogram*, and its file should be named as *HW3_SQTA_microprogram.v* .
The order of the port list of this Verilog module must be *Clk*, *X*1, *X*2, *X*3, *Z*1, *Z*2, *Z*3.

(d) Please write a **test bench** to test the circuit module designed in (c). The testbench module should be named as *t_HW3_SQTA_microprogram*, and its file should be named as *t_HW3_SQTA_microprogram.v* . Start the test from the initial state S0. *Xi* should change 1/4 clock period after the rising edge of the clock. After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.
The test bench should include the following input sequence at least:

Clk	X1	X2	X3
0	1	1	0
1	0	0	0
2	1	0	1
3	0	1	1
4	1	0	0
5	0	1	0
6	1	0	1
7	1	1	1
8	0	0	0

B. Write a behavioral Verilog code for a floating-point multiplier using the IEEE 754 single precision floating-point format. Use an overloaded multiplication operator instead of using an add-shift multiplier. Ignore special cases such as infinity, denormalized, and not-a-number formats. Truncate the final result instead of rounding. Indicate whether the product is overflow or underflow.

(a) Draw the **block diagram** and **SM chart**.

(b) Please write the **Verilog circuit module** for this circuit. The circuit module should be

named as *HW3_FPMUL_754SP*, and its file should be named as *HW3_FPMUL_754SP.v* . The order of the port list of this Verilog module must be *Clk*, *St*, *FPmplier*, *FPmcand*, *Done*, *Ovf*, *Unf*, *FPproduct*.

(c) Please write a **test bench** to test the circuit module designed in (b). The testbench module should be named as *t_ HW3_FPMUL_754SP*, and its file should be named as *t_ HW3_FPMUL_754SP.v* . After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.

The test bench should include the testing of the following inputs (in IEEE 754 single precision format) at least:

0 00110011 10010000000000000000000 × 0 11001100 11001100110011001100110
0 01010101 01010101010101010101010 × 0 11101110 00110011001100110011001
0 11110011 01010101010101010101010 × 1 11001100 11001100110011001100110
1 01110000 10101010101010101010101 × 0 00001111 00001111000011110000111
1 00000101 10101010101010101010101 × 1 00001111 00001111000011110000111
1 00001111 00001111000011110000111 × 1 10011001 10010000000000000000000

◆ 作業及 HDL 模組繳交 (Hand in)

- **作業繳交： word 檔，命名為 HW3_學號_姓名。內容包含下列項目：**
  Submit you homework report in a word file, named HW3_StudentID_Name , including the following items:

  A. i. 繪製 A(a)的 **SM chart**、說明 **two-address control word** 之格式與 **ROM size**、及採傳統 LUT 設計之 **ROM size**。
  For A(a), draw the **modified SM chart** for the two-address microprogramming structure, describe the format of its control word and the ROM size, and the ROM size of the traditional LUT method for implementing the original SM chart.

  ii. 繪製 A(b)的 **SM chart**、說明 **one-address control word** 之格式與 **ROM size**。
  For A(b), draw the **modified SM chart** for the one-address microprogramming structure, and describe the format of its control word and the ROM size.

  iii. 附上 A(d)模擬結果之波型圖，並解釋波形圖是否正確。
  Show the waveform of the simulation results for the circuit module in A(d), and explain whether the results are correct or not.

  B. i. 說明你的設計。繪製 B(a)的**方塊圖**與 **SM chart**。
  Describe your design for Problem B. Draw the **block diagram** and **the SM chart** in B(a).

  ii. 附上 B(c)模擬結果之波型圖，並解釋波形圖是否正確。
  Show the waveform of the simulation results for the circuit module in B(c), and explain whether the results are correct or not.

- **Verilog modules 檔案繳交：Hand in the following Verilog modules**
  HW3_SQTA_microprogram.v

t_ HW3_SQTA_microprogram.v
HW3_FPMUL_754SP.v
t_ HW3_FPMUL_754SP.v

- 助教會使用不同的測試模組來驗證同學的電路模組正確性。
  After you hand in your code, TA will use similar TestBench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

◆ 注意事項與繳交截止日期 (Notes and Deadline)

- 請用 **ModelSim Student Edition 10.4a** 做為開發環境。
  Develop your lab in ModelSim Student Edition 10.4.a.
- 請務必依照各題中之規定命名模組及檔案，並遵循各電路模組之輸出入順序。
  Be sure to name the modules and files and follow the order of the port list as described above.
- 助教會使用不同的測試模組來驗證同學的電路模組正確性。
  After you hand in your code, TA will use similar Testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

A. 本作業為一人一組。請將 Verilog 電路模組(.v)與作業報告 word 檔全部壓縮成一個 **zip** 或 **rar** 檔，命名為「**HW3_學號_姓名**」(如 ： 「**HW3_0616000_王大明**」)，並上傳至 **New e3** 平台。作業報告如為手寫，請務必用深色筆書寫，並確認掃描後檔案清晰易讀。
This homework is one student per group. Please compress the Verilog circuit modules and the word file described above all into one **zip** or **rar** file, name the compressed file as "HW2_StudentID_Name" (for example, "HW2_0616000_Kent Chang"), and upload the compressed file onto e-Campus platform. If your homework report is handwritten, please use the dark colored pen and make sure that it is clearly and legibly after scan.

B. 繳交截止日期為 **2019/12/17 (二) 23:55**。每遲交一天，本作業扣總分 **10%**，至多可遲交四天。
The deadline is **2019/12/17 (Tue.) 23:55.** The penalty of late hand-in is 10% deduction of the total point per day, and four days late at most.

- **禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。**
  Any assignment work by fraud will get a zero point