Neil Deo

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Education

University of Illinois Urbana-Champaign Champaign, IL

Bachelor of Science in Computer Engineering & Minor in Semiconductor Engineering *Aug. 2023 – May 2027*

- **Relevant Coursework**: Computer Organization and Design, Semiconductor Devices, FPGA Systems Laboratory, IC Device Theory & Fabrication, Logic Synthesis, Computer Systems & Programming, Data Structures
- **Scholarships/Honors**: Samsung Semiconductor Scholarship Recipient, James Scholar

Experience

Silimate (YC 2023) June 2025 – August 2025

Hardware Modelling Intern *Mountain View, CA*

- Built novel interpolation algorithms and inference flows to **predict dynamic power** of RTL designs **within 20% of commercial power estimators**
- Developed and deployed a **transistor-based architectural redesign** that **improved model accuracy by over 50%**
- Designed a comprehensive CocoTB verification suite that generated ground-truth power data to rigorously validate model predictions and ensure end-to-end robustness of the power estimation pipeline

ASAP - Center for Advanced Semiconductor Chips August 2025 – Present

Undergraduate Research Assistant *Champaign, IL*

- Worked on **COMSOL** models of solid-state lithium-ion devices to quantify ion transport, producing a reference framework now used by researchers to benchmark custom transport models
- Working under Prof. Shaloo Rakheja to develop **Electrochemical RAM (ECRAM)** simulations to characterize **power consumption and switching energy**, enabling consistent comparison across neuromorphic device designs

Shothawk AI May 2024 – Present

AI Engineering Intern *Peoria, IL*

- Led an architectural shift to a DETR-based weapons-detection model, raising precision from **23.6%** to **80%**, significantly improving detection reliability
- Built a comprehensive and diverse dataset of **100k+ images** by collecting stills, YouTube video frames, and extensive negative samples to reduce false positives
- Improved model tracking performance by roughly **45%** through the integration and optimization of the Norfair tracking library

Projects

FPGA AI Accelerator | *SystemVerilog, Python* March 2025 – May 2025

- **Engineered a custom systolic-array AI accelerator on FPGA**, implementing **FP8** and **BF16** floating-point pipelines for high-throughput matrix computation
- Deployed the DeepTornado neural network onto the accelerator through a **scan-chain weight-loading** architecture and **FIFO-buffered input streaming**, enabling fully in-hardware inference

Out-of-Order RISC-V Processor | *SystemVerilog* September 2025 - Present

- Building an out-of-order RISC-V core with **explicit register renaming**, speculative execution, and an **early branch-recovery mechanism** to reduce misprediction penalties
- Implementing a tournament-style branch predictor that **adaptively selects between a GShare predictor and a two-level predictor** enhancing control-flow accuracy across varied workloads

FPGA CLB Logic Design | *SystemVerilog, C++* August 2024 - November 2024

- Designed and implemented a c**onfigurable logic block (CLB) architecture** inspired by the XC2064 FPGA, supporting a scan-chain programming interface for dynamic reconfiguration
- Built a custom bitstream generation tool in C++ that compiles defined logic into scan-chain data

Technical Skills

Languages: SystemVerilog, Python, Tcl, C/C++, Assembly, Scala, Java
EDA Tools: Verilator, OpenROAD, OpenSTA, yosys, CocoTB, COMSOL, Synopsys VCS, Synopsys Design Compiler
Packages/Developer Tools: PyTorch, LangChain, NumPy, SciPy, pybind11, pyosys, Git, CMake, uv, Meson
Awards: Best Health Hack (UIUC Pulse Overdrive Hardware Hackathon)