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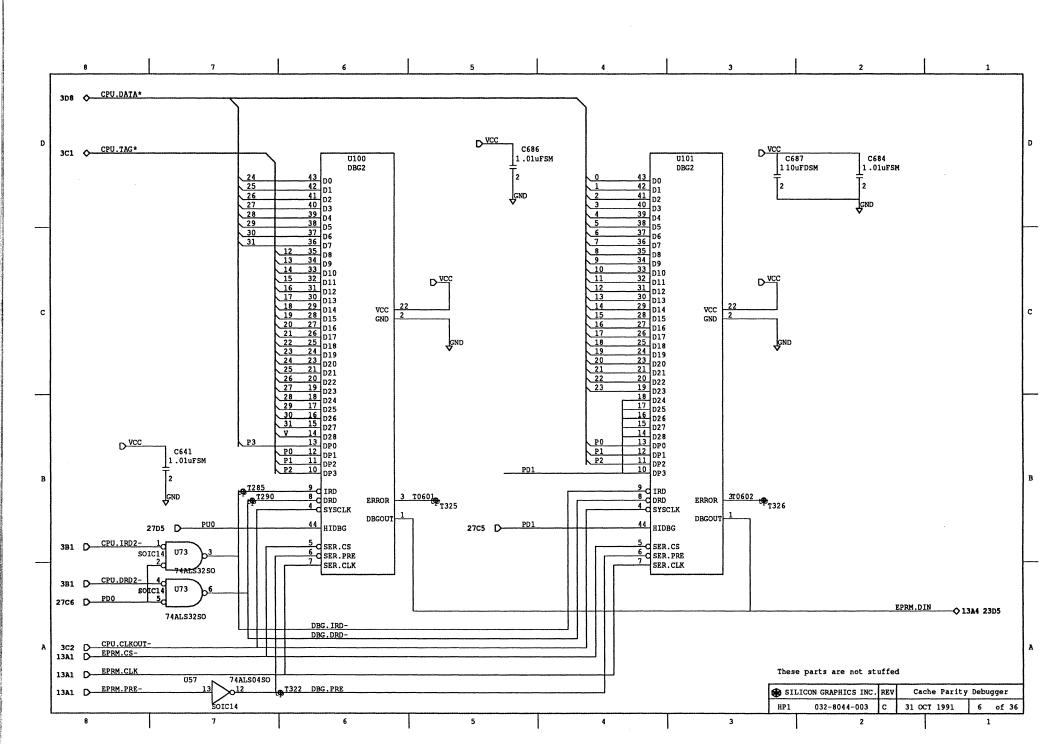
Table of Contents Table of Contents CPU and FPU Cache Blank DBG Read Buffer PIC1 Memory Drivers 10 Main Memory Bank 0 11 Main Memory Bank 1 12 Main Memory Bank 2 13 HPC1 14 EtherNet 15 SCSI & Keyboard/Mouse 16 Boot PROM and RTC 17 Serial Controllers 18 Serial Drivers and Receivers 19 CPU and Peripheral Clocks 20 Printer Port Buffer 21 INT2 22 Graphics Registers 23 Backplane Connector 24 Option Card Connectors 25 Reset, LED, and more... 26 GIO Clocks 27 Pull Ups/Downs and Spares 28 The Terminator 29 Audio Power Supply 30 Audio Analog Output 31 Microphone Input 32 Audio Line In 33 Audio Line Out 34 Audio Digital I/O 35 DSP 36 ACTEL silicon graphics inc. REV Table of Contents 31 OCT 1991 032-8044-003 2 of 36

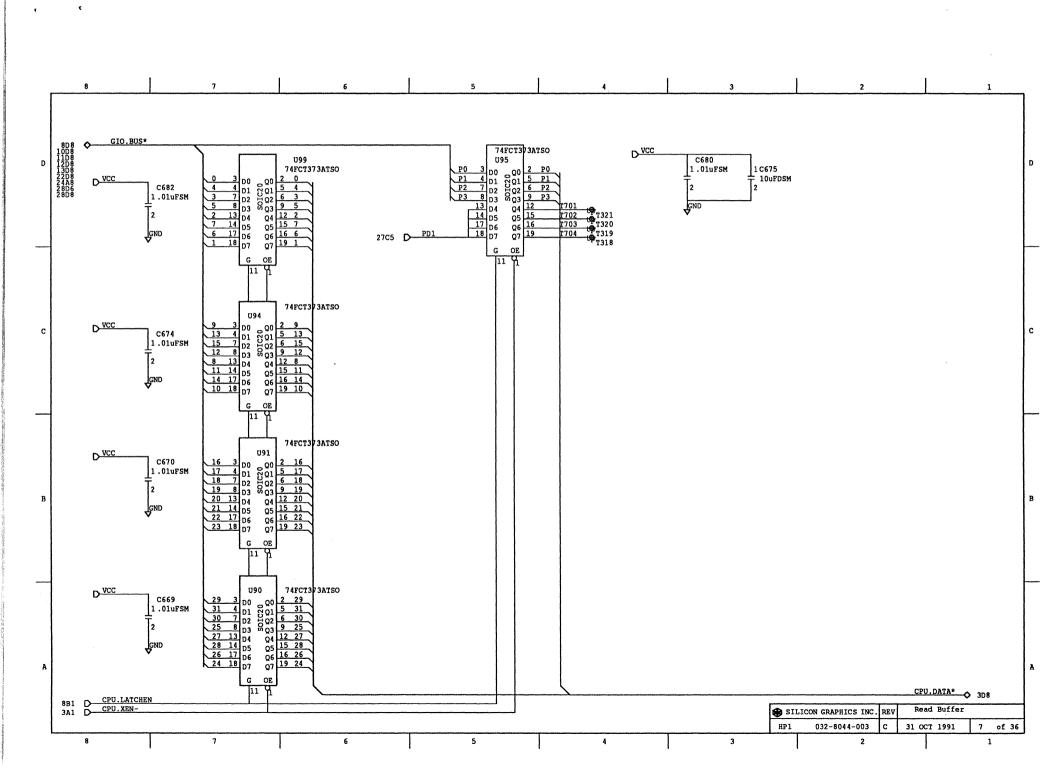
-D 4C8 8D8 ◆ CPU.DATA* CPU . ADDR* E2 D0 D1 D1 F3 D2 E3 A2 G2 D3 G1 D4 A3 D VCC A10 U96 H2 D5 B10 R3010PGA C671 C661 C662 U85 D D1 A5 R3000APGA A6 C683 C677 C676 C10 H1 1 10uFDSM 1 0.1uFSM1 .01uFSM D2 F2 D6 H3 D8 1 10uFDSM | 1 0.1uFSM1.01uFSM B11 lъз B12 D4 J3 D9 A9 B4 D11 D5 A10 A3 10 A11 B5 12 J1 D10 D12 106 E11 K2 D11 GND 107 8 F11 D8 L2 D12 10 F12 D9 M1 D12 D13 D14 A13 B7 13 10 H12 D10 D11 A13 A14 A15 A16 A16 A10 14 K1 D15 CPU.TAG* ♦ 4D8 6D8 8D8 M2 D16 L3 D17 12 J12 13 J11 D12 A17 A10 13 J11 D13 14 L12 D14 15 L11 D15 N2 D18 N3 D19 TAG12 B14 TAG13 C13 D15 P2 D20 D20 D21 D22 D22 16 L4 D16 18 13 TAG14 D13 19 D17 L3 TAG15 B15 18 20 15 D18 K3 D19 P1 D22 N5 D24 E13 16 CPU.CLKOUT-TAG16 -D 6A8 8B8 19D3 С 20 L2 22 TAG17 D14 17 20 <u>D2</u> D20 D21 D21 D22 D23 D23 O3 D25 P5 D26 23 C15 18 TAG18 TAG19 D15 19 P6 D27 TAG20 E14 25 20 CLK* 19C4 D-Q5 D27 Q5 D28 Q7 D29 21 22 24 H1 26 F14 TAG21 D24 G2 D25 TAG22 G14 25 27 P8 D30 TAG23 F15 G1 28 23 E1 D27 D28 D26 Q4 D31 E1 DP0 J2 DP1 M3 DP2 29 30 24 TAG24 TAG25 H14 25 28 TAG26 K15 31 P0 26 27 29 D1 D29 D2 30 D30 31 B2 D31 DP0 N6 DP3 TAG28 J13 P1 28 TAG29 J14 P2 29 P1 M4 DP1 C6 FPINT P3 30 TAG30 P2 H2 DP2 P3 B3 DP3 H2 DP2 L14 31 TAG31 C9 INTRO TAGPO C14 P0 TAGP1 G15 P1 A11 C INTR1 B10 C INTR3 C10 C INTR4 A12 C INTR5 TAGP2 K14 P2 FPCLKIN B9 PLLONB 2XRD FPPRES | L10 CPU.FPPRES- | 8B8 | 8B7 | 25C8 | 8B8 | 8B TAGV N15 EXCEP DL7 CPU.EXCEP A5 2XSMP IRD1 0P12 IRD2 0B6 IWR1 0P13 IWR2 0P3 DRD1 0N11 B2 SMP CPU.IRD1---D 4B8 B7 2XPHI RUN DM9 CPU.RUN CPU.IRD2-PHI —D 6B8 8B8 A7 RESET SYSCLK B5 2XSYS CPU.FPBUSY B11 CPU.IWR1-CPBUSY FPCOND M6 A8 COND 0 COND 1 CPU.FPCOND FPCLK A3 R672 CPU.DRD1-22KSM DRD2 DB2 CPU.DRD2-| DRD2 | —Ď 6A8 CPU.FPCLK CPU.DWR1--D 4B8 CPU.ACCTYPO D 8B8 CPU.WRBUSY-8B1 D CPU.RDBSY CPU.ACCTYP1 D 8B8 CPU.ACCTYP2 D 8B8 8B1 D CPU.BUSERR-25C6 D CPU.RESET-B12 A14 Q10 P9 P9 2XSYS Q9 P10 P10 2XRD MEMRD ON13 MEMWR ON12 CPU.MEMRD- D 8B8 CPU.MEMWR-—Ď 8B8 MEMWR DETE XEN DP7 RUN DN14 EXCEP DQ8 CLK DQ11 CLK DQ13 SMP CPU.XEN-SYS CPU.INT*-21C1 25C6 25C8 **0**-CPU.CPCOND0 A ICLK 013 DCLK P11 CPU. ICLK -D 4A8 CPU.DCLK P14 CPSYNC -D 4A8 25B3 CPU.FPSYNC CPU and FPU silicon graphics inc. Rev 032-8044-003 31 OCT 1991 3 of 36 3

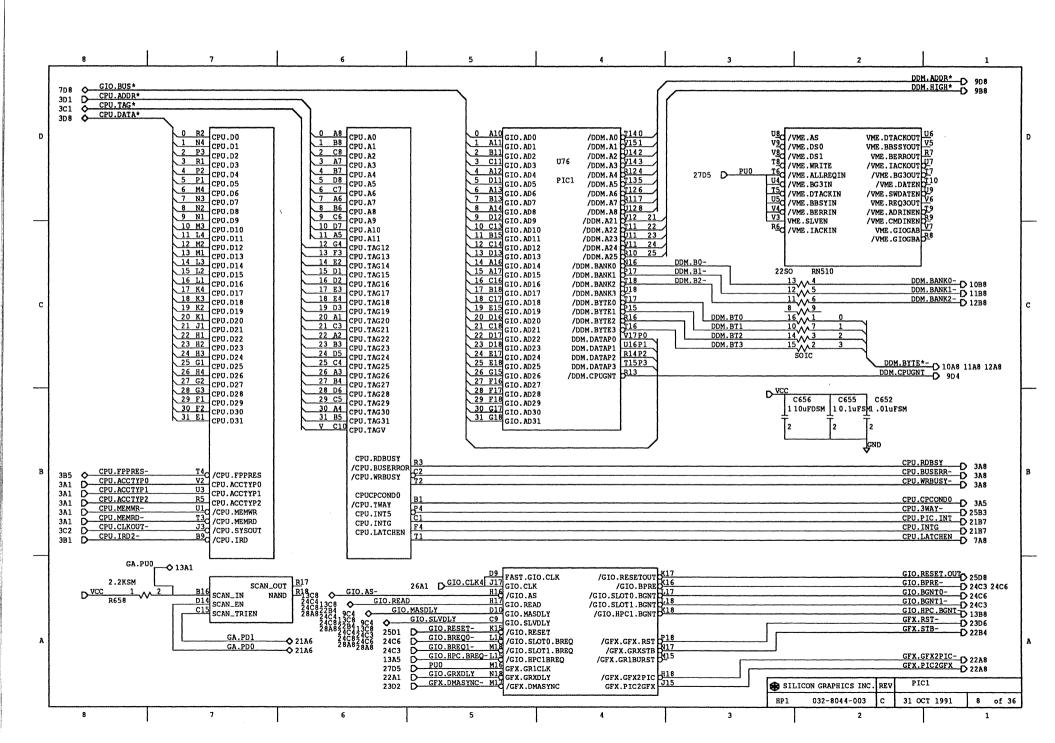
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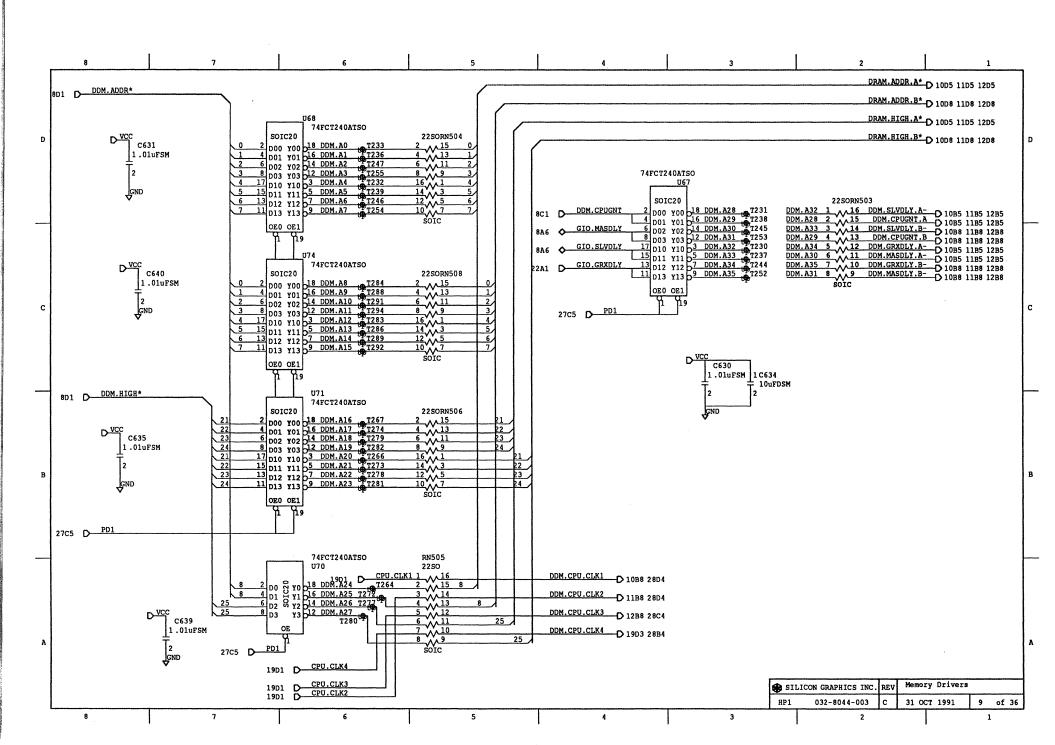
D VCC C32 C33 3C1 ♦ CPU.TAG* 1 4700pFSM 1 4700pFSM 1 4700pFSM 1 4700pFSM 1 4700pFSM 3D8 CPU.DATA* GND 20 11 D0 21 12 D1 22 13 D2 23 15 D3 U86 24 16 D4 8Kx20x2.52PL 25 17 D5 12 D0 13 D1 15 D2 13 12 D1 14 13 D2 15 15 D3 U97 16 16 D4 8Kx20x2.52PL U87 17 D5 8Kx20x2.52PL 6 18 D6 D7 17 17 D5 18 18 D6 19 20 D7 20 21 D8 21 22 D9 22 32 D10 23 33 D11 D5 25 17 D5 26 18 D6 27 20 D7 28 21 D8 29 22 D9 8 21 D8 9 22 D9 29 22 D9 30 32 D10 31 33 D11 P0 34 D12 P1 36 D13 P2 37 D14 P3 38 D15 10 32 D10 11 33 D11 12 34 D12 24 34 25 36 D12 13 36 D13 D13 14 37 D14 D15 D16 D16 26 37 D14 27 38 D15 39 D16 28 39 17 42 D17 D18 D19 D19 D16 P1 P2 V 42 D17 29 42 D17 30 43 D18 31 44 D19 43 D18 3D1 D CPU. ADDR* 44 D19 D19 AΩ ΑO AΩ 8 8 A1 A1 A1 7 A2 A2 A2 A3 A3 A3 5 5 A4 A4 A4 4 A5 A5 A5 3 A6 A6 A6 51 50 51 50 A7 A7 A7 A8 A8 A8 49 49 49 A9 A9 A9 48 48 48 A10 A10 A10 47 47 47 A11 A11 A11 46 46 46 A12 A12 A12 CE CE 25B1 D GATED.3WAY-31 30 /CE /CE /CE 27C6 D PD0 30 30 25 /OEA /OEB 25 /OL.. 28 /OEB 25 /OL.. 28 /OEB CPU.IRD1-3B1 D CPU.DRD1-24 /WA 29 /WB 24d /WA CPU.IWR1-3B1 D-/WA 3B1 D CPU.DWR1-29 /WB /WB CPU.ICLK LEA LEA LEA 3A1 D CPU.DCLK 52 LEB 52 52 LEB LEB C666 C660 C664 C665 C659 C663 C681 C679 C678 1 10uFDSM 1 0.1uFSM1 .01uFSM 1 10uFDSM | 10.1uFSM .01uFSM 1 10uFDSM | 1 0.1uFSM .01uFSM GND Cache SILICON GRAPHICS INC. REV 032-8044-003 31 OCT 1991 4 of 36 8 7 6 5 4 3 1

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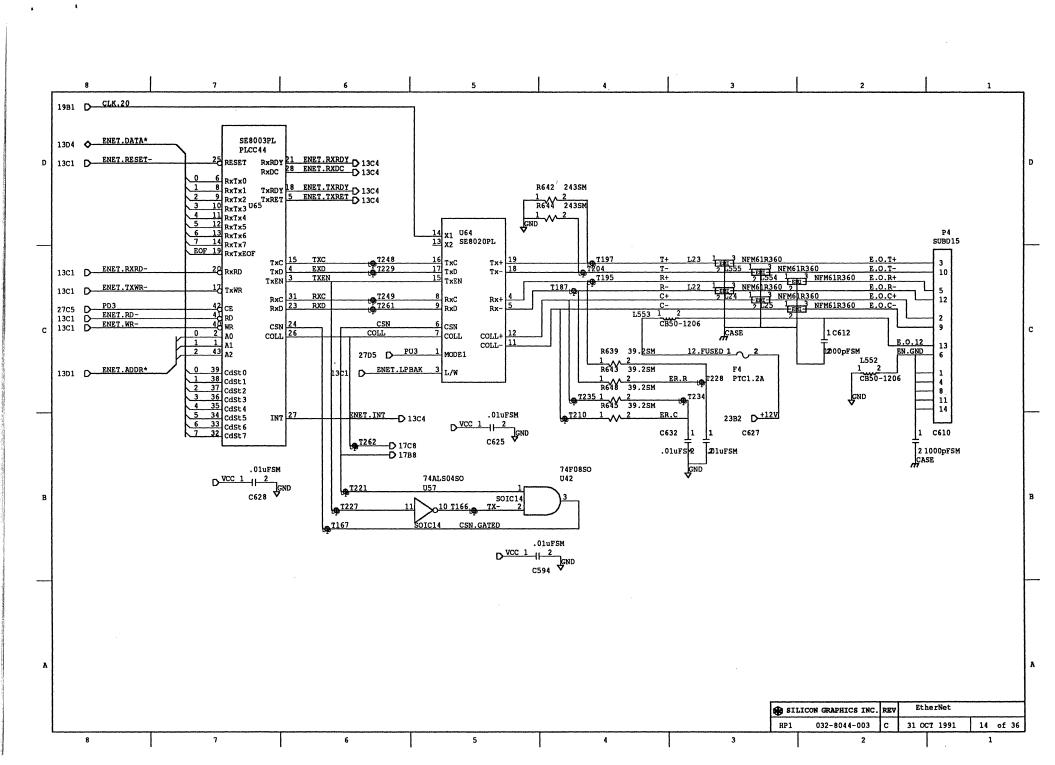
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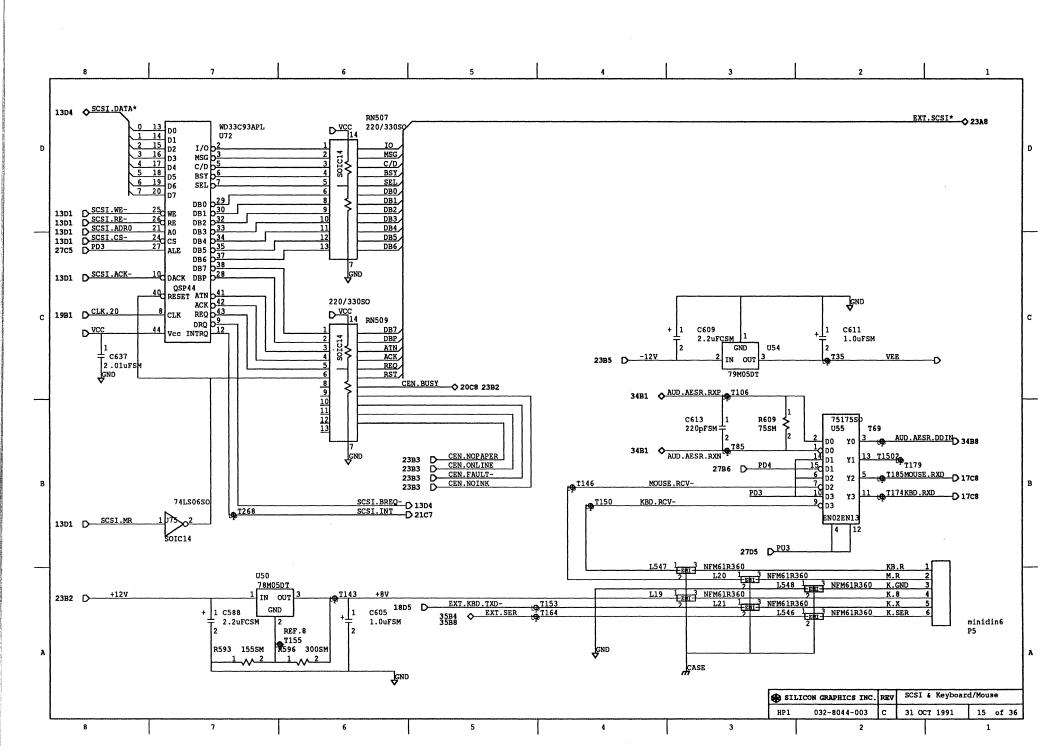
7D8 GIO.BUS* 9D1 D DRAM.ADDR.B* 9D1 D DRAM, ADDR. A* 9D1 D DRAM.HIGH.B* 9D1 D DRAM.HIGH.A* D VCC D VCC D vcc D VCC S4A S1A S2A S3A simm simm VCC 18 VCC 18 VCC 18 VCC 18 GIO D7 GIO D7 GIO D7 GIO D7 VCC 46 6 11 VCC 46 14 11 VCC 46 22 11 VCC 46 30 11 GIO D6 GIO D6 GIO D6 GIO D6 VCC 62 13 13 21 13 29 13 VCC 62 GIO D5 GIO D5 GIO D5 GIO D5 15 20 15 19 49 15 28 GIO D4 GIO D4 GIO D4 GIO D4 27 49 49 3 49 11 GIO D3 GIO D3 GIO D3 GIO D3 18 51 17 53 16 55 P2 7 2 51 51 26 51 GIO D2 GIO D2 GIO D2 GIO D2 25 53 24 55 1 53 53 GIO D1 GIO D1 GIO D1 GIO D1 0 55 GIO DO 55 GIO DO GIO DO GIO DO C587 P3 7 P07 GIO Par GIO Par GIO Par GIO Par 1 10uFDSM DRAM A8 DRAM A8 DRAM A8 DRAM A8 21 21 DRAM A7 DRAM A7 DRAM A7 DRAM A7 23 23 GND 23 23 DRAM A6 DRAM A6 DRAM A6 DRAM A6 27 27 27 27 DRAM A5 DRAM A5 DRAM A5 DRAM A5 29 29 29 29 DRAM A4 DRAM A4 DRAM A4 DRAM A4 31 31 31 DRAM A3 DRAM A3 DRAM A3 DRAM A3 37 37 37 37 DRAM A2 DRAM A2 DRAM A2 DRAM A2 39 39 39 39 DRAM A1 DRAM A1 DRAM A1 DRAM A1 41 41 41 41 DRAM AO DRAM AO DRAM AO DRAM AO 56 57 56 56 57 56 HIGH A25 HIGH A25 HIGH A25 HIGH A25 24 57 24 HIGH A24 HIGH A24 HIGH A24 HIGH A24 59 59 59 59 HIGH A23 HIGH A23 HIGH A23 HIGH A23 22 61 61 22 61 HIGH A22 HIGH A22 HIGH A22 HIGH A22 63 63 63 HIGH A21 HIGH A21 HIGH A21 HIGH A21 9D1 D DDM.CPUGNT.A DDM.CPUGNT.B CPU Gnt CPU Gnt CPU Gnt CPU Gnt 8C1 D DDM.BANKO-/Bank Sel /Bank Sel /Bank Sel /Bank Sel /Byte Sel /Byte Sel /Byte Sel /Byte Sel 9D1 D DDM.SLVDLY.A-DDM.SLVDLY.B-√GIO SlvDly /GIO SlvDly /GIO SlvDly /GIO SlvDly D DDM.MASDLY.A-47 D DDM.MASDLY.B-47 d 47 d /GIO MasDly 9C1 9C1 /GIO MasDly /GIO MasDly /GIO MasDly d /GIO GRXDly 17 d DDM.GRXDLY.A-17 DDM.GRXDLY.B-/GIO GRXD1 9C1 D-GIO GRXD1y /GIO GRXD1 GIO.RESET-25D1 D DDM.CPU.CLK1 d /Reset /Reset /Reset /Reset 35 33 35 35 33 35 9A4 CPU Clk CPU Clk CPU Clk CPU Clk D GIO.CLK1 33 33 26B1 GIO Clk GIO Clk GIO Clk GIO Clk GND C1001 1 18pF 12 36 6 36 6 GND 140 10 12 14 16 20 22 24 26 10 10 40 10 GND GND GND GND GND GND GND GND 12 12 14 12 GND GND GND GND GND GND GND GND 14 44 GND GND GND GND GND GND GND GND 16 20 22 24 16 16 20 48 GND GND GND GND GND GND GND GND 20 22 24 26 50 50 GND GND GND GND GND GND GND GND 52 54 58 60 DDM.BYTE*-22 GND GND GND GND GND GND GND GND 24 54 8C1 D GND GND GND GND GND GND GND CND 26 28 30 26 GND GND GND GND GND GND GND GND 28 30 28 60 28 60 64 GND GND GND GND GND GND GND GND 30 GND GND GND GND GND GND GND GND Note: Parity bits are little endian to support MIPS notation Byte ordering is big endian Main Memory Bank 0 SILICON GRAPHICS INC. REV 032-8044-003 31 OCT 1991 10 of 36

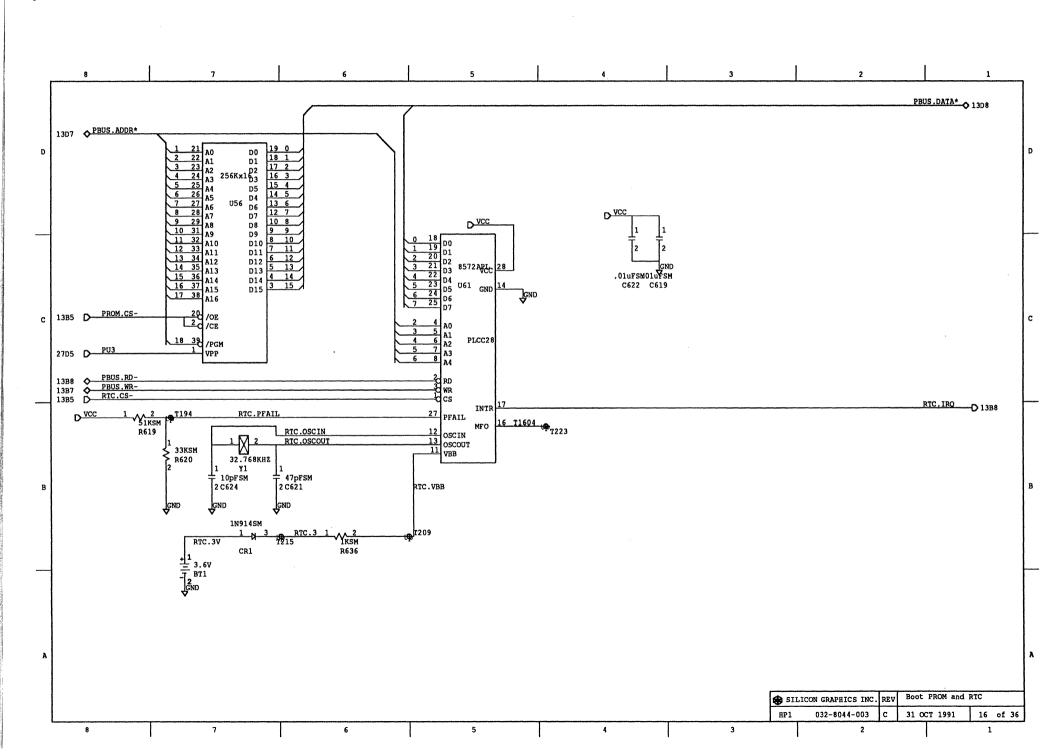
7D8 GIO.BUS* 9D1 D DRAM. ADDR. A* DRAM.ADDR.B* DRAM.HIGH.B* DRAM.HIGH.A* 9D1 D-9D1 D-D VCC D VCC D VCC D VCC S1B S2B S3B S4B simm simm VCC simm VCC simm VCC VCC 18 VCC 18 GIO D7 GIO D7 GIO D7 GIO D7 6 11 VCC 46 VCC 46 VCC 46 30 11 VCC 46 GIO D6 GIO D6 GIO D6 GIO D6 5 13 VCC 62 13 13 VCC 62 VCC 62 29 13 VCC 62 GIO D5 GIO D5 GIO D5 GIO D5 20 15 19 49 28 15 27 49 4 15 15 GIO D4 GIO D4 GIO D4 GIO D4 3 49 49 GIO D3 GIO D3 GIO D3 GIO D3 2 51 51 18 51 26 51 GIO D2 GIO D2 GIO D2 1 53 GIO D1 GIO D2 53 55 17 53 25 53 GIO D1 GIO D1 GIO D1 16 55 0 55 24 55 GIO DO GIO DO GIO DO GIO DO P07 7 P2 7 P3 7 GIO Par GIO Par GIO Par GIO Par DRAM A8 DRAM A8 DRAM A8 DRAM A8 21 21 C653 DRAM A7 DRAM A7 DRAM A7 DRAM A7 1 10uFDSM 23 23 23 23 DRAM A6 DRAM A6 DRAM A6 DRAM A6 27 27 27 27 DRAM A5 DRAM A5 DRAM A5 DRAM A5 29 29 29 29 DRAM A4 DRAM A4 DRAM A4 DRAM A4 31 37 31 31 GND DRAM A3 DRAM A3 DRAM A3 DRAM A3 37 37 37 DRAM A2 DRAM A2 DRAM A2 DRAM A2 39 39 39 DRAM A1 DRAM A1 DRAM A1 DRAM A1 41 41 41 41 DRAM AO DRAM AO DRAM AO DRAM AO 56 57 56 57 <u>56</u> 57 56 57 HIGH A25 HIGH A25 HIGH A25 HIGH A25 24 23 22 HIGH A24 HIGH A24 HIGH A24 HIGH A24 59 59 59 HIGH A23 HIGH A23 HIGH A23 HIGH A23 61 61 61 61 HIGH A22 HIGH A22 HIGH A22 HIGH A22 63 63 63 63 HIGH A21 HIGH A21 HIGH A21 HIGH A21 9D1 D DDM.CPUGNT.A DDM.CPUGNT.B CPU Gnt CPU Gnt CPU Gnt CPU Gnt 8C1 D DDM.BANK1-/Bank Sel /Bank Sel /Bank Sel /Bank Sel /Byte Sel /Byte Sel /Byte Sel /Byte Sel 9C1 D DDM.SLVDLY.B-9C1 D DDM.MASDLY.B-9D1 DDM.SLVDLY.A-9C1 DDM.MASDLY.A-/GIO SlvDl GIO SlvDly 45 d /GIO SlvDly 47 0 /GIO MasDly /GIO SlvDly 47 GIO MasDly 17 GIO GRXDly 47 9C1 /GIO MasDly 9C1 D DDM.GRXDLY.A-17 d /GIO GRXDly DDM.GRXDLY.B-17 /GIO GRXDly GIO.RESET-/Reset /Reset /Reset /Reset 35 33 DDM.CPU.CLK2 35 35 33 D-9A4 CPU Clk CPU Clk CPU Clk CPU Clk D GIO.CLK2 33 33 26B1 GIO Clk GIO Clk GIO Clk GIO Clk GND 34 36 GND GND GND GND GND GND GND GND GND 6 6 GND GND GND GND GND GND GND GND 8 10 12 14 16 20 22 24 26 28 30 GND GND GND GND GND GND 10 10 12 GND GND GND GND GND GND GND GND 12 14 GND GND GND GND GND GND GND GND GND 14 16 20 22 24 GND GND GND GND GND GND GND 16 20 48 GND GND GND GND GND GND GND GND 20 50 50 50 GND GND GND GND GND GND GND GND GND DDM.BYTE*-52 54 22 24 GND GND GND GND GND GND GND 24 8C1 D GND GND GND GND GND GND GND GND 58 26 26 26 GND GND GND GND GND GND 28 GND GND 60 64 28 30 28 60 GND GND GND GND GND GND GND GND 30 64 GND Note: Parity bits are little endian to support MIPS notation Byte ordering is big endian SILICON GRAPHICS INC. REV Main Memory Bank 1 032-8044-003 31 OCT 1991 11of 36

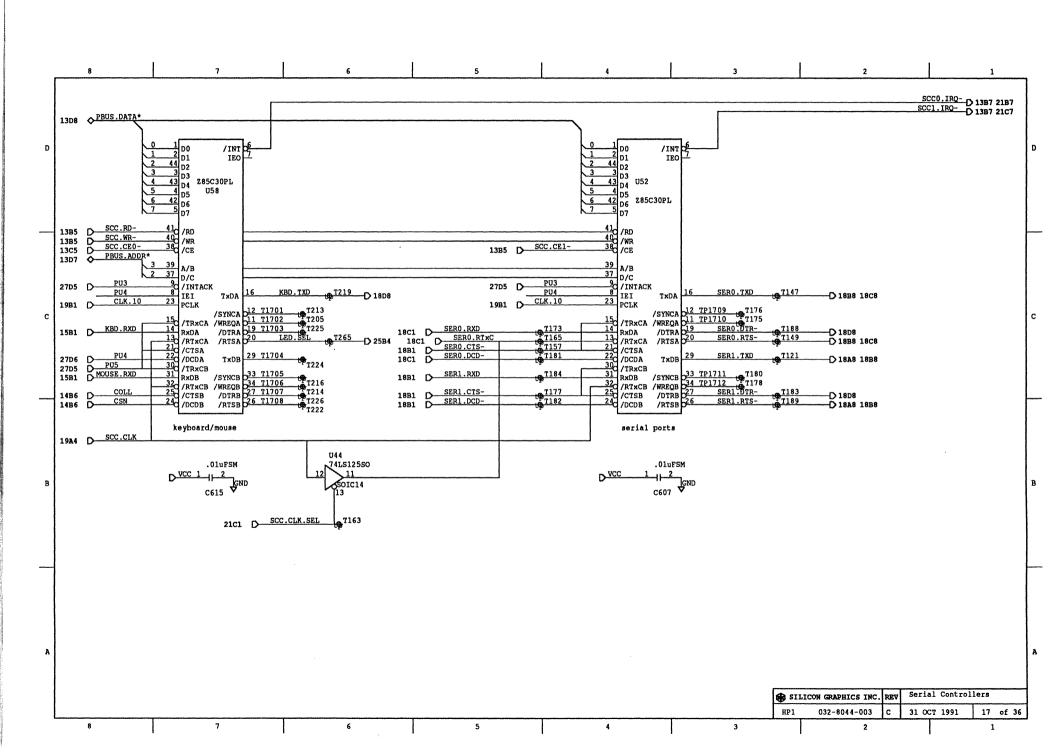
7D8 O GIO.BUS* 9D1 D DRAM. ADDR. A* DRAM.ADDR.B* 9D1 D DRAM.HIGH.B* 9D1 D DRAM.HIGH.A* D VCC D VCC D ACC D VCC S3C S1C S2C S4C simm simm VCC simm VCC VCC 18 VCC 18 VCC 18 VCC GIO D7 GIO D7 GIO D7 GIO D7 VCC 46 14 11 VCC 22 11 VCC 46 30 11 VCC 46 GIO D6 GIO D6 GIO D6 GIO D6 13 13 13 29 13 VCC 62 VCC 62 VCC 62 GIO D5 GIO D5 GIO D5 GIO D5 4 15 12 15 20 15 28 15 GIO D4 GIO D4 GIO D4 GIO D4 3 49 11 49 19 49 27 49 GIO D3 GIO D3 GIO D3 GIO D3 10 51 18 51 26 51 GIO D2 GIO D2 GIO D2 GIO D2 53 55 1 53 9 17 53 25 53 GIO D1 GIO D1 GIO D1 GIO D1 0 55 GIO DO 8 16 55 24 55 GIO DO GIO DO GIO DO P1 7 P2 7 P3 7 P07 GIO Par GIO Par GIO Par GIO Par C654 DRAM A8 DRAM A8 DRAM A8 DRAM A8 21 21 1 10uFDSM DRAM A7 DRAM A7 DRAM A7 DRAM A7 23 23 23 23 DRAM A6 DRAM A6 DRAM A6 DRAM A6 27 27 27 27 DRAM A5 DRAM A5 DRAM A5 DRAM A5 29 29 29 GND 29 DRAM A4 DRAM A4 DRAM A4 DRAM A4 31 31 31 31 DRAM A3 DRAM A3 DRAM A3 DRAM A3 37 37 DRAM A2 DRAM A2 DRAM A2 DRAM A2 39 39 DRAM A1 DRAM A1 DRAM A1 DRAM A1 41 41 41 DRAM AO DRAM AO DRAM AO DRAM AO 56 57 56 57 56 HIGH A25 HIGH A25 HIGH A25 HIGH A25 24 24 HIGH A24 HIGH A24 HIGH A24 HIGH A24 59 59 59 HIGH A23 HIGH A23 HIGH A23 HIGH A23 22 61 61 22 61 61 HIGH A22 HIGH A22 HIGH A22 HIGH A22 63 63 63 HIGH A21 HIGH A21 HIGH A21 HIGH A21 9D1 D DDM.CPUGNT.A DDM.CPUGNT.B 9C1 D-CPU Gnt CPU Gnt CPU Gnt CPU Gnt 8C1 D DDM.BANK2-3_ /Bank Sel /Bank Sel /Bank Sel /Bank Sel 5 /Byte Sel /Byte Sel /Byte Sel /Byte Sel 45 d /GIO SlvDly 45 d /GIO SlvDly /GIO MasDly 9C1 D DDM.SLVDLY.B-/GIO SlvDly 9D1 DDM.MASDLY.A- 47 GIO S1vDly
9C1 DDM.COVDLY A- 17 GIO MasDly 47 C /GIO MasDly D DDM.GRXDLY.B-9C1 D DDM.GRXDLY.A-17 17 17.7 /GIO GRXDly /GIO GRXDly /GIO GRXDly /GIO GRXDly GIO.RESET-D-/Reset /Reset /Reset D DDM.CPU.CLK3 35 35 35 35 ` CPU Clk CPU C1k CPU Clk CPU C1k D GIO.CLK3 33 33 33 33 26A1 GIO Clk GIO Clk GIO Clk GIO Clk GND 6 36 36 GND GND GND GND GND GND GND GND 8 10 12 14 38 38 GND GND GND GND GND GND GND GND 10 10 10 GND GND GND GND GND GND GND GND 12 14 16 12 12 14 GND GND GND GND GND GND GND GND 14 44 GND GND GND GND GND GND GND GND 16 20 22 24 16 20 22 GND GND GND GND GND GND GND GND 20 22 20 50 GND GND GND GND GND GND GND GND 22 DDM.BYTE*-GND GND GND GND GND GND GND GND 24 8C1 D-GND GND GND GND GND GND GND GND 26 28 58 60 26 28 26 28 26 28 58 GND GND GND GND GND GND GND GND 60 GND GND GND GND GND GND GND GND 30 GND 30 GND GND GND GND GND GND GND GND GND Note: Parity bits are little endian Yo support MIPS notation Byte ordering is big endian SILICON GRAPHICS INC. REV Main Memory Bank 2 032-8044-003 12 of 36 31 OCT 1991 7 5

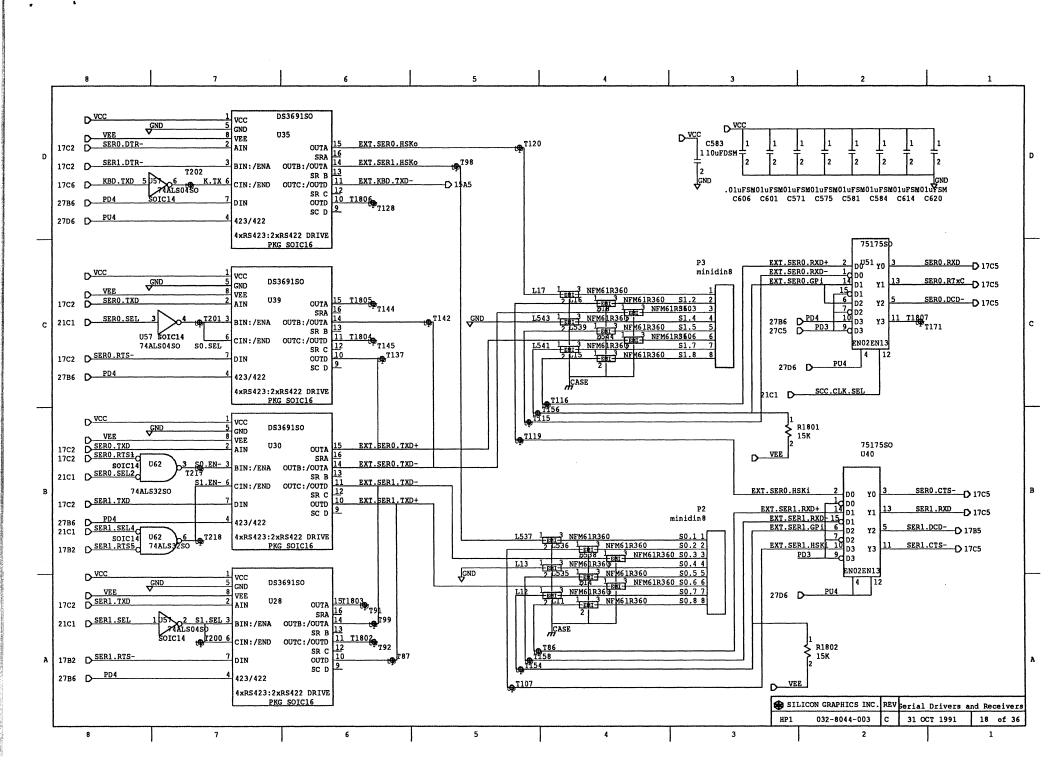
PBUS . DATA* SCSI .DATA* 0 K2 SC.DO 1 K3 SC.D1 PBUS.ADDR* SCSI,CS-SCSI.CS-SCSI.RE-D 15D8 /SC.CSD2 /SC.RED2 2 K4 SC.D2 3 L1 SC.D3 SCSI.WE- D 15D8 /SC.WED 5 L1 SC.D3 5 L3 SC.D5 6 L4 SC.D6 7 M3 SC.D7 P3 C/SC.REQ GIO.BUS* 7D8 🗢 GIO BUS SCSI.MR -**(**) 15B8 SC.MR GIO.AD0 GIO.AD16 V12 16 T12 17 PB.D0 D12 SCSI.ADR0 D 15D8 SCSI.ACK- D 15C8 1 D2 PB.A0 SC.AO PB.D1 C13 1 15B5 D SCSI.BREQ-14D8 CENET.DATA* /SC.ACK B4 GIO. AD2 GIO. AD18 T14 19 GIO. AD4 GIO. AD20 N15 20 N15 21 2 E3 PB.A2 PB.D2 B14 2 3 F4 PB.A3 4 C1 PB.A4 5 B1 PB.A5 PB.D3 B15 3 EtherNet 3 J3 0 V1 1 T4 2 R5 3 U3 4 V2 EN.D0 EN.D1 EN.D2 EN.D3 PB.D4 C14 ENET ADDR' PB.D5 D13 5 GIO.AD5 GIO.AD21 N15 21 5 M2 6 C2 PB.A6 PB.D6 A16 6 6 N1 GIO.AD6 GIO.AD22 P16 22 PB.D7 A17 7 GIO.AD7 GIO.AD23 P17 23 7 E4 PB.A7 9 P2 GIO.AD8 GIO.AD24 P18 24 N17 25 10 N4 GIO.AD9 GIO.AD25 N17 25 PB.D8 B16 8 4 V2 EN.D4 EN. A0 V11 0 EN. A1 R10 1 8 D3 PB.A8 PB.D9 D14 9 9 A1 PB.A9 5 T5 EN.D5 PB.D10 C15 10 PB.D11 A18 11 GIO.AD10 GIO.AD26 M17 26 L15 27 L12 20 CIO.AD11 GIO.AD27 L12 27 L12 20 CIO.AD27 L12 20 CIO.AD2 10 A2 PB. A10 6 V4 EN.D5 7 R7 EN.D7 EOF V5 EN.D8 T10 EN.A2 12 D5 PB. A12 PB.D12 C16 L17 28 GIO.AD12 GIO.AD28 PB.D13 B18 13 GIO.AD13 GIO.AD29 L18 29 13 C4 ENET.RD--D 14C8 PB.A13 /EN.RD PB.D14 C17 14 GIO.AD14 GIO.AD30 G17 30 U63 14 A3 ENET.WR-/EN.WR -D 14C8 PB.A14 ENET.RESET- D 14D8 PB.D15 E15 15 14B6 D ENET.INT HPC1 T13 EN. INTin 15 T11 GIO. AD15 GIO. AD31 H15 31 15 B4 /EN.RST PB.A15 PB.D16 C18 16 PB.D17 17 R8 EN.TXRDY /EN.TXWR ENET.TXWR-16 D6 ENET.TXRDY PB.A16 14D6 D--D 14C8 17 C5 PB.A17 PB.A18 14D6 D ENET.RXRDY 26A1 DGIO.CLK4 T9 GIO.CLK V7 EN.RXRDY /EN.RXRD ENET.RXRD-D 14C8 PB.D18 F15 ENET.INT.OUT D 2107 U13 EN . RXDC ENET.RXDC 14D6 D-EN.INT PB.D19 E16 19 ENET.LPBAK D 14C6 19 B5 PB.A19 V13 EN.TXRET 25D1 DGIO.RESET-U8 C/GIO.RESET ENET.TXRET 14D6 D-EN.LPBK PB.D20 D18 20 O INT2 .DATA* ♦GIO.AS-PB.D21 E17 21 INT2 PB.D22 E18 22 0 T16 INT.D0 1 V18 INT.D1 PB.D23 G15 23 /INT.RE V15 /INT.WE V16 INT2.RD--D 21D8 2 R16 INT.D2 3 P15 INT.D3 4 T17 INT.D4 5 U18 INT.D5 GIO. SLVDLY T6 GIO. SLVDLY INT2.WR--D 21D8 /DRT.CE1 DE1 SCC.CE0-/DRT.CE1 DF2 SCC.CE1-/GIO.BREQ INT.A0 T15 0 INT.A1 R14 1 8A1 DGIO.HPC.BGNTB-Q/GIO.BGNT /DRT.CE2 DE1 | G3 | SCC.CE3-6 R17 INT.D6 INT.A2 U16 2 INT.A3 V17 3 V9 HPC0 7 R18 INT.D7 /DRT.RD DT SCC.RD-/DRT.WR DC6 SCC.WR-♦ PBUS.RD-Printer INT2.ADDR* -D 21D8 -d/PB.RD **-D** 1708 A6 d /PB.WR 1 H17 CN.D1 CN.INT K15 K18 CN.D1 /CN.STATRD K18 0 H16 CN.DO O PBUS.WR-PP.INT -D 17C8 30B8 **-D** 21C7 PP.STATRD- D 20D8 17D1 D SCC0.IRQ-17D1 D SCC1.IRQ-2 H18 CN.D2 CN.DATAEN L16 3 J15 CN.D3 /CNDMAWR M16 C7
D8
DRT.IRQ0 /PROM.CE
DRT.IRQ1 /RTC.CE
DRT.IRQ2 /MDM.CE
DV SLOT.CEDRT.IRQ2 /MDM.CE
DV SLOT.CEDRT.IRQ2 /MDM.CE PP.DATAEN--D 20D8 PP.CNDMAWR- D 20D8 /CNDMAWR M18 -D 16C8 PP.RMTWREN-D 20A8
PP.STBINEN-D 20B8 | 4 | 016 | CN.D3 | CNDMAWR | 16 | CN.D4 | CN.RMTWREN | 16 | S | J17 | CN.D5 | CN.STBITEN | 18 | CN.D6 | CN.STBOTEN | CN.D7 | N18 | CN.D7 | N18 | CN.D7 | CN.D -D 24D4 24D8 25A8 ♦PINT.1-A7 PP.STBOUTEN- D 20B8 -D 35A7 36A7 D RTC. IRQ D PU1 VID. VSYNC N18 /CN. ACK F10 /CN. RDY CN. BUSY 517 B13 PP.ACK-20A1 D PP.STB-27D6 A14 VID. IRQ PP.BUSY -O 20A1 23D6 D VID. VFIELD В9 23D3 VID.FIELD DGFX. INT-C12 EEPROM 22A1 GFX.IRO PBUS .GNT-D9 d /PB.GNT PBUS .BR- D 35C7 /PB.REQ DA8 -D 6A8 23D4 EE CLK C11 EPRM.CLK -D 6A8 23D8 SA12 D10 PBUS SA12 35C5 /EE.PRE 011 EPRM.PRE--D 6A8 23D3 25A4 C10 /XY SA14 A10 35C5 DDSP.XY 6A1 C EPRM.DIN B12 EE.DIN PBUS.SA14 35C5 EPRM.DOUT EE . DOUT -D 23D3 GIO.HPC.BREQ-D 8A5 TEST GA.PUO TESTEN ---**◇** 8A7 GA.PU1 021A6 SCAN_IN T120 SCAN_EN C633 C629 T121 SCAN_TRIEN TESTOUT T3 110uFDSM ‡01uFSM SCANOUT 2 silicon graphics inc. REV HPC1 032-8044-003 31 OCT 1991 13 of 36 3

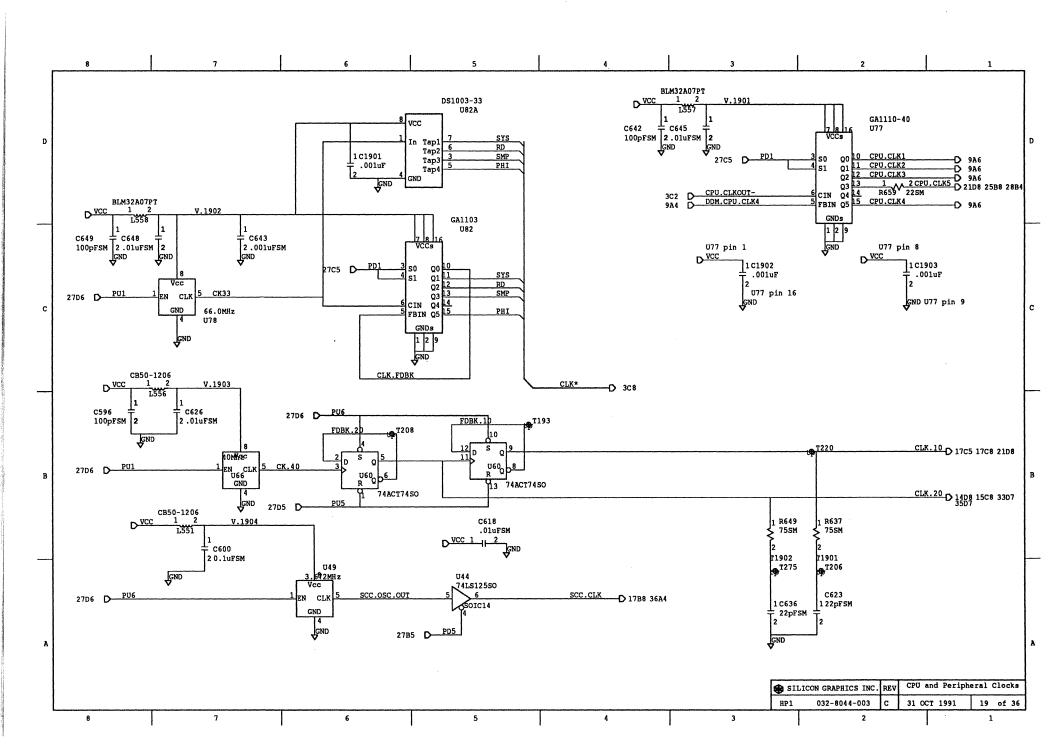






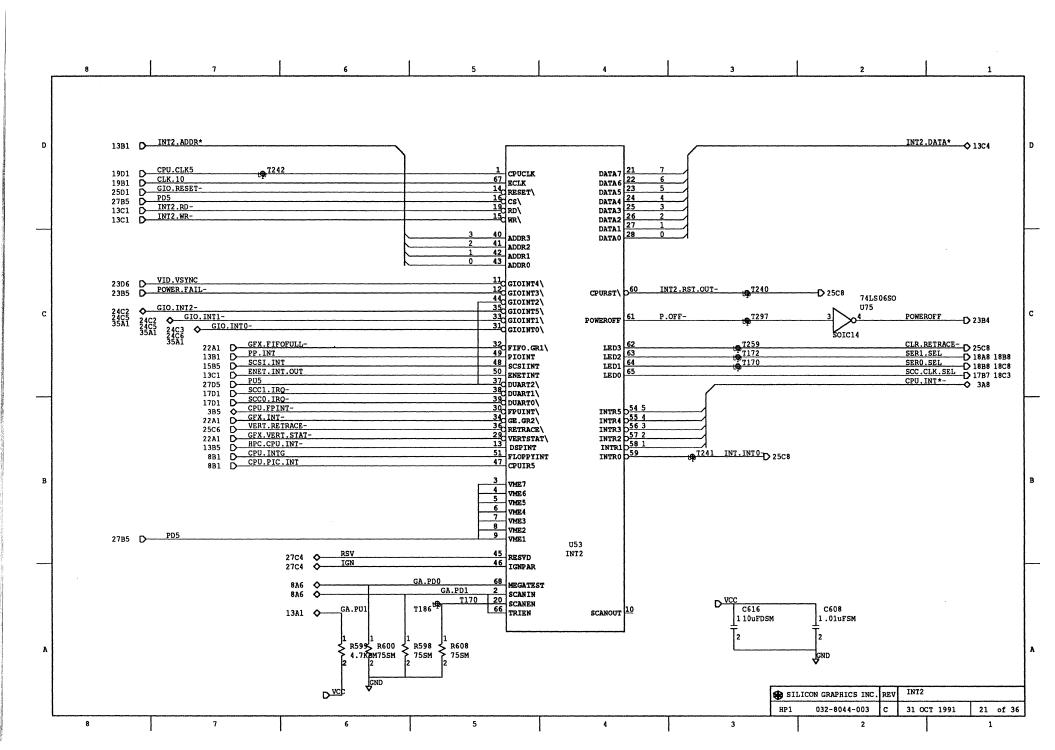


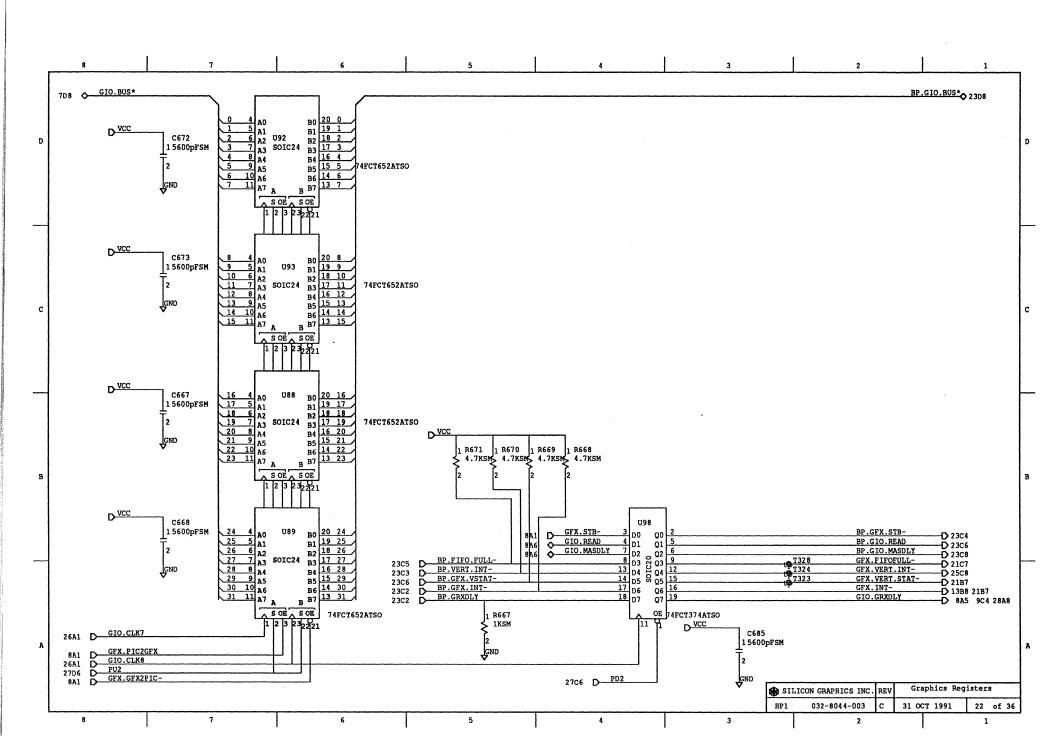


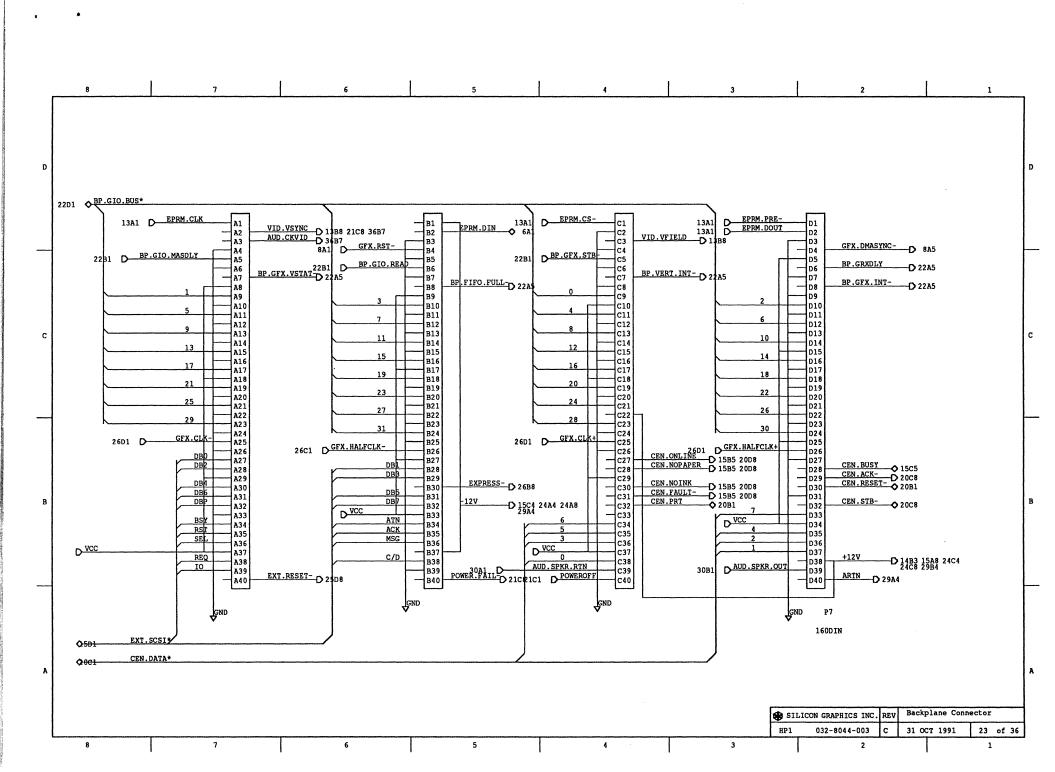


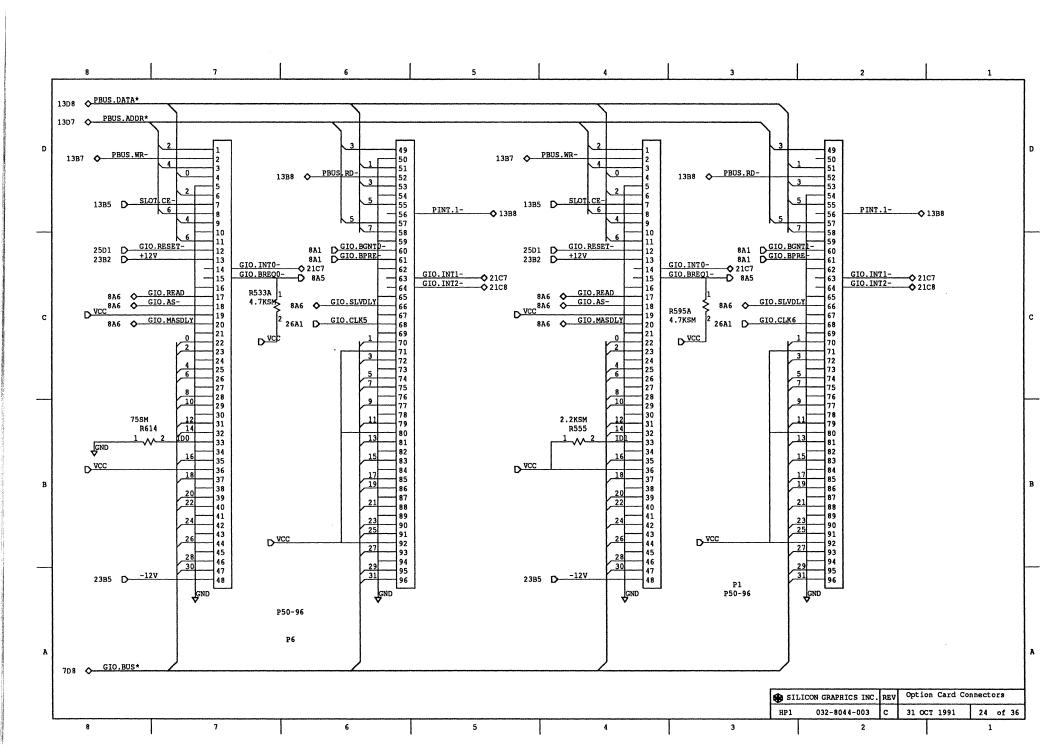
1 13B4 ♦ PP.DATA* U83 74ALS652SO 13B1 D PP.CNDMAWR-13B1 D PP.DATAEN-27D6 D PU2 C657 13B1 D PP.STATRD-A2 SOIC24 B3 17 .01uFSM D VCC 1 II 2 23B3 CEN.ONLINE
23B3 CEN.NOPAPER
23B3 CEN.NOPAPER 23B3 D CEN.NOINK SOE SOE 1 2 3 232221 23B3 D CEN.FAULT-CEN.DATA* **-**♦ 23A8 U80 74ALS24450 D0 © Y0 D1 © Y1 D2 © Y1 D2 © Y2 D3. 9 Y3 D3. 9 Y3 PD3 27C5 D-27C5 D CEN.ACK-23B2 D CEN.STB-74ALS24450 C650 17 DO O YO 3 15 D1 D Y1 5 13 D2 D Y2 7 11 D3 Y3 9 15C5 CEN.BUSY OE 27C6 D PD2 CEN.BUSY.B CEN.STB.B-U84 13B1 D PP.STBOUTEN-74LS125SD CEN.PRT 13B1 D PP.STBINEN-CEN.RESET-D1 Y1 D1 Y1 6 4 OE1 9 D2 Y2 8 10 OE2 12 D3 Y3 11 13 OE3 .01uFSM SOIC14 -D 13B4 -◆ 13B1 PP.BUSY -D 13B4 A 13B1 D PP.RMTWREN-C651 .01uFSM Printer Port Buffer SILICON GRAPHICS INC. REV 032-8044-003 31 OCT 1991 20 of 36

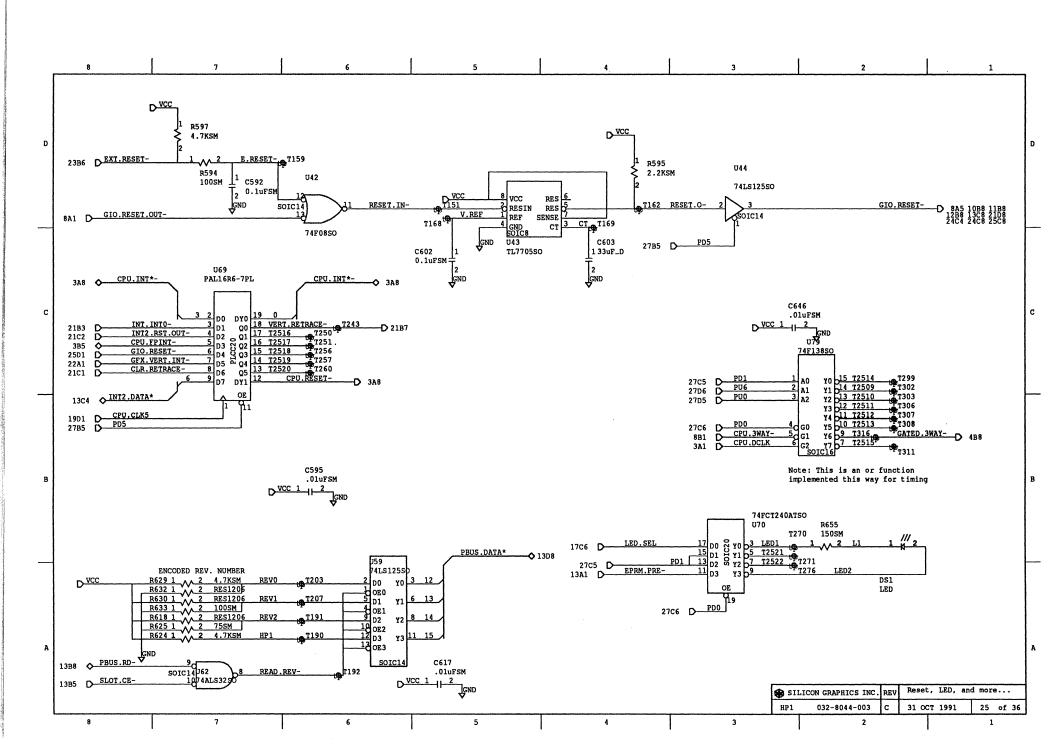
7

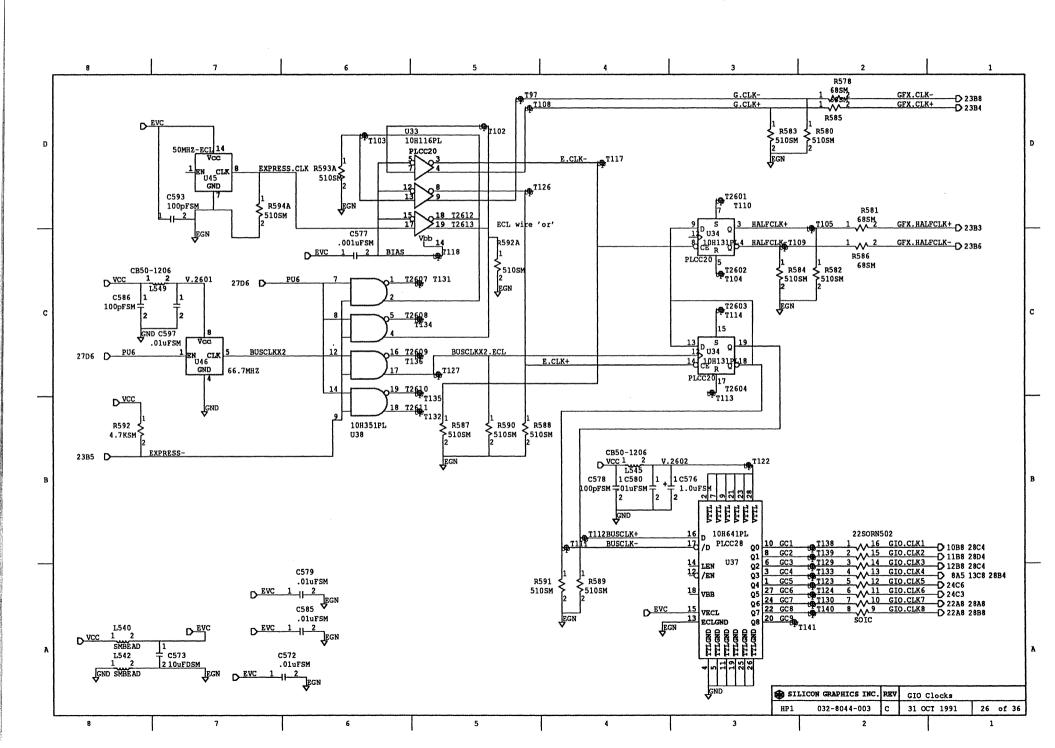


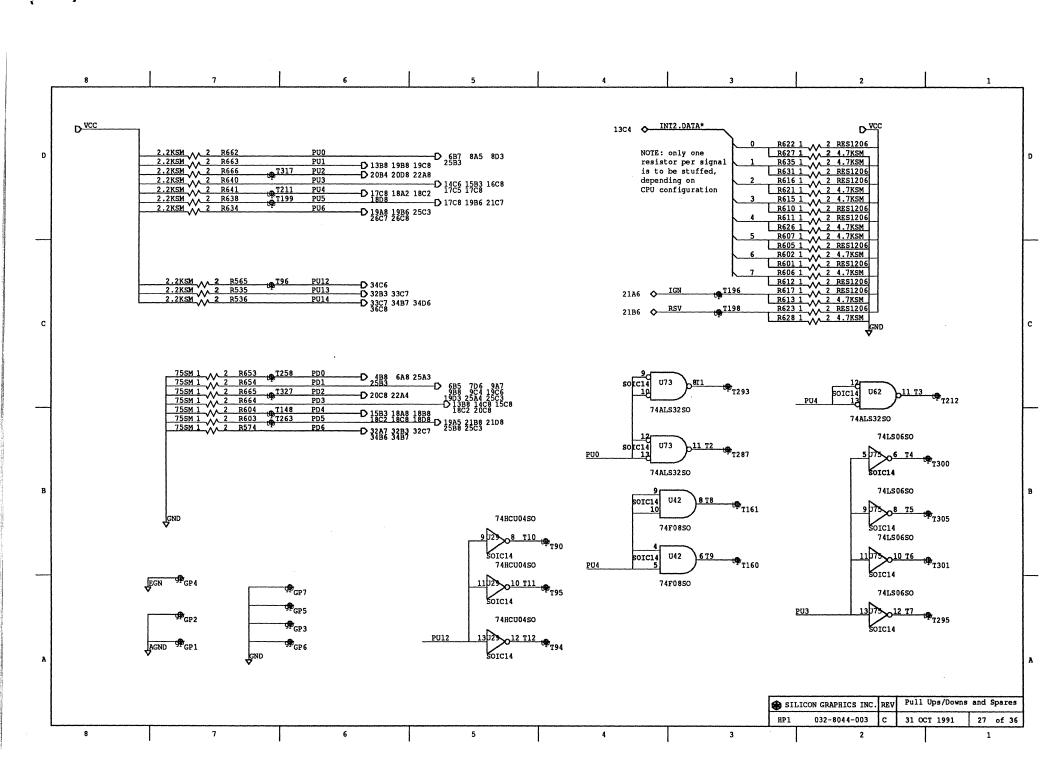


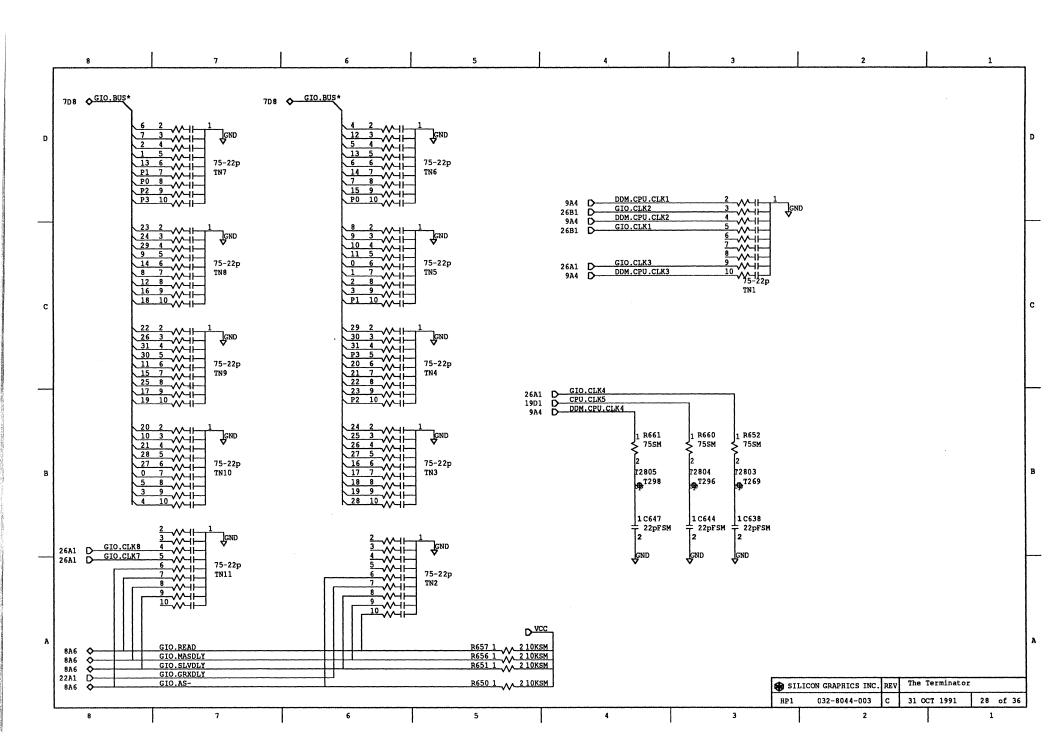


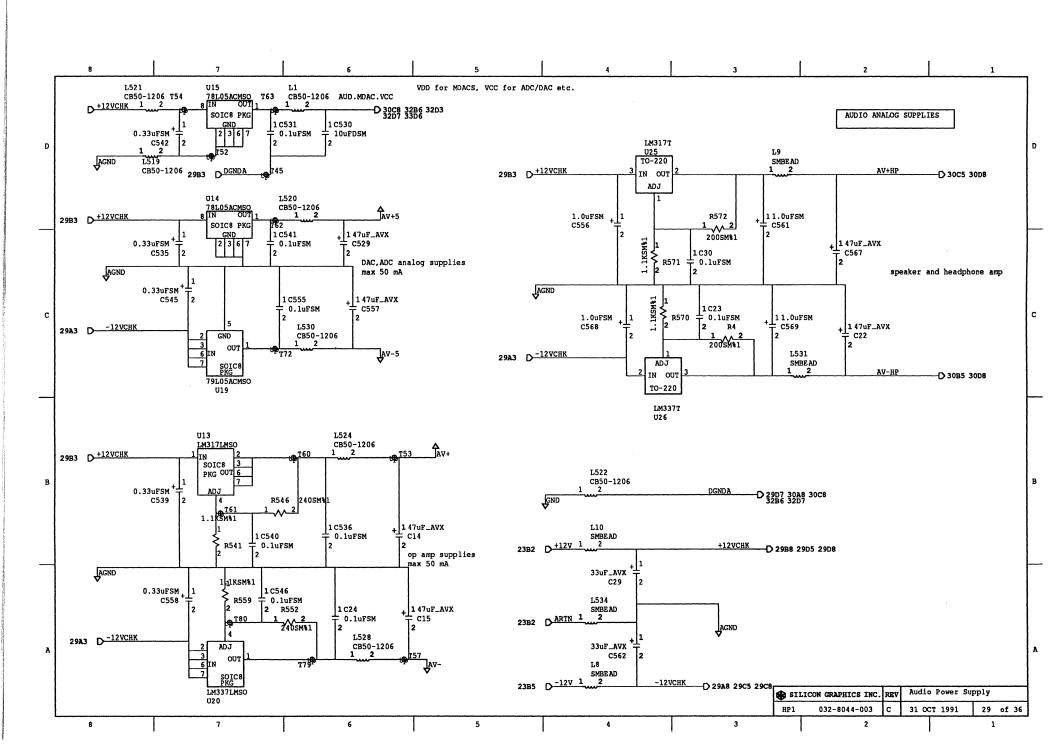


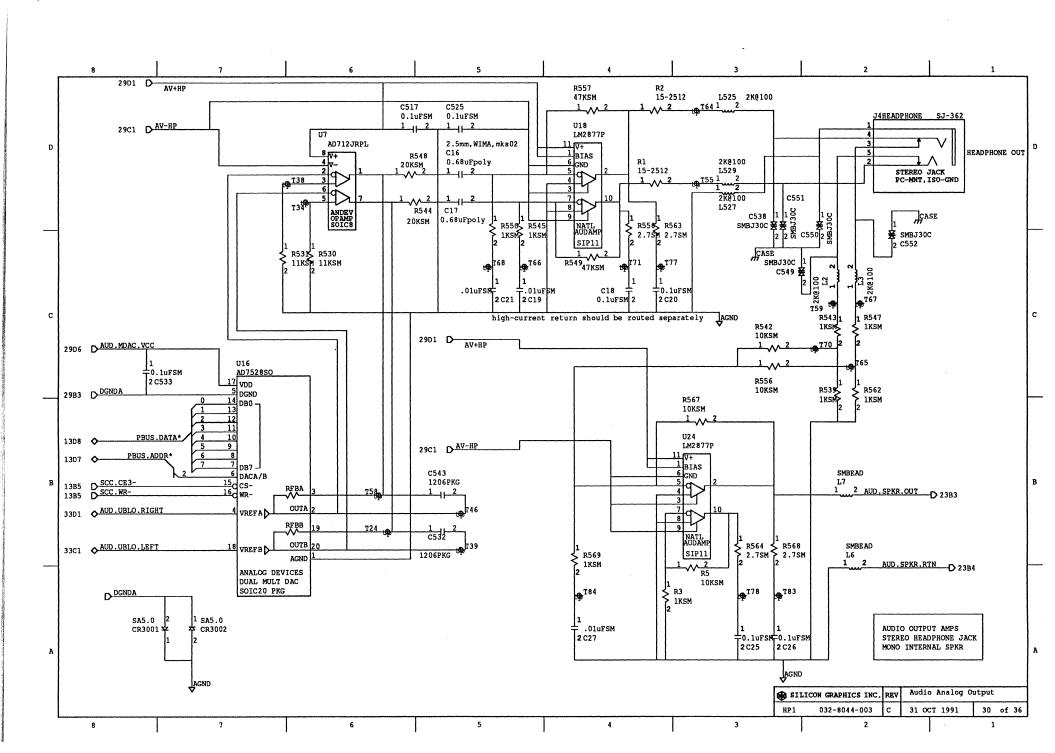


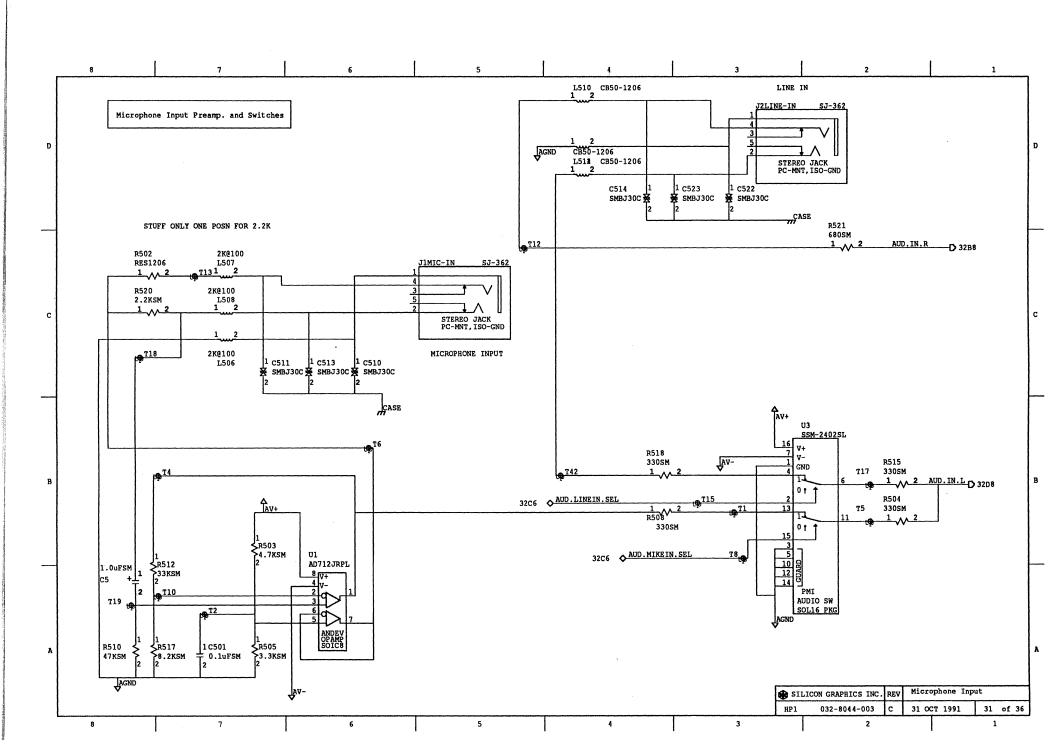


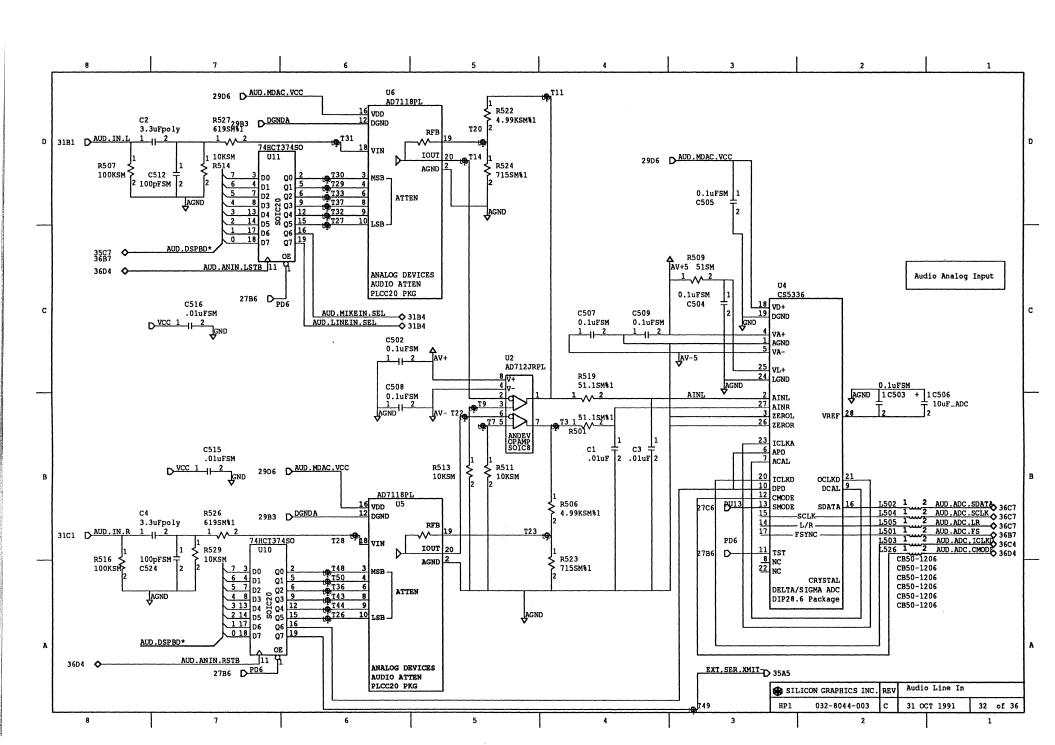








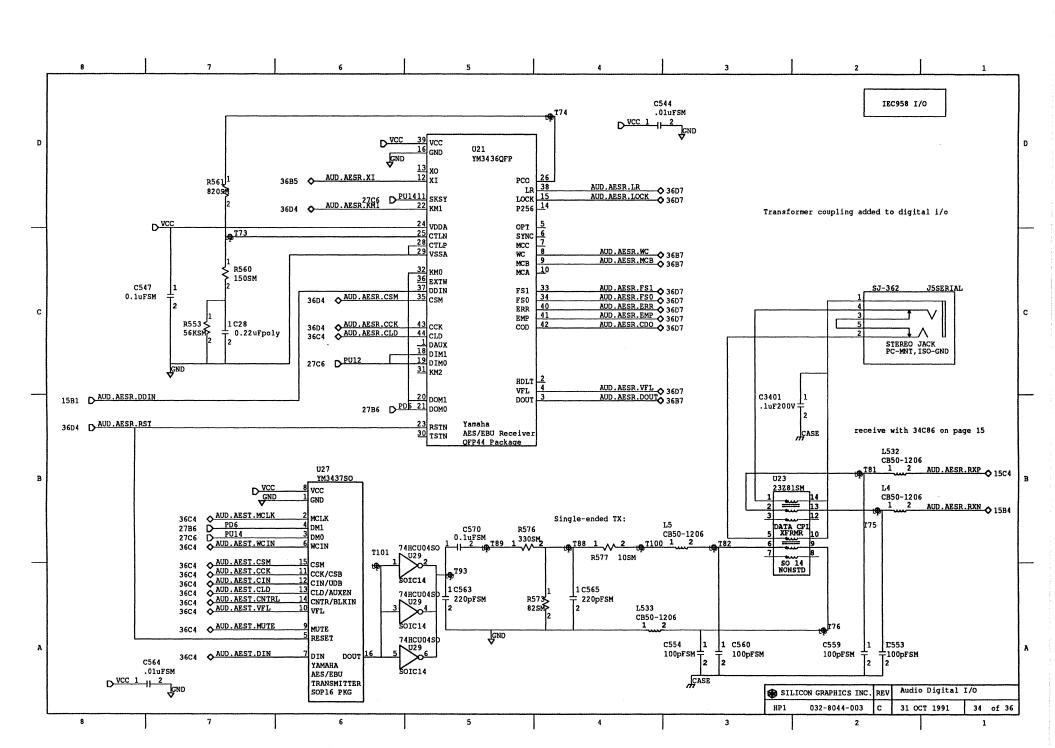




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AV+ AGND AV+529D6 D AUD.MDAC.VCC 1 C526 C518 1 C519 T₂ 0.1uFSM 0.1uFSM 0.1uFSM U9 AGND AD1864PL Analog Output C520 · +VL ٦ AGND 0.luFSM 16 DGND DIG SUPPLY 1 C521 U8 ل**ـ ۷**۱-C6 19B1 D CLK.20 ‡ 0.1uFSM GND AD712JRPL C11 360pF%1 820pF%1 +VS] ANA SUPPLY R533 R532 6.19KSM%1 6.19KSM%1 YM3434 DVEE 1 AUD.UBLO.RIGHT ♦ 30B8 TRIM RF CB50-1206 MSB TUOI L509 1 C 9 VDD1 SJ 390pF%1= AUD.UBLO.LEFT \$ 30B8 ANDEV OPAMP SOIC8 VDD2 VOUT CK AGND VSS AGND SHL DR SHR 16 C10 36C4 AUD.FIL.BCI
AUD.FIL.SDSY
AUD.FIL.SDSY ₹741 820pF%1 2 L513 1 2 1 L515 1 2 всо C8 SDSY WCO AUD.FIL.DIN 9 L511 1 360pF%1 TRIM CK SDI DLO RF R525 R528 DRO MSB IOUT 27C6 D PU1414 6.19KSM%1 6.19KSM%1 ST SJ С CB50-1206 15 16/18 VOUT 27C6 D----CB50-1206 AGND PU13 AHAMAY CB50-1206 1 C7 DIG FILTER CB50-1206 ± 390pF\$1 ANALOG DEVICES DIP16.3 PKG DUAL 18-BIT DAC AGND PLCC28 PKG C534 D VCC 1 | 2 GND L518 2K@100 1 2 LINE OUT NE5532DSL J3LINE-OUT AV+ R540 C12 SJ-362 12 +Vcc 4-Vcc 2K@100 619SM%1 3.3uFpoly L523 R534 619SM%1 3.3uFpol L516 2K@100 1 2 STEREO JACK PC-MNT, ISO-GND R537 100KSM 100KSM 1 C527 1 C528 BOARD EDGE 姜 SMBJ30C C537 SMBJ30C SMBJ30C AGND CASE AV-SILICON GRAPHICS INC. REV Audio Line Out 032-8044-003 31 OCT 1991 33 of 36 5 3

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8 DSP56001QFP20 PBUS.DATA* U41 CXK58258AJ-30 U31 CXK58258AJ-35 U36 CXK58258AJ-35 CLOCK CLK.20 127 EXTAL XTAL 19B1 D D VCC 28 VCC PBUS.DATA* 13D8 **O**-GND GND GND PORT A GND 82 54 3 D0 D0 D0 D 85 57 4 D1 D1 D1 58 5 10 18 13 D2 D2 D2 87 60 6 11 19 15 D3 D3 D3 88 61 7 12 D4 D4 D4 6 65 8 92 17 D5 D5 D5 7 67 9 93 18 **○**13D7 D6 D6 D6 8 94 68 10 D7 D7 D7 PBUS.ADDR* 9 96 70 11 9 10 97 10 71 12 A0 A0 ΑO 11 99 11 12 102 12 13 104 13 75 13 **A**1 A1 A1 12 76 14 A2 A2 A2 13 77 15 A3 A3 A3 14 105 14 79 16 A4 A4 A4 15 106 15 15 80 17 A5 A5 A5 16 108 16 A6 A6 A6 17 109 17 A7 A7 A7 17 109 17 18 113 18 19 114 19 20 115 20 21 118 21 22 119 22 23 120 23 45 BR 10 A8 **A8** A8 PS 52 A9 A9 A9 С A10 A10 A10 DS DY-X/Y 48 DSP.XY D 13A8 MR 47 PBUS.RD- ◆ 13B8 13A5 D PBUS. WR 46 PBUS.WR- ◆ 13B7 BG 43 PBUS.GNT- D 13A8 13A5 D PBUS.SA14 A11 A11 A11 PBUS.SA12 A12 A12 A12 A13 (+CS) A13 (+CS) A13 (+CS) 13A5 D PBUS.BR-A14 (NC) A14 (NC) A14 (NC) 32C8 AUD.DSPBD* AUD.CE-PORT B 13B5 D CS CS CS PBUS.WR-(HO) WR WR WR 22 PBUS .RD-(H1) OE OE OE (H2) 19 SRAM SRAM SRAM 3 (H3) 32K x 8 32K x 8 32K x 8 (H4) 4 (8K x 8) (8K x 8) (8K x 8) 5 (H5) PKG SOJ28.3 PKG SOJ28.3 PKG SOJ28.3 6 (H6) AUD.DSPBA* \$36A7 7 (H7) DSP BOOTS /IRQA=0 /IRQB=1 5 2 3 5 8 5 6 8 (HA0) NORMAL EXPANDED MODE 9 (HA1) C574 .01uFSM 10 (HA2) U57 DSP System 11 (HR/W) 74ALS04S0 C582 .01uFSM 12 (HEN-) EXT.SER AUD.DSPBR-13 (HREQ-) 15A5 AUD.DSPBW-C591 .01uFSM (HACK-) **-**♦ 36A7 SOIC14 74LS125SO PORT C **⊕** T125 DSP.SCI.RXD 27 8 EXT.SER RXD SCI TXD DSP.SCI.TXD 9 **-**♦ 15A5 SOIC14 DSP.SCI.SCLK 29 36A2 SCLK D vcc POWER D VCC RN501 EXT.SER.KMIT-STD 39 DSP.SSI.STO D 42 SRD DSP.SSI.SRD 13 767-141-R10K DATA -**♦** 36A7 36A5 DSP.SSI.SC1/RXFS 40 SC1 SC2 37 DSP.SSI.SC2/TXFS 35 33 PBUS . RD-FS -**♦** 36A5 36A5 13 GIO. INTO-12 GIO. INT1-21C7 11 GIO. INT2-21C8 SCK 32 DSP.SSI.SCK 34 55 DSP.SSI.SCO/RXCK 31 36 63 SC0 CK PBUS . WR-36A5 -**♦** 36A5 PBUS.BR-64 100 101 128 129 VCC 56 PBUS . GNT-INT + MODE 123 MODA/IRQA 121 NMI, MODB/IRQB 124 RESET DSP. IROA-73 DSP.RST-13B5 GND DSP.IRQB-74 DSP. IRQB-36A2 per EMI recomm. 90 13B8 OPINT.1-DSP.RST-13B5 D 91 R NETWORK MOTOROLA 111 112 MOTOROLA PKG S014 DIGITAL C590 C589 DIGITAL SIGNAL 10uFDS 0.1uFSM 130 SIGNAL PROCESSOR 131 PROCESSOR PKG QFP132 DSP silicon graphics inc. Rev 35 of 36 032-8044-003 31 OCT 1991 7 5

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