ECSE 2920: Design Methodology

Deliverable 6

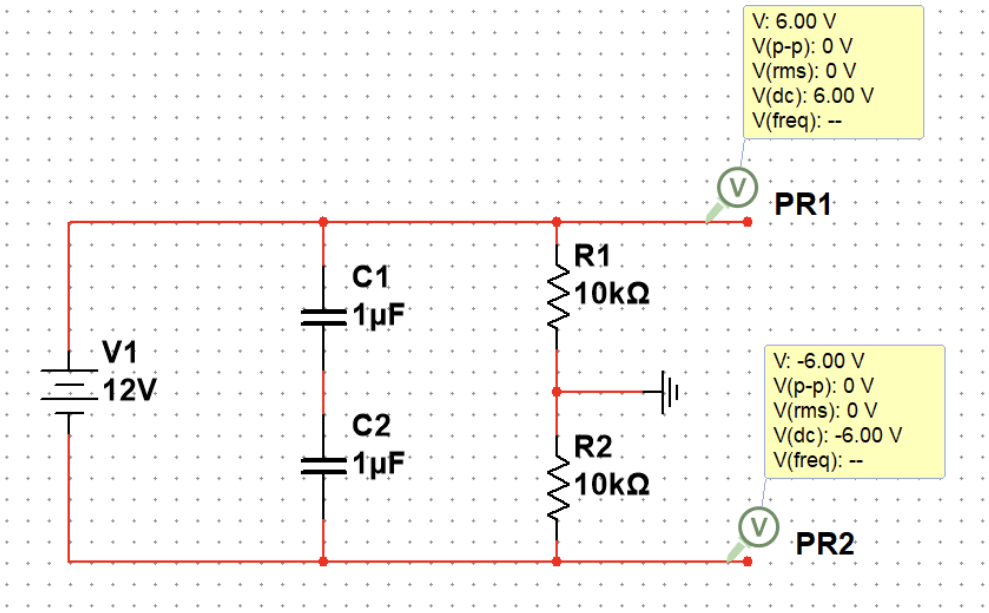
Group 6

02/15/2023

Part 1: Negative Voltage Simulation

Requirements:

- **Provide a schematic (digitally drawn in your chosen PCB software) AND a simulation of your design from multisim, LTSpice, Simulink, Altium, etc.**
- **Need to show a stand-alone circuit working with your +12V DC source coming from a lab power supply.**
    - **Your V+ and V- reference point should be around +/- 6 volts**



To start our simulation, we decided to work in Multisim since it was the most user-friendly and each of us on the team have used it before. The picture above demonstrates our idea for a voltage splitter to take the +12V DC supply and creates two new voltage references, each one being +6V and -6V respectively. In the research for this circuit, we've found that we can use two capacitors connected together in series in order to store some of the electrical energy. This creates a potential difference between the two terminals of the capacitor. We've taken advantage of this potential difference to have a positive and a negative terminal. In order to divide the +12V between our two terminals, our circuit includes a voltage divider using two 10kOhm resistors connected in series with each other. This effectively takes the +12V and splits it into +6V on one terminal and -6V on the other one.

We will include our Multisim simulation file in the submission of this week's deliverable.

Part 2: ADC

Requirements:

- **For this deliverable provide an ADC design of at least 4-bits**
- **This is a stand-alone design and does not need to be attached to the PI**

(For better clarity, the image of our Multisim circuit is on the next page)

The page below contains our 4-bit ADC circuit design. On the far left side of the picture is our "VANALOG" signal. This is meant to be our input analog signal that's to be converted to a digital signal in our output. We arbitrarily picked a 3V analog signal for testing purposes. In order to convert the signal, we've employed the LM339N IC in our circuit. The LM339N is a quad comparator IC that contains four independent voltage comparators in a single package. It has a wide range of applications, including voltage level detection, waveform shaping, pulse and square wave generation, and (in our case) analog-to-digital conversion. An image of the pin layout and a link to the datasheet page will be provided in this deliverable. We've taken the +12V DC supply and split it amongst pins 4,6, 8, and 10. For each pin, the voltage of the +12V is divided by 2 for each pin. In other words, the +12V is split into +6V, +3V, and +1.5V for each pin. This can be seen in the schematic as well in the picture on the next page.

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6 Pin Configuration and Functions

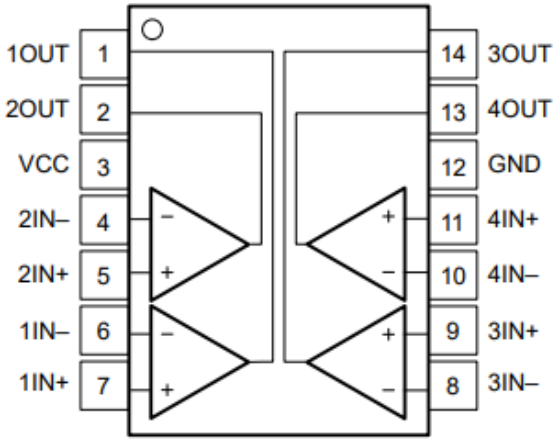
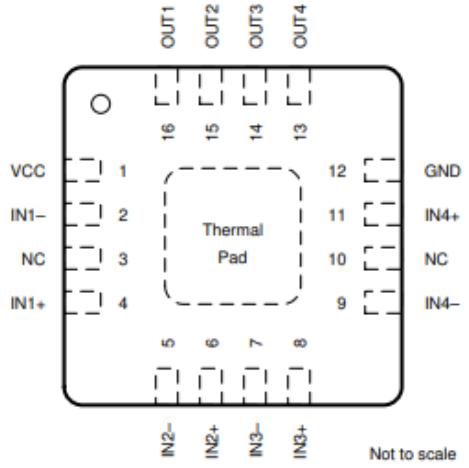


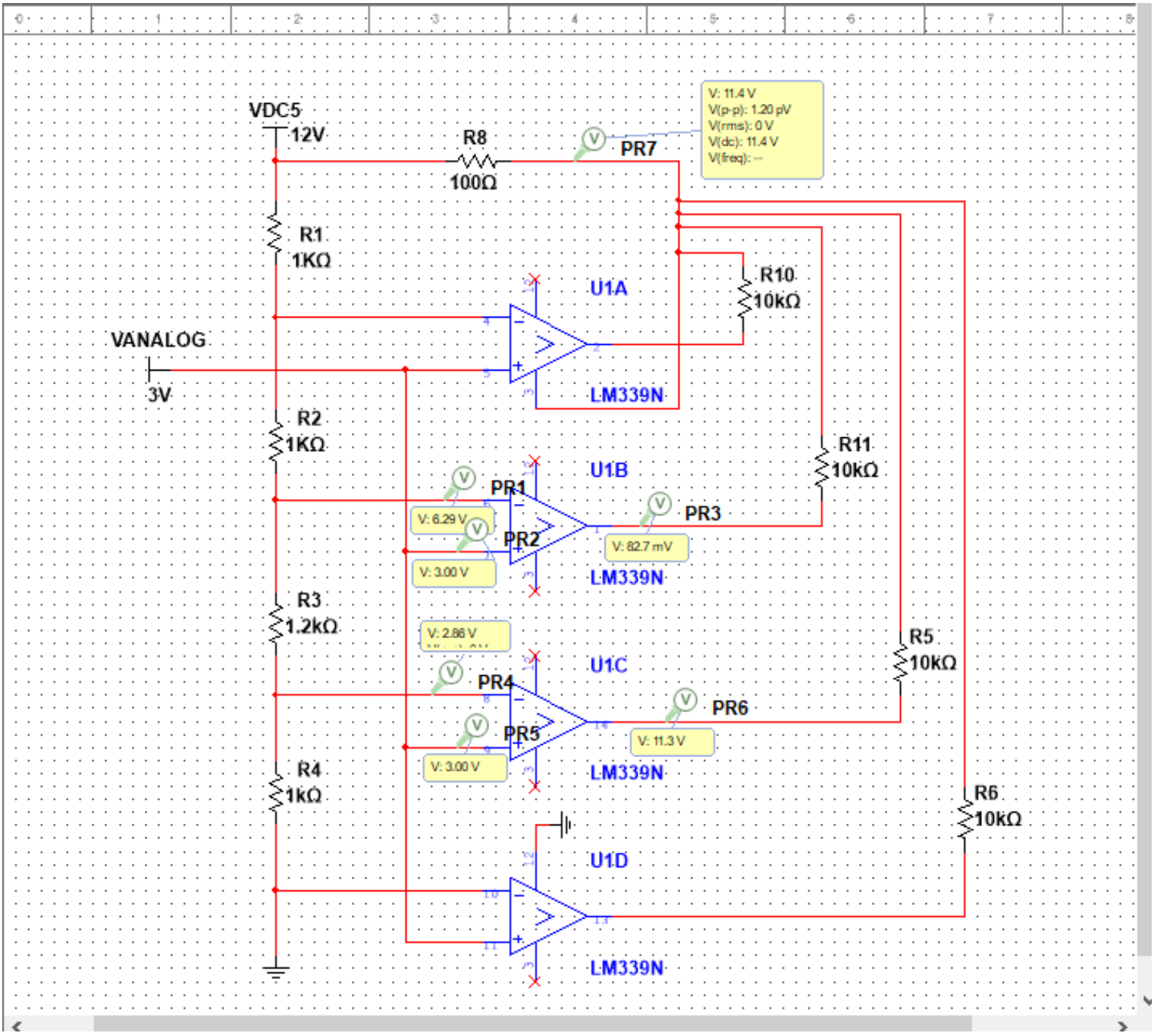
Figure 6-1. D, DB, N, NS, PW, DYY, J Packages
14-Pin SOIC, SSOP, PDIP, SO, TSSOP, SOT-23, CDIP
Top View



NOTE: Connect exposed thermal pad directly to GND pin.

Figure 6-2. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View

Datasheet:
https://www.ti.com/lit/ds/symlink/lm339.pdf?HQS=dis-dk-null-digikeymode-dsf-pf-null-wwe&ts=1676389773462

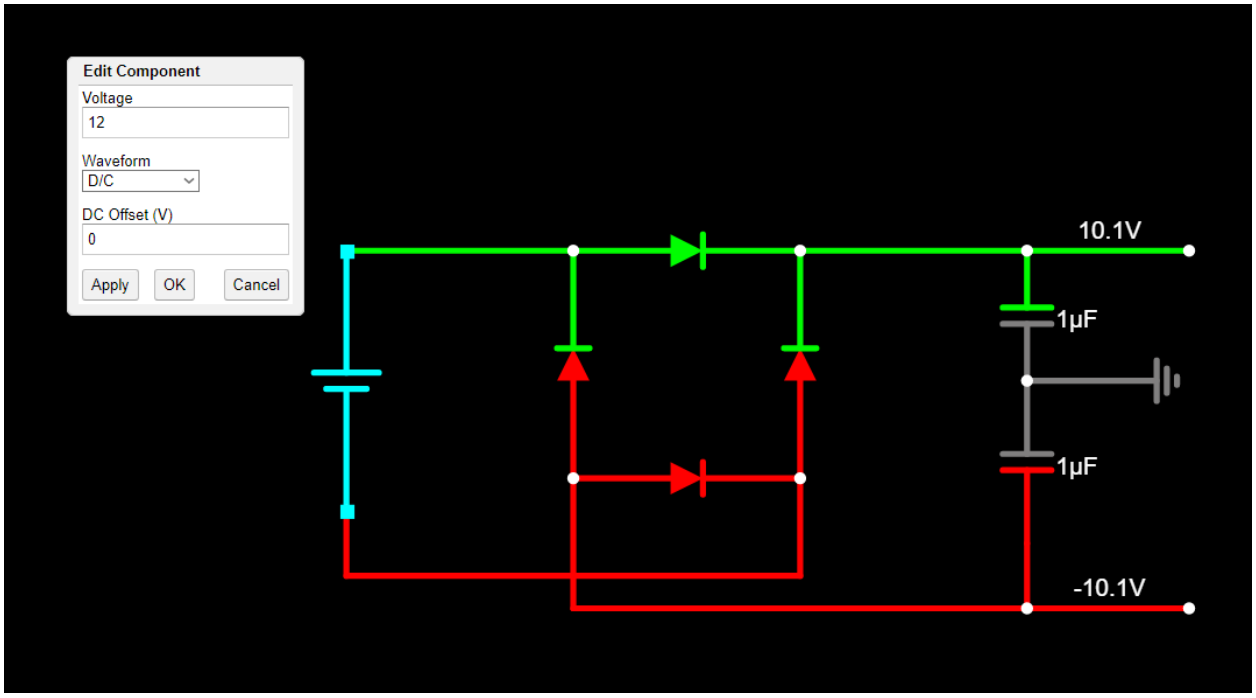


This is the screenshot of our 4-bit ADC design. Please see the paragraph written on the page above for our explanation of our design and why we chose certain components.

Part 3: Team Design Decisions

With every project and circuit comes several decisions that we have to make as engineers in order to achieve an end goal. For instance, there are countless ways that one could construct an Analog-to-Digital Converter circuit. The most popular ADC that we found is a Successive Approximation (SAR) ADC, which converts an analog signal to a digital signal in a step-by-step manner by using a binary search algorithm to find the digital code that best approximates the input signal. Another one that we found was the Flash ADC, which (as the name suggests) is very fast in performance but is relatively expensive; it uses a bank of comparators to convert an analog signal to a digital code in a single clock cycle.

Another decision that we had to make was deciding which design we wanted to commit to for our voltage splitter circuit. At first we had found a design for a potential circuit which splits the +12V DC into two positive and negative terminals using a half-wave rectifier circuit with a low pass filter to create the negative voltage. We tried playing around with certain diodes and capacitor values, but we could not get the circuit to properly split the two ends evenly into +6V and -6V. In the end, we settled with our current design and we're pretty content with how it turned out.



A prototype of our voltage splitter circuit using a half-wave rectifier. For some reason, the two terminals were split into +10.1V and -10.1V, respectively. Changing the capacitor values for 10uF to 1uF did not change anything.

Conclusion and Participation

This picture was taken immediately after class on Monday. After passing Checkpoint C the week before, we came into this week's deliverable with high spirits. As always, Neil drafted up the plan for this week's deliverable and we jumped into action. For this week's deliverable, Daniel and Kevin took the lead in brainstorming ideas for each of our circuit diagrams. We knew that we weren't required to have a working circuit this week, but that didn't stop us from trying our best to get something on the table. We played around in Multisim for a while until we found solutions for each of our respective circuits. Once each circuit passed the desired outcome for each scenario that we needed it to do, we switched over to Eagle and used CAD in order to sketch up a proper diagram. For this week's deliverable, we will be submitting 5 files: One Multisim file for our ADC, one Eagle file for our ADC schematic, one Multisim file for our voltage splitter, one Eagle file for our voltage splitter schematic, and this week's deliverable write up.