K9F1208X0C

Document Title

64M x 8 Bits NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	Nov. 10th 2005	Advance
0.1	2.7V part is added	July 13th 2006	Advance
0.2	Address of Read 2 is changed (A_4~A_7 : Don't care -> Fixed "Low")	Aug. 1st 2006	Advance
0.3	1. Add tRPS/tRCS/tREAS parameter for status read 2. Add nWP timing guide	Oct. 12th 2006	Advance
0.4	1. Change from tRPS/tRCS/tREAS to tRPB/tRCB/tREAB parameter for 1.8V device busy state	Nov. 14th 2006	Advance
0.5	1. Sequential Row Read is added	Nov. 15th 2006	Preliminary
1.0	1. tCRY is changed (50ns+tR(R/B) --> 5us)	Dec. 28th 2006	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.
http://www.samsung.com/Products/Semiconductor/

64M x 8 Bits NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9F1208R0C-J	1.65V ~ 1.95V	x8	FBGA
K9F1208B0C-P	2.5V ~ 2.9V		TSOP1
K9F1208U0C-P	2.7V ~ 3.6V		TSOP1
K9F1208U0C-J			FBGA

FEATURES

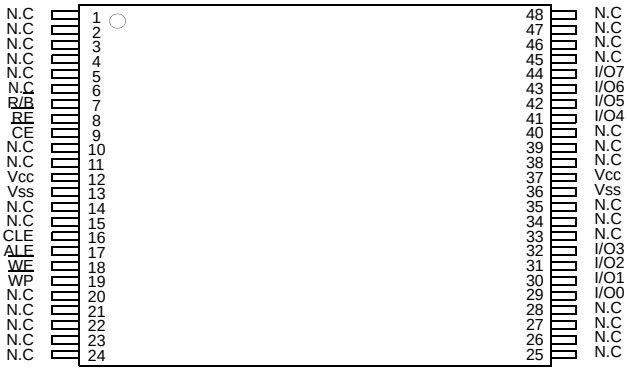
- Voltage Supply
  - 1.8V Device(K9F1208R0C) : 1.65V ~ 1.95V
  - 2.7V Device(K9F1208B0C) : 2.5V ~ 2.9V
  - 3.3V Device(K9F1208U0C) : 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (64M + 2M) x 8bits
  - Data Register : (512 + 16) x 8bits
- Automatic Program and Erase
  - Page Program : (512 + 16) x 8bits
  - Block Erase : (16K + 512)Bytes
- Page Read Operation
  - Page Size : (512 + 16)Bytes
  - Random Access : 15μs(Max.)
  - Serial Page Access : 42ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles (with 1bit/512Byte ECC)
  - Data Retention : 10 Years
- Command Register Operation
- Unique ID for Copyright Protection
- Package
  - K9F1208U0C-PCB0/PIB0 : Pb-Free Package 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9F1208X0C-JCB0/JIB0: Pb-Free Package 63-Ball FBGA(8.5 x 13 x 1.2mmt)
  - K9F1208B0C-PCB0/PIB0 : Pb-Free Package 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)

GENERAL DESCRIPTION

Offered in 64Mx8bits, the K9F1208X0C is 512Mbit with spare 16Mbit capacity. The device is offered in 1.8V, 2.7V and 3.3V Vcc. Its NAND cell provides the most cost-effective solutIon for the solid state mass storage market. A program operation can be performed in typical 200μs on the 528-bytes and an erase operation can be performed in typical 2ms on a 16K-bytes block. Data in the page can be read out at 42ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F1208X0C′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.
The K9F1208X0C is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP1)

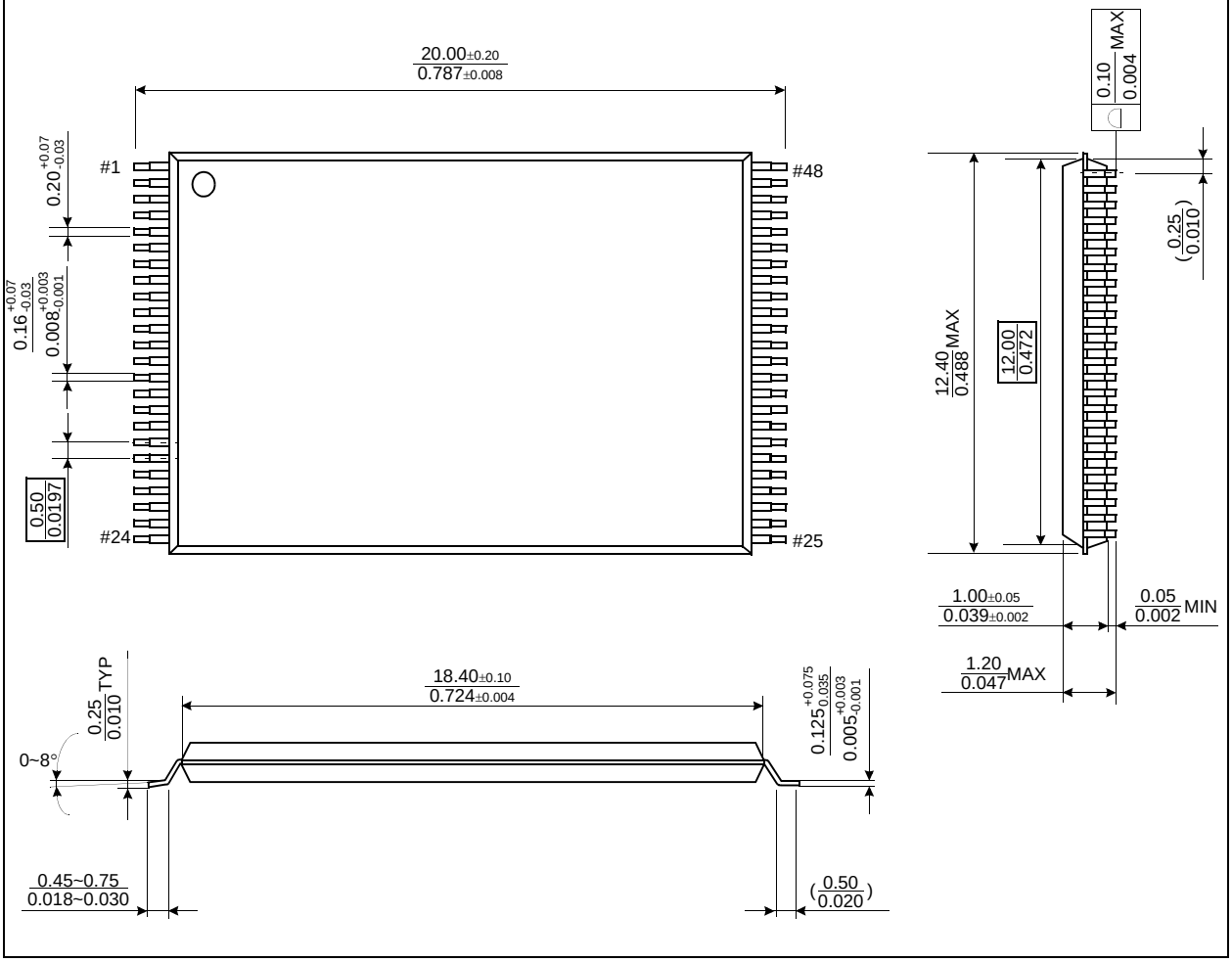
K9F1208X0C-PCB0/PIB0



PACKAGE DIMENSIONS

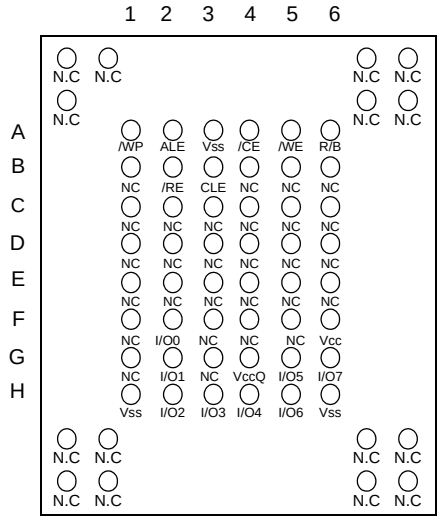
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



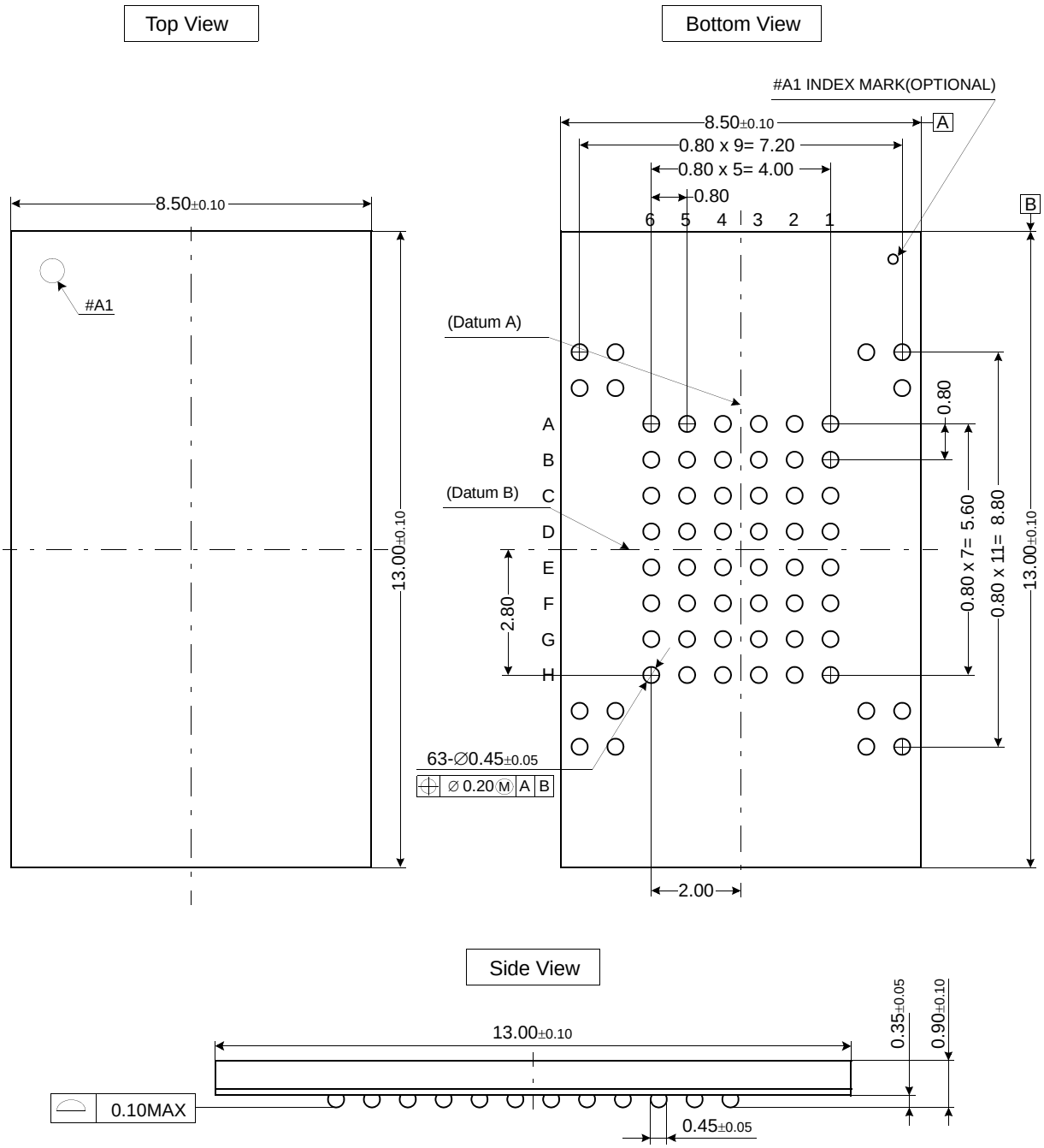
PIN CONFIGURATION (FBGA)

K9F1208X0C-JCB0/JIB0



Top View

63-Ball FBGA (measured in millimeters)



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase opertion. Regarding $\overline{CE}$ control during read operation, refer to 'Page read' section of Device operation .
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
$R/\overline{B}$	**READY/BUSY OUTPUT** The $R/\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	**POWER** V_{CC} is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.
DNU	**DO NOT USE** Leave it disconnected.

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

Figure 1. K9F1208X0C FUNCTIONAL BLOCK DIAGRAM

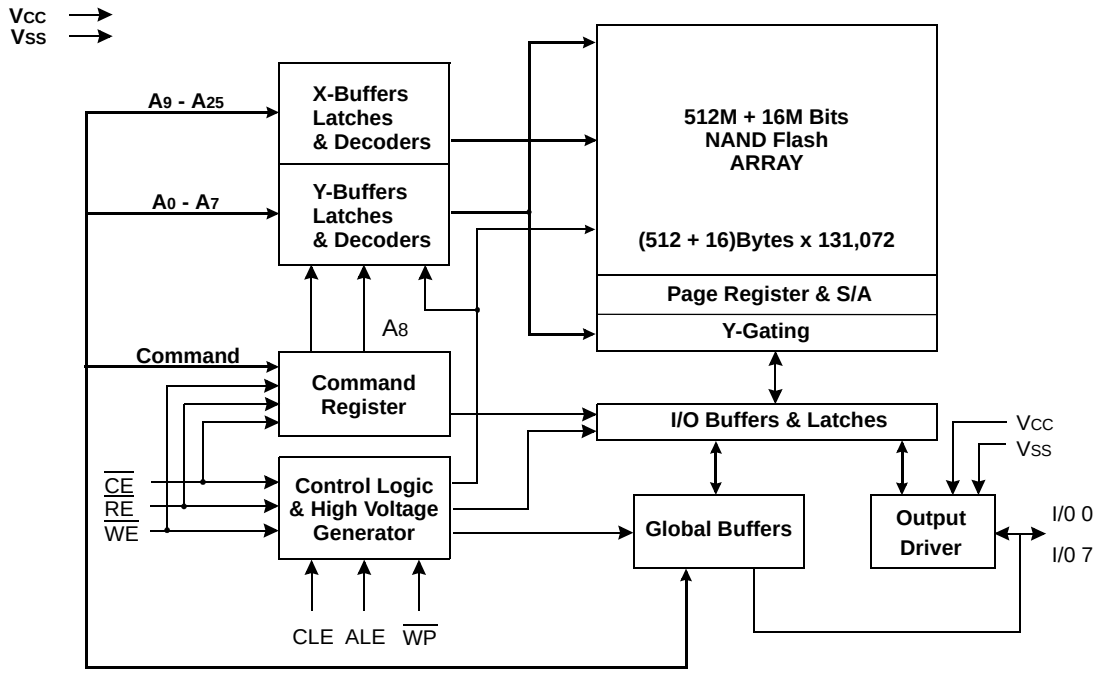
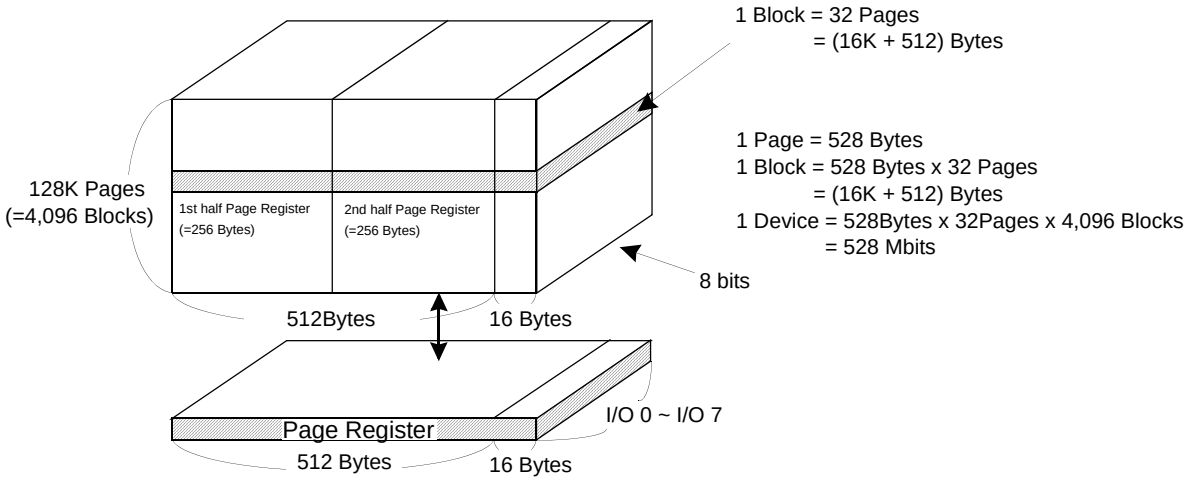


Figure 2. K9F1208X0C ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24
4th Cycle	A25	*L	*L	*L	*L	*L	*L	*L

Column Address
Row Address (Page Address)

NOTE : Column Address : Starting Address of the Register.
00h Command(Read) : Defines the starting address of the 1st half of the register.
01h Command(Read) : Defines the starting address of the 2nd half of the register.
* A8 is set to "Low" or "High" by the 00h or 01h Command.
* L must be set to "Low".
* The device ignores any additional input of address cycles than reguired.

Product Introduction

The K9F1208X0C is a 528Mbits(553,648,218 bits) memory organized as 131,072 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-bytes data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed two NAND structures. A NAND structure consists of 16 cells. Total 135,168 NAND structures reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4,096 separately erasable 16K-bytes blocks. It indicates that the bit by bit erase operation is prohibited on the K9F1208X0C.

The K9F1208X0C has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. The 64M byte physical space requires 26 addresses, thereby requiring four cycles for byte-level addressing : 1 cycle of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the 3 cycles of row address are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F1208X0C.

Table 1. Command Sets

Function	1'st Cycle	2'nd Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Block Protect 1	41h	-	
Block Protect 2	42h	-	
Block Protect 3	43h	-	
Read Status	70h	-	O
Read Protection Status	7Ah	-	

NOTE : 1. The 00h/01h command defines starting address of the 1st/2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			1.8V Device	2.7V/3.3V Device	
Voltage on any pin relative to VSS		V_{CC}	-0.6 to + 2.45	-0.6 to + 4.6	V
		V_{IN}	-0.6 to + 2.45	-0.6 to + 4.6	
		$V_{I/O}$	-0.6 to Vcc + 0.3 (< 2.45V)	-0.6 to Vcc + 0.3 (< 4.6V)	
Temperature Under Bias	K9F1208X0C-XCB0	T_{BIAS}	-10 to +125		°C
	K9F1208X0C-XIB0		-40 to +125		
Storage Temperature	K9F1208X0C-XCB0	T_{STG}	-65 to +150		°C
	K9F1208X0C-XIB0				
Short Circuit Current		I_{OS}	5		mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND at the condision of K9F1208X0C-XCB0 : T_A=0 to 70°C or K9F1208X0C-XIB0 : T_A=-40 to 85°C)

Parameter	Symbol	1.8V(K9F1208R0C)			2.7V(K9F1208B0C)			3.3V(K9F1208U0C)			Unit
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{CC}	1.65	1.8	1.95	2.5	2.7	2.9	2.7	3.3	3.6	V
	V_{SS}	0	0	0	0	0	0	0	0	0	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	K9F1208X0C									Unit
				1.8V			2.7V			3.3V			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	ICC1	tRC=42ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	8	20	-	10	20	-	10	20	mA
	Program	ICC2	-	-	8	20	-	10	20	-	10	20	
	Erase	ICC3	-	-	8	20	-	10	20	-	10	20	
Stand-by Current(TTL)		ISB1	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	-	-	1	-	-	1	
Stand-by Current(CMOS)		ISB2	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	-	10	50	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10	-	-	±10	
Input High Voltage		V_{IH}		V_{CC} -0.4	-	V_{CC} +0.3	Vcc -0.4	-	Vcc +0.3	2.0	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.4	-0.3	-	0.5	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	K9F1208R0C: I_{OH}=-100µA K9F1208B0C: I_{OH}=-100µA K9F1208U0C: I_{OH}=-400µA	V_{CC} -0.1	-	-	Vcc -0.4	-	-	2.4	-	-	
Output Low Voltage Level		V_{OL}	K9F1208R0C: I_{OL}=100µA K9F1208B0C: I_{OL}=100µA K9F1208U0C: I_{OL}=2.1mA	-	-	0.1	-	-	0.4	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	3	4	-	3	4	-	8	10	-	mA

Notes :
1. Typical values are measured at Vcc=3.3V, TA=25°C. And not 100% tested.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	4,026	-	4,096	Blocks

NOTE :
1. The K9F1208X0C may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.
3. Minimum 1,004 valid blocks are guaranteed for each contiguous 128Mb memory space.

AC TEST CONDITION

(K9F1208X0C-XCB0 :TA=0 to 70°C, K9F1208X0C-XIB0:TA=-40 to 85°C).

Parameter	Value		
	K9F1208R0C	K9F1208B0C	K9F1208U0C
Input Pulse Levels	0V to V_{CC}	0V to Vcc	0.4V to 2.4V
Input Rise and Fall Times	5ns	5ns	5ns
Input and Output Timing Levels	$V_{CC}/2$	Vcc/2	1.5V
K9F1208R0C:Output Load (Vcc:1.8V +/-10%) K9F1208B0C:Output Load (Vcc:2.7V +/-10%) K9F1208U0C:Output Load (Vcc:3.3V +/-10%)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=30pF	1 TTL GATE and CL=100pF
K9F1208U0C:Output Load (Vcc:3.0V +/-10%)	-	-	1 TTL GATE and CL=50pF

CAPACITANCE(TA=25°C, VCC=1.8V/2.7V/3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input (4 clocks)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input (4 clocks)
L	L	L	⎍	H	H	Data Input	
L	L	L	H	⎎	X	Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}(1)	-	200	500	μs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	1	cycle
	Spare Array		-	-	2	cycle
Block Erase Time		t_{BERS}	-	2	3	ms

NOTE NOTE: 1.Typical Program time is defined as the time within which more than 50% of the whole pages are programmed at Vcc of 3.3V and 25'C

AC TIMING CHARACTERISTICS FOR COMMAND / ADDRESS / DATA INPUT

Parameter	Symbol	Min	Max	Unit
CLE setup Time	t_{CLS}	21	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
$\overline{CE}$ setup Time	t_{CS}	31	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	ns
$\overline{WE}$ Pulse Width	t_{WP}(1)	21	-	ns
ALE setup Time	t_{ALS}	21	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	42	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NOTE: **The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low.**

AC CHARACTERISTICS FOR OPERATION

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	15	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
RE Pulse Width	t_{RP}	21	-	ns
WE High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	42	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	30	ns
$\overline{CE}$ Access Time	t_{CEA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	10	-	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device resetting time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs
RE Pulse Width during Busy State	t_{RPB}(2)	35	-	ns
Read Cycle Time during Busy State	t_{RCB}(2)	50	-	ns
$\overline{RE}$ Access Time during Busy State	t_{REAB}(2)	-	40	ns

Parameter		Symbol	Min	Max	Uni
K9F1208X0C-P only	Last RE High to Busy(at sequential read)	t_{RB}	-	100	ns
	$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read)	t_{CRY}	-	5	µs
	$\overline{CE}$ High Hold Time(at the last serial read)(4)	t_{CEH}	100	-	ns

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. This parameter (t_{RPB}/t_{RCB}/t_{REAB}) must be used only for 1.8V device.
3. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is so called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 517. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

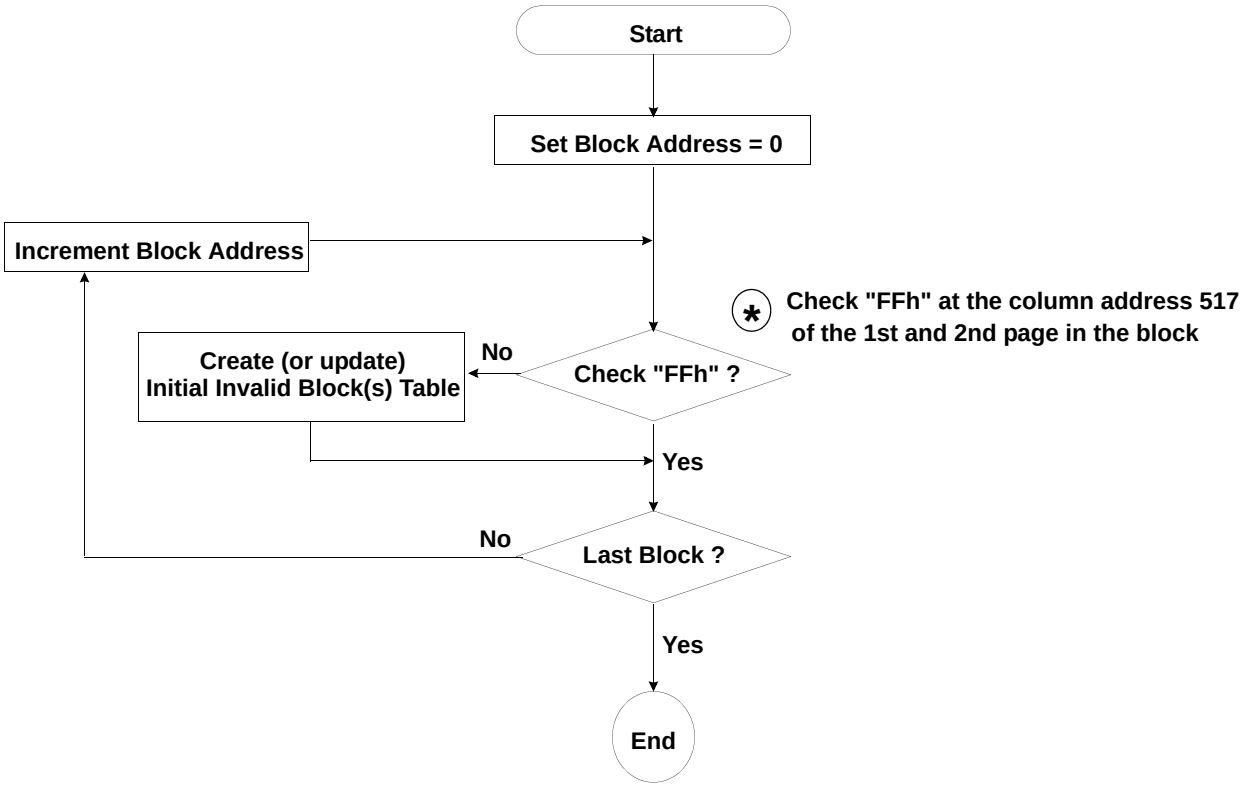


Figure 3. Flow chart to create initial invalid block table.

NAND Flash Technical Notes *(Continued)*

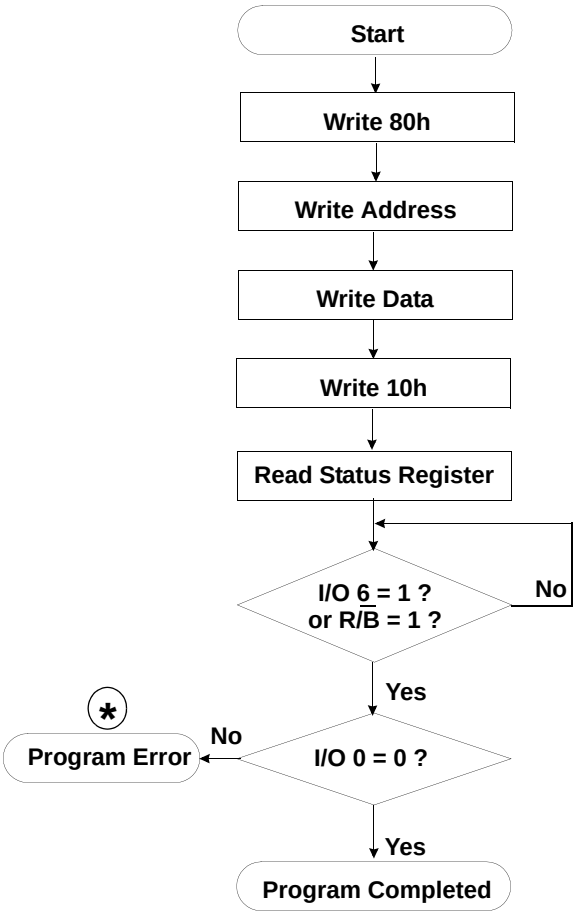
Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure rate in the qualification report does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bits detection

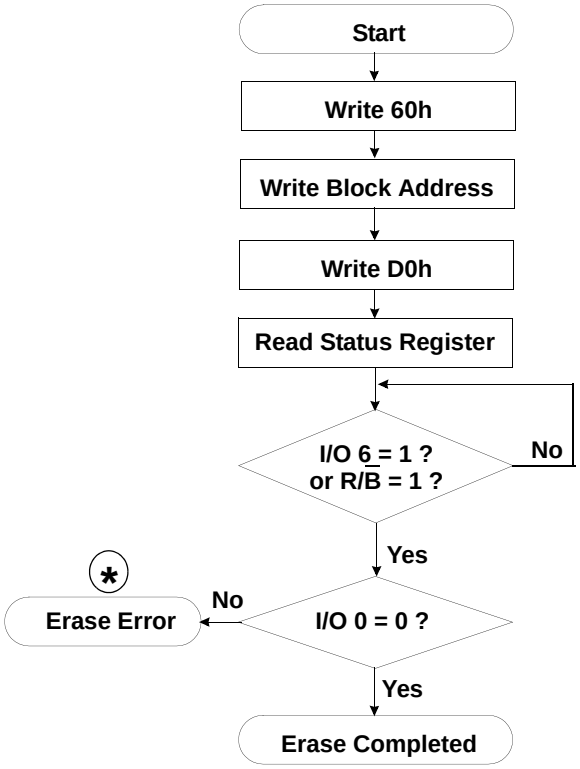
Program Flow Chart



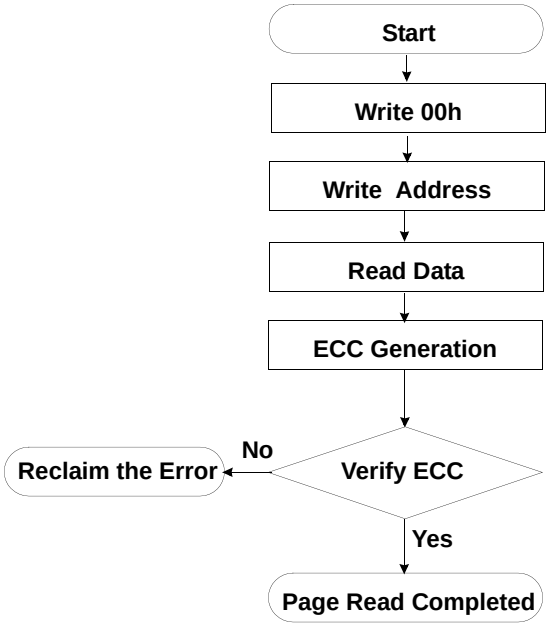
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes (Continued)

Erase Flow Chart

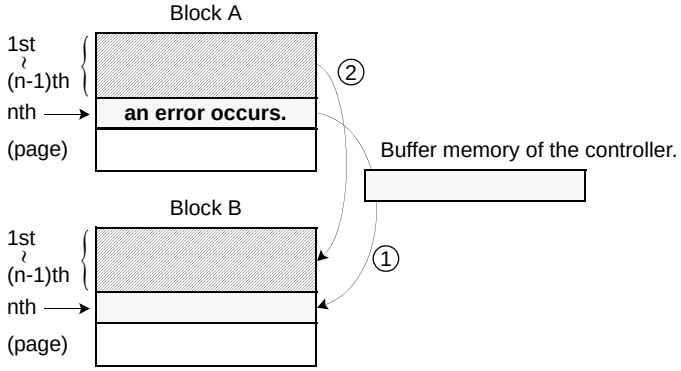


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1. When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2. Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3. Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4. Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Pointer Operation of K9F1208X0C

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

Table 2. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

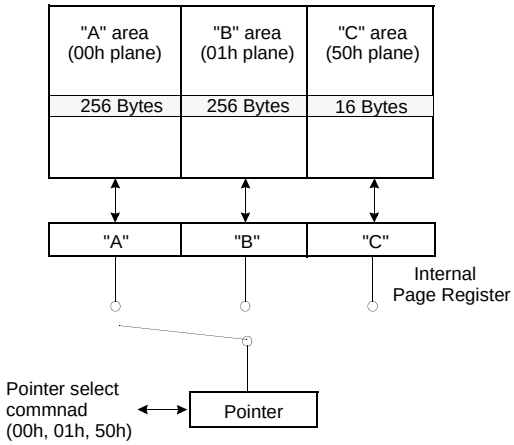
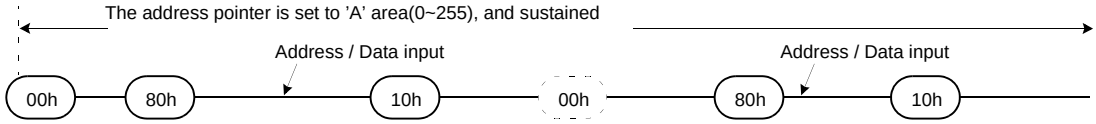


Figure 4. Block Diagram of Pointer Operation

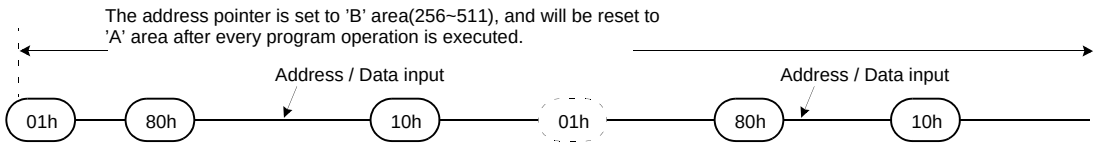
(1) Command input sequence for programming 'A' area



'A','B','C' area can be programmed.
It depends on how many data are inputted.

'00h' command can be omitted.

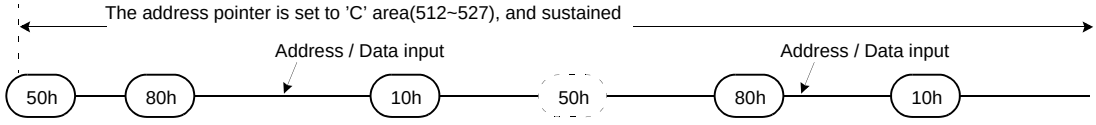
(2) Command input sequence for programming 'B' area



'B', 'C' area can be programmed.
It depends on how many data are inputted.

'01h' command must be rewritten before
every program operation

(3) Command input sequence for programming 'C' area



Only 'C' area can be programmed.

'50h' command can be omitted.

System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528bytes page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 5. Program Operation with $\overline{CE}$ don't-care.

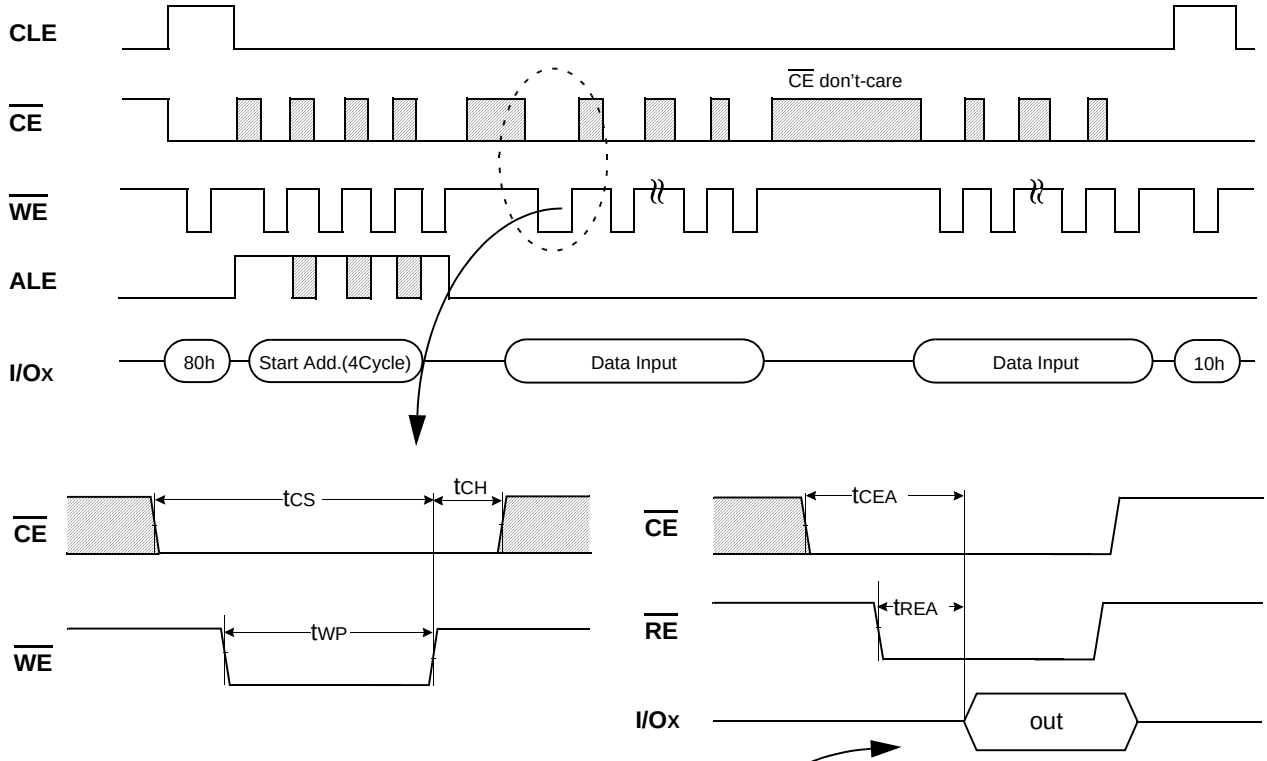
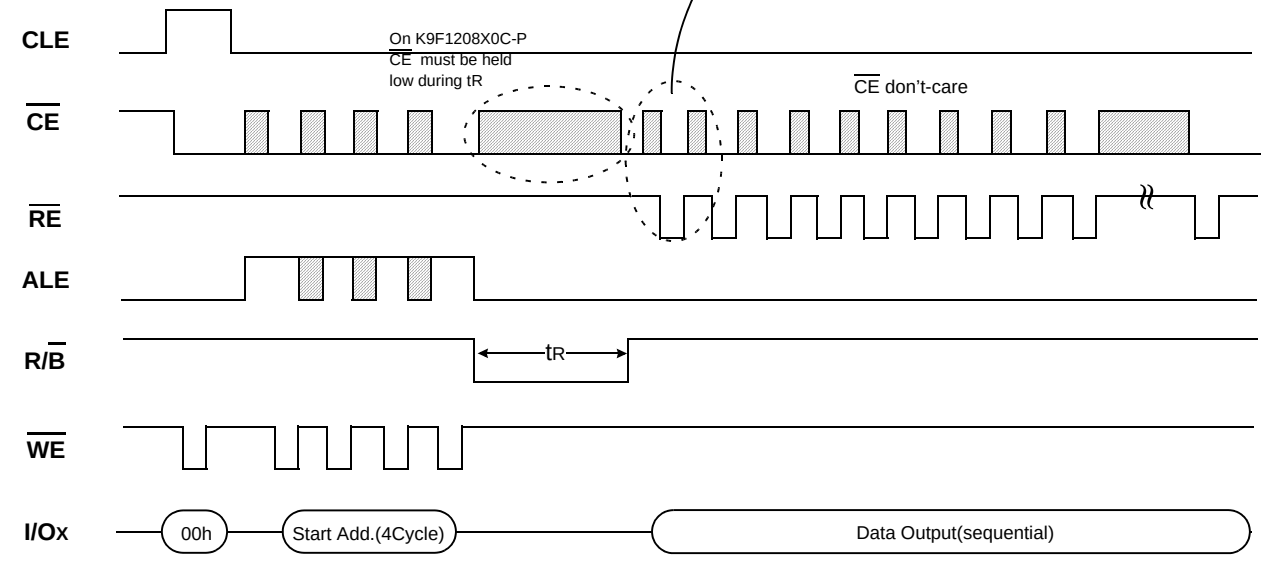
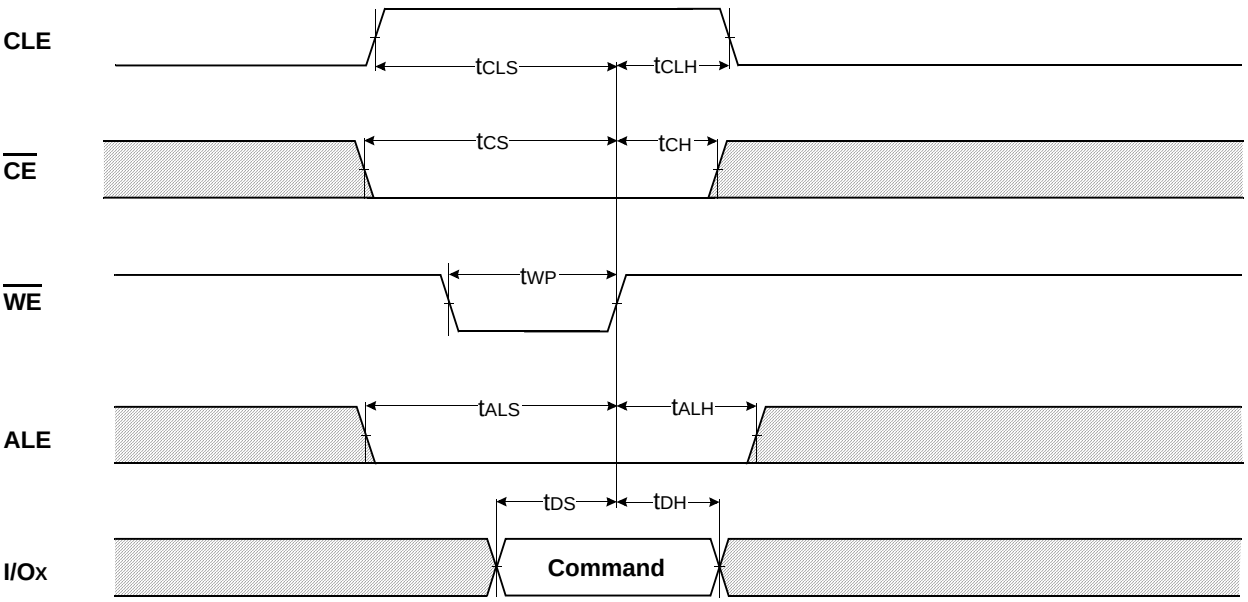


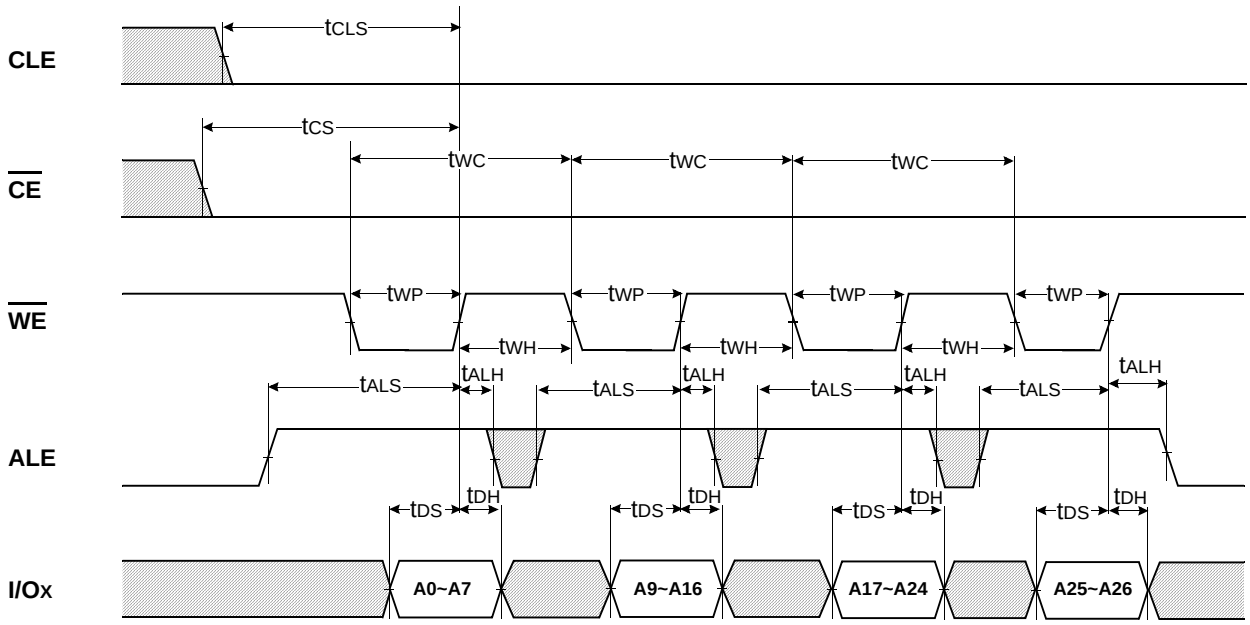
Figure 6. Read Operation with $\overline{CE}$ don't-care.



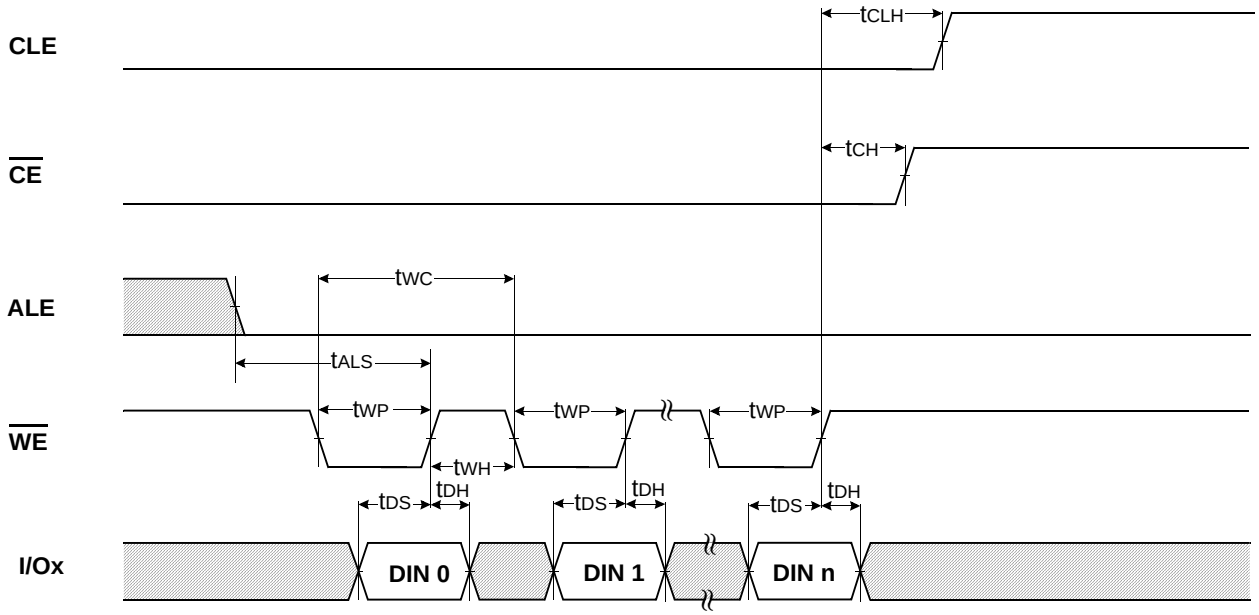
*** Command Latch Cycle**



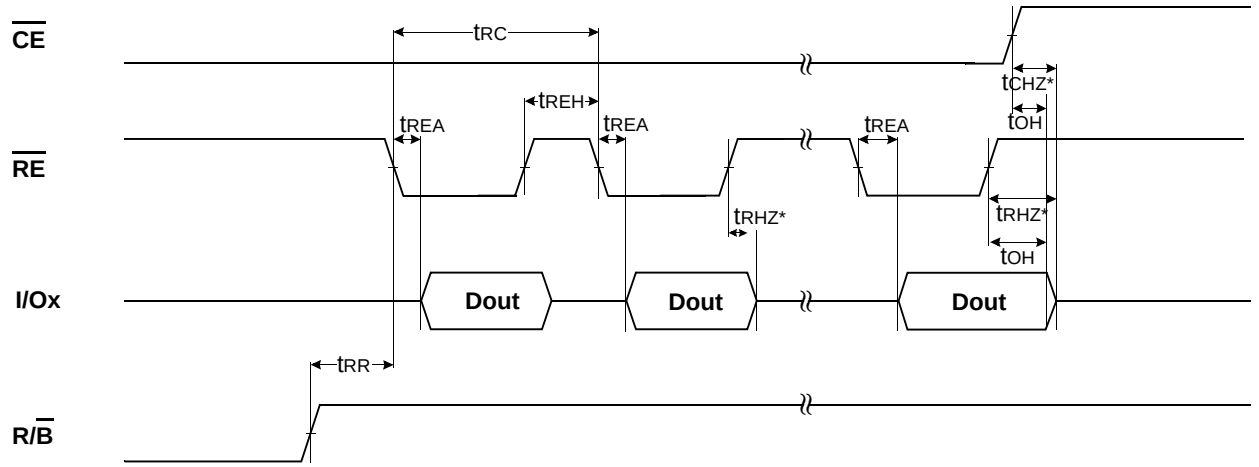
*** Address Latch Cycle**



*** Input Data Latch Cycle**

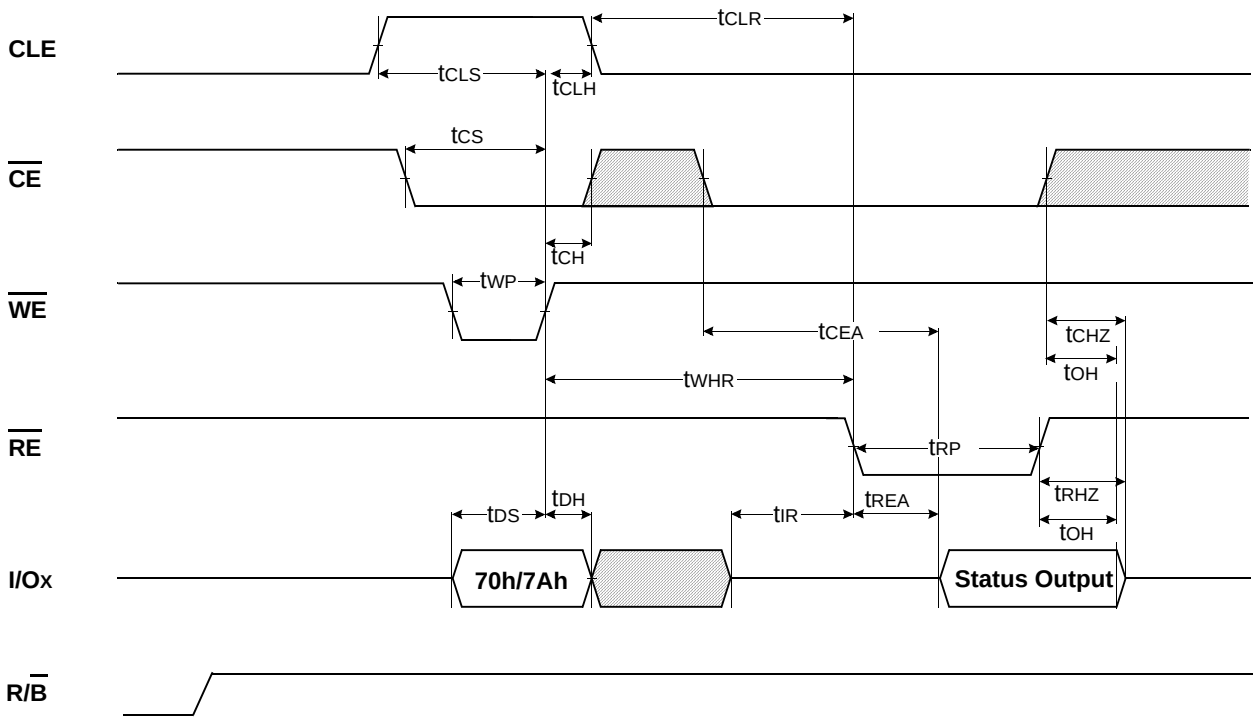


*** Serial access Cycle after Read**(CLE=L, $\overline{WE}$=H, ALE=L)

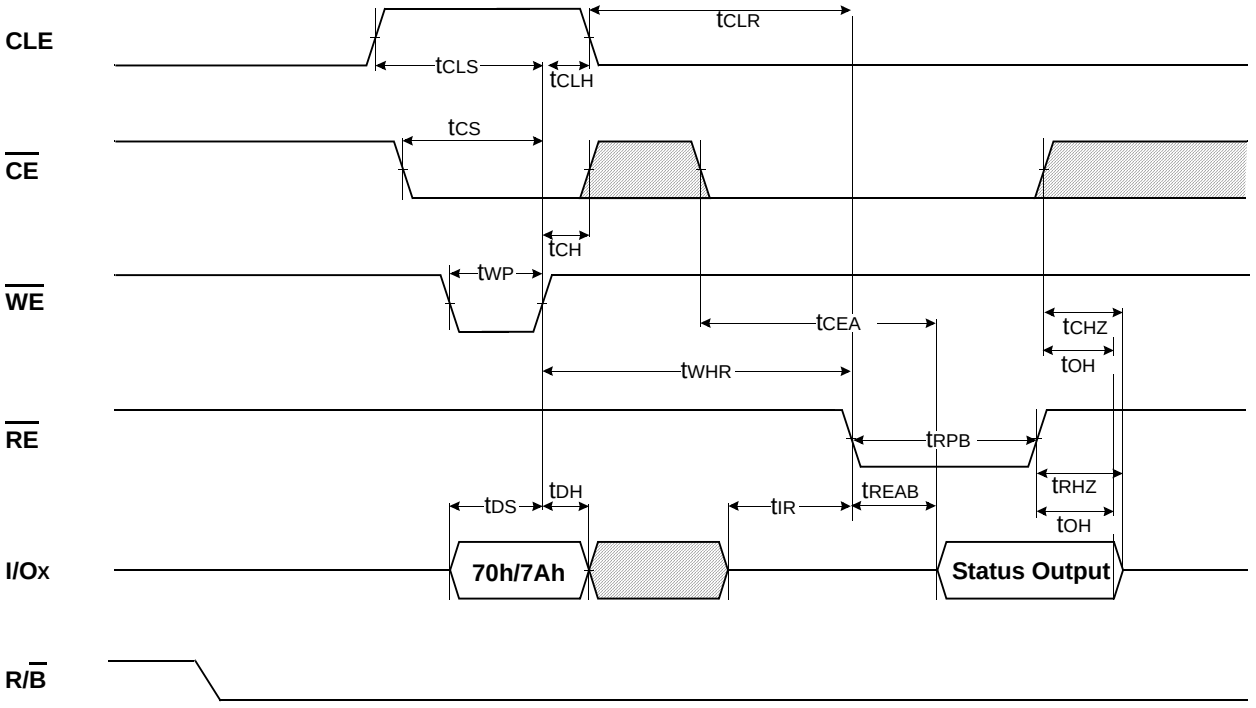


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

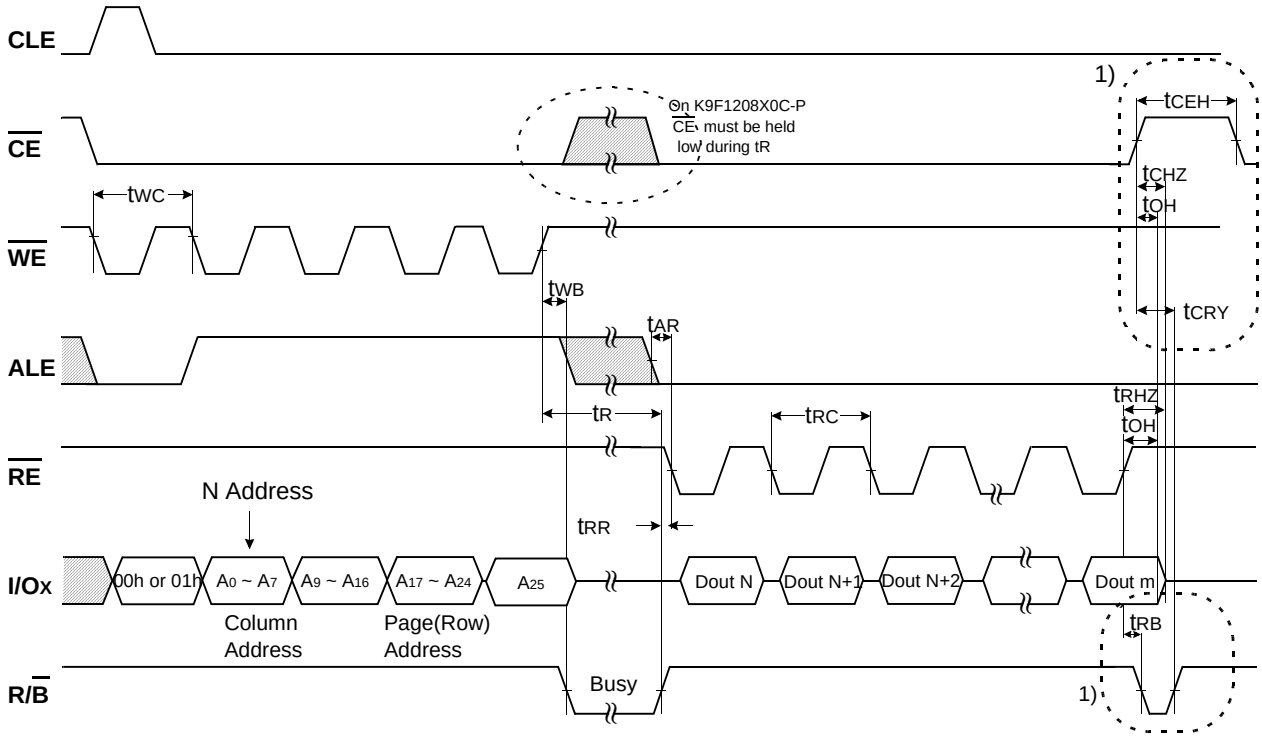
Status Read Cycle (During Ready State)



Status Read Cycle (During Busy State)



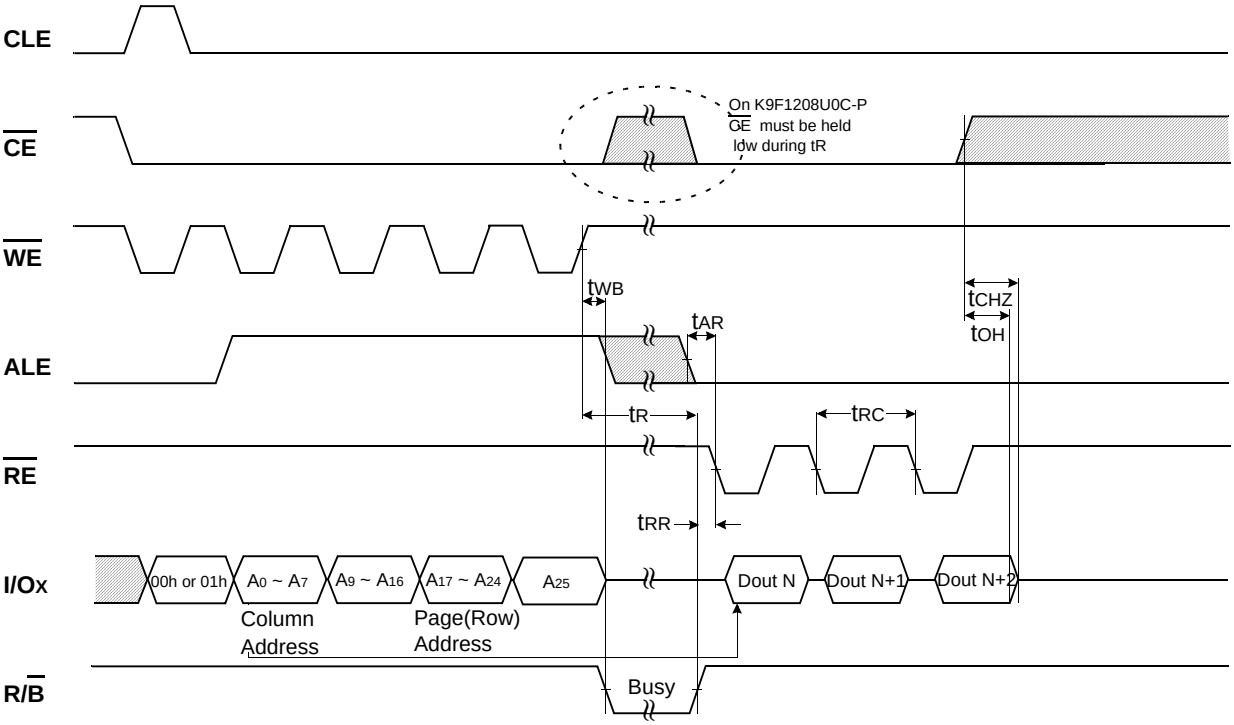
READ1 OPERATION (READ ONE PAGE)



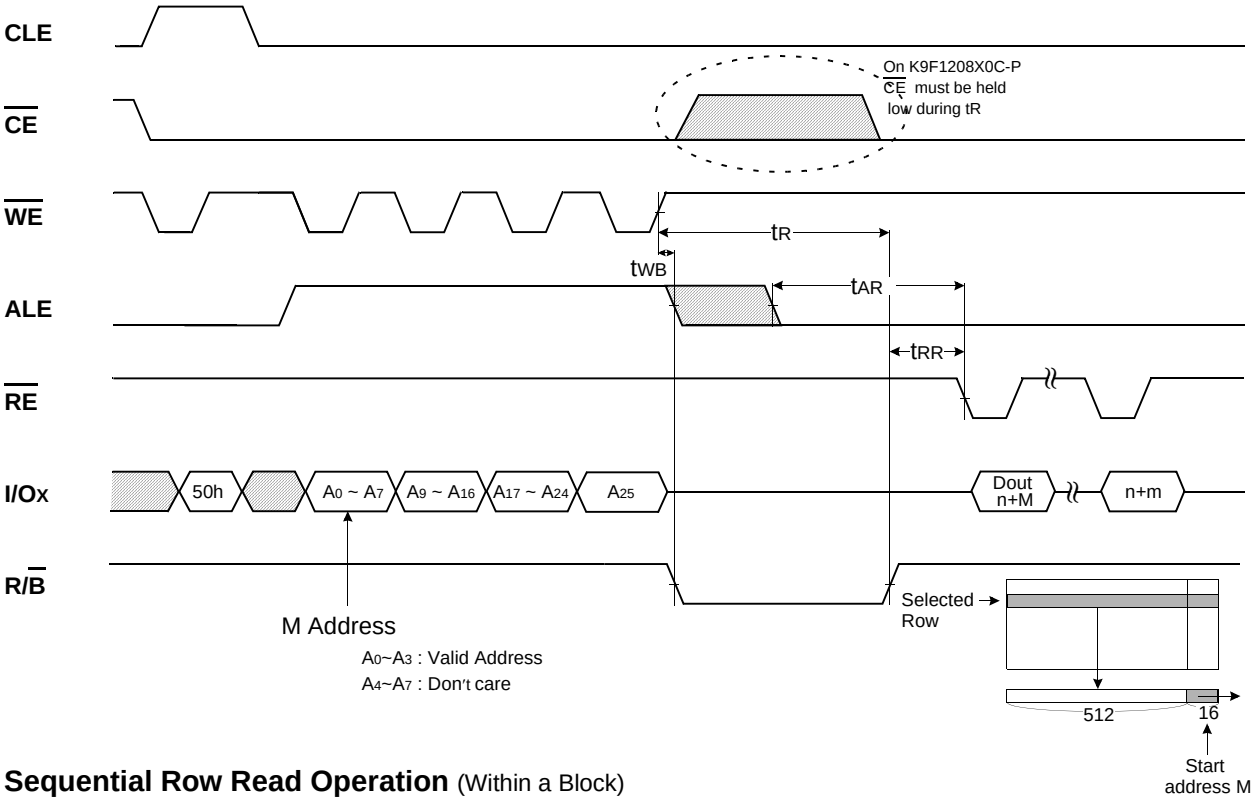
X8 device : m = 528 , Read CMD = 00h or 01h

NOTES : 1) is only valid on K9F1208X0C-P

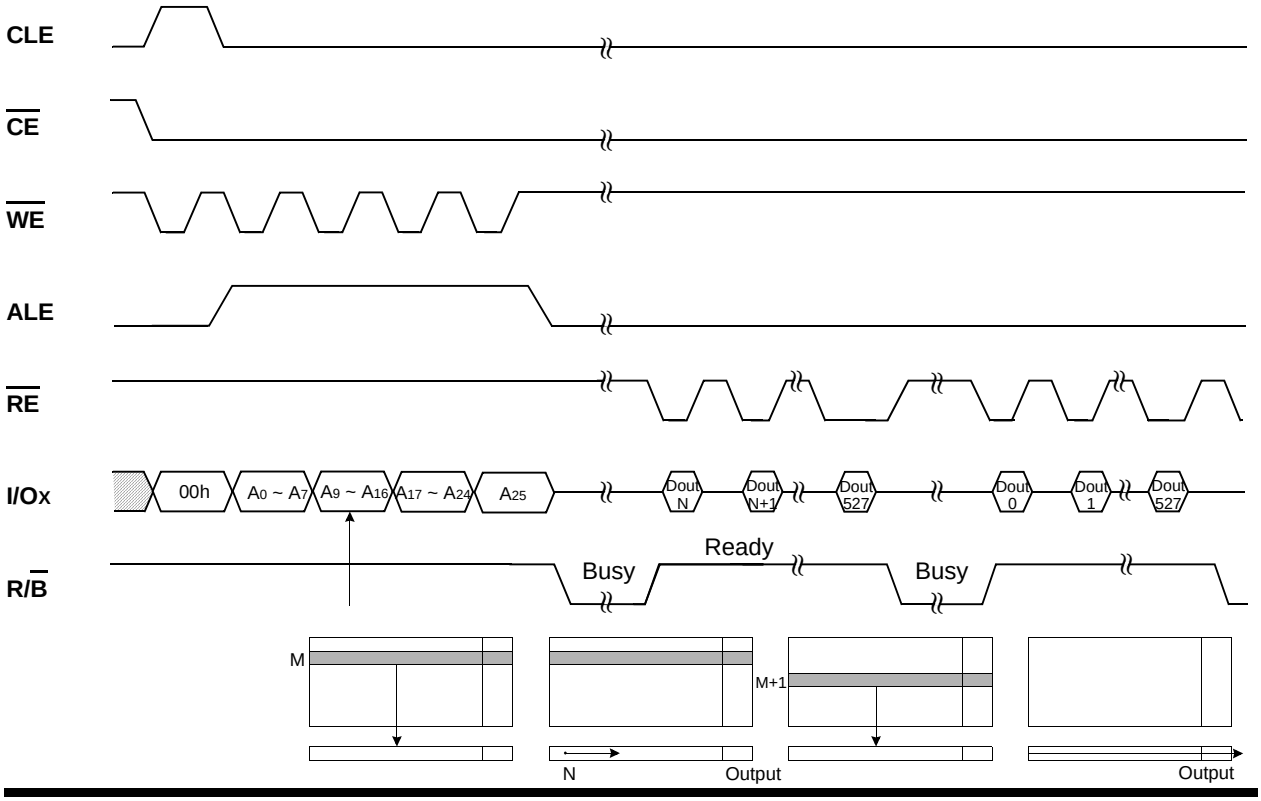
Read1 Operation (Intercepted by CE)



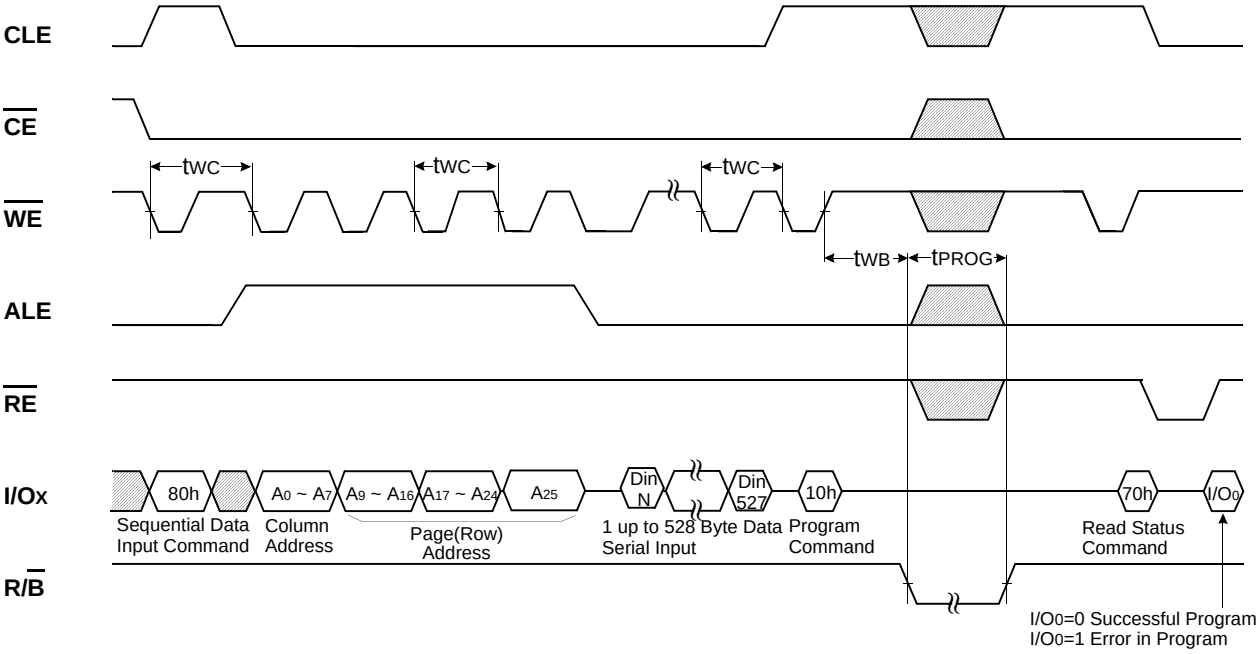
Read2 Operation (Read One Page)



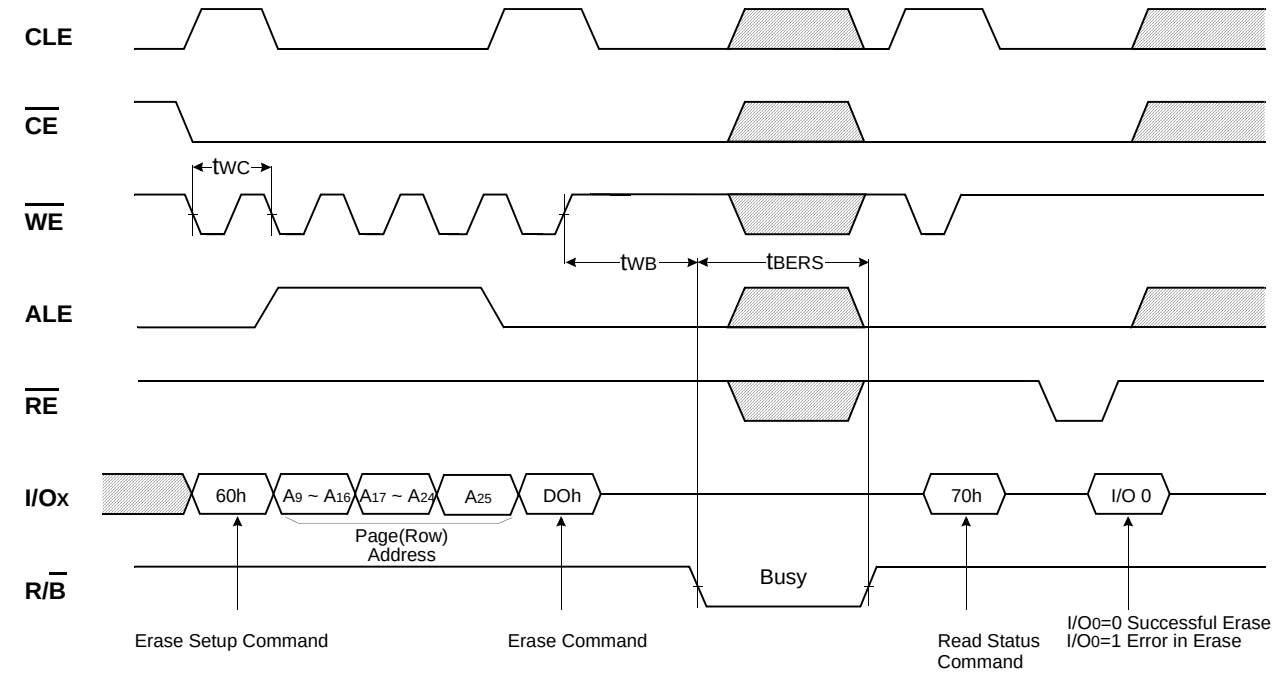
Sequential Row Read Operation (Within a Block)



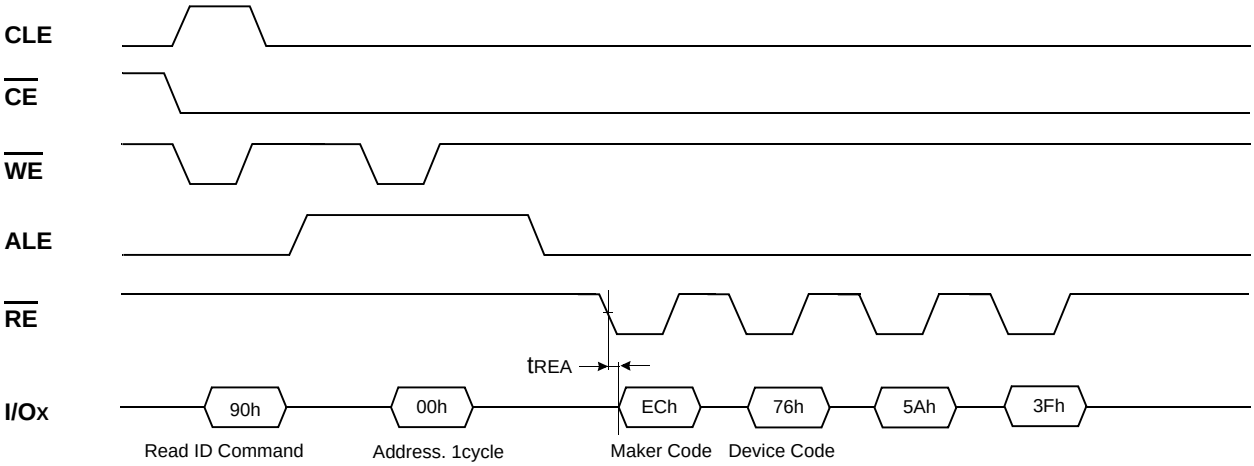
Page Program Operation



Block Erase Operation (Erase One Block)



Read ID Operation



ID Defintition Table
90 ID : Access command = 90H

	Value	Description
1st Byte	ECh	Maker Code
2nd Byte	76h	Device Code
3rd Byte	5Ah	Don't support Copy Back Operation
4th Byte	3Fh	Don't support Multi Plane Operation

Device Operation

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.

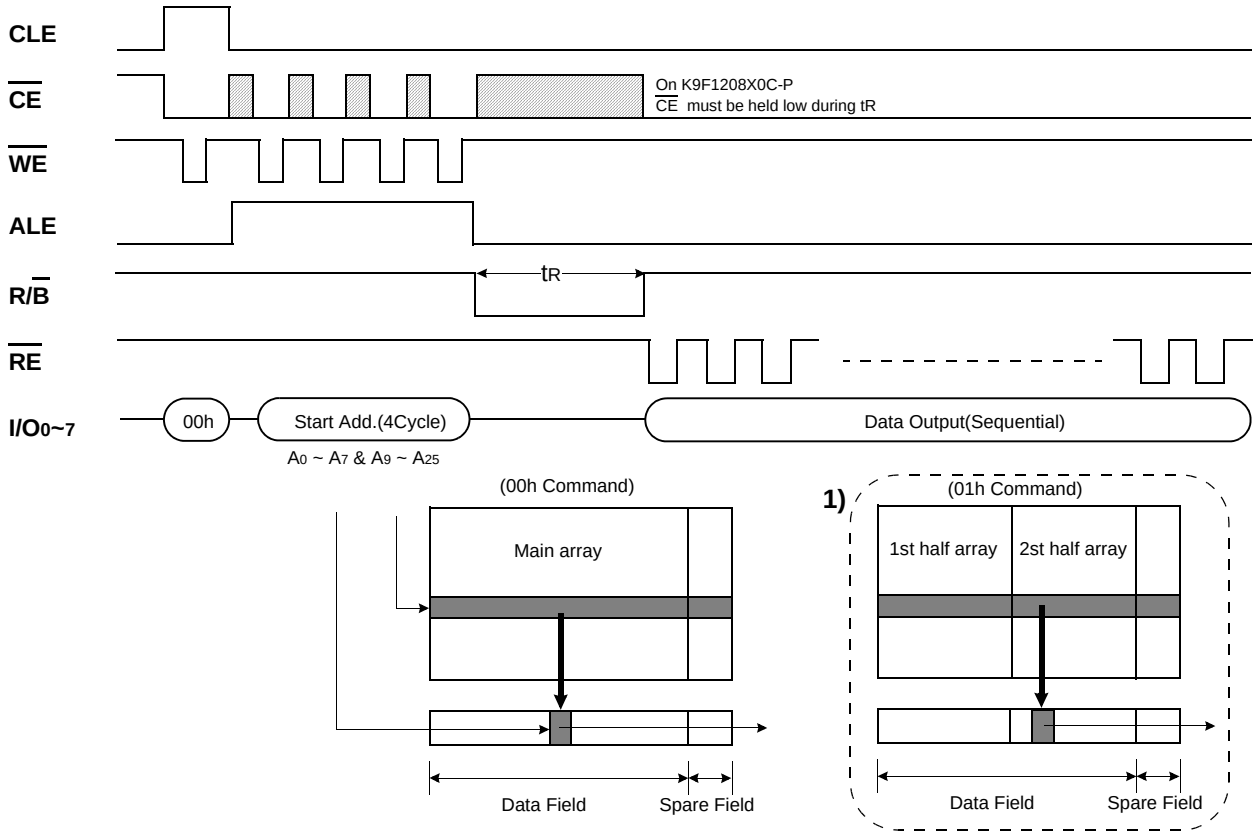
The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 15μs(t_R). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. $\overline{CE}$ must be held low while in busy for K9F1208X0C-PXB0, while $\overline{CE}$ is don't-care with K9F1208X0C-JXB0. If $\overline{CE}$ goes high before the device returns to Ready, the random read operation is interrupted and Busy returns to Ready as the defined by tCRY. Since the operation was aborted, the serial page read does not output valid data. Once the data in a page is loaded into the registers, they may be read out in 42ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 512 to 527 bytes may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 7 to 10 show typical sequence and timings for each read operation.

Sequential Row Read is available only on K9F1208X0C-P :

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 15μs again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is readout, the sequential read operation must be terminated by bringing $\overline{CE}$ high. When the page address moves onto the next block, read command and address must be given. Figures 9, 10 show typical sequence and timings for sequential row read operation.

Figure 7. Read1 Operation



NOTE :
1) After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 8. Read2 Operation

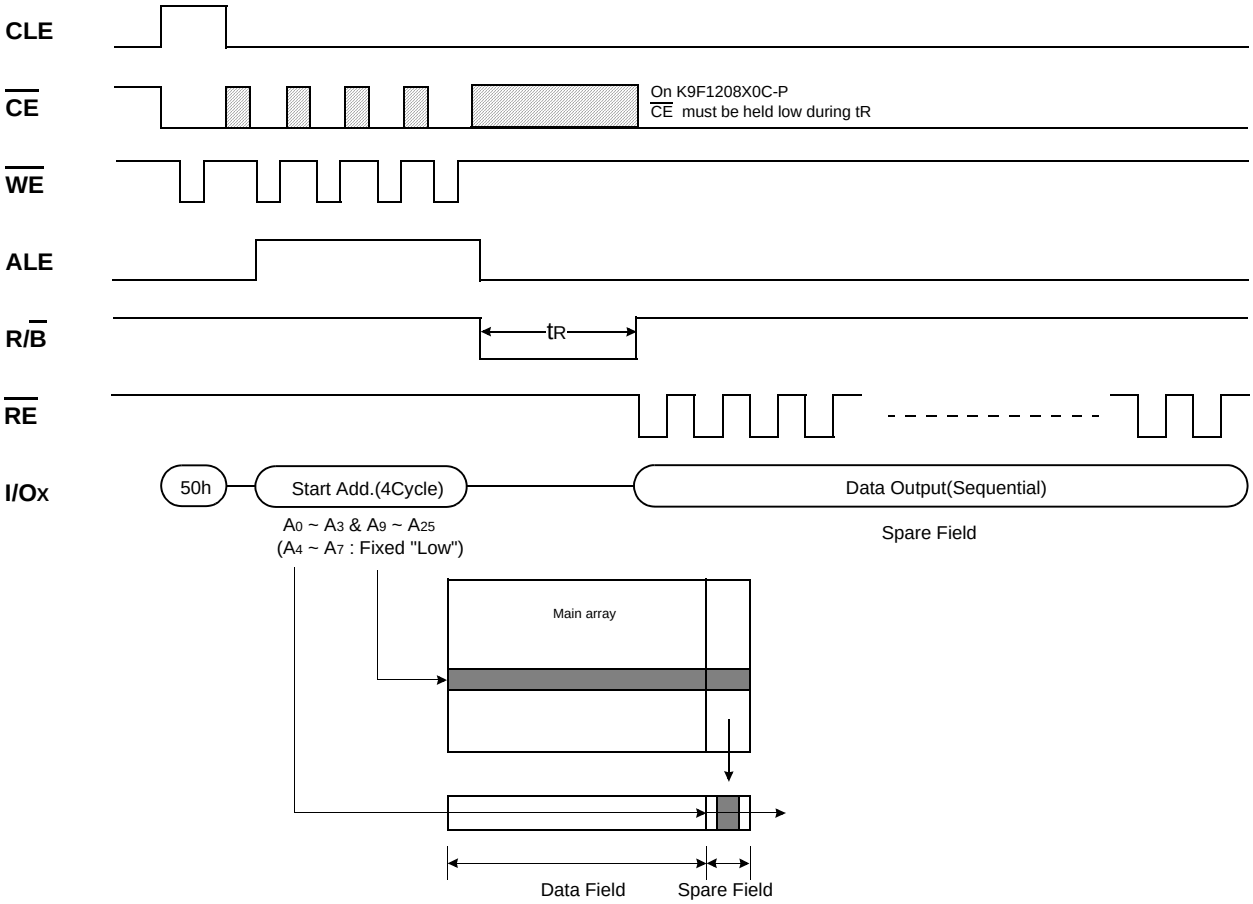
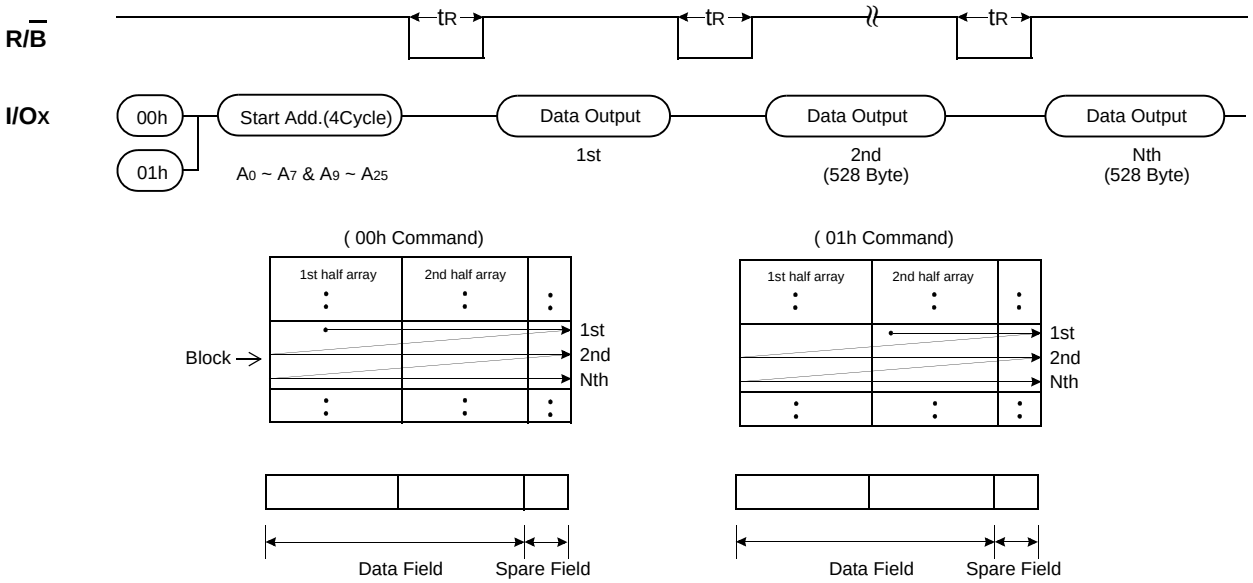
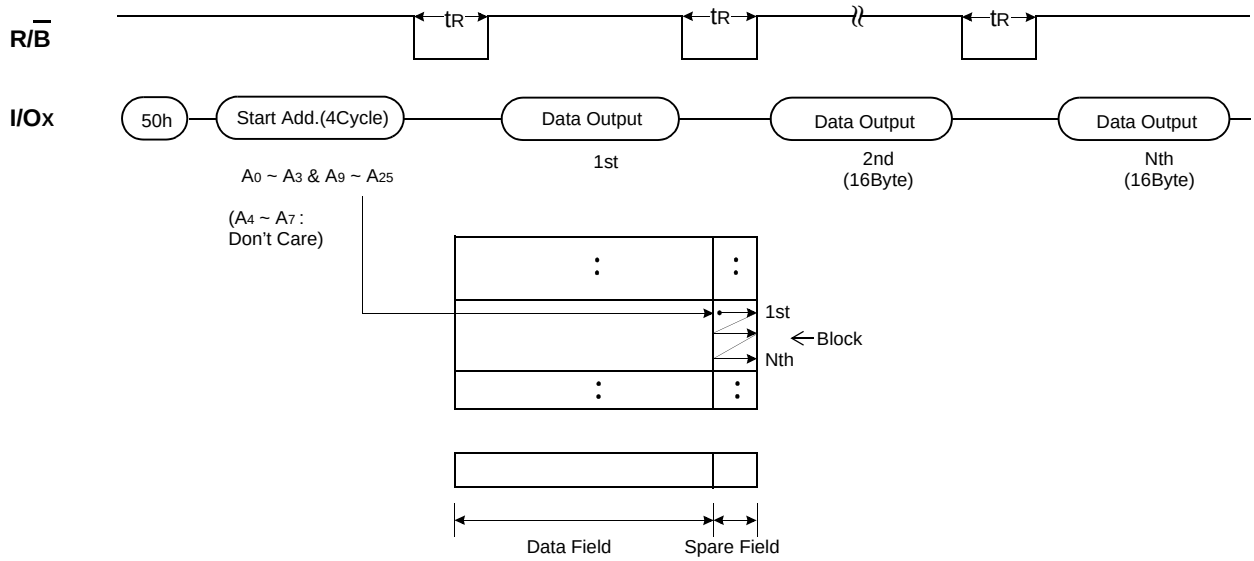


Figure 9. Sequential Row Read1 Operation (only for K9F1208X0C-P valid within a block)



The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read-out, the sequential read operation must be terminated by bringing $\overline{CE}$ high. When the page address moves onto the next block, read command and address must be given.

Figure 10. Sequential Row Read2 Operation (only for K9F1208X0C-P valid within a block)

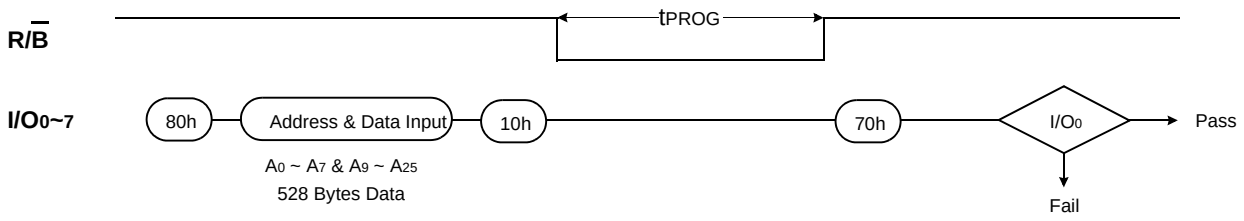


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte or consecutive bytes up to 528 byte, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 11). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure11. Program Operation

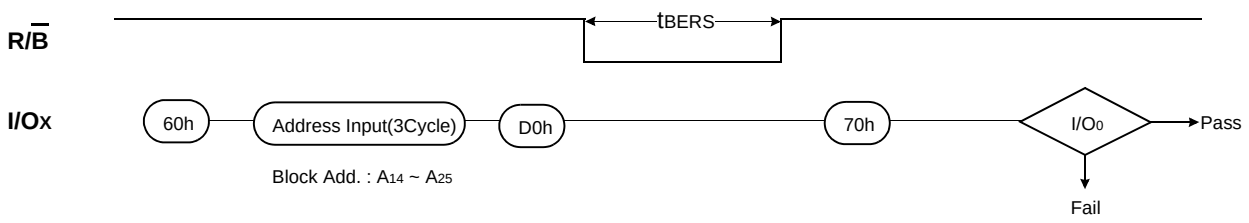


BLOCK ERASE

The Erase operation is done on a block(16K Bytes) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{14} to A_{26} is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 8 details the sequence.

Figure 12. Block Erase Operation



BLOCK PROTECT

Each block is protected from programming and erasing, controlled by the protect flag written in a specified area in the block. Block Proctect opreation is initiated by wirting 4xh-80h-10h to the command register along with four address cycles. Only address A_{14} to A_{26} is valid while A_0 to A_{13} is fixed as 00h. The data must not be loaded. Once the Block Protect opreation starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of Page Program operation for protecting a block by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while Block Protect operation is in progress. But, if Reset command is inputted while Block Protect operation is in progress, the block will not be guaranteed whether it is protected or not. When the Page Program operation for protecting a block is completed, the Write Status Bit(I/O 0) may be checked(Figure 13). The command register remains in Read Status command mode until another valid command is written to the command register.

When programming is prohibited by 41h command, the protect flag and the data of protected block can be erased by Block Erase operation. Once erasing is prohibited by 42h/43h command, the protect flag and the data of protected block can not be erased. If 80h-10h is written to command register along with four address cycles at the program protected block or at the program/erase protected block, and if 60h-D0h is written to command register along with three address cycles at the program/erase protected block, the R/$\overline{B}$ pin changes to low for tR. The Block Protect operation must not be excuted on the aleady protected block. The Block Protect operation will be aborted by Reset command(FFh). The Block Protect operation can only be used from first block to 200th block.

The device contains a Status Register which may be used to read out the state of the selected block. After writing 7Ah command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last(Figure 14). Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it.

Three commands are provided to protect the block.

41h : Programming is prohibited
42h : Erasing is prohibited
43h : Both programming and erasing are prohibited

Figure 13. Block Protect Operation

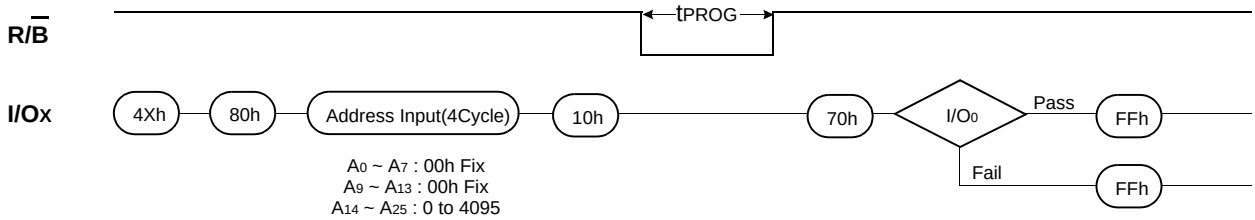


Figure 14. Read Block Status

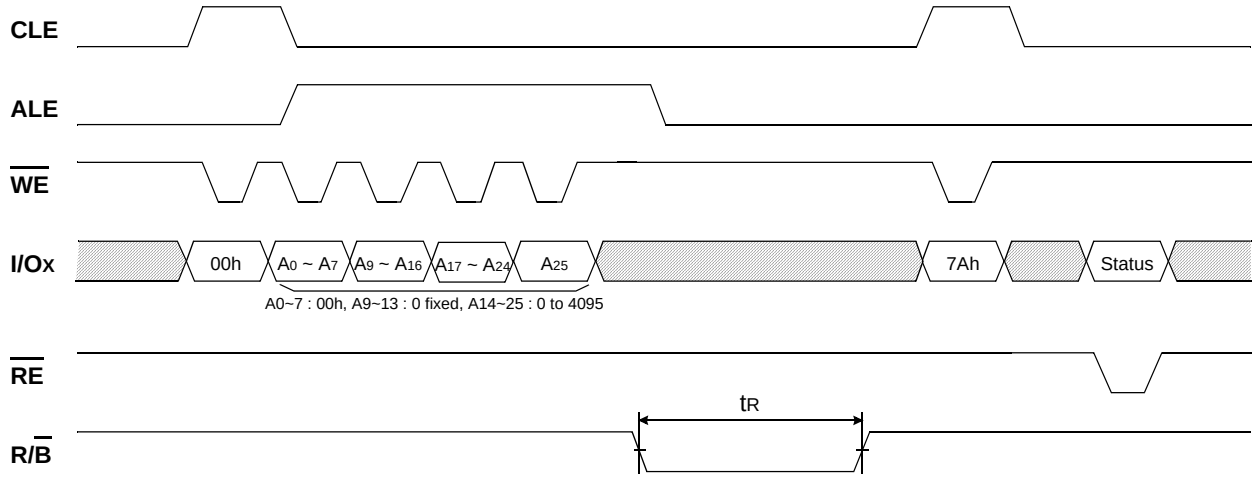


Table 3. Status Register Definition for 7Ah Command

I/O	Status	Definition	
I/O 0	Programming Protect	Not protected : "0"	Protected : "1"
I/O 1	Erasing Protect	Not protected : "0"	Protected : "1"
I/O 2	Not use	Don't -cared	
I/O 3	Not Use	Don't -cared	
I/O 4	Not Use	Don't -cared	
I/O 5	Not Use	Don't -cared	
I/O 6	Device Operation	Busy: "0"	Ready : "1"
I/O 7	Write Protect	Protected : "0"	Not protect : "1"

NOTE :
1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

Table 4. Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared
I/O 2	Not use	Not use	Not use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

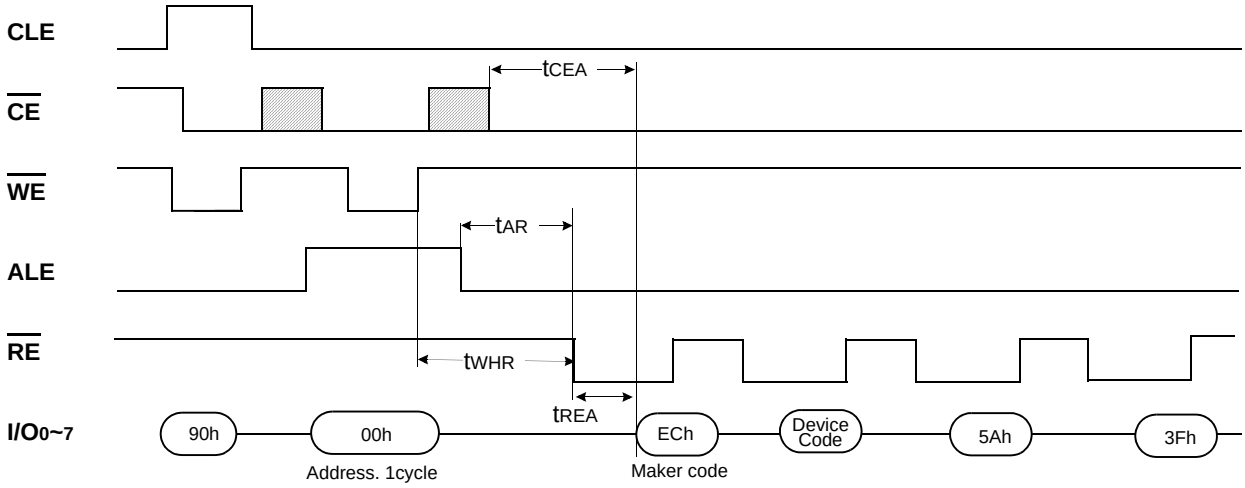
NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd, 4th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 15 shows the operation sequence.

Figure 15. Read ID Operation



Device	Device Code
K9F1208R0C	36h
K9F1208B0C	76h
K9F1208U0C	76h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written. Refer to Figure 16 below.

Figure 16. RESET Operation

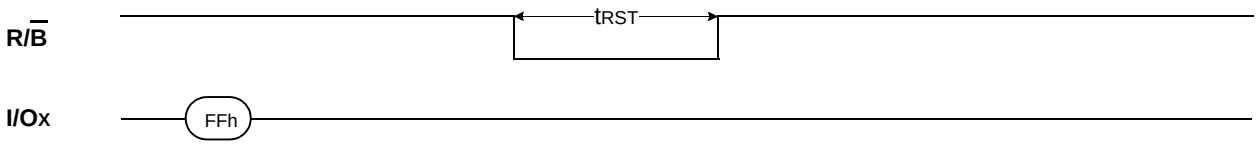
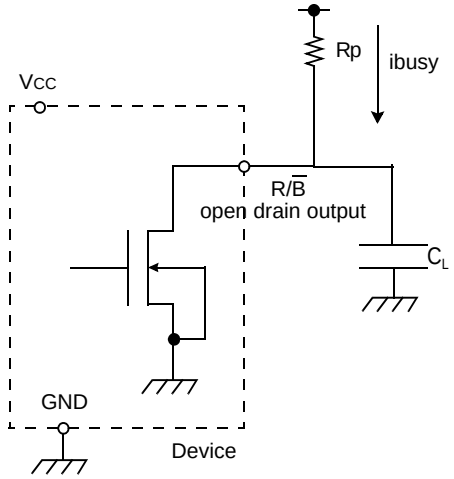


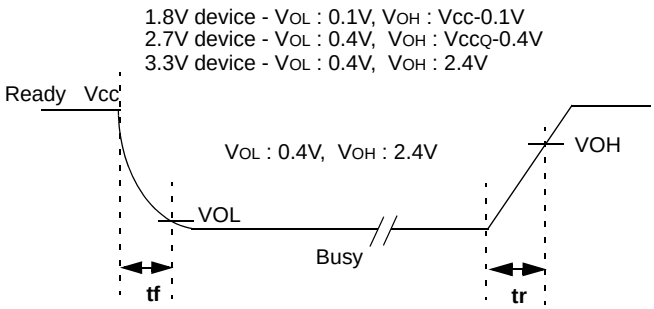
Table 5. Device Status

	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

READY/$\overline{\text{BUSY}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 17). Its value can be determined by the following guidance.





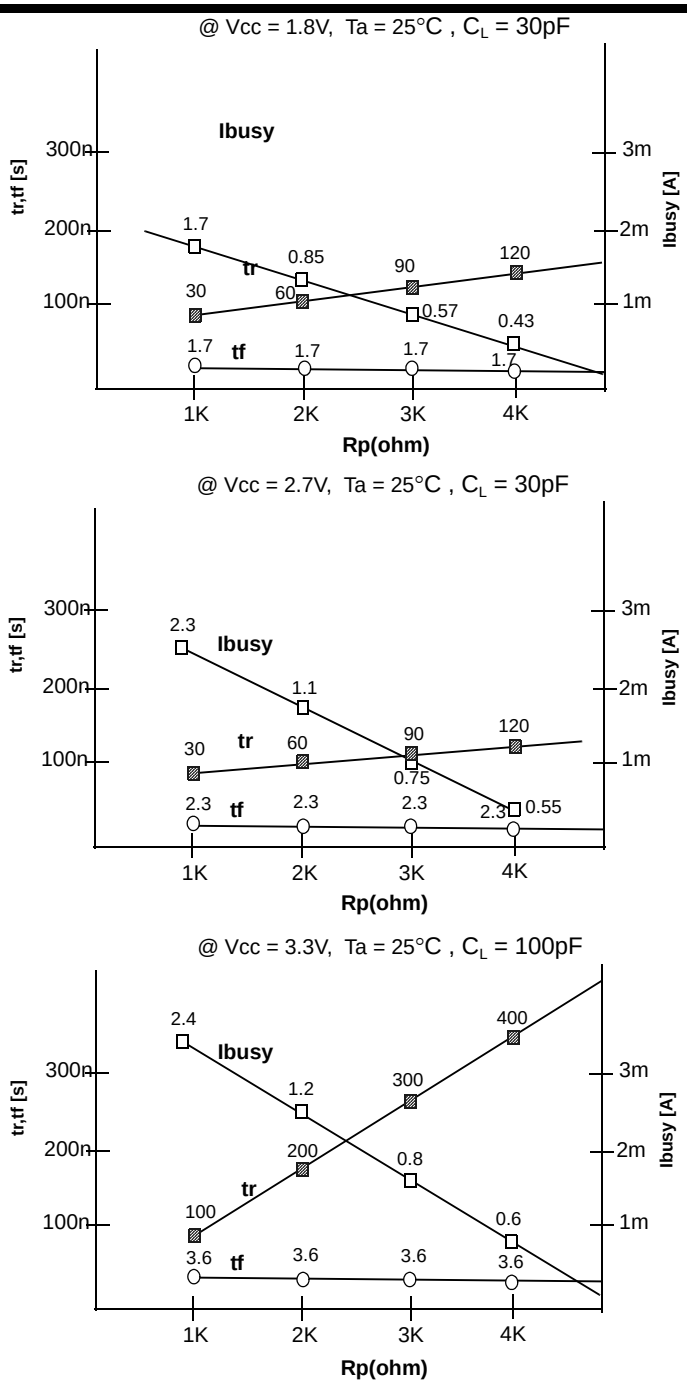


Figure 17. Rp vs tr ,tf & Rp vs ibusy

Rp value guidance

$$Rp(min, 1.8V part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

$$Rp(min, 2.7V part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{2.5V}{3mA + \Sigma I_L}$$

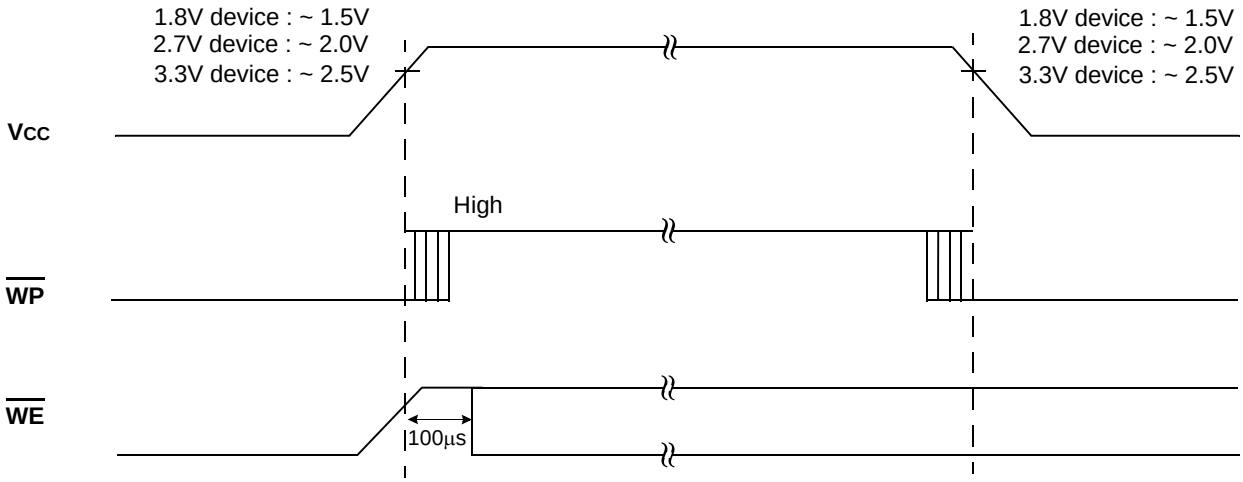
$$Rp(min, 3.3V part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power-up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V(1.8V device), 1.8V(2.7V device), 2V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 100μs is required before internal circuit gets ready for any command sequences as shown in Figure 18. The two step command sequence for program/erase provides additional software protection.

Figure 18. AC Waveforms for Power Transition



$\overline{WP}$ AC Timing guide

Enabling $\overline{WP}$ during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Figure A-1. Program Operation

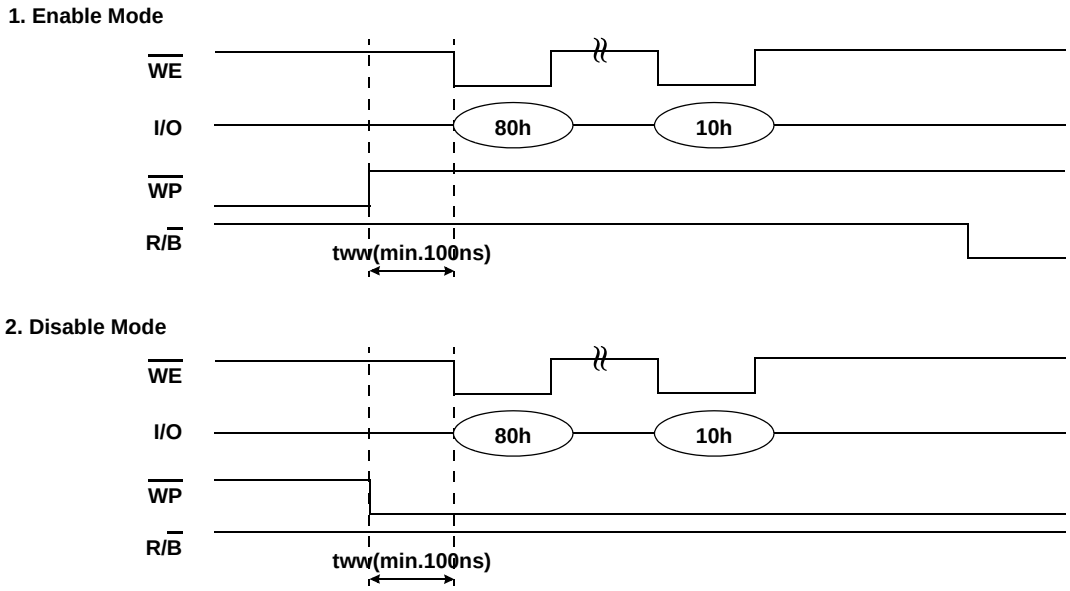


Figure A-2. Erase Operation