



UNIVERSITÀ
DEGLI STUDI
FIRENZE

Parallel Programming

Final assignment

Lucia Giorgi

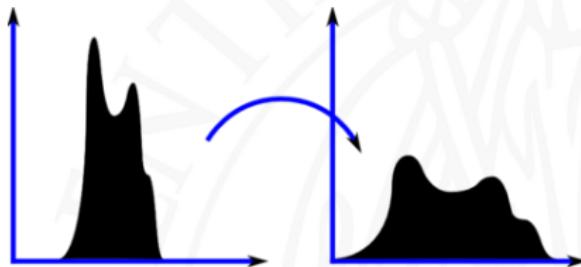
12/01/24



- 1 Histogram Equalization
- 2 Cuda
- 3 Experiments and results



Histogram equalization is a digital image processing method by which you can calibrate the contrast using the image histogram.



Histogram Equalization



Figure: Image before and after histogram equalization



Histogram Equalization

- Compute the histogram: for every possible value of a pixel (0 - 255) count how many pixels have that value $p(v)$ for $v \in [0, L - 1]$, $L = 256$



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- Compute the CDF:

$$\text{cdf}(v) = \sum_{k=1}^v p(k)$$



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- Compute the CDF:

$$\text{cdf}(v) = \sum_{k=1}^v p(k)$$

- For every image pixel compute the new value:

$$h(v) = \frac{\text{cdf}(v) - \text{cdf}_{\min}}{MN - \text{cdf}_{\min}} \cdot (L - 1)$$



Histogram Equalization

RGB → HSV → histogram equalization on V → RGB

Three kernels:

- `histogram()`
generates the histogram from the input image
- `Brent_Kung_scan_kernel()`
calculates the CDF
- `equalizer()`
generates the output image



Histogram

- $M \cdot N$ threads
- $\text{BLOCK_DIM_X} * \text{BLOCK_DIM_Y}$ threads per block
- **shared memory:** $256 * \text{sizeof(int)}$ bytes

Shared memory $256 * \text{sizeof(int)}$

0	1	2	3	...	255
1	0	0	0	0	0

Global memory

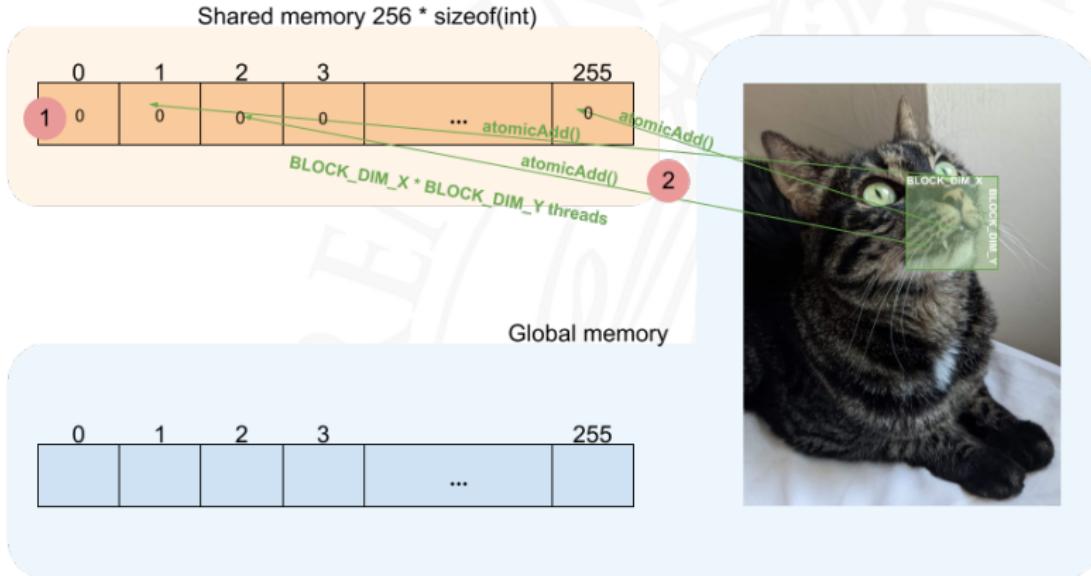
0	1	2	3	...	255





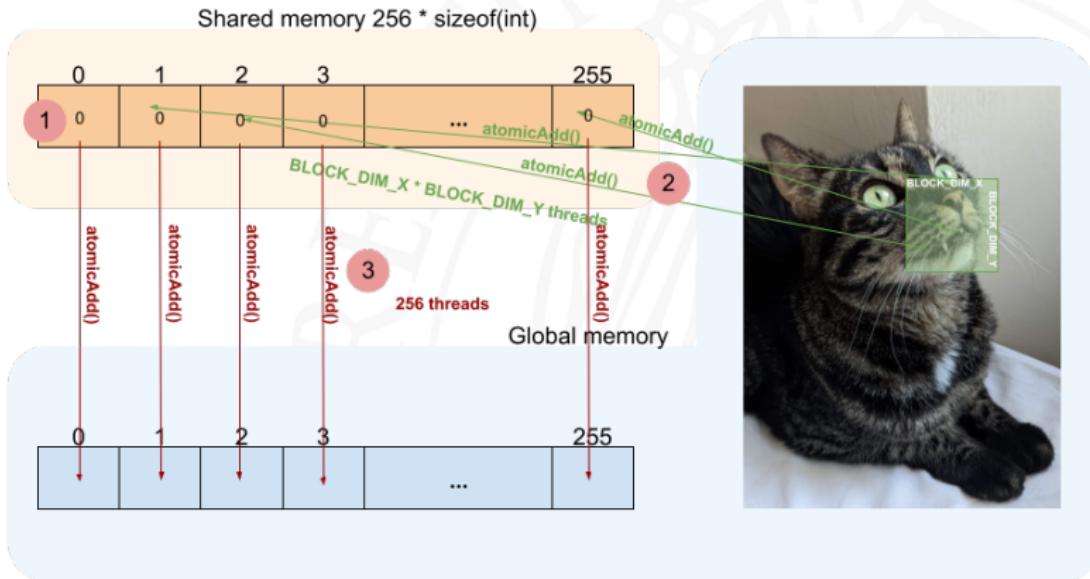
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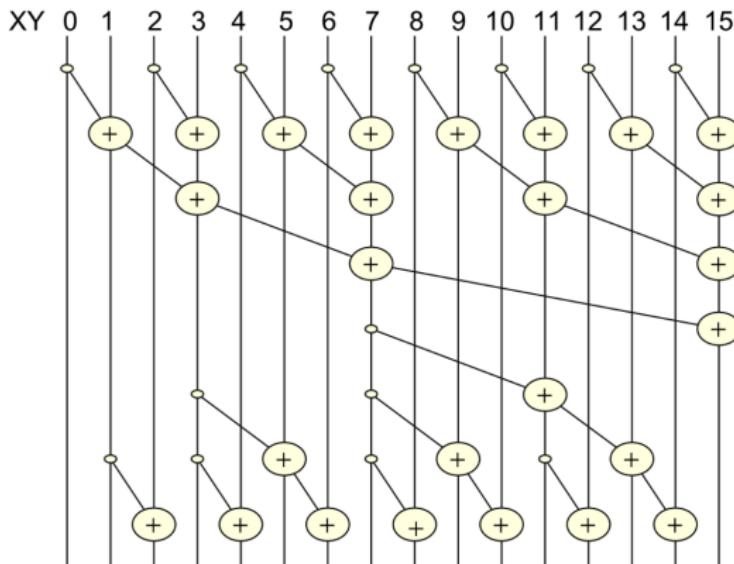




Histogram

```
__global__ void histogram(const unsigned char* image, int* hist, int width, int height) {
    __shared__ int HIST[HIST_SIZE];
    int tx = blockIdx.x * blockDim.x + threadIdx.x;
    int ty = blockIdx.y * blockDim.y + threadIdx.y;
    int t_id = tx + ty * width;
    int t_id_block = threadIdx.x + threadIdx.y * BLOCK_DIM_X;
    if (t_id_block < HIST_SIZE) { // shared memory initialization
        HIST[t_id_block] = 0;
    }
    __syncthreads();
    if (tx < width && ty < height) {
        atomicAdd(&(HIST[image[t_id]]), 1); // local histogram
    }
    __syncthreads();
    if (t_id_block < HIST_SIZE) {
        atomicAdd(&(hist[t_id_block]), HIST[t_id_block]); // global histogram
    }
}
```

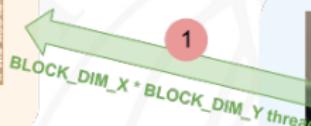
Based on the Brent–Kung adder design



Equalizer

- $M \cdot N$ threads
- $\text{BLOCK_DIM_X} * \text{BLOCK_DIM_Y}$ threads per block
- **shared memory:** $\text{BLOCK_DIM_X} * \text{BLOCK_DIM_Y} * \text{sizeof(int)}$ bytes

Shared memory
 $\text{BLOCK_DIM_X} * \text{BLOCK_DIM_Y} * \text{sizeof(int)}$



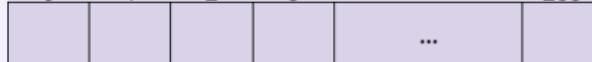
Global memory



Constant memory

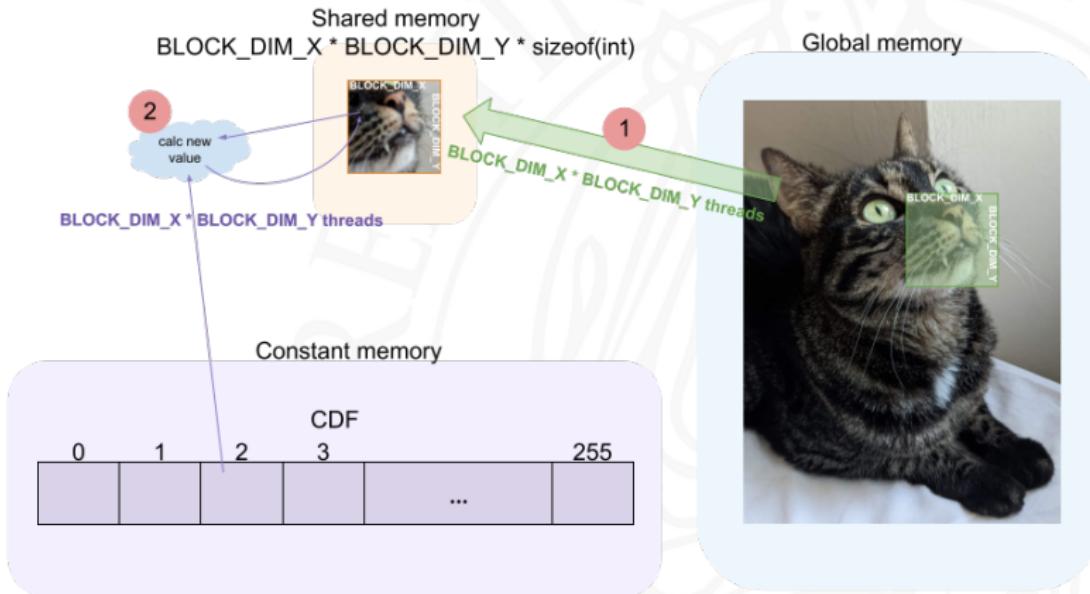
CDF

0 1 2 3 ... 255



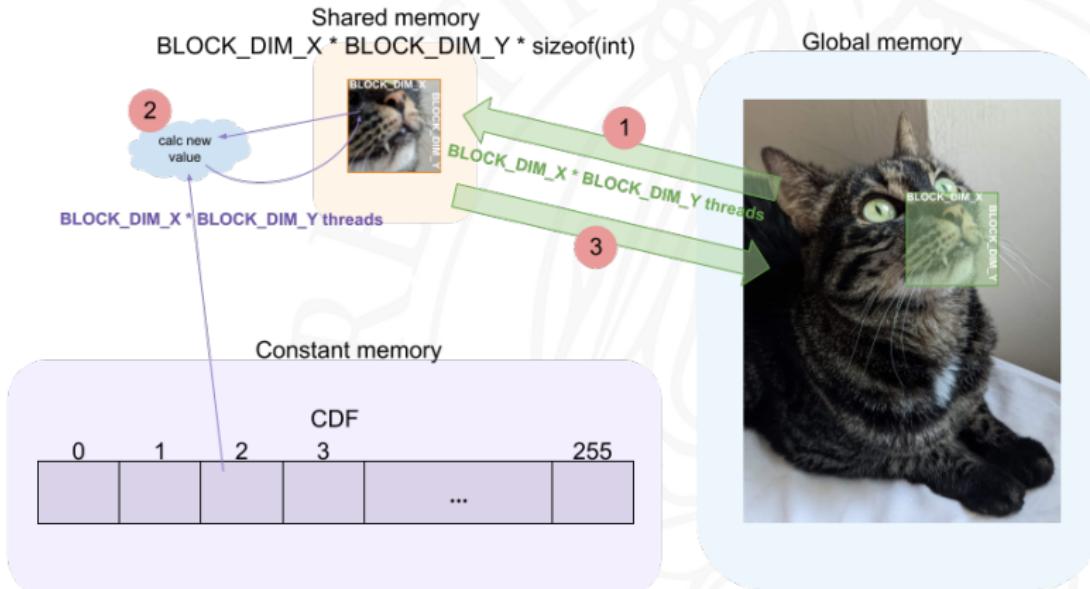
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Equalizer

```
__constant__ int d_CDF[HIST_SIZE];
__global__ void equalizer(unsigned char* image, int cdf_val_min, int width, int height) {
    __shared__ unsigned char IMG[BLOCK_DIM_X * BLOCK_DIM_Y];
    int tx = blockIdx.x * blockDim.x + threadIdx.x;
    int ty = blockIdx.y * blockDim.y + threadIdx.y;
    int t_id = tx + ty * width;
    int t_id_block = threadIdx.x + threadIdx.y * BLOCK_DIM_X;
    if (tx < width && ty < height) {
        IMG[t_id_block] = image[t_id];
    }
    __syncthreads();
    if (tx < width && ty < height) {
        IMG[t_id_block] = long(d_CDF[IMG[t_id_block]] - cdf_val_min) * (HIST_SIZE - 1) /
                           (width * height - cdf_val_min);
    }
    __syncthreads();
    if (tx < width && ty < height) {
        image[t_id] = IMG[t_id_block];
    }
}
```



Experiments

- Multiple image sizes
 - 10 images per size (5 vertical + 5 horizontal)

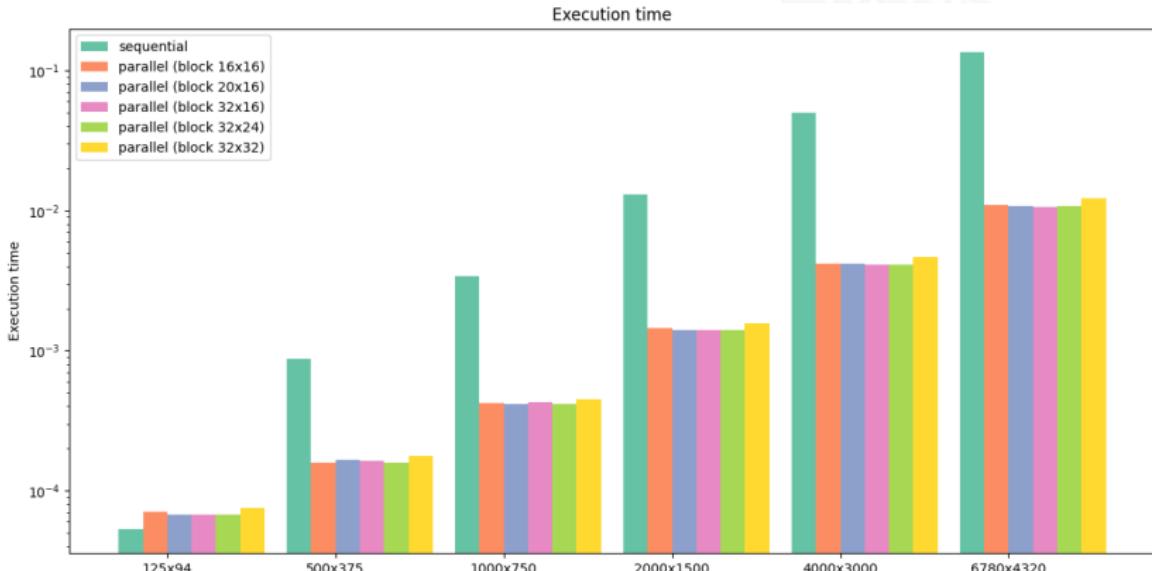
Experiments

- Multiple image sizes
 - 10 images per size (5 vertical + 5 horizontal)
- Multiple block sizes
 - ($\min \text{BLOCK_DIM_X} * \text{BLOCK_DIM_Y} = 256$)

Experiments

- Multiple image sizes
 - 10 images per size (5 vertical + 5 horizontal)
- Multiple block sizes
 - $(\min \text{BLOCK_DIM_X} * \text{BLOCK_DIM_Y} = 256)$
- “Dummy” image for initialization
 - NVIDIA Nsight Systems (profiling)

Results



Results

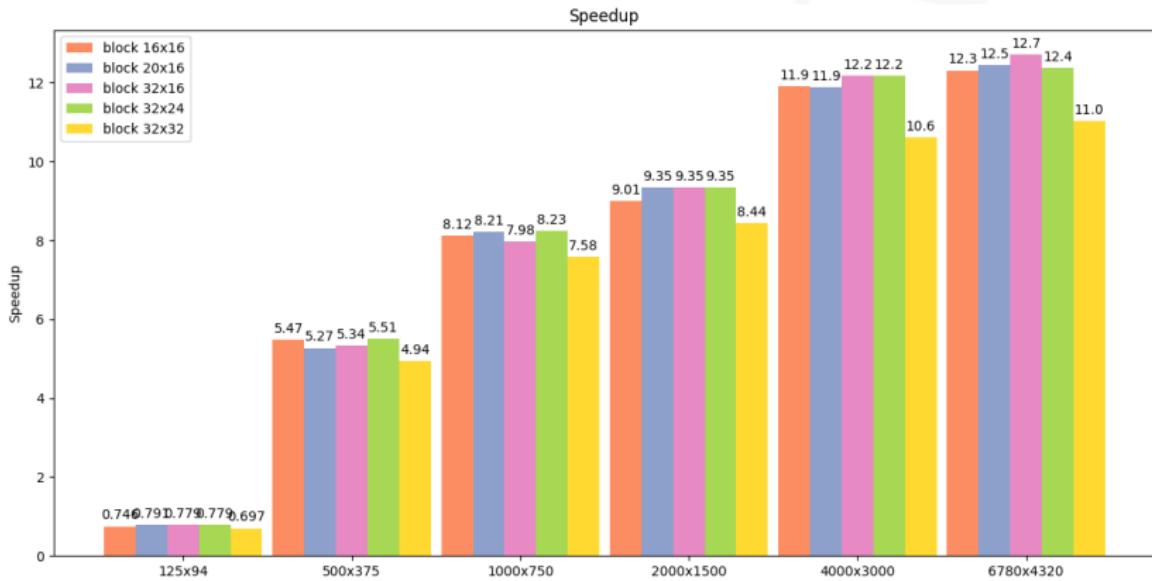


Figure: Speedup



Occupancy

In order to use

NVIDIA Nsight Compute - Occupancy Calculator

- `__host__ cudaError_t cudaGetDeviceProperties (cudaDeviceProp* prop, int device)`
for info about the GPU
 - total shared memory per multiprocessor
- `--ptxas-options=-v` flag in nvcc
for info about the kernels
 - number of registers
- NVIDIA website for the compute capability

Occupancy

- 67% for $32 \times 32 = 1024$ block size
- 83% for $20 \times 16 = 320$ block size
- 100% for the other block sizes

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Block size $32 \times 32 = 1024$:

- Maximum number of threads per SM: 1536
- Threads per SM for: 1024
- $1024/1536 = 0.67$



Equalizer

NVIDIA Night Compute

File Connectors Debug Profile Tools Window Help

Project Explorer Default Project

Search project.

Compute Capability: 3.6 Threads Per Block: 1024

Shared Memory Size Config (byte): 102400 Registers Per Thread: 27

Global Load Cache Mode: L1H2 (1x) User Shared Memory Per Block (bytes): 1024

Apply Reset

Tables Graph GPU Data

Occupancy Data

Property	Value
Active Threads per Multiprocessor	1024
Active Warps per Multiprocessor	32
Active Threadblocks per Multiprocessor	1
Occupancy of each Multiprocessor	67 %

Physical Limit of GPU (3.6):

Property	Limit
Threads per Warp	32
Max Warps per Multiprocessor	48
Max Threadblocks per Multiprocessor	1
Maximum Thread Block Size	1024
Registers per Multiprocessor	65536
Max Registers per Thread Block	65536
Max Registers per Thread	255
Shared Memory per Multiprocessor (bytes)	102400
Max Shared Memory per Block	102400
Register Allocation Unit Size	256
Max Registers per Register Allocation Unit	32768
Shared Memory Allocation Unit Size	128
Warp Allocation Granularity	4
Shared Memory Per Block (bytes) (CUBLA runtime use)	1024

Allocated Resources:

Resources	Per Block	Limit Per SM	Allocatable Blocks per SM
Warp (Threads Per Block / Threads Per Warp)	59	48	1
Registers (Warp limit per SM due to per warp reg count)	32	64	2
Shared Memory (bytes)	2048	102400	60

Occupancy Limiters:

Limited by	Blocks per SM	Warp Per Block	Warp Per SM
Max Warps or Max Blocks per Multiprocessor	1	32	32
Registers per Multiprocessor	2		
Shared Memory per Multiprocessor	50		

Posizioni

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