Integrated Device Technology, Inc.

FAST CMOS 18-BIT R/W BUFFER

IDT54/74FCT162701T/AT

FEATURES:

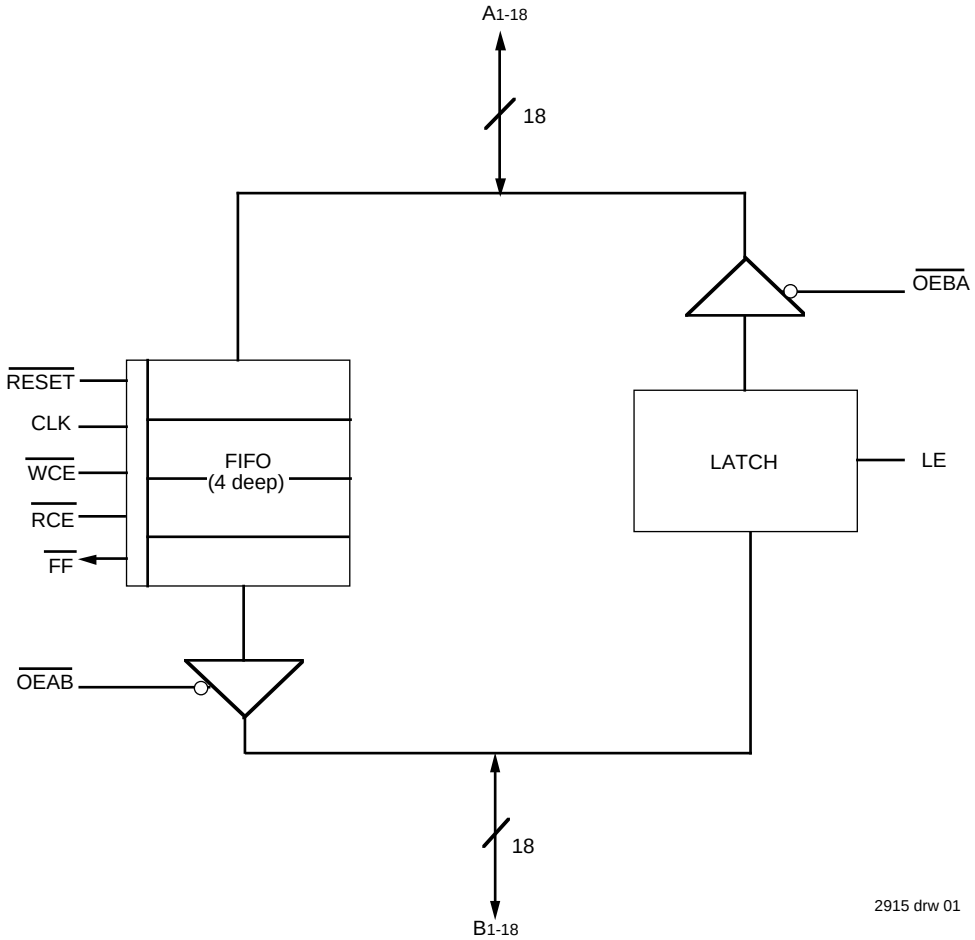
- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤1μA (max.)**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
- Extended commercial range of -40°C to +85°C
- Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- Ideal for new generation x86 write-back cache solutions
- Suitable for modular x86 architectures
- Four deep write FIFO
- Latch in read path
- Synchronous FIFO reset

DESCRIPTION:

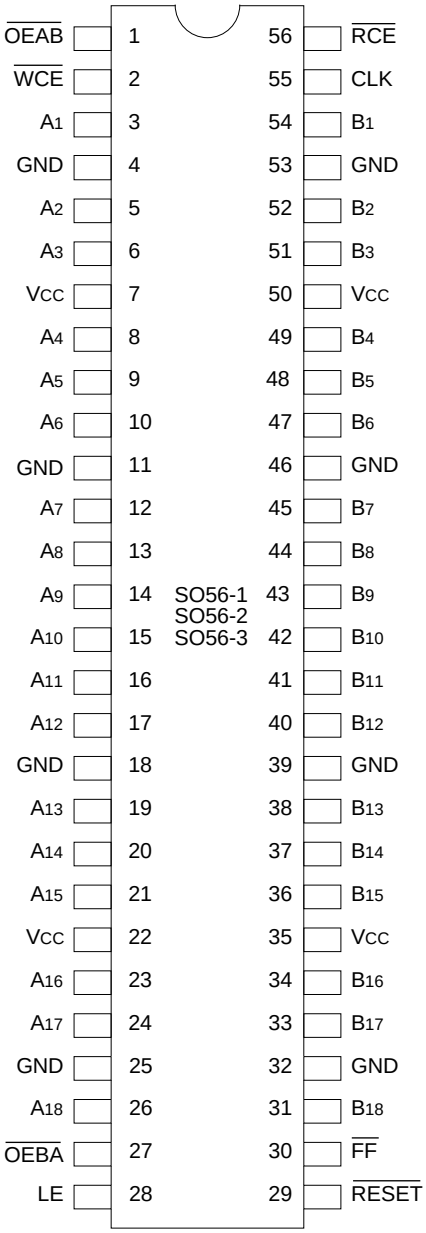
The FCT162701T/AT is an 18-bit Read/Write buffer with a four deep FIFO and a read-back latch. It can be used as a read/write buffer between a CPU and memory or to interface a high-speed bus and a slow peripheral. The A-to-B (write) path has a four deep FIFO for pipelined operations. The FIFO can be reset and a FIFO full condition is indicated by the full flag ($\overline{FF}$). The B-to-A (read) path has a latch. A HIGH on LE, allows data to flow transparently from B-to-A. A LOW on LE allows the data to be latched on the falling edge of LE.

The FCT162701T/AT has a balanced output drive with series termination. This provides low ground bounce, minimal undershoot and controlled output edge rates.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



SSOP/ TSSOP/TVSOP TOP VIEW

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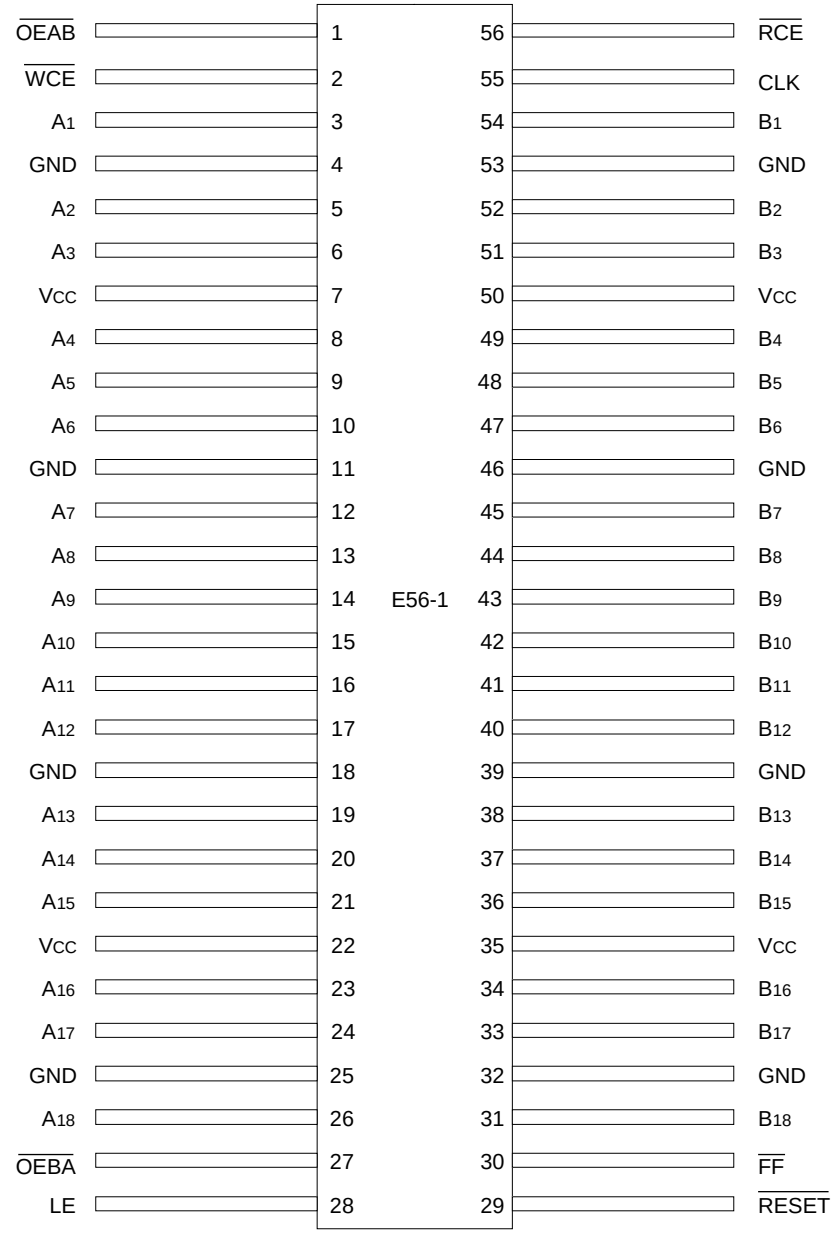

CERPACK TOP VIEW

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PIN DESCRIPTION

Pin Names	I/O	Description
A_{1-18}	I/O	18 bit I/O port.
B_{1-18}	I/O	18 bit I/O port.
CLK	I	Clock for write path FIFO. Clocks data into FIFO when $\overline{WCE}$ is low, clocks data out of FIFO when $\overline{RCE}$ is low. When FIFO is full all further writes to the FIFO are inhibited. When FIFO is empty all reads from the FIFO are inhibited. CLK also resets the FIFO when $\overline{RESET}$ is low.
$\overline{WCE}$	I	Enable pin for FIFO input clock.
$\overline{RCE}$	I	Enable pin for FIFO output clock.
$\overline{FF}$	O	Write path FIFO full flag. Goes low when FIFO is full.
$\overline{RESET}$	I	Synchronous FIFO reset - when low CLK resets the FIFO. The FIFO pointers are initialized to the "empty" condition and FIFO output is forced high (all ones). The FIFO full flag ($\overline{FF}$) will be high immediately after reset.
$\overline{OEAB}$	I	Output Enable pin for B port.
$\overline{OEBA}$	I	Output Enable pin for A port.
LE	I	Read path latch enable pin. When high, data flows transparently from B port to A port, B data is latched on the falling edge of LE.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

FUNCTIONAL DESCRIPTION:

This device is useful as a read/write buffer for modular high end designs. It provides multi-level buffering in the write path and single deep buffering in the read path, and is suited to write back cache implementation. The read path provides a transparent latch.

The four deep FIFO uses one clock with two clock enable pins, $\overline{WCE}$ and $\overline{RCE}$ to clock data in and out. The FIFO has an external full flag which goes LOW when the FIFO is full. Internal read and write pointers keep track of the words stored in the FIFO. A write attempt to a full FIFO is ignored. An attempt to read from an empty FIFO will have no effect and the last read data remains at the output of the FIFO. The FIFO may be reset by the synchronous $\overline{RESET}$ input. This resets the read and write pointers to the original "empty" condition and also sets all B outputs = 1. Simultaneous read and write attempts (clock data into FIFO as well as clock data out of FIFO) are possible except on FIFO empty and full boundaries. When the FIFO is empty, and a simultaneous read and write is attempted, the read is ignored while the write is executed. If the same is attempted when the FIFO is full, the write is ignored while the read is executed. Normal operation of the four deep FIFO in the write path is independent of the read path operation.

Power, ground and data pin positions on the FCT162701T match those on the FCT16501T/162501T, allowing an easy upgrade.

APPLICATIONS: 486 INTERFACE

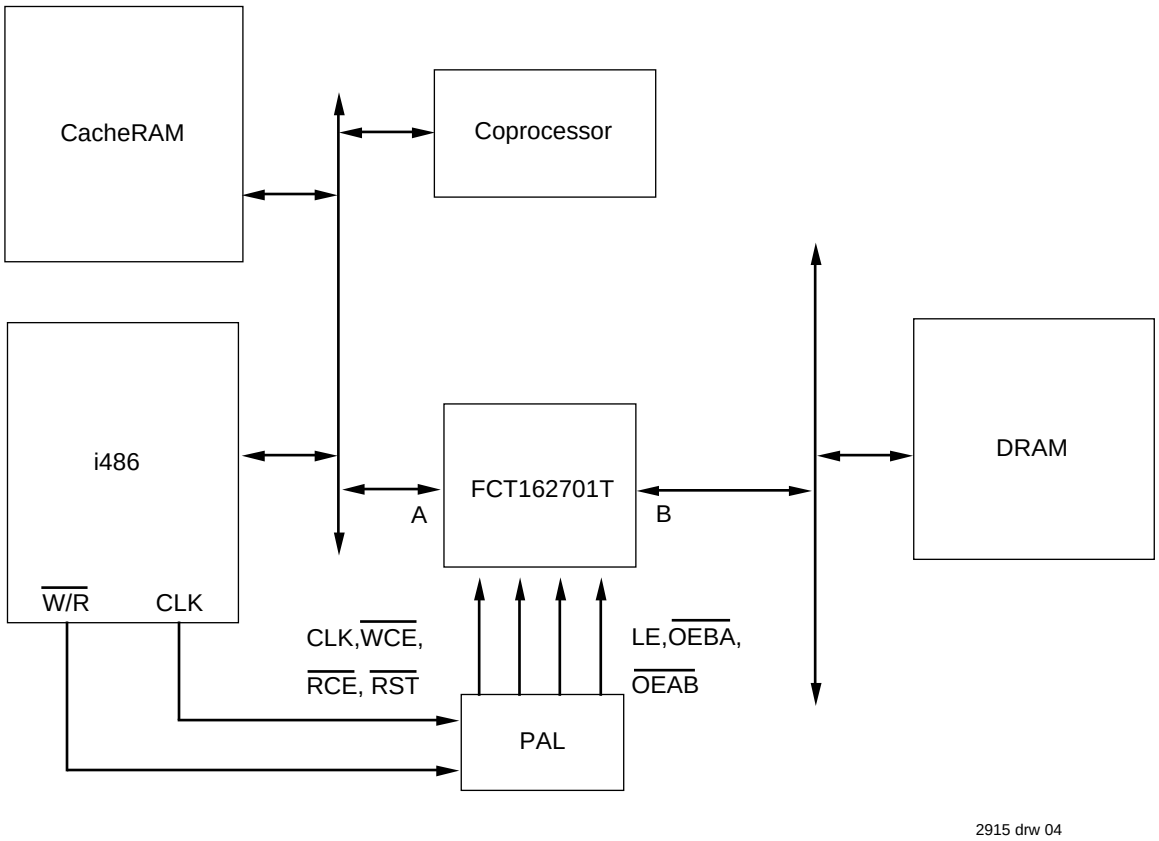

Figure 1. FCT162701T Application Example

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	1.5	mA
$I_{CCD (CLK)}$	Dynamic Power Supply Current due to clock switching[4]	V_{CC} = Max. Outputs Open	CLK Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	180	240	µA/ MHz
$I_{CCD (O/P)}$	Dynamic Power Supply Current due to output switching[4]		One Bit Toggling 50% Duty Cycle		—	80	120	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle		V_{IN} = V_{CC} V_{IN} = GND	—	1.8	2.9[5]	mA
		$\overline{OEAB}$ = GND; $\overline{OEBA}$ = V_{CC} LE = $\overline{WCE}$ = $\overline{RCE}$ = GND $\overline{RESET}$ = V_{CC} All Inputs Low		V_{IN} = 3.4V V_{IN} = GND	—	2.1	3.7[5]	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle		V_{IN} = V_{CC} V_{IN} = GND	—	2.2	3.5	
		$\overline{OEAB}$ = GND; $\overline{OEBA}$ = V_{CC} LE = $\overline{WCE}$ = $\overline{RCE}$ = GND $\overline{RESET}$ = V_{CC} One Bit Toggling at fo = 5MHz 50% Duty Cycle		V_{IN} = 3.4V V_{IN} = GND	—	2.7	5.0	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN}) = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD (CLK)} \times f_{CP} + I_{CCD (O/P)} \times f_O N_O$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

	Parameter	Test Conditions[1]	FCT162701T		FCT162701AT		
			Min.[2]	Max.[2]	Min.[2]	Max.[2]	Unit
PROPAGATION DELAYS							
1	B_{1-18} to A_{1-18}	Read path/latch	1.5	6.5	1.5	5.5	ns
2	LE (Low to Hi) to A_{1-18}	Read path/latch	1.5	5.7	1.5	4.7	ns
3	CLK to $\overline{FF}$	Write path	2	7.0	2	6.0	ns
4	CLK to B_{1-18}	Write path	1	6.0	1	5.2	ns
SETUP & HOLD TIMES[3]							
5	A_{1-18} to CLK (Low to Hi) Setup	Write path	2.5	—	2.5	—	ns
6	A_{1-18} to CLK (Low to Hi) Hold	Write path	0	—	0	—	ns
7	B_{1-18} to LE (Hi to Low) Setup	Read path/latch	3	—	3	—	ns
8	B_{1-18} to LE (Hi to Low) Hold	Read path/latch	0	—	0	—	ns
9	$\overline{WCE}$, $\overline{RCE}$ (Low) to CLK Setup	Write path	3	—	3	—	ns
10	$\overline{WCE}$, $\overline{RCE}$ (Low) to CLK Hold	Write path	0	—	0	—	ns
11	$\overline{RESET}$ (Low) to CLK Setup	Write path	3	—	3	—	ns
12	$\overline{RESET}$ (Low) to CLK Hold	Write path	0	—	0	—	ns
ENABLE & DISABLE TIMES[3]							
13	$\overline{OEBA}$ Low to A_{1-18} Enable	Write path	1.5	7.0	1.5	6.0	ns
14	$\overline{OEBA}$ High to A_{1-18} Disable	Write path	1.5	6.0	1.5	5.0	ns
15	$\overline{OEAB}$ Low to B_{1-18} Enable	Read path	1.5	7.0	1.5	6.0	ns
16	$\overline{OEAB}$ High to B_{1-18} Disable	Read path	1.5	6.0	1.5	5.0	ns
MINIMUM PULSE WIDTHS							
17	CLK HIGH or LOW Pulse Width	Write path	3.0	—	3.0	—	ns
18	LE HIGH Pulse Width	Read path/latch	3.0	—	3.0	—	ns

NOTES:

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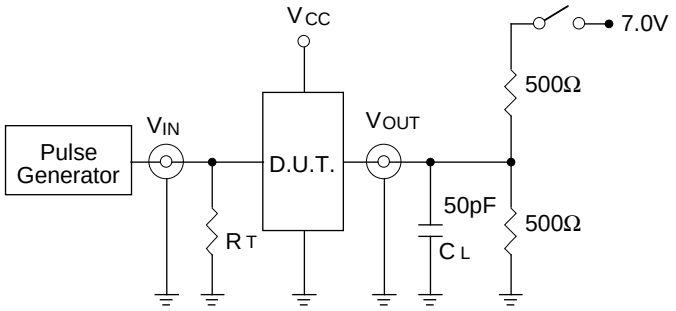
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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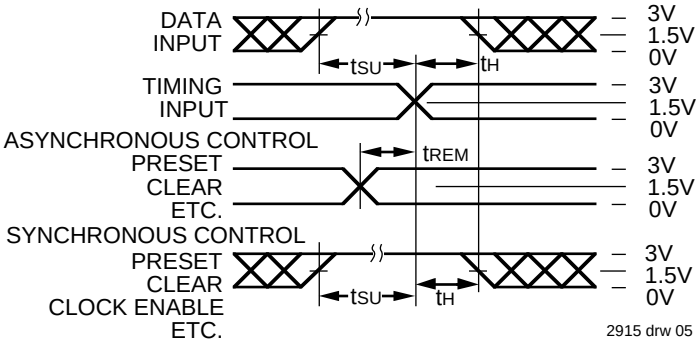
DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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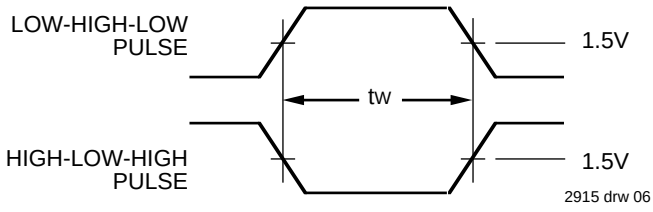
PULSE WIDTH



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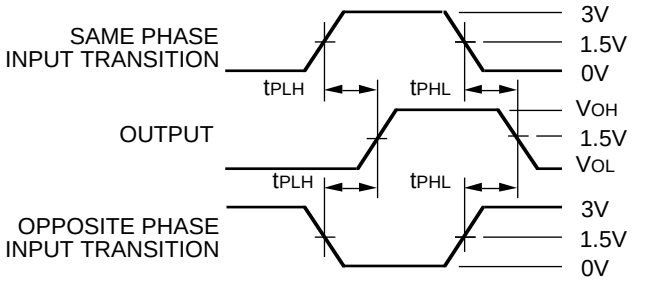
PROPAGATION DELAY



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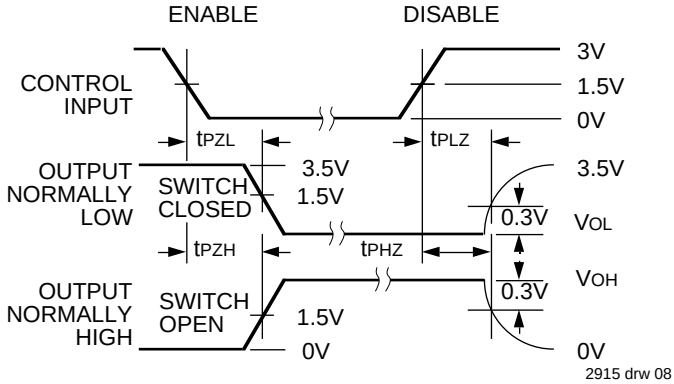
ENABLE AND DISABLE TIMES



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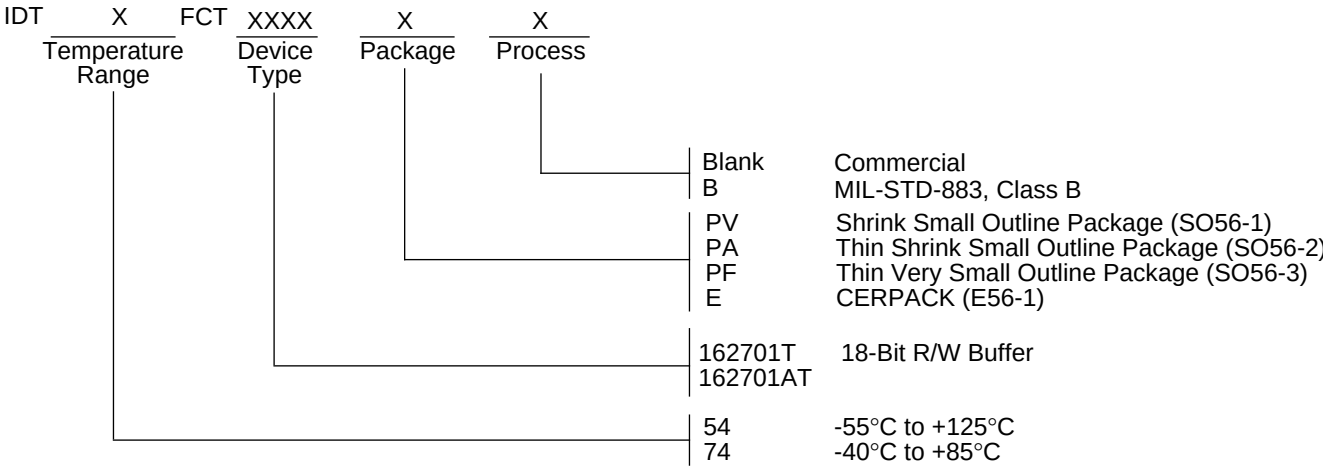
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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