8x16 Analog switch array chip
CH446Q

5x24 Analog switch array chip
CH446X

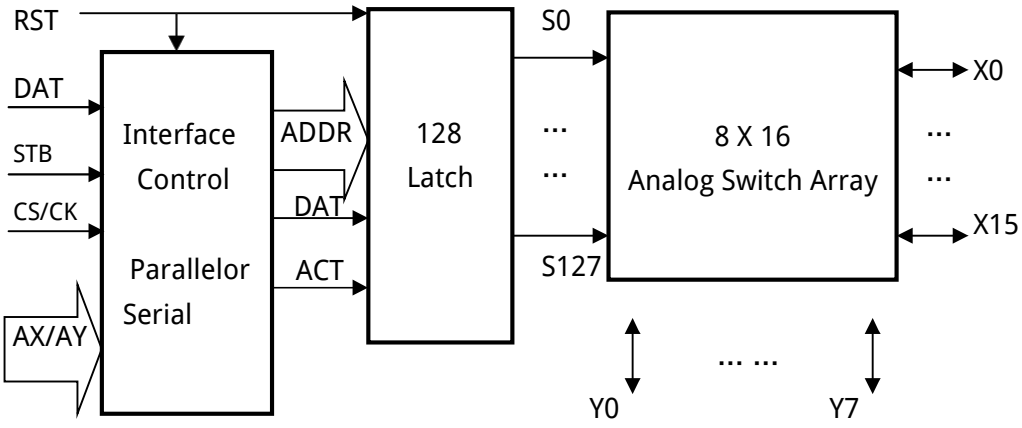
manual

Version: 1D

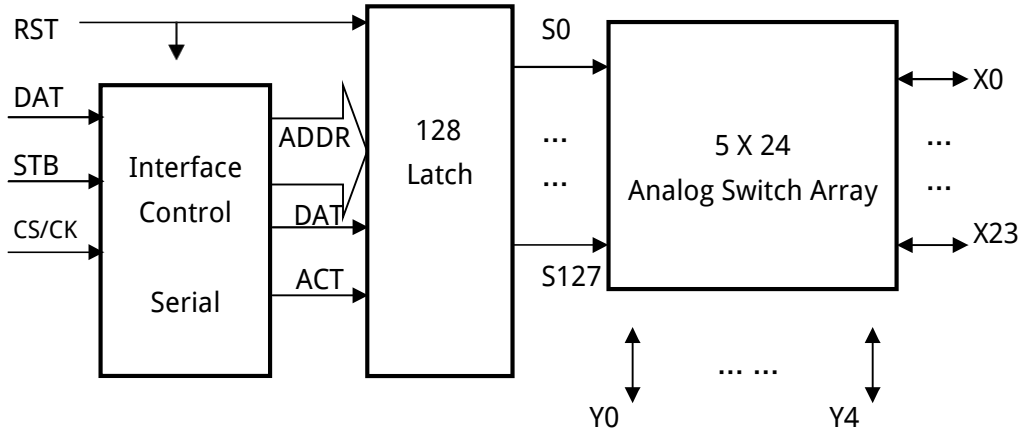
http://wch.cn

1、Overview

CH446Q is an 8x16 matrix analog switch chip. CH446Q contains 128 analog switches, which are distributed at each cross point of the 8x16 signal channel matrix. Each analog switch can be turned on or off independently, thereby realizing any routing of 8x16 signal channels.



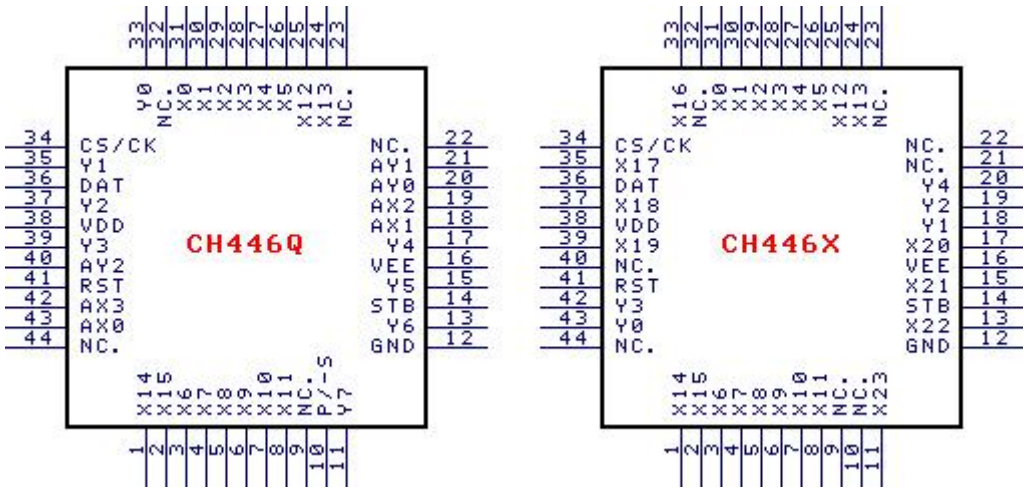
CH446X is a 5x24 matrix analog switch chip. CH446X contains 120 analog switches, which are distributed at each cross point of the 5x24 signal channel matrix. Each analog switch can be turned on or off independently, thereby realizing any routing of 5x24 signal channels.



2、Features

- CH446Q has 128 built-in independent analog switches, which are distributed at each cross point of the 8x16 signal channel matrix.
- CH446X has 120 built-in independent analog switches, which are distributed at each cross point of the 5x24 signal channel matrix.
- CH446Q supports 7-bit parallel address input and is compatible with existing similar products.
- Supports serial address shift input, saving pins.
- Support 4V to 12V single power supply voltage, support +5V and -7V dual power supply voltage.
- When the voltage difference between the positive and negative power supply is 12V, the maximum on-resistance Ron is 65Ω, and △Ron does not exceed 10Ω.
- Pure CMOS process, low static power consumption.
- Adopt LQFP-44 lead-free package, compatible with RoHS, provide conversion board to PLCC44 package.

3、Encapsulation



Package form	width		Pin pitch		Package description	Order model
LQFP-44	10*10mm		0.8mm	31.5mil	Standard LQFP44 foot patch	CH446Q
LQFP-44	10*10mm		0.8mm	31.5mil	Standard LQFP44 foot patch	CH446X

4、Pin

4.1. CH446Q Pin

Pin number	Pin name	type	Pin description
38	VDD	power supply	Positive power supply, the voltage must be greater than or equal to GND
12	GND	power supply	Common ground, digital signal reference ground, voltage is 0V
16	VEE	power supply	Negative power supply, the voltage must be less than or equal to GND
41	RST	enter	External manual reset input, active at high level
10	P/-S	enter	Address input method selection: High level is parallel input mode; low level is serial input mode
36	DAT	enter	In serial address mode, it is serial data input and switch data input; in parallel address mode, it is switch data input, Correspondingly turn on when it is high level, turn off when it is low level
14	STB	enter	Strobe input, high level effective
34	CS/CK	enter	In serial address mode, it is serial clock input, and the rising edge is valid; In parallel address mode, it is chip select input, active at high level
43、18、19、42	AX0 ~ AX3	enter	In serial address mode, it is an unused pin and must be directly connected to GND; In parallel address mode, the address input selected for the X port
20、21、40	AY0 ~ AY2	enter	In serial address mode, it is an unused pin and must be directly connected to GND; In parallel address mode, the address input selected for the Y port
31、30、29、28、27、26、3、4、5、6、7、8、25、24、1、2	X0 ~ X15	Analog signal input and output	X port of 8x16 matrix analog switch
33、35、37、39、17、15、13、11	Y0 ~ Y7	Analog signal input and output	Y port of 8x16 matrix analog switch
9、22、23、32、44	NC.	Empty feet	Unused pins, connection is prohibited

4.2. CH446X pin

Pin number	Pin name	type	Pin description
38	VDD	power supply	Positive power supply, the voltage must be greater than or equal to GND
12	GND	power supply	Common ground, digital signal reference ground, voltage is 0V
16	VEE	power supply	Negative power supply, the voltage must be less than or equal to GND
41	RST	enter	External manual reset input, active at high level
36	DAT	enter	Serial data input and switch data input; When used as switch data input, high level is open, low level is closed
14	STB	enter	Strobe input, high level effective
34	CS/CK	enter	Serial clock input, the rising edge is valid
31、30、29、28、27、26、3、4、5、6、7、8、25、24、1、2、33、35、37、39、17、15、13、11	X0 ~ X23	Analog signal input and output	X port of 5x24 matrix analog switch
43、18、19、42、20	Y0 ~ Y4	Analog signal input Output	Y port of 5x24 matrix analog switch
9、10、21、40、22、23、32、44	NC.	Empty feet	Unused pins, connection is prohibited

5、Function Description

Refer to the block diagram on the homepage, the CH446Q chip is divided into three parts: interface control logic, 128 latches, and 128 analog switch arrays. The interface control logic also includes serial address to parallel address conversion.

128 analog switches are distributed at each cross point of an 8x16 matrix composed of 16 X ports and 8 Y ports, so that any X port and any Y port can be turned on or off when needed, or even Make certain two X ports connect to a certain Y port respectively to realize indirect conduction between any two X ports or any two Y ports.

The 128 latches are used to control the on or off of 128 analog switches respectively. The 128 latches are addressed from 0 to 127, which are selected after being decoded by the 7-bit address ADDR6~ADDR0. Inputting a high-level reset signal from the RST pin can clear all latches, which will cause all analog switches to turn off. When an analog switch needs to be turned on or off, the address of the latch should be provided through the 7-bit ADDR, and the switch data should be provided through DAT (1 is turned on, 0 is turned off), and then an ACT activation pulse is generated to switch the data Write to the latch specified by ADDR decoding to realize the control of a specified analog switch.

The interface control logic is mainly used to generate ADDR addresses and ACT activation pulses. In the parallel address input mode, the 7-bit address input ADDR0 ~ ADDR6 is composed of pins AX0 ~ AX3, AY0 ~ AY2 from low to high. When the chip select signal input by the CS/CK pin is high, the STB pin The input high-level strobe pulse generates the ACT activation pulse. When the CS/CK pin is low, the ACT signal is not generated. In the serial address input mode, the clock is input from the CS/CK pin, and on each rising edge, ADDR6, ADDR5 are sequentially input from the DAT pin until ADDR1, ADDR0 (corresponding to AY2, AY1 until AX1, AX0, respectively), The CS/CK pin needs to provide 7 rising edges to get a 7-bit address, and the high-level strobe input from the STB pin directly generates the ACT activation pulse.

In fact, in the parallel address input mode, the ACT signal is the "AND" of the CS/CK pin input and the STB pin input, while in the serial address input mode, the ACT signal is only the input from the STB pin. The RST reset signal takes precedence over the ACT signal. When RST is input high, the ACT signal will be ignored and all latches will always be cleared. During the active period of the ACT activation pulse, the DAT pin can dynamically change the input switch data, and make the corresponding analog switch turn on or off in real time, but before the end of the ACT signal (that is, before the falling edge of STB), the DAT pin The input data should remain stable in order to latch the data correctly.

CH446X and CH446Q have similar functions, with 3 differences: ①, the former is a 5x24 matrix composed of 24 X ports and 5 Y ports, the latter is an 8x16 matrix composed of 16 X ports and 8 Y ports; ②, the former only supports Serial address mode, the latter supports two modes: parallel address and serial address; ③. Although CH446X also has 128 latches, there are only 120 analog switches, and 8 latches have no purpose.

The following table is the decoding truth table of CH446Q chip's 7-bit address ADDR, and it is also the address table of 128 analog switches.

intersection Y end-X end	ADDR6 AY2	ADDR5 AY1	ADDR4 AY0	ADDR3 AX3	ADDR2 AX2	ADDR1 AX1	ADDR0 AX0	Addressing Serial number
Y0-X0	0	0	0	0	0	0	0	00H
Y0-X1	0	0	0	0	0	0	1	01H
Y0-X2	0	0	0	0	0	1	0	02H
Y0-X3	0	0	0	0	0	1	1	03H
Y0-X4	0	0	0	0	1	0	0	04H
Y0-X5	0	0	0	0	1	0	1	05H
Y0-X6	0	0	0	0	1	1	0	06H
Y0-X7	0	0	0	0	1	1	1	07H
Y0-X8	0	0	0	1	0	0	0	08H
Y0-X9	0	0	0	1	0	0	1	09H
Y0-X10	0	0	0	1	0	1	0	0AH
Y0-X11	0	0	0	1	0	1	1	0BH
Y0-X12	0	0	0	1	1	0	0	0CH
Y0-X13	0	0	0	1	1	0	1	0DH
Y0-X14	0	0	0	1	1	1	0	0EH
Y0-X15	0	0	0	1	1	1	1	0FH
Y1-X0	0	0	1	0	0	0	0	10H
Y1-X1	0	0	1	0	0	0	1	11H
.								
Y1-X14	0	0	1	1	1	1	0	1EH
Y1-X15	0	0	1	1	1	1	1	1FH
Y2-X0	0	1	0	0	0	0	0	20H
.								
Y2-X15	0	1	0	1	1	1	1	2FH
.								
Y7-X0	1	1	1	0	0	0	0	70H
.								
Y7-X14	1	1	1	1	1	1	0	7EH
Y7-X15	1	1	1	1	1	1	1	7FH

The following figure is an example of serial address input, which controls the analog switch of the 24H address (between Y2 and X4), first on and then off.

The following table is the decoding truth table of CH446X chip 7-bit address ADDR, and it is also the address table of 120 analog switches.

intersection Y end-X end	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	Addressing Serial number
Y0-X0	0	0	0	0	0	0	0	00H
Y0-X1	0	0	0	0	0	0	1	01H
Y0-X2	0	0	0	0	0	1	0	02H
Y0-X3	0	0	0	0	0	1	1	03H

Y0-X4	0	0	0	0	1	0	0	04H
Y0-X5	0	0	0	0	1	0	1	05H
Y0-X6	0	0	0	0	1	1	0	06H
Y0-X7	0	0	0	0	1	1	1	07H
Y0-X8	0	0	0	1	0	0	0	08H
Y0-X9	0	0	0	1	0	0	1	09H
Y0-X10	0	0	0	1	0	1	0	0AH
Y0-X11	0	0	0	1	0	1	1	0BH
Y0-X12	0	0	0	1	1	0	0	0CH
Y0-X13	0	0	0	1	1	0	1	0DH
Y0-X14	0	0	0	1	1	1	0	0EH
Y0-X15	0	0	0	1	1	1	1	0FH
Y0-X16	0	0	1	0	0	0	0	10H
Y0-X17	0	0	1	0	0	0	1	11H
Y0-X18	0	0	1	0	0	1	0	12H
Y0-X19	0	0	1	0	0	1	1	13H
Y0-X20	0	0	1	0	1	0	0	14H
Y0-X21	0	0	1	0	1	0	1	15H
Y0-X22	0	0	1	0	1	1	0	16H
Y0-X23	0	0	1	0	1	1	1	17H
Y4-X0	0	0	1	1	0	0	0	18H
Y4-X1	0	0	1	1	0	0	1	19H
Y4-X2	0	0	1	1	0	1	0	1AH
Y4-X3	0	0	1	1	0	1	1	1BH
Y4-X4	0	0	1	1	1	0	0	1CH
Y4-X5	0	0	1	1	1	0	1	1DH
no connection	0	0	1	1	1	1	0、1	1EH、1FH
Y1-X0	0	1	0	0	0	0	0	20H
				.				
Y1-X23	0	1	1	0	1	1	1	37H
Y4-X6	0	1	1	1	0	0	0	38H
				.				
Y4-X11	0	1	1	1	1	0	1	3DH
no connection	0	1	1	1	1	1	0、1	3EH、3FH
Y2-X0	1	0	0	0	0	0	0	40H
				.				
Y2-X23	1	0	1	0	1	1	1	57H
Y4-X12	1	0	1	1	0	0	0	58H
				.				
Y4-X17	1	0	1	1	1	0	1	5DH
no connection	1	0	1	1	1	1	0、1	5EH、5FH
Y3-X0	1	1	0	0	0	0	0	60H
				.				
Y3-X23	1	1	1	0	1	1	1	77H
Y4-X18	1	1	1	1	0	0	0	78H
				.				
Y4-X23	1	1	1	1	1	0	1	7DH

no connection	1	1	1	1	1	1	0、1	7EH、7FH

6、parameter

6.1. Absolute maximum value (critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

name	Parameter Description	Minimum	Max	unit
TA	Ambient temperature during work	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VDD	When VEE=GND=0V, VDD power supply voltage	-0.5	16	V
VEE	When VDD=GND=0V, VEE power supply voltage	-16	+0.5	V
Vaio	The voltage on the analog signal input or output pin, VDD>=GND>=VEE	VEE-0.5	VDD+0.5	V
Vdio	The voltage on the digital signal input or output pin, VDD>=GND>=VEE	GND-0.5	VDD+0.5	V
Isw	Continuous passing current of analog switch	0	15	mA
Iall	The sum of the continuous passing current of all analog switches	0	100	mA

6.2. Recommended working voltage

name	Parameter Description		Minimum	Max	unit
VDD	GND=0V, The voltage difference between VDD and VEE is less than 13.2V	VDD power supply voltage	4	13.2	V
VEE		VEE supply voltage	-8.8	0	V
Vaio	The voltage on the analog signal input or output pin, VDD>=GND>=VEE		VEE	VDD	V
Vdio	The voltage on the digital signal input or output pin, VDD>=GND>=VEE		GND	VDD	V

The power supply voltage should meet two conditions: VDD>GND>=VEE and VDD>GND+4V, Recommend the following combination:

VDD=12V & GND=0V & VEE=0V (VDD-GND=12V, VDD-VEE=12V)

VDD=5V & GND=0V & VEE=0V (VDD-GND=5V, VDD-VEE=5V)

VDD=6V & GND=0V & VEE=-6V (VDD-GND=6V, VDD-VEE=12V)

VDD=5V & GND=0V & VEE=-7V (VDD-GND=5V, VDD-VEE=12V)

VDD=5V & GND=0V & VEE=-5V (VDD-GND=5V, VDD-VEE=10V)

6.3. Electrical parameters (test conditions: TA=25°C, VDD=12V, GND=0V, VEE=0V, the voltage difference between both ends of the analog switch is 0.4V)

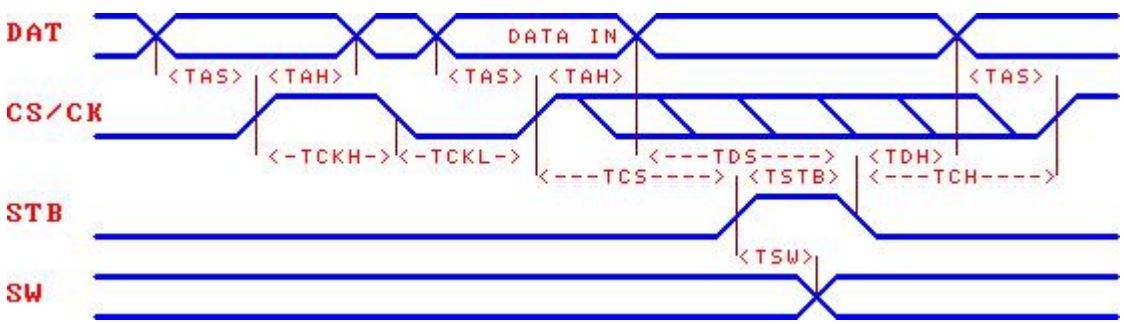
name	Parameter Description	Minimum	Typical value	Max	unit
ICC0	Quiescent power supply current, all digital pins are connected to VDD or GND		1	100	uA
ICC5	Quiescent power supply current, VDD=5V, 2.4V for all digital pins		0.4	1.5	mA
ICC12	Quiescent supply current, 3.4V on all digital pins		5	15	mA
VIL	Digital pin low-level input voltage, VDD-GND=5V	-0.5		0.8	V
VIH	Digital pin high level input voltage, VDD-GND=5V	2.0		VDD+0.5	V
VIH12	Digital pin high level input voltage	3.3		VDD+0.5	V
ILEAK	Input leakage current of digital pin		0.1	10	uA
IOFF	The leakage current of the analog switch in the closed state		±1	±500	nA
RON12	Analog switch on resistance, VDD-VEE=12V, 25℃		45	65	Ω
RON12T	Analog switch on-resistance, VDD-VEE=12V, 85℃		55	80	Ω
RON5	Analog switch on resistance, VDD-VEE=5V, 25℃		120	185	Ω
RON5T	Analog switch on-resistance, VDD-VEE=5V, 85℃		150	225	Ω
△RON	The difference of on-resistance of multiple analog switches, VDD-VEE=12V		5	10	Ω

6.4. Analog switch timing parameters (test conditions: TA=25°C, VDD=5V, GND=0V, VEE=-7V, analog signal 2Vpp)

name	Parameter Description	Minimum	Typical value	Max	unit
CSW	Pin capacitance of analog switch port, F=1MHz		10	25	pF
CFT	Analog switch feedthrough capacitance, F=1MHz		0.5		pF
F3DB	Analog switching frequency response, 3DB, RL=3KΩ		50		MHz
TPS	Analog switch signal pass delay, RL=1KΩ, CL=50pF		12	30	nS

6.5. Interface timing parameters (test conditions: TA=25°C, VDD=5V, GND=0V, VEE=-7V, refer to the attached picture)

name	Parameter Description	Minimum	Typical value	Max	unit
CDI	Pin capacitance of digital signal input, F=1MHz		7	15	pF
TPAS	The setup time of the parallel input address to the rising edge of STB	8			nS
TPAH	Hold time of parallel input address to STB falling edge	6			nS
TAS	DAT input address to CS/CK rising edge establishment time	7			nS
TAH	The hold time of the DAT input address to the rising edge of CS/CK	3			nS
TDS	Settling time of DAT input data to the falling edge of STB	8			nS
TDH	Hold time of DAT input data to the falling edge of STB	6			nS
TCS	CS/CK rising edge to STB rising edge setup time	10			nS
TCH	CS/CK rising edge to STB falling edge hold time	7			nS
TCKL	Low level width of CS/CK clock signal	10			nS
TCKH	CS/CK clock signal high level width	10			nS
TSTB	STB input high-level active pulse width	10			nS
TRST	RST input high-level active pulse width	15			nS
TSW	DAT, STB or RST to analog switch execution delay	5	30	70	nS



7、application

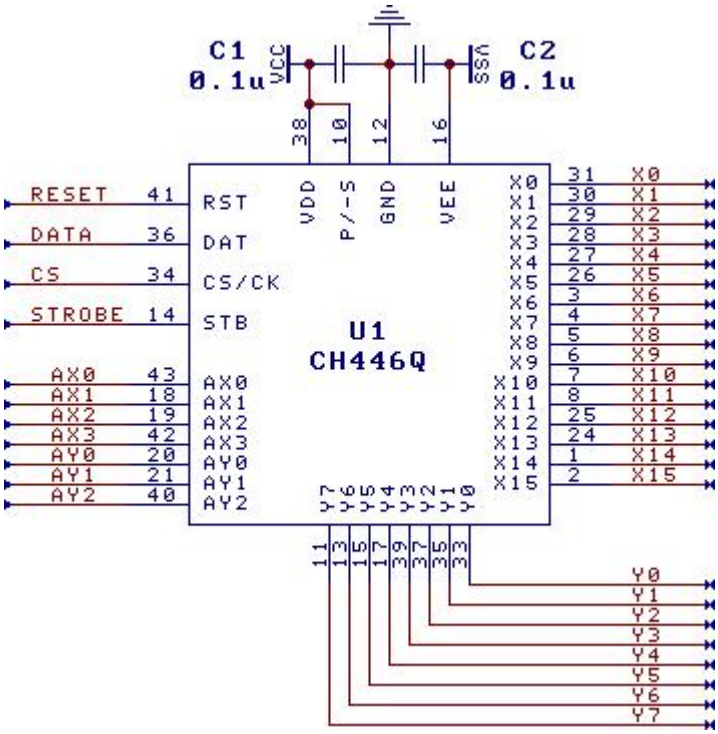
7.1. Parallel address input (below)

Control steps in parallel address input mode: provide address through AX0 ~ AX3 and AY0 ~ AY2 pins, provide data through DAT pin, and provide a high level pulse to STB pin (and CS/CK pin).

In the parallel address input mode, in order to save the control pins of the microcontroller, the CS/CK pin can be short-circuited with the STB pin, or withThe VDD pin is short-circuited, and only the STB pin is kept under the control of the microcontroller.

If VEE is connected to negative voltage, then the analog switch can pass the analog signal of negative voltage, otherwise, if VEE is connected to GND, the analog switch can only pass the analog signal higher than -0.3V.

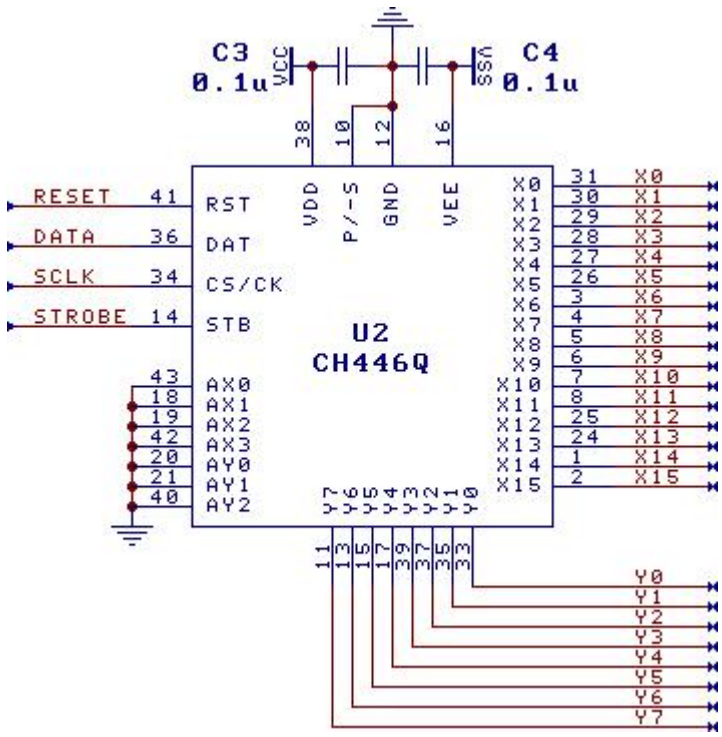
Since the analog circuit and the digital circuit share VDD, in order to reduce interference, the VDD and VEE pins must be connected with decoupling capacitors, and it is recommended that the edge of the digital input signal be appropriately slowed down to reduce the transmission frequency. In addition, for the application environment with strong interference, the MCU can refresh CH446 regularly every few seconds to ensure that each analog switch is in the correct switching state.



7.2. Serial address input (picture below)

Control steps in serial address input mode: sequentially provide 7-bit address through DAT pin and use 7 rising edges of CS/CK pin to move into CH446, provide data through DAT pin and provide a high level pulse to STB pin .

If the single-chip microcomputer is connected to CH446 through the SPI bus, then bit 7 of the 8-bit data provided by SPI will be discarded by CH446, bit 6 to bit 0 of SPI are used as addresses, and the serial data output pin of the SPI of the single-chip microcomputer is connected to the DAT pin to provide a switch For data, the MCU uses an independent pin to control the STB pin of CH446.



7.3. MCU interface program

The C language and ASM assembly interface programs of commonly used single-chip microcomputers are provided on the website.

7.4. Pin conversion

In parallel address input mode, CH446Q is basically compatible with MT8816, but the package and pins are different. The difference is that some pins of the X port of the 8x16 matrix analog switch are different (or their addressing is different). For the differences, refer to the table below.

ADDR3-ADDR0 or AX3-AX0 addressing	CH446Q in LQFP44 package		MT8816 in PLCC44 package	
	Pin number	Pin name	Pin number	Pin name
0110	3	X6	31	X12
0111	4	X7	30	X13
1000	5	X8	9	X6
1001	6	X9	10	X7
1010	7	X10	11	X8
1011	8	X11	12	X9
1100	25	X12	13	X10
1101	24	X13	14	X11

The PLCC44 package conversion board can realize the conversion from LQFP44 to PLCC44 by adjusting the pin sequence through internal PCB wiring according to the above table.