ADAPTING AN R4600 DESIGN TO THE R4650

APPLICATION NOTE AN-139

BY Robert Napaa

INTRODUCTION

The IDT R4650 RISC microprocessor is the third generation 64-bit architecture targeted for a variety of performance-hungry embedded applications. It is the second derivative of the Orion family (also referred to as the R4600). The R4650 removes some of the functional units not frequently used in embedded applications, such as double precision floating point arithmetic and a TLB. The R4650 adds new features that are in line with its target applications, such as a dedicated integer DSP core, cache locking, improved real-time support and an optional 32-bit bus interface.

The R4650 is bus- and upwardly software compatible with the Orion family. It maintains the same bus protocol as the R4600 in both the 64-bit and the 32-bit external bus options. The external bus protocol refers to the handshaking between the CPU and the external logic as well as the timing for the various bus transactions. This insures that ASICs and system logic designed to interface to the R4600 will work with the R4650 without modifications. However, the external clock structure of the R4650 is different from that of the R4600 which provides greater flexibility to the system designer.

This Application Note explains: 1) the differences the internal and external clock distribution tree of the R4600 and the R4650, and 2) how to convert the R4650 clocks into R4600 compatible clocks to interface to existing ASICs and external logic.

DIFFERENT CLOCK STRUCTURE

The R4600 and the R4650 have different input and output clock structures but maintaining the same bus protocol.

R4600 Clocks

The R4600 implements the same clock structure as the first generation 64-bit devices such as the R4000 and the R4400. The R4600 uses a single input clock (MasterClock) that is doubled internally by one PLL to generate the pipeline clock (PClk). A second PLL doubles MasterClock, then divides it by a constant number (from 2 to 8 as programmed during reset) to generate the output clocks (RClock, TClock, MasterOut and SyncOut). These clocks are used by the system logic to interface to the R4600 during read and write operations. Figure 1 illustrates the architecture of the R4600 internal clock distribution tree. A more detailed explanation of the usage of these clocks is presented in the *"IDT79R4600 Hardware User's Manual"*.

R4650 Clocks

The R4650 uses a completely different architecture for the internal clock distribution tree. The R4650 uses a single input clock (MasterClock). MasterClock is multiplied internally using a single PLL by a constant number (from 2 to 8 as programmed during reset) to generate the pipeline clock

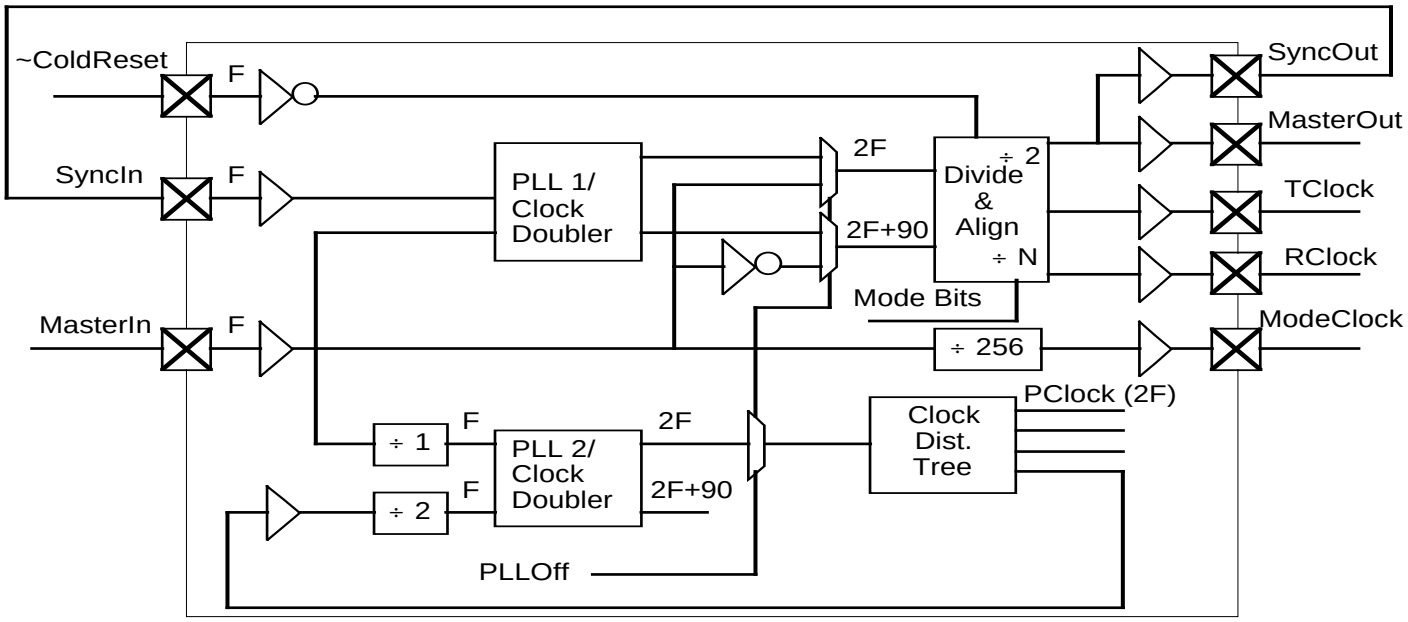


Figure 1. R4600 Clock Distribution Tree and PLLs

(PClk). The R4650 does not generate any output clock. The MasterClock should be used as the system control logic clock. The R4650 guarantees that the interface signals with the external system logic will be sampled using the rising edge of MasterClock. Figure 2 illustrates the internal clock tree of the R4650.

An advantage of the R4650 is that the MasterClock frequency may be kept small. Similarly, the absence of output clocks from the R4650 reduces the power consumption of the device. This architecture allows several systems to synchronize using a single input clock at any frequency without being locked by the clocks provided by the CPU. This is particularly advantageous for backplane applications where the input clock is provided from the backplane to several plugged-in cards.

GENERATING R4600-COMPATIBLE CLOCKS

Systems using the R4650 can reuse the logic and ASICs already developed to work with the R4600. This mechanism requires the generation of MasterOut, SyncOut, RClock and TClock, or alternatively, a subset of these according to the system requirements. The functionality of the different clocks is explained more in detail in the *"IDT79R4600 Hardware User's Manual"*.

The clock distribution tree has to be implemented at the input of the R4650. The R4600 clock generation is illustrated in Figure 3. In this case, a buffer is used to delay the input clock to the R4650. The output of the buffer is equivalent to TClock, MasterOut and SyncOut. The input of the buffer is equivalent to RClock. For a tight delay between RClock and TClock, it is better to use a buffer that has a very narrow window for the min and the max input to output delays. An example of such a clock buffer is the Motorola MC10H645 buffer, which guarantees a single nanosec difference between the min and the max delays.

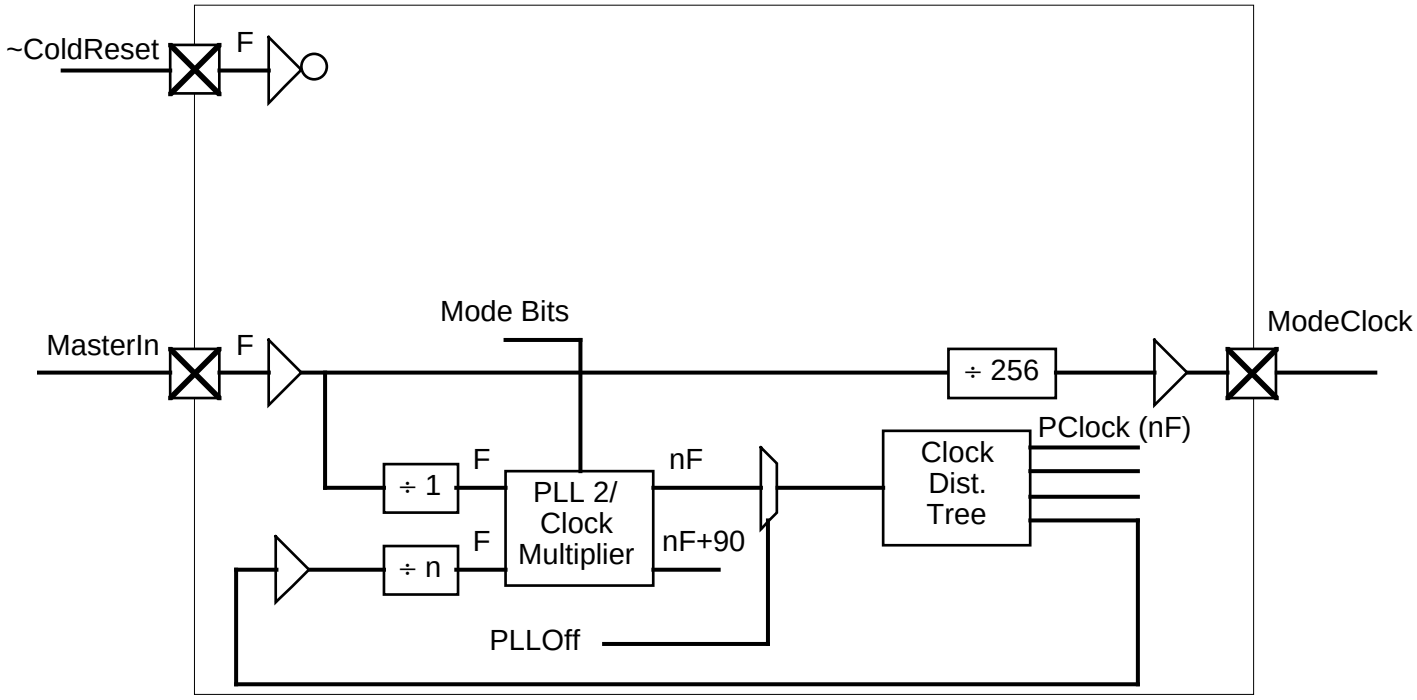


Figure 2. R4650 Clock Distribution Tree and PLL

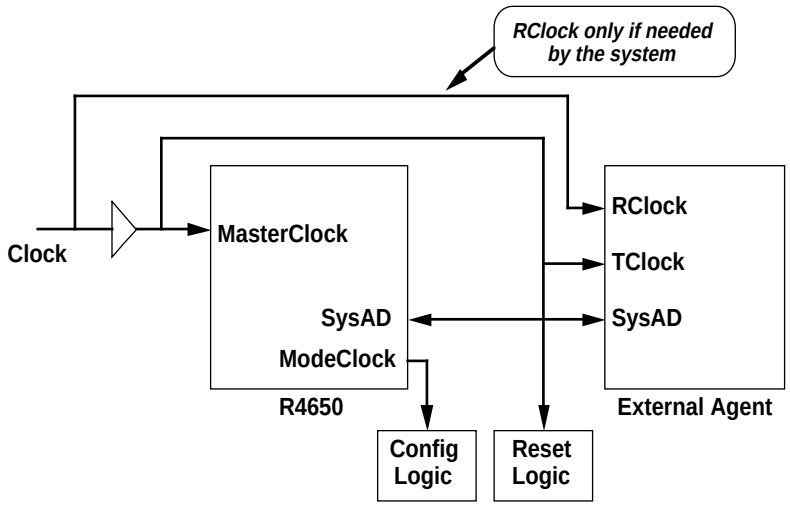


Figure 3. Generating R4600-Compatible Clocks

It is also important to note that in systems using only the R4650, the SyncOut to SyncIn path is irrelevant, since neither the R4650 nor the system logic use these clocks. The MasterOut could be relevant, depending on the system architecture.

DESIGNING A SYSTEM THAT SUPPORTS BOTH CPUs

It is possible to design a single system to support either the R4600 or the R4650 on a single PCB board. The same design allows using the R4600 for high performance applications, while using the R4650 to serve the medium performance segment of the market. This approach preserves the investment in the ASIC development, the system logic, the system

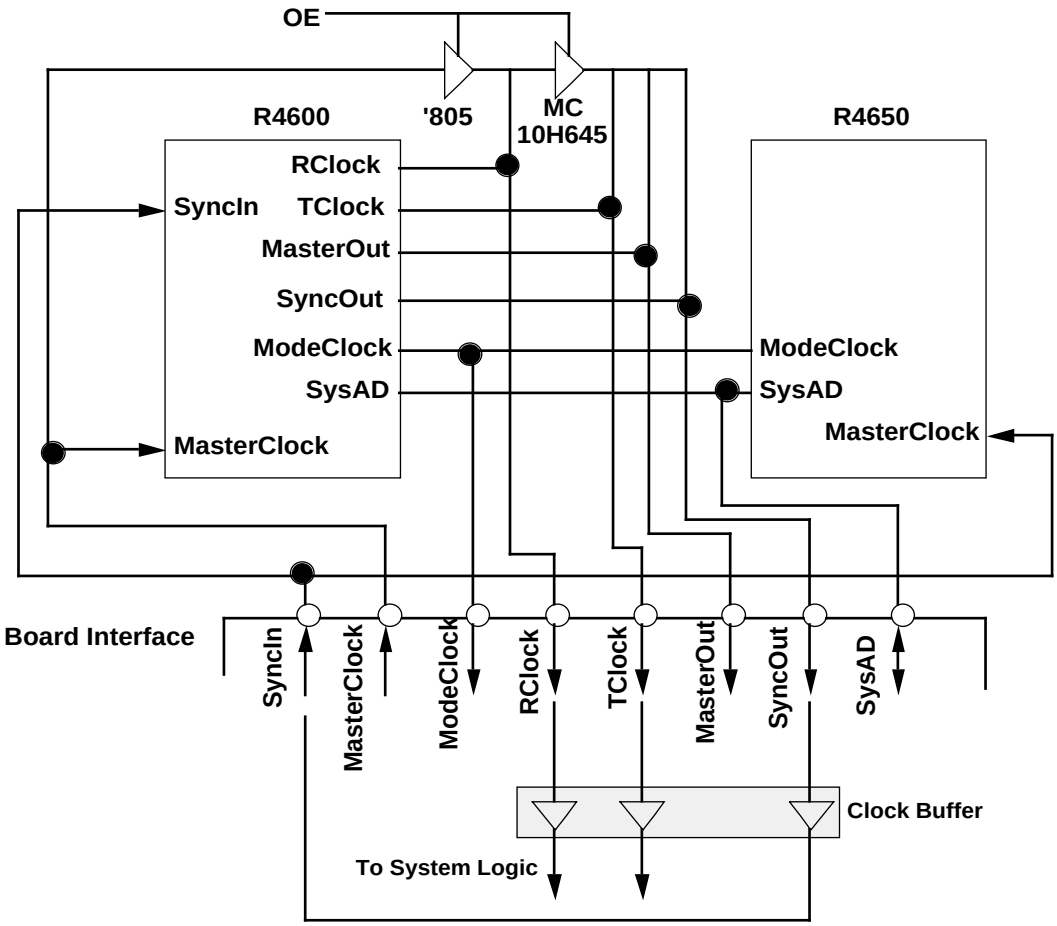


Figure 4. Single System With R4600 and R4650

software and so on. Figure 4 illustrates the block diagram for a system that can support both CPUs on the single PCB.

In this implementation, the clock from the external oscillator, MasterClock, is fed as the input clock to the R4600. It is also fed to the clock distribution circuitry that generates RClock, TClock, MasterOut and SyncOut to be used when the R4650 is used. It is important to note that only one CPU should be plugged-in at any onetime. The clock distribution circuitry is tri-statable when the R4600 is used, since it produces these clocks.

The SyncOut clock is routed on the PCB and returned as SyncIn. The SyncIn clock is fed to the R4600 to align the internal clocks used to sample the system interface, with the RClock and TClock seen by the system logic. In the case of the R4650 the SyncIn clock is used as the input MasterClock to the CPU. This ensures that the input clock to the R4650 is aligned to the system clocks (RClock and TClock) that are generated by the clock distribution circuitry.

THE 79S461

The 79S461 is a small module that supports both the R4600 and the R4650 on a single PCB. It plugs into the PGA socket of the R4600 on any design. It allows the system designer to evaluate the performance of either CPU in the system without modifications to the existing design. Figure 5 illustrates the block diagram of the 79S461. In addition, the schematics of the S461 board are attached to the end of this App Note to provide a better understanding in converting from one clock architecture to the other.

CONCLUSION

It is relatively easy to adapt a design that is based on the R4600 to support the R4650 on a single PCB. This approach offers a great flexibility in selecting the appropriate CPU for the level of performance needed without redesigning the system. The same design allows using the R4600 for high performance applications, while using the R4650 to serve the medium performance segment of the market.

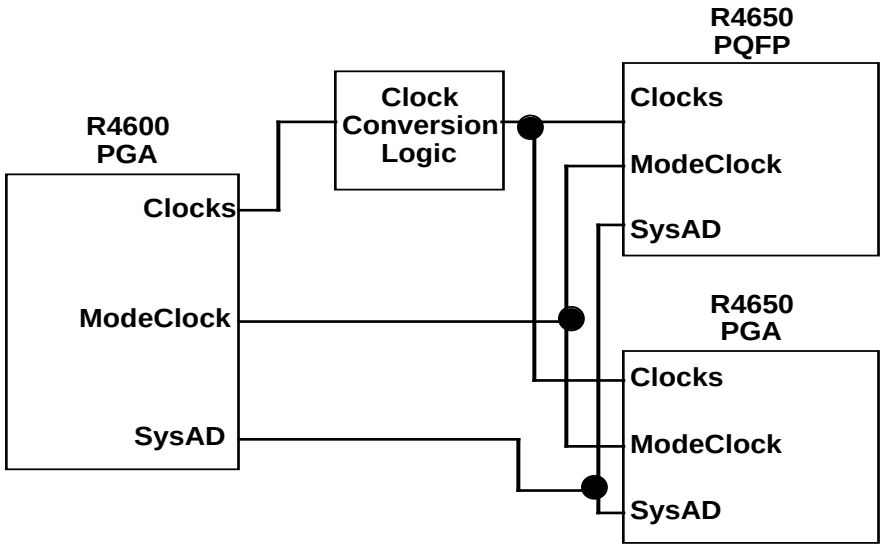
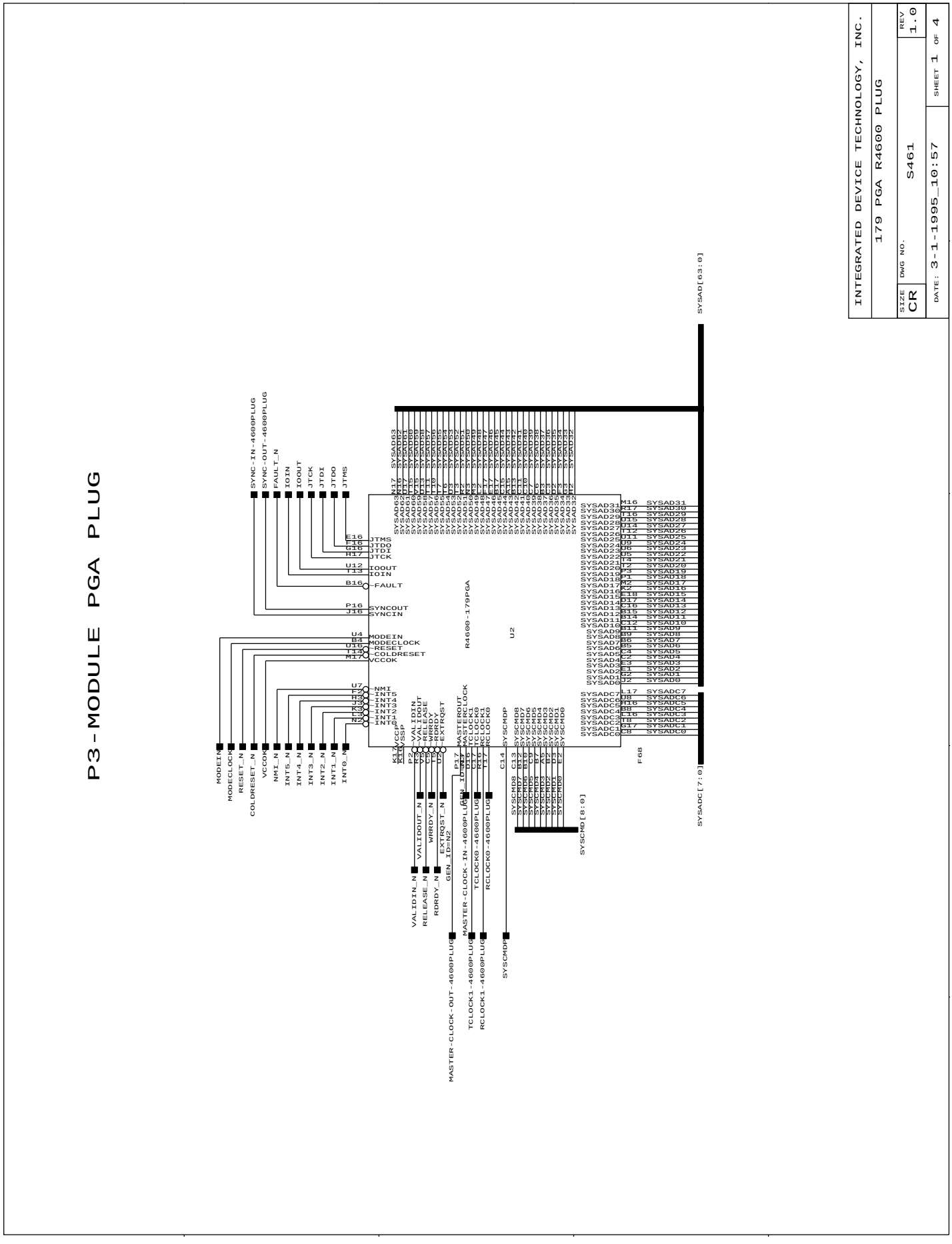
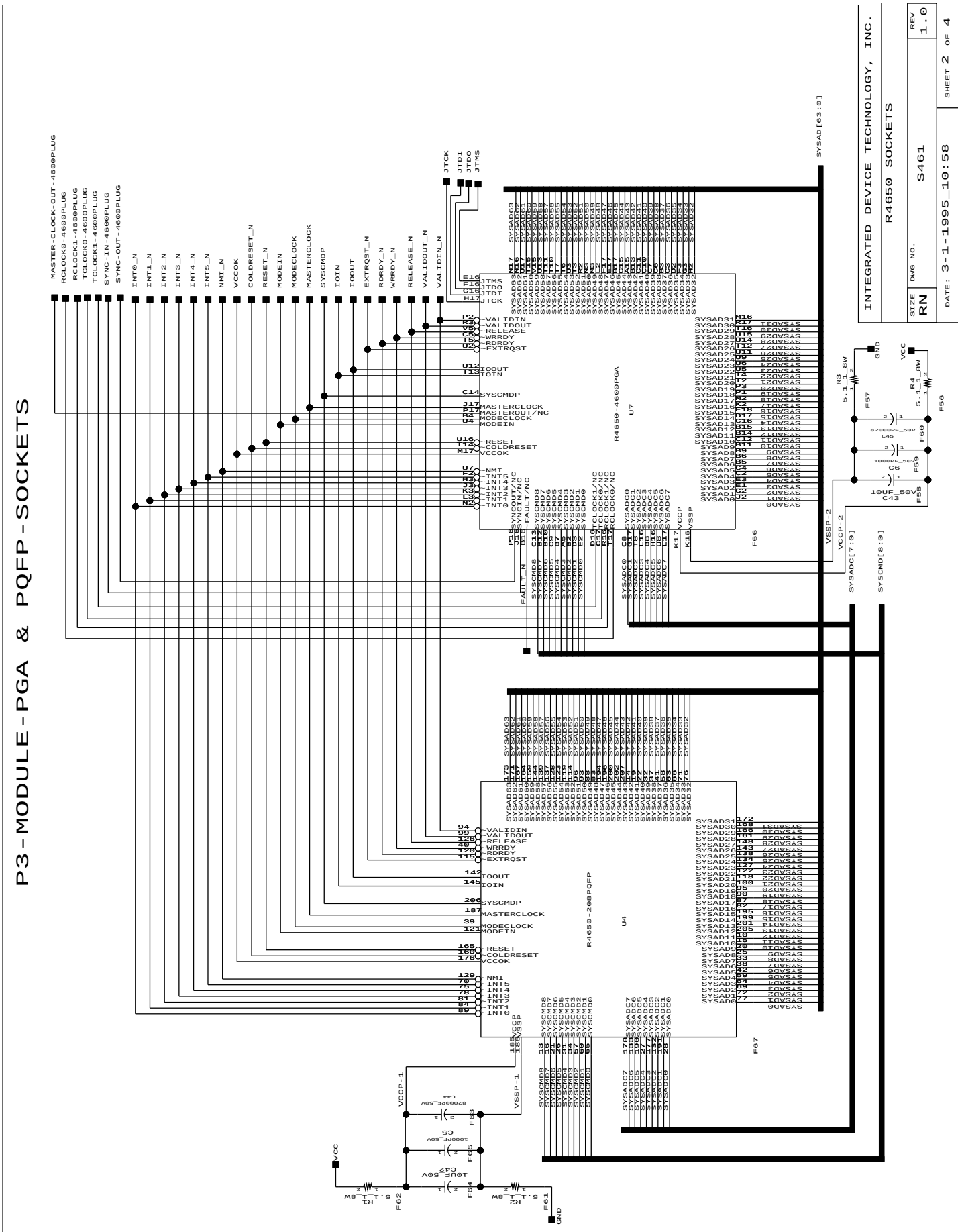
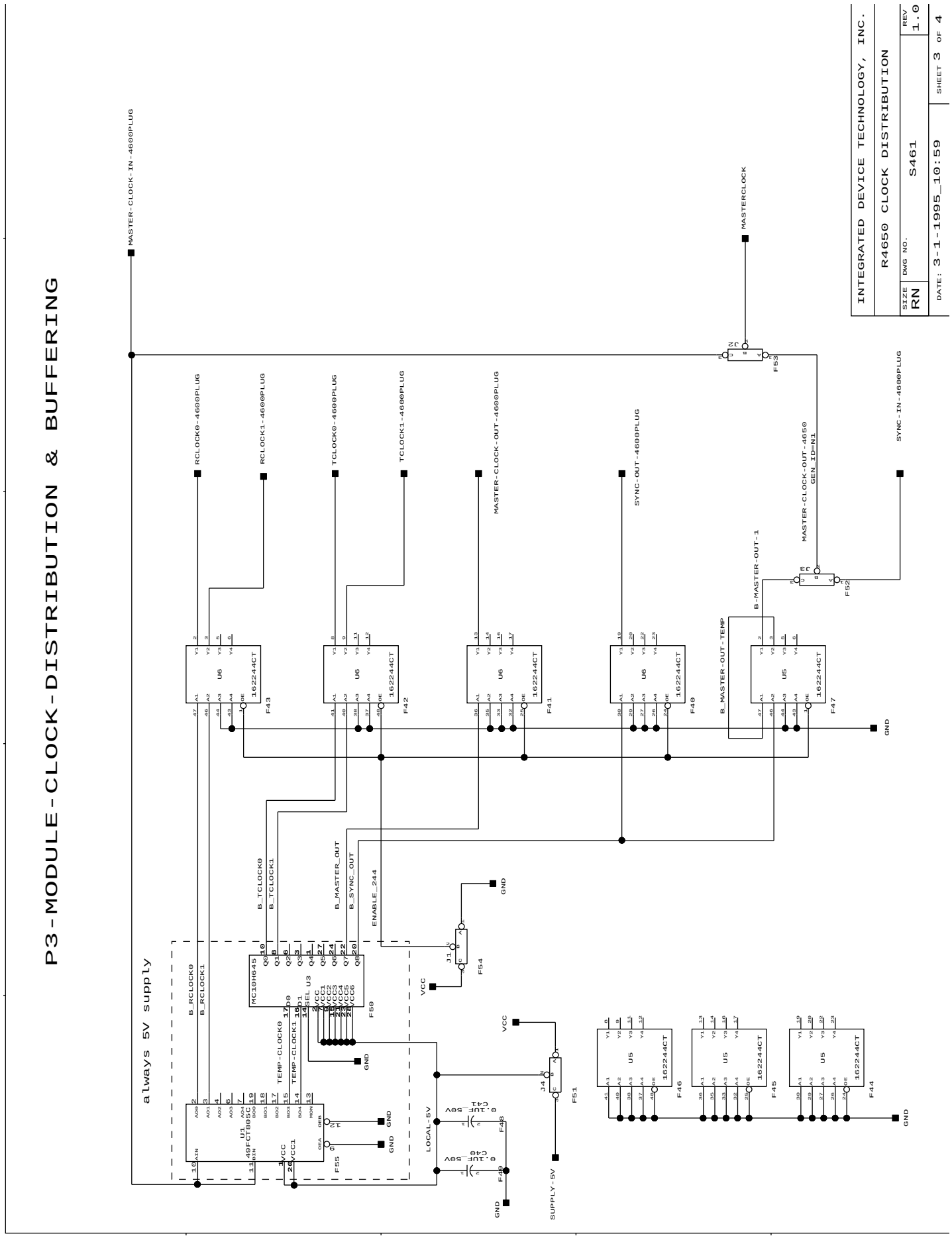
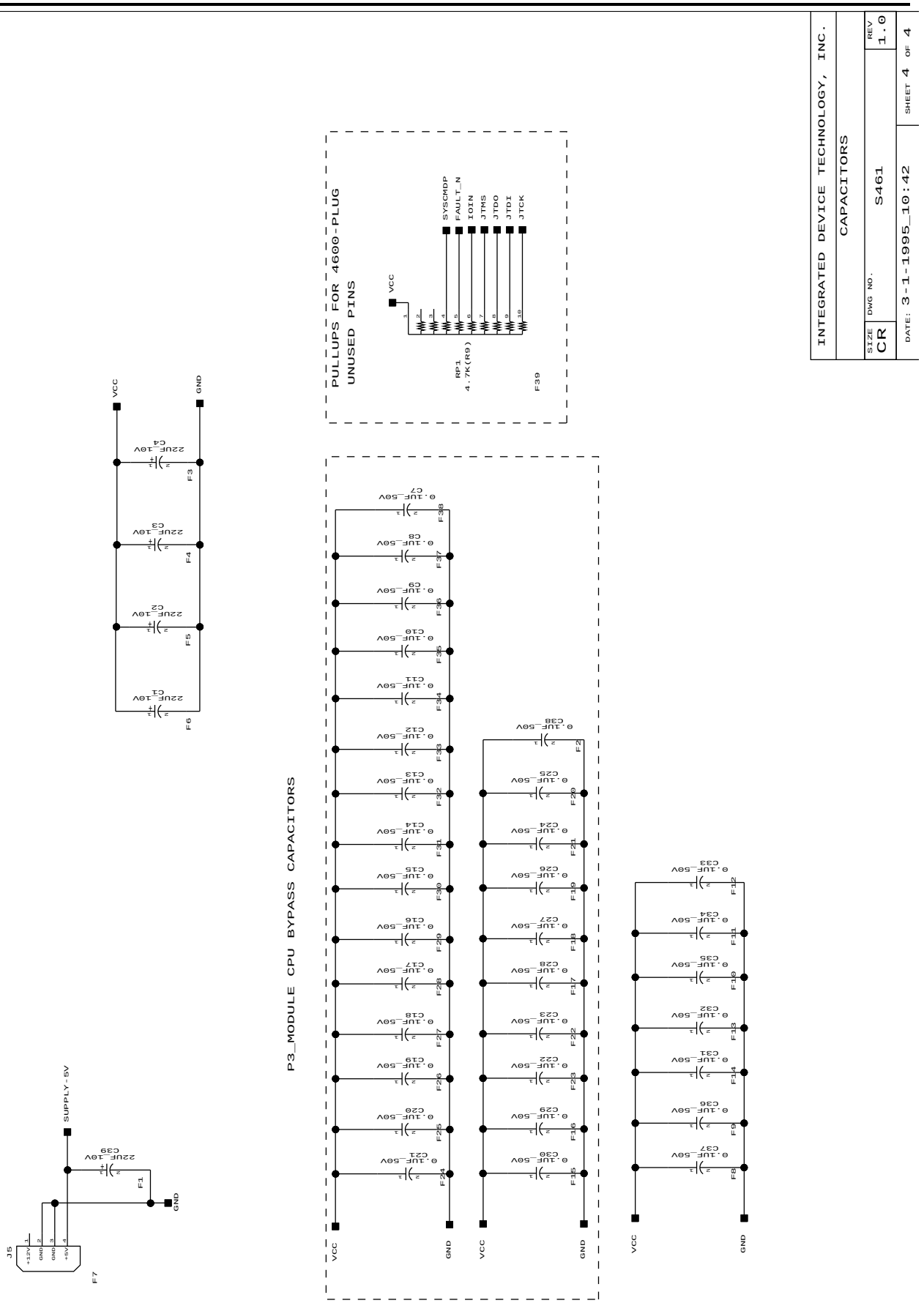


Figure 5. 79S461 Block Diagram





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CAPACITORS
SIZE CR
DWG NO. S461
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DATE: 3-1-1995_10:42
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PULLUPS FOR 4600-PLUG
UNUSED PINS
VCC
SYSCMDP
FAULT_N
IOIN
JTMS
JTDO
JTDI
JTCK
RP1
4.7K(R9)
F39
P3_MODULE CPU BYPASS CAPACITORS
VCC
GND
22UF_10V
0.1UF_50V
SUPPLY-5V
J5
+12V
GND
GND
+5V
F1
F2
F3
F4
F5
F6
F7
F8
F9
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