ATA Flash Disk Controller

SST55VD020

Fact Sheet

FEATURES:

- **Industry Standard ATA/IDE Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6
  - Supports up to Multi-word DMA Mode-4
  - Supports up to Ultra DMA Mode-4
- **Interface for Standard NAND Flash Media**
  - Flash Media Interface: Single or Dual 8-bit access
    - Supports up to 4 flash media devices per channel
    - Supports up to 8 flash media devices directly
    - Supports up to 64 flash media devices with external decoding logic
  - Supports Single-Level Cell (SLC) or Multi-Level Cell (MLC) flash media
    - 2 KByte and 4 KByte program page size
- **3.0V Power Supply**
- **5.0V or 3.0V Host Interface Through V_{DDQ} Pins**
- **Low Current Operation:**
  - Active mode: 25 mA/35 mA (3.0V/5.0V) (typical)
  - Sleep mode: 80 µA/100 µA (3.0V/5.0V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Expanded Data Protection**
  - WP#/PD# pin configurable by host for prevention of data overwrites
  - Added data security through user-selectable protection zones
- **20-byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-byte Unique ID
  - User-Programmable 10-byte ID
- **Programmable, Multitasking NAND Interface**
- **Firmware Storage in Embedded SuperFlash®**
- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard ATA/IDE commands
  - Implements dynamic and static wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Built-in Hardware ECC**
  - Corrects up to 8 random single-bit errors per 512-byte sector
- **Built-in Internal System Clock**
- **Multi-tasking Technology Enables Fast Sustained Write Performance (Host to Flash)**
  - Supports up to 30 MB/sec
- **Fast Sustained Read Performance (Flash to Host)**
  - Up to 30 MB/sec
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
  - 5 sec. (typical) for flash drive recognition and setup
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Packages Available**
  - 100-lead TQFP – 14mm x 14mm
  - 85-ball VFBGA – 6mm x 6mm
- **All non-Pb (lead-free) Devices are RoHS Compliant**

PRODUCT DESCRIPTION

The SST55VD020 is the heart of a high-performance, flash media-based data storage system. The ATA Flash Disk Controller recognizes the control, address, and data signals on the ATA/IDE bus and translates them into memory accesses for standard NAND-type flash media. Utilizing both Single-Level Cell (SLC) and Multi-Level Cell (MLC) flash media, this technology supports solid state mass storage applications by offering new, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The ATA Flash Disk Controller supports standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4, and Ultra DMA Mode-4 interface. The ATA/IDE interface is widely used in such products as portable and desktop computers, portable media player, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, and set-top boxes.

The ATA Flash Disk Controller uses SuperFlash® memory technology and is factory pre-programmed with an embedded flash file system. Upon initial power-on, the SST55VD020 recognizes attached flash media devices, sets up a bad block table, executes all necessary handshaking routines for flash media support, and, finally, performs the low-level format. This process typically takes about 3 second plus 0.5 seconds per gigabyte of drive capacity, allowing a 4 GByte flash drive to be fully initialized in about 5 seconds. For added manufacturing flexibility, system debug, re-initialization, and user customization can be accomplished through the ATA/IDE interface.

Fact Sheet

The SST55VD020 high-performance ATA Flash Disk Controller offers sustained read and write performance up to 30.0 MB/sec. The SST55VD020 directly supports up to 8 flash media devices or, through simple decoding logic, can support up to 64 flash media devices.

The SST55VD020 offers added security protection for confidential information stored in the flash media. It allows up to four protection zones which can be set by the user to be Read/Write, Read-only, or Hidden (Read-disabled). The ATA Flash Disk Controller can access the data within the protected zones through a password-protected command.

The controller also provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

The ATA Flash Disk Controller comes pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID.

The ATA Flash Disk Controller comes packaged in an industry-standard, 100-lead TQFP package or a 85-ball VFBGA package for easy integration into an SMT manufacturing process.

1.0 GENERAL DESCRIPTION

The ATA Flash Disk Controller contains a microcontroller and embedded flash file system integrated in TQFP and VFBGA packages. Refer to Figure 2-1 for the ATA Flash Disk Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

1.1 Performance-optimized ATA Flash Disk Controller

The ATA Flash Disk Controller translates standard ATA signals into flash media data and control signals. The following components contribute to the ATA Flash Disk Controller's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU coordinates all related components to complete requested operations.

1.1.2 Internal Direct Memory Access (DMA)

The ATA Flash Disk Controller uses internal DMA which allows instant data transfer from buffer to flash media. This increases the data transfer rate by eliminating the microcontroller overhead associated with the traditional, firmware-based approach.

1.1.3 Power Management Unit (PMU)

The power management unit controls the power consumption of the ATA Flash Disk Controller. It reduces the power consumption of the ATA Flash Disk Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

1.1.4 SRAM Buffer

The ATA Flash Disk Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the ATA Flash Disk Controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media Writes and Reads.
2. Provides both dynamic and static flash media wear-leveling to spread the flash writes across all unused memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.
4. Manages system security for the selected protection zones.

1.1.6 Error Correction Code (ECC)

The ATA Flash Disk Controller uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data.

High performance is achieved through hardware-based error detection and correction.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to provide trace information during debugging process.

1.1.8 Programmable, Multi-tasking NAND Interface

The multi-tasking interface enables fast, sustained write performance by allowing multiple Read, Program, and Erase operations to multiple flash media devices. The programmable NAND interface enables timely support of fast changing NAND technology.

2.0 FUNCTIONAL BLOCKS

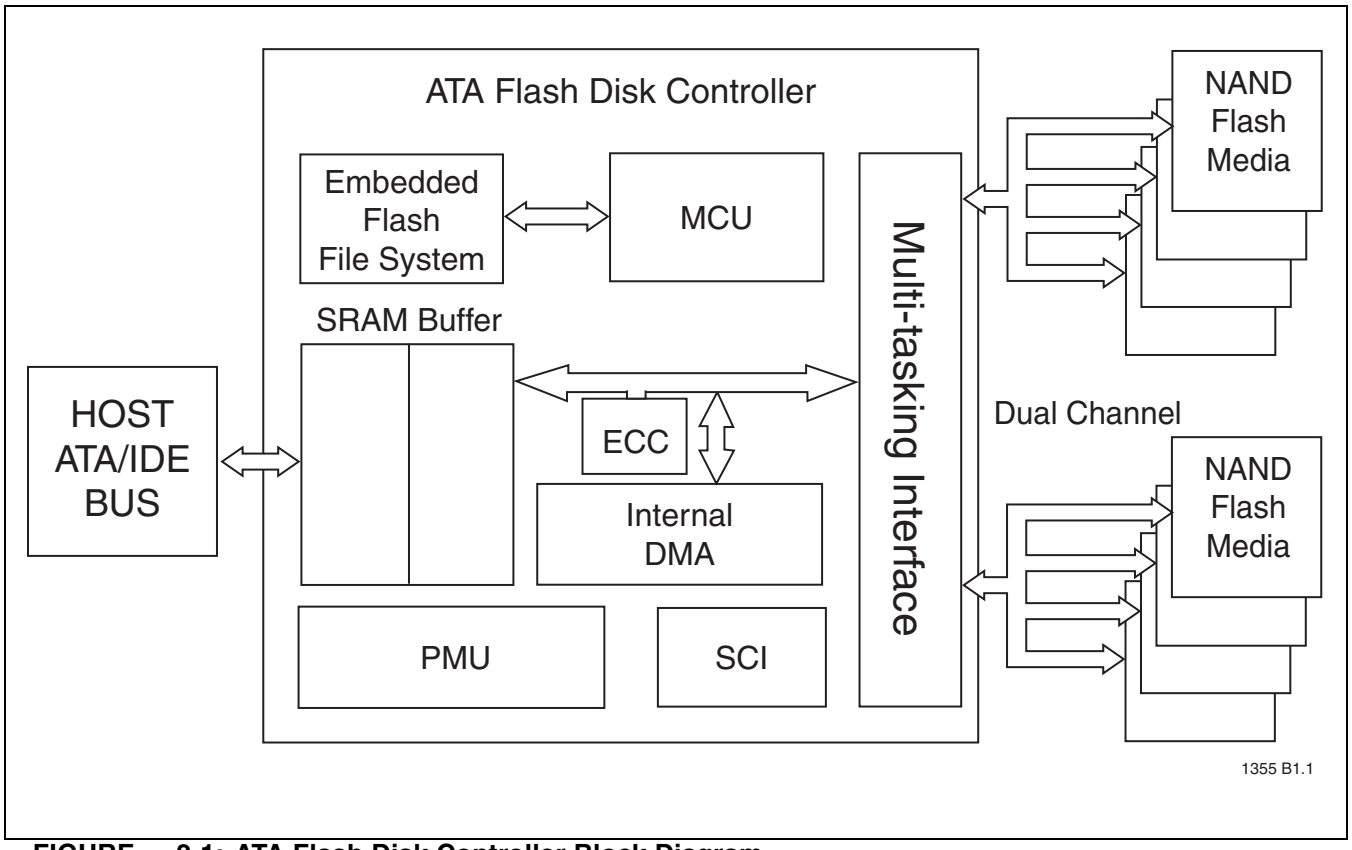
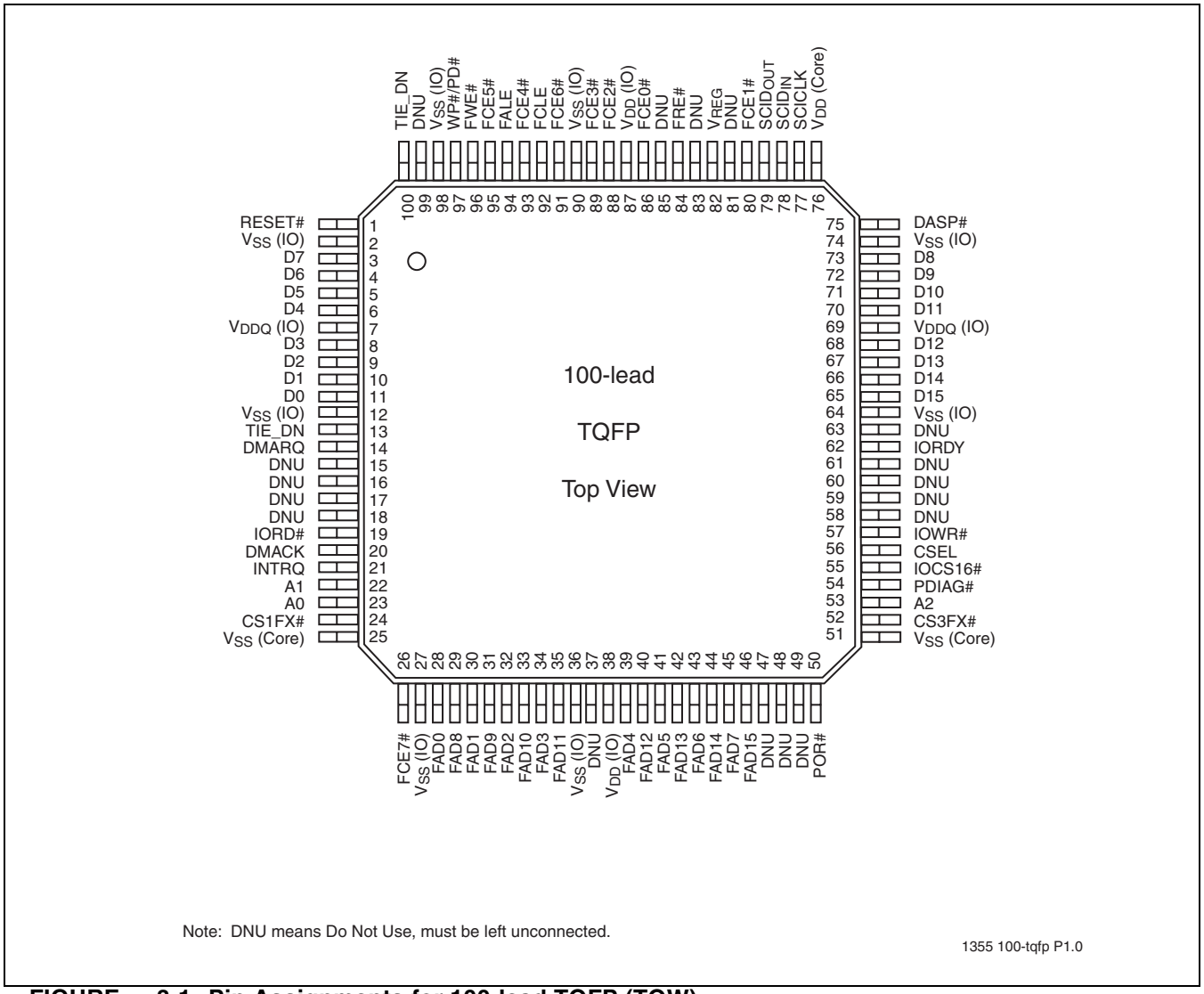


FIGURE 2-1: ATA Flash Disk Controller Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the ATA Flash Disk Controller sources are outputs.

The ATA Flash Disk Controller functions in ATA mode, which is compatible with IDE hard disk drives.



Note: DNU means Do Not Use, must be left unconnected.

1355 100-tqfp P1.0

FIGURE 3-1: Pin Assignments for 100-lead TQFP (TQW)

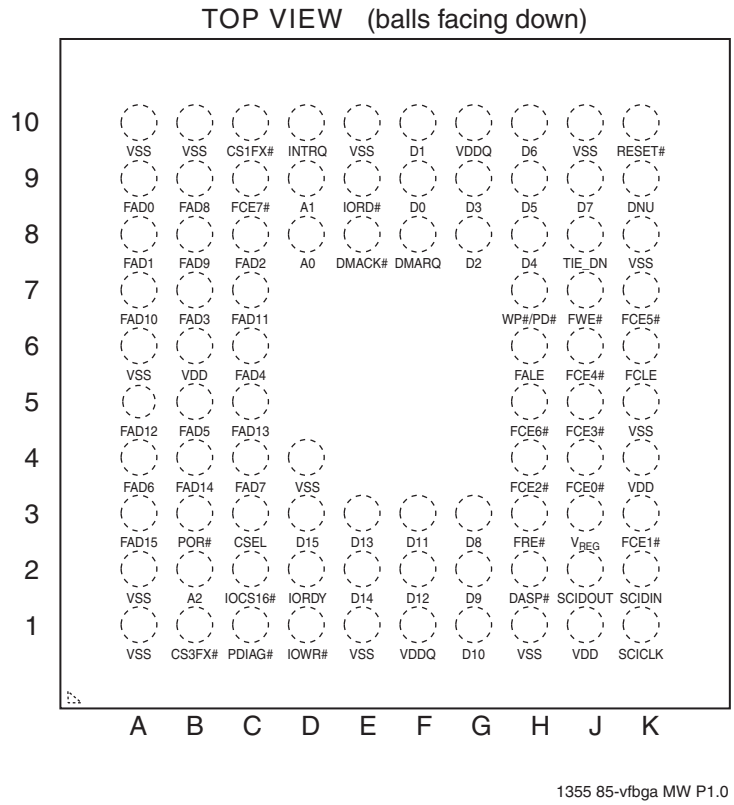


FIGURE 3-2: Pin Assignments for 85-ball VFBGA (MVW)

TABLE 3-1: Pin Assignments (1 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
Host Side Interface					
A2	53	B2	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	22	D9			
A0	23	D8			
D15	65	D3	I/O	I1Z/O2	D[15:0] Data bus
D14	66	E2			
D13	67	E3			
D12	68	F2			
D11	70	F3			
D10	71	G1			
D9	72	G2			
D8	73	G3			
D7	3	J9			
D6	4	H10			
D5	5	H9			
D4	6	H8			
D3	8	G9			
D2	9	G8			
D1	10	F10			
D0	11	F9			
DMACK	20	E8	IU	I2U	DMA Acknowledge - input from host
DMARQ	14	F8	O	O1	DMA Request to host
IORDY	62	D2	O	O1	IORDY: When Ultra DMA mode DMA Write is not active and the device is not ready to respond to a data transfer request, this signal is negated to extend the Host transfer cycle. However, it is never negated by this controller.
DDMARDY#					DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
DSTROBE					DSTROBE: When Ultra DMA mode DMA Write is active, this signal is the data-out strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
CS1FX#	24	C10	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	52	B1			CS3FX# is used to select the Alternate Status register and the Device Control register.
CSEL	56	C3	IU	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, or tied to V_{DDQ}, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.

TABLE 3-1: Pin Assignments (Continued) (2 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
IORD#	19	E9	I	I2Z	IORD#: This is an I/O Read Strobe generated by the host. When Ultra DMA mode is not active, this signal gates I/O data from the device.
HDMARDY#					HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
HSTROBE					HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	57	D1	I	I2Z	This is an I/O Write Strobe generated by the host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device.
STOP					When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst
IOCS16#	55	C2	O	O2	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	21	D10	O	O1	This signal is the active high Interrupt Request to the host.
PDIAG#	54	C1	IU/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	75	H2	IU/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	1	K10	IU	I2U	This input pin is the active low hardware reset from the host.
WP#/PD#	97	H7	IU	I3U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting. This pin accepts only in the 3.3V V_{DD} signal level.
Flash Media Interface					
FRE#	84	H3	O	O5	Active Low Flash Media Chip Read
FWE#	96	J7			Active Low Flash Media Chip Write
FCLE	92	K6			Active High Flash Media Chip Command Latch Enable
FALE	94	H6			Active High Flash Media Chip Address Latch Enable
FAD15	46	A3	IU/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	44	B4			
FAD13	42	C5			
FAD12	40	A5			
FAD11	35	C7			
FAD10	33	A7			
FAD9	31	B8			
FAD8	29	B9			

TABLE 3-1: Pin Assignments (Continued) (3 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
FAD7	45	C4	IU/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	43	A4			
FAD5	41	B5			
FAD4	39	C6			
FAD3	34	B7			
FAD2	32	C8			
FAD1	30	A8			
FAD0	28	A9			
FCE7#	26	C9	O	O4	Active Low Flash Media Chip Enable pin
FCE6#	91	H5			
FCE5#	95	K7			
FCE4#	93	J6			
FCE3#	89	J5			
FCE2#	88	H4			
FCE1#	80	K3			
FCE0#	86	J4			
Serial Communication Interface (SCI)					
$SCID_{OUT}$	79	J2	O	O4	SCI interface data output
$SCID_{IN}$	78	K2	IU	I3U	SCI interface data input
SCICLK	77	K1	IU	I3U	SCI interface clock
Miscellaneous					
V_{SS} (IO)	2 12 27 36 64 74 90 98	A2 A6 A10 D4 E1 E10 H1 J10 K5 K8	PWR		Ground for I/O
V_{SS} (Core)	25 51	A1 B10	PWR		Ground for Core
V_{DD} (IO)	38 87	B6 K4	PWR		V_{DD} (3.3V)
V_{DD} (Core)	76	J1	PWR		V_{DD} (3.3V)
V_{DDQ} (IO)	7 69	F1 G10	PWR		V_{DDQ} (5V/3.3V) for Host interface
V_{REG}	82	J3	O		External Capacitor Pin
POR#	50	B3	I	Analog Input[2]	Power-on Reset (POR). Active Low
$T_{IE_}$DN	13 100	J8			Pin needs to be connected to V_{SS}.

TABLE 3-1: Pin Assignments (Continued) (4 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
DNU[3]	15	K9			
	16				
	17				
	18				
	37				
	47				
	48				
	49				
	58				Do Not Use, must be left unconnected.
	59				
	60				
	61				
	63				
	81				
	83				
	85				
	99				

T3-1.3 1355

1. IU or IxU = Input with on-chip pull-up.
   I or IxZ = Input without on-chip pull-up.
2. Analog input is connected to V_{DD} for supply voltage detection
3. All DNU pins should not be connected.

4.0 PRODUCT ORDERING INFORMATION

SST 55 VD 020 - 60 - C -TQW E
XX XX XXX - XX - X -XXX X

Environmental Attribute
E* = non-Pb

Package Modifier
W = 100 leads or 85 ball positions

Package Type
TQ = TQFP
MV = VFBGA

Operation Temperature
C = Commercial: 0°C to +70°C
I = Industrial: -40°C to +85°C

Frequency
60= 60 MHz

Device Number
020 = UDMA/ATA Controller

Function
D = Disk/Media Controller

Voltage
V = 2.7-3.465V

Product Series
NAND Controller

* Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

4.1 Valid Combinations

Valid combinations for SST55LD020

SST55VD020-60-C-TQWE	SST55VD020-60-C-MVWE
SST55VD020-60-I-TQWE	SST55VD020-60-I-MVWE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

5.0 PACKAGING DIAGRAM

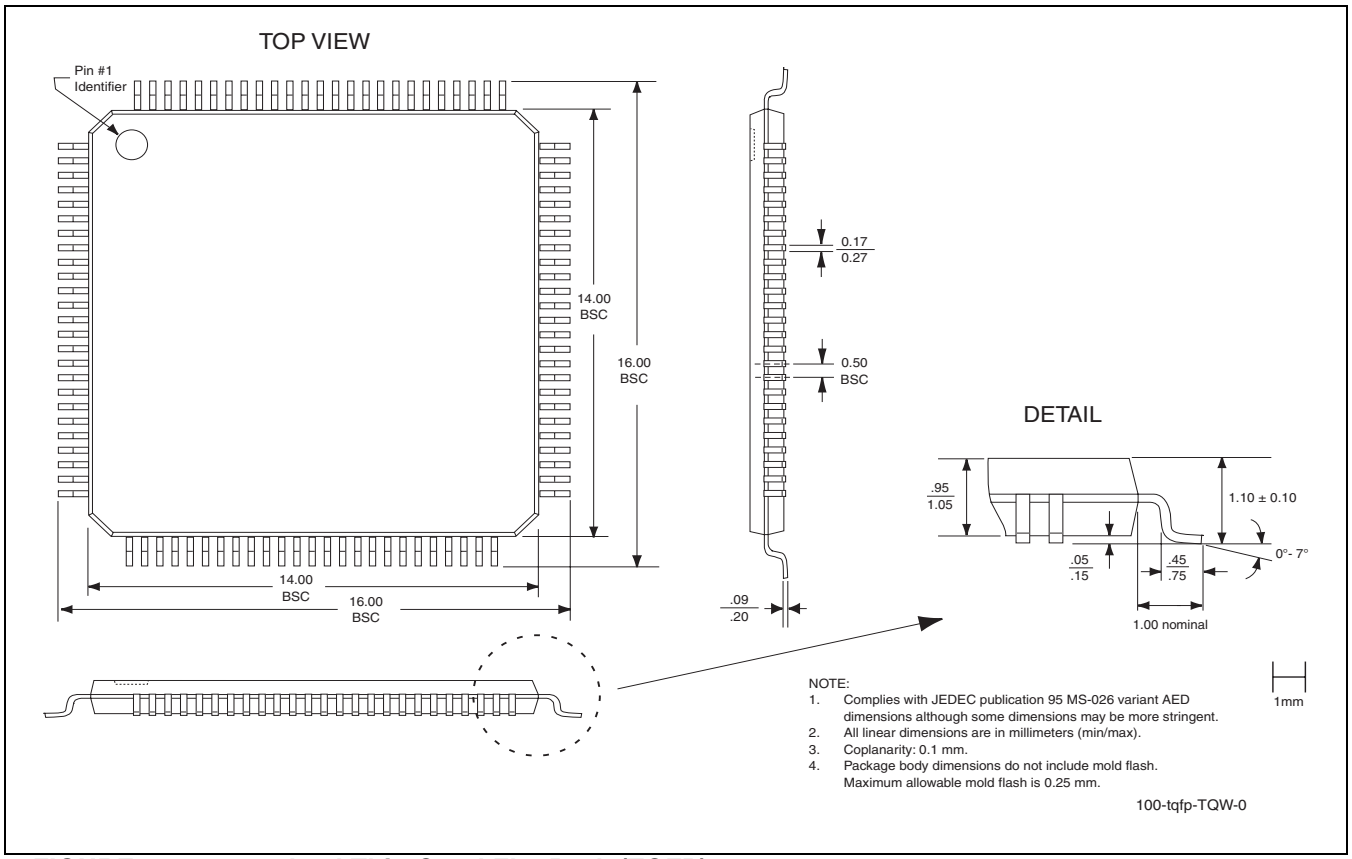
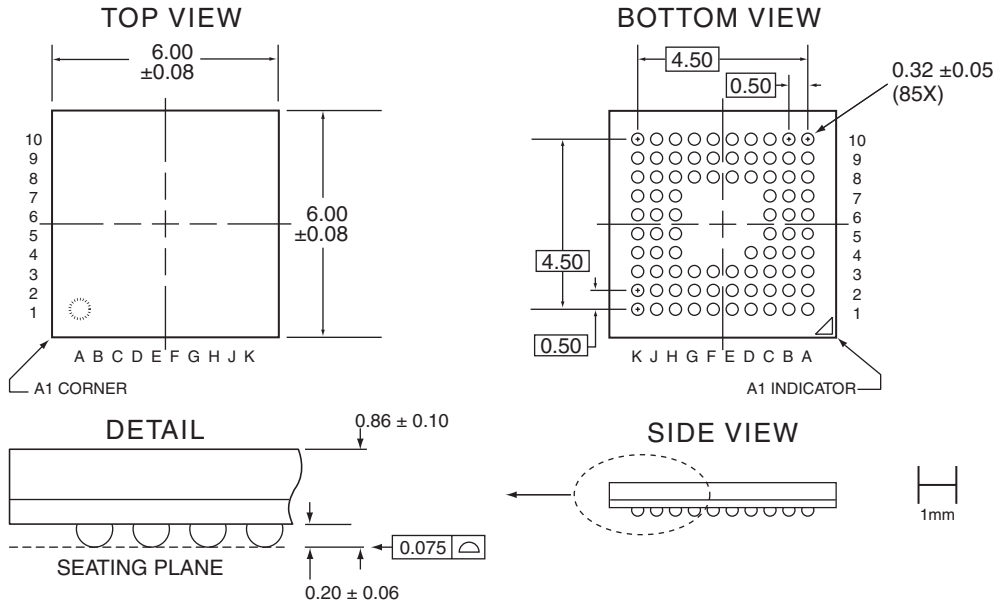


FIGURE 5-1: 100-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQW



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-225, this specific package is not registered
2. All linear dimensions are in millimeters
3. Coplanarity: 0.075 mm
4. Ball opening size is 0.29 mm (± 0.05 mm)

85-vfbga-MVW-6x6-32mic-0.0

FIGURE 5-2: 85-ball Very-Thin, Fine-Pitch, Ball Grid Array (VFBGA)
SST Package Code: MVW

TABLE 5-1: Revision History

Number	Description	Date
00	• Initial Release Fact Sheet	Aug 2007