Yannan (Nellie) Wu

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Education

Masssachusetts Institute of Technology — Cambridge, MA
Ph.D. *in Computer Science (GPA: 5.0/5.0)* — ***Aug. 2017 – present***
M.S. *in Computer Science (GPA: 5.0/5.0)* — ***Feb. 2020***
Advisors: Prof. Joel Emer & Vivienne Sze

Cornell University — Ithaca, NY
B.S. *in Electrical & Computer Engineering (GPA: 4.02/4.3; 4.0=A)* — ***May. 2017***

Research Interests and Objectives

My current research interest lies in the areas of computer architecture and computer systems. More specifically, I am interested in modeling and designing energy-efficient hardware accelerators for data and computation-intensive applications. **I'm looking for full-time positions starting around June 2023.**

Work Experience

- NVIDIA Computer Architecture Research Intern — May 2021 - Aug. 2021
- NVIDIA Computer Architecture Research Intern — May 2020 - Aug. 2020
- Goldman Sachs Technology Analyst — June 2016 - Aug. 2016

Skills

- C, C++, Python, MATLAB, Verilog, Docker, Git, Bash, LaTex, Markdown, HTML

Selected Research Experience

- **Co-design for Structured-Sparse DNN**: proposed a new hardware-aware structured sparsity pattern for DNN pruning; co-designd a hardware accelerator and a pruning procedure to allow efficient processing of accurate DNN models.
- **Saprseloop**: proposed a design space classification of sparse tensor accelerators; based on the classification, developed a fast, accurate and flexible analytical modeling tool for sparse tensor accelerators.
- **Timeloop-Accelergy Infrastructure**: developed an integrated modeling framework for dense DNN accelerators; provided open-source accelerator design specifications for the community.
- **Accelergy**: proposed a systematic methodology to describe the diverse components in various accelerator designs; based on the methodology, developed a flexible energy and area estimation framework.

Selected Patents and Publications

- **Pruning And Accelerating Neural Networks With A Novel Sparsity Structure**
  Yannan Wu, Po-An Tsai, Saurav Muralidharan, Joel S. Emer
  US Patent Application Number: 63/236,629
- **Sparseloop: An Analytical Approach to Sparse Tensor Accelerator Modeling**
  Yannan Nellie Wu, Po-An Tsai, Angshuman Parashar, Vivienne Sze, Joel S. Emer
  IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2022 ***(Distinguished Artifact Award)***
- **An Architecture-Level Energy and Area Estimator for Processing-In-Memory Accelerator Designs**
  Yannan Nellie Wu, Vivienne Sze, Joel S. Emer
  IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2020
- **Accelergy: An Architecture-Level Energy Estimation Methodology for Accelerator Designs**
  Yannan Nellie Wu, Joel S. Emer, Vivienne Sze
  IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov. 2019

Conference Tutorials

- **ISCA21 Tutorial: Sparse Tensor Accelerators: Abstraction and Modeling**
  Yannan Nellie Wu with Joel S. Emer, Vivienne Sze, Po-An Tsai, and Angshuman Parashar
- **ISCA20, ISPASS20, MICRO19 Tutorial: Tools for Evaluating DNN Accelerator Designs**
  Yannan Nellie Wu with Joel S. Emer, Vivienne Sze, Angshuman Parashar, and Po-An Tsai

Selected Awards

- MICRO22 Distinguished Artifact Award — Oct. 2022
- MIT Jacob's Presidential Fellowship — Sept. 2017 - May. 2018
- Cornell ECE Early Career Scholarship — June. 2014 - Aug. 2014