Yannan (Nellie) Wu

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Education

Masssachusetts Institute of Technology — Cambridge, MA

- *Ph.D. in Electrical Engineering and Computer Science; GPA: 5.0/5.0* — *Aug. 2017 – present*
  Advisors: Prof. Joel Emer & Vivienne Sze

Masssachusetts Institute of Technology — Cambridge, MA

- *M.S. in Electrical Engineering and Computer Science; GPA: 5.0/5.0* — *Aug. 2017 – Feb. 2020*
  Advisors: Prof. Joel Emer & Vivienne Sze

Cornell University — Ithaca, NY

- *B.S. in Electrical & Computer Engineering; GPA: 4.02/4.3 (4.0 = A)* — *Aug. 2013 – May. 2017*
  Minor: Computer Science

Research Interests

My current research interest lies in the areas of computer architecture and computer systems. More specifically, I am interested in modeling and designing energy-efficient hardware accelerators for data and computation-intensive applications.

Patents

- **Pruning And Accelerating Neural Networks With Structured Sparsity**
  Yannan Wu, Po-An Tsai, Saurav Muralidharan, Joel S. Emer
  US Patent Application Number: 63/236,629

Conference Tutorials

- **Sparse Tensor Accelerators: Abstraction and Modeling**
  Yannan Nellie Wu with Joel S. Emer, Vivienne Sze, Po-An Tsai, and Angshuman Parashar
  IEEE International Symposium on Computer Architecture (ISCA), June, 2021
- **Tools for Evaluating Deep Neural Network Accelerator Designs**
  Yannan Nellie Wu with Joel S. Emer, Vivienne Sze, Angshuman Parashar, and Po-An Tsai
  - *ACM/IEEE International Symposium on Computer Architecture (ISCA)*, June 2020
  - *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2020
  - *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Oct. 2019

Publications

- **Sparseloop: An Analytical Approach to Sparse Tensor Accelerator Modeling**
  Yannan Nellie Wu, Po-An Tsai, Angshuman Parashar, Vivienne Sze, Joel S. Emer
  IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2022
- **Architecture-Level Energy Estimation for Heterogeneous Computing Systems**
  Francis Wang, Yannan Nellie Wu, Matthew Woicik, Vivienne Sze, Joel S. Emer
  IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2021
- **Sparseloop: An Analytical, Energy-Focused Design Space Exploration Methodology for Sparse Tensor Accelerators**
  Yannan Nellie Wu, Po-An Tsai, Angshuman Parashar, Vivienne Sze, Joel S. Emer
  IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2021
- **An Architecture-Level Energy and Area Estimator for Processing-In-Memory Accelerator Designs**
  Yannan Nellie Wu, Vivienne Sze, Joel S. Emer
  IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2020

- **A Systematic Approach for Architecture-Level Energy Estimation of Accelerator Designs**
  Yannan Nellie Wu
  Master Thesis, Massachusetts Institute of Technology, Feb. 2020
- **Accelergy: An Architecture-Level Energy Estimation Methodology for Accelerator Designs**
  Yannan Nellie Wu, Joel S. Emer, Vivienne Sze
  IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov. 2019

Conference/Journal Reviewer Services

- *IEEE Journal of Solid-State Circuits (JSSC)*
- *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*
- *IEEE Transactions on Very Large Scale Integration Systems (VLSI)*
- *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*

Honors and Scholarships

- MIT Jacob's Presidential Fellowship — Sept. 2017 - May. 2018
- Member of IEEE-HKN Eta Kappa Nu Honor Society — Oct. 2015 - May. 2017
- Cornell University College of Energineering Dean's List — All Semesters (2013 - 2017)
- Cornell Undergraduate Research Funding — June 2015 - Aug. 2015
- Cornell ECE Early Career Scholarship — June. 2014 - Aug. 2014

Research Experience

- **Graduate Research Assistant** — Massachusetts Institute of Technology
  Advised by: Professors Joel Emer & Vivienne Sze — *Aug. 2017 - Present*
  - **Performance Modeling of Various Deep Neural Network (DNN) and Tensor Accelerators**
    - Designed Python-based infrastructure with modularized and parameterizable architecture building blocks for cycle accurate simulations of DNN accelerator designs.
    - Developed an energy and area estimation infrastructure called Accelergy for analyzing accelerators' energy consumption at an architectural level without RTL implementation.
    - Studied the hardware architecture charateristics for processing in memory DNN accelerator designs.
    - Developed a flexible and modularized modeling methodology for diverse sparse tensor accelerator designs.
    - Developed a software-hardware co-design algorithm for efficient processing of structurally pruned DNN models.
- **Undergraduate Research Assistant** — Cornell University
  Advised by: Professors Jose Martinez, Rachit Agarwal & Christina Delimitrou — *Aug. 2014 - May 2017*
  - Reinforcement Learning Aided Garbage Collection for FLASH SSD
  - User-Centric Energy-Efficient Scheduling on Multi-Core Mobile Device
  - ECE3140 Embedded System Lab Development
  - Analyze the performance of disaggregated datacenter architecture in cloud

Work Experience

- NVIDIA Corporation Computer Architecture Research Intern — May 2021 - Aug. 2021
- NVIDIA Corporation Computer Architecture Research Intern — May 2020 - Aug. 2020
- Goldman Sachs Technology Analyst — June 2016 - Aug. 2016

Teaching Experience

- MIT 6.825 Hardware Architecture for Deep Learning Lead TA — Jan. 2020 - May. 2020
- MIT 6.888 Hardware Architecture for Deep Learning TA (part-time) — Jan. 2019 - May. 2019
- Cornell ECE 3140 Embedded Systems TA — Jan. - May. 2016 & Aug.- Dec 2015
- Cornell ECE 2300 Digital Logic & Comp. Arch. TA — Jan. - May. 2015 & Aug. - Dec. 2014
- Cornell MATH 1920 Multivariable Calc. Course Assistant — Jan. - May. 2015 & Aug. - Dec. 2014
- Cornell CS 1112 MATLAB Programming Course Consultant — Jan. 2014 - May. 2014

Leadership

- MIT Sidney Pacific Residence Hall Publicity Chair — May. 2019 - May. 2020
- MIT Sidney Pacific Residence Hall Social Chair — May 2018 - May 2019
- Cornell Society of Women Engineers General Body Chair — Aug. 2014 - May 2015

Skills

- C, C++, Python, Docker, Linux, Verilog, Java, MATLAB, LaTex, Markdown, HTML, Synopsys design compiler

Core Courses

Graduate: Hardware Architecture for Deep Learning, Computer Architecture, Digital Circuit Designs, Numerical Simulations, Digital Image Processing

Undergraduate: Advanced Computer Architecture, Operating Systems, Embedded Systems, Database Systems, Computer Networks and Telecommunications, Probability and Inference, Microelectronics