



**FIGURE 4.17 The simple datapath with the control unit.** The input to the control unit is the 6-bit opcode field from the instruction. The outputs of the control unit consist of three 1-bit signals that are used to control multiplexers (RegDst, ALUSrc, and MemtoReg), three signals for controlling reads and writes in the register file and data memory (RegWrite, MemRead, and MemWrite), a 1-bit signal used in determining whether to possibly branch (Branch), and a 2-bit control signal for the ALU (ALUOp). An AND gate is used to combine the branch control signal and the Zero output from the ALU; the AND gate output controls the selection of the next PC. Notice that PCSrc is now a derived signal, rather than one coming directly from the control unit. Thus, we drop the signal name in subsequent figures.

datapath. In the next few figures, we show the flow of three different instruction classes through the datapath. The asserted control signals and active datapath elements are highlighted in each of these. Note that a multiplexor whose control is 0 has a definite action, even if its control line is not highlighted. Multiple-bit control signals are highlighted if any constituent signal is asserted.

Instruction
R-format
lw
sw
beq

**FIGURE 4.18**

row of the table are  $r_s$  and  $r_t$ , and  $w$  writes a register replaced with PC. Instructions in the  $PC$  column give the control flow.  $MemWrite$  are set for store instructions.  $MemRead$  are set for load instructions. The branch bit  $br$  is set for a subtraction instruction if  $br == 1$  and  $is_0 == 0$ : since the register is zero, the two rows of the table are added by the

Figure 4.1  
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of informati

1. The instruction register
2. Two registers for control
3. The ALU and code (ALU function)
4. The register file and the instruction

Similarly,

7w \$t

in a style similar  
asserted cont  
five steps (sim

1. An increment operation
2. A register operation