IGEP.0022 - IGEPv2 EXPANSION - PROTO B3 -30/09/2010

REV	Description	DATE	BY
A2	First Release	24/05/2010	JAP
A3	J960 New Part Number. SAMTEC HLE SERIE (BOTTOM ENTRY)	26/05/2010	JAP
A4	U401 Incorrect schematic signals U204 Deleted 2V8 from 3V3 by using 1n4148 diodes J405 Add pins S1 and S2 connected to GND	9/06/2010	JAP
A5	Deleted U201. New U204 Regulator LM3966 for MODEM GSM/GPRS Deleted R201, F201 and D201 J991 pinout	22/06/2010	JAP
A6	New R420 between MODEM_PWRMON and 2V8 R411 and R412 new values U501A new value TVP5151PBS J990 and J960 new values U302 new value TSC2046IPWR	20/07/2010	JAP
B1	1. J301 and J302 LCD Data Bus new pinout (from 24-bit RGB to 24-bit BGR). 2. LVDS DSS interface new pinout (from 18-bit RGB ro 18-bit BGR)	9/09/2010	JAP
B2	3. Deleted nets UART3_TXD_3V3 and UART3_RXD_3V3. 4. RS232 driver various corrections 5. VGA - Deleted D801, D801, F801, R802, C811, D803 6. VGA - New capacitor 100nF from VREF to VGA_AVCC 7. VGA - C812, C813 and C814 from 47pF to 10pf 8. VGA - all BAV99L DNI 9. VGA - New BUS VGA_D[0..23] 10. LCD - New bus LCD_D[0:23]	21/09/2010	JAP
B3	11. LCD - Deleted net LCD_3V3. LCD_3V3=3V3 12. CAN - U702 OE connected to 1V8 13. CAN - new net CAN_IRQ 14. LVDS - Add new R907 and R908 15. TFT: Erased net LCD_DEN from J301:32 connector 16. TFT: New R320 J301:32 to 3V3 17. VIDEO: Erase net CAM_RESET and CAM_PDN from JC30:23,24. Erase R519 and R521. 18. CONNECTORS: Add new R909 and R910. I2C pull up 19. CONECTORS: Erased net I2C_SCL and I2C_SDA from JC30:21,22. 20. VIDEO : Y501 crystal should be 27MHZ (before 14.31818MHz) 21. VGA - U801 = ADV7125KSTZ140	30/09/2010	JAP

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COVER

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MAIN POWER SUPPLY (5V)

J201
RASM722P
GND

LINEAR REGULATOR (5v -> 3V8) / 3A

DC_5V
(*) 2A
U204
LP3966
IN
OUT
SHDN
GND
ADJ
R221 10K
R204 22K
R203 10K
C214 68uF
C201 68pF
C213 33uF
(*) 2A
VBAT
TP201

3V8 (VBAT,MODEM GSM/GPRS)

LINEAR REGULATOR (VBAT / 5V -> 3v3) / 1A

DC_5V
R205 0R
(*) 2A
VBAT
R206 DNI 0R
(*) 2A
U202
TPS73701
3V3_EN
3V3_ADJ
C206 1uF
R208 30.1K 1%
R207 52.3K 1%
C205 100nF
C208 10uF
C207 100nF
3V3
TP202
D107 DNI MMSD4148
D106 DNI MMSD4148
R214 DNI 0R
R215 DNI 0R
2V8
TP207
R213 DNI 1K

3V3 (LCD, VGA, RS232)

3V3
DC_3V3
R219 DNI 0R

(MODEM GSM/GPRS)

LINEAR REGULATOR (VBAT / 5v -> 1v8) / 1A

R209 10K
3V3_EN
11 LCD_EN
LCD_EN
Q201 MMUN2233
R210 10K
U203
TPS73701
1V8_ADJ
C210 1uF
R212 56.2K 1%
C209 100nF
R211 28K 1%
C212 10uF
C211 100nF
1V8
TP203
1V8
VIO_1V8
R220 DNI 0R

1V8 (VIDEO DECODER)

TP204
TP205
GND

Close to power jack
R216 0R
GND_EARTH
J202
DNI TAL1

1V8
R217 10K
SW201
SW_PB_SPST
BUTTON1 11

1V8
R218 10K
SW202
SW_PB_SPST
BUTTON2 11

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MAIN POWER

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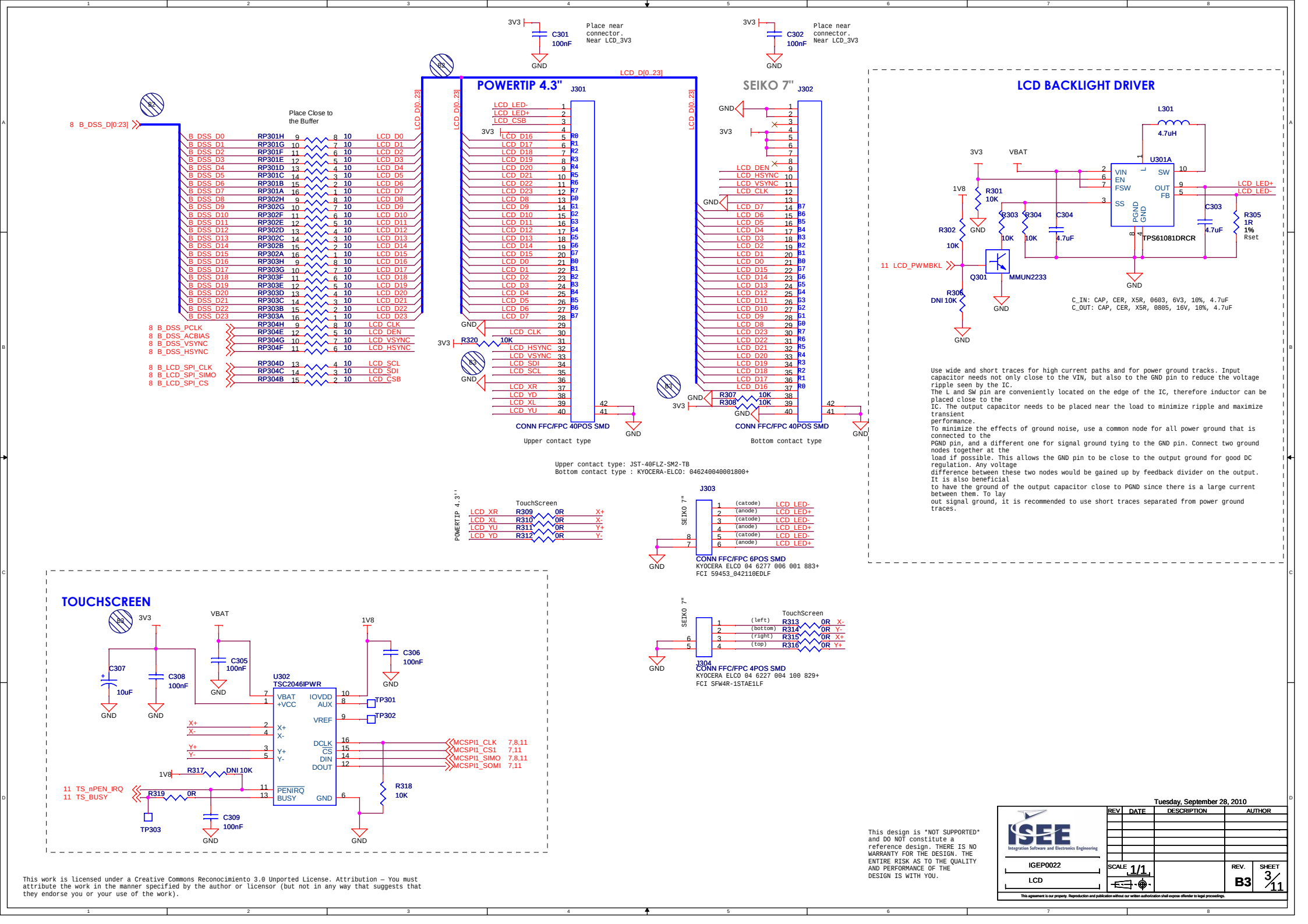
LCD BACKLIGHT DRIVER
L301
4.7uH
U301A
TPS61081DRCR
R301 10K
R302 10K
R303 10K
R304 10K
C304 4.7uF
C303 4.7uF
R305 1R 1% Rset
Q301 MMUN2233
R306 DNI 10K
11 LCD_PWMBKL
LCD_LED+
LCD_LED-
C_IN: CAP, CER, X5R, 0603, 6V3, 10%, 4.7uF
C_OUT: CAP, CER, X5R, 0805, 16V, 10%, 4.7uF
Use wide and short traces for high current paths and for power ground tracks. Input capacitor needs not only close to the VIN, but also to the GND pin to reduce the voltage ripple seen by the IC.
The L and SW pin are conveniently located on the edge of the IC, therefore inductor can be placed close to the
IC. The output capacitor needs to be placed near the load to minimize ripple and maximize transient
performance.
To minimize the effects of ground noise, use a common node for all power ground that is connected to the
PGND pin, and a different one for signal ground tying to the GND pin. Connect two ground nodes together at the
load if possible. This allows the GND pin to be close to the output ground for good DC regulation. Any voltage
difference between these two nodes would be gained up by feedback divider on the output. It is also beneficial
to have the ground of the output capacitor close to PGND since there is a large current between them. To lay
out signal ground, it is recommended to use short traces separated from power ground traces.
POWERTIP 4.3" J301
SEIKO 7" J302
LCD_D[0..23]
Place Close to the Buffer
8 B_DSS_D[0:23]
8 B_DSS_PCLK
8 B_DSS_ACBIAS
8 B_DSS_VSYNC
8 B_DSS_HSYNC
8 B_LCD_SPI_CLK
8 B_LCD_SPI_SIMO
8 B_LCD_SPI_CS
RP301H RP301G RP301F RP301E RP301D RP301C RP301B RP301A
RP302H RP302G RP302F RP302E RP302D RP302C RP302B RP302A
RP303H RP303G RP303F RP303E RP303D RP303C RP303B RP303A
RP304H RP304E RP304G RP304F RP304D RP304C RP304B
R320 10K
CONN FFC/FPC 40POS SMD
Upper contact type
Bottom contact type
Upper contact type: JST-40FLZ-SM2-TB
Bottom contact type : KYOCERA-ELCO: 046240040001800+
C301 100nF
C302 100nF
Place near connector. Near LCD_3V3
TouchScreen
POWERTIP 4.3"
LCD_XR R309 0R X+
LCD_XL R310 0R X-
LCD_YU R311 0R Y+
LCD_YD R312 0R Y-
J303
SEIKO 7"
CONN FFC/FPC 6POS SMD
KYOCERA ELCO 04 6277 006 001 883+
FCI 59453_042110EDLF
J304
CONN FFC/FPC 4POS SMD
KYOCERA ELCO 04 6227 004 100 829+
FCI SFW4R-1STAE1LF
TOUCHSCREEN
U302 TSC2046IPWR
C305 100nF
C306 100nF
C307 10uF
C308 100nF
C309 100nF
R317 DNI 10K
R318 10K
R319 0R
TP301
TP302
TP303
11 TS_nPEN_IRQ
11 TS_BUSY
MCSPI1_CLK 7,8,11
MCSPI1_CS1 7,11
MCSPI1_SIMO 7,8,11
MCSPI1_SOMI 7,11
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IGEP0022
LCD
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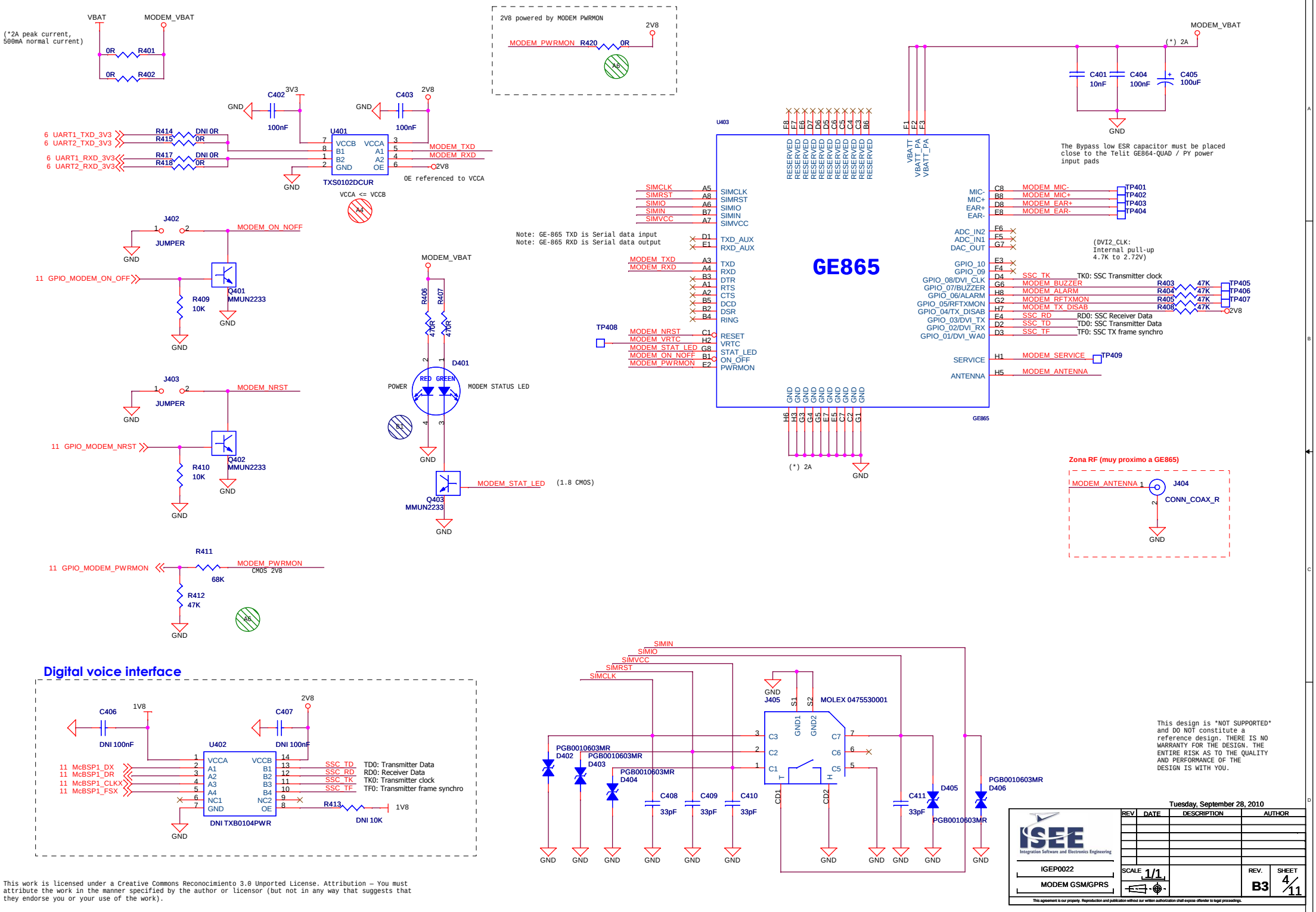

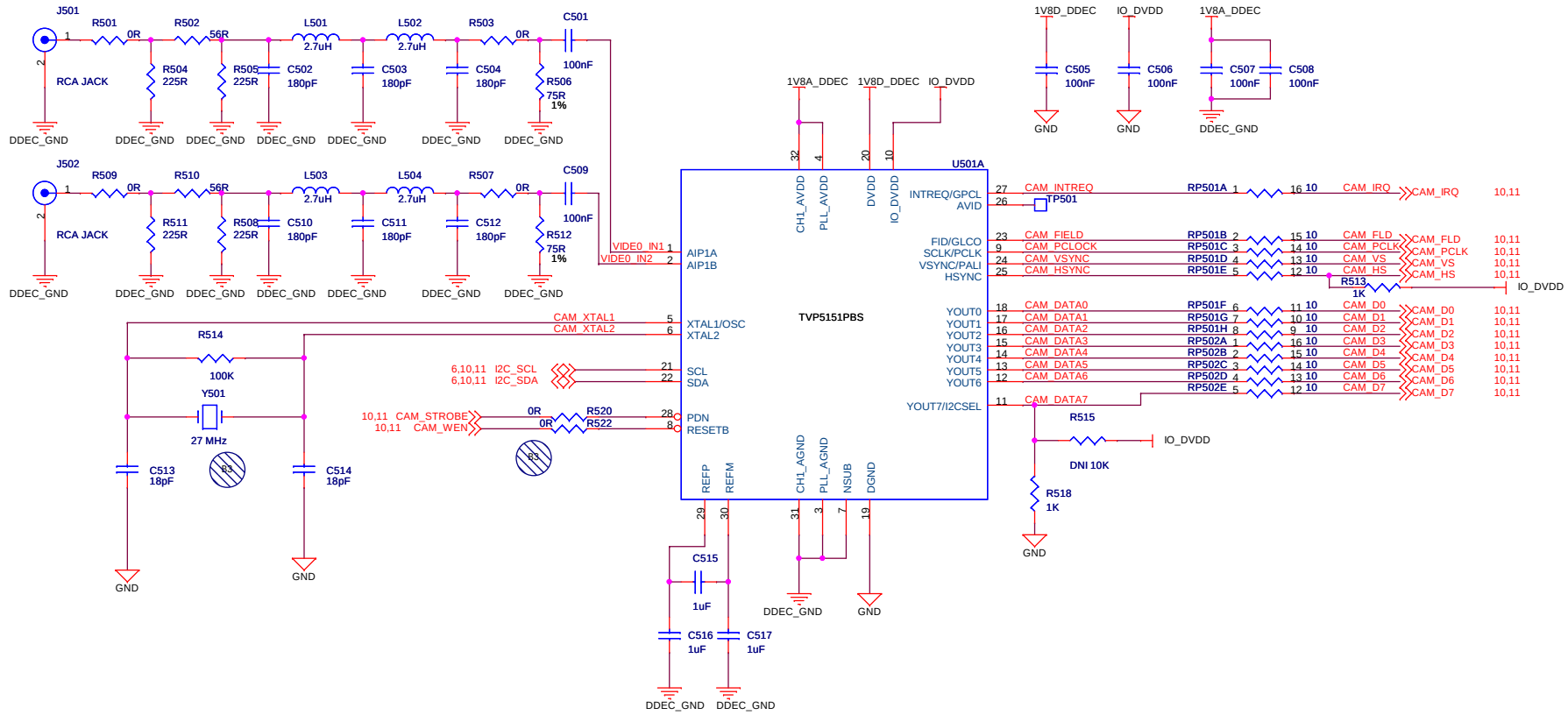

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VIDEO DECODER

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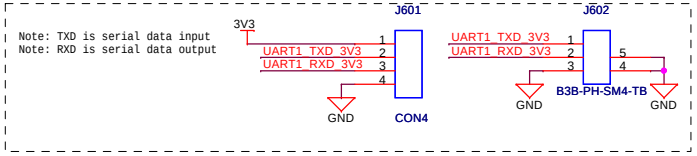
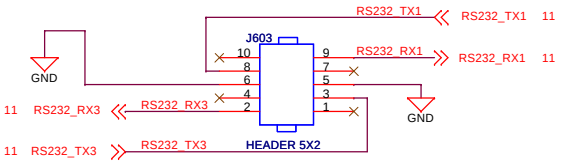


RS232 CONNECTOR



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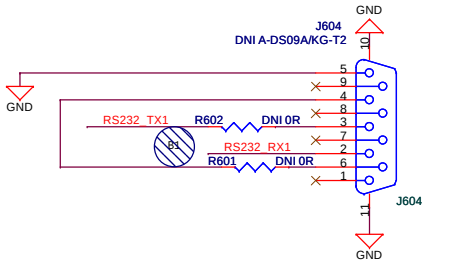
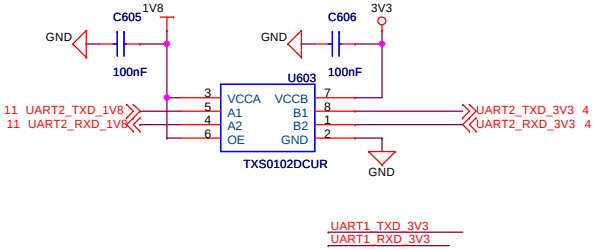
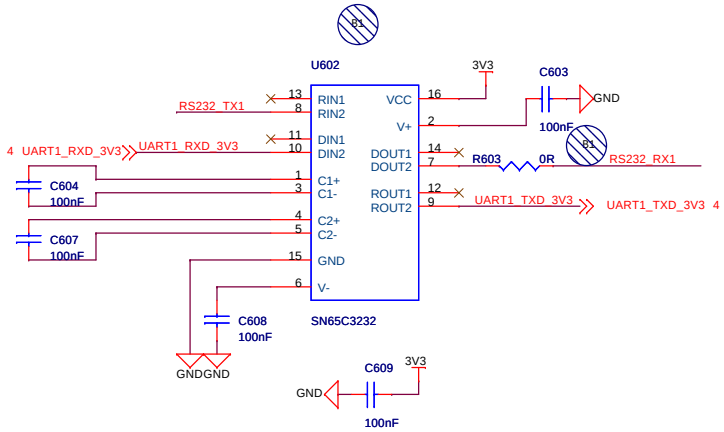
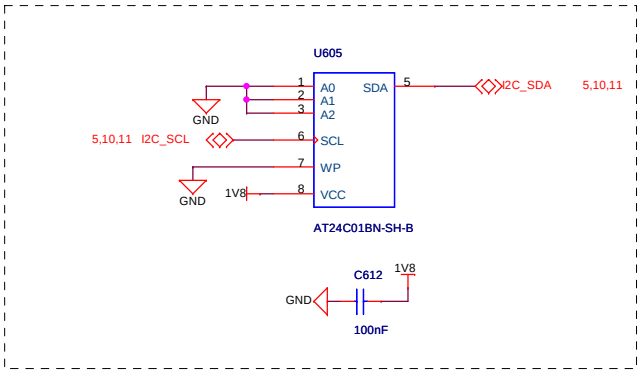






I2C EEPROM



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RS232

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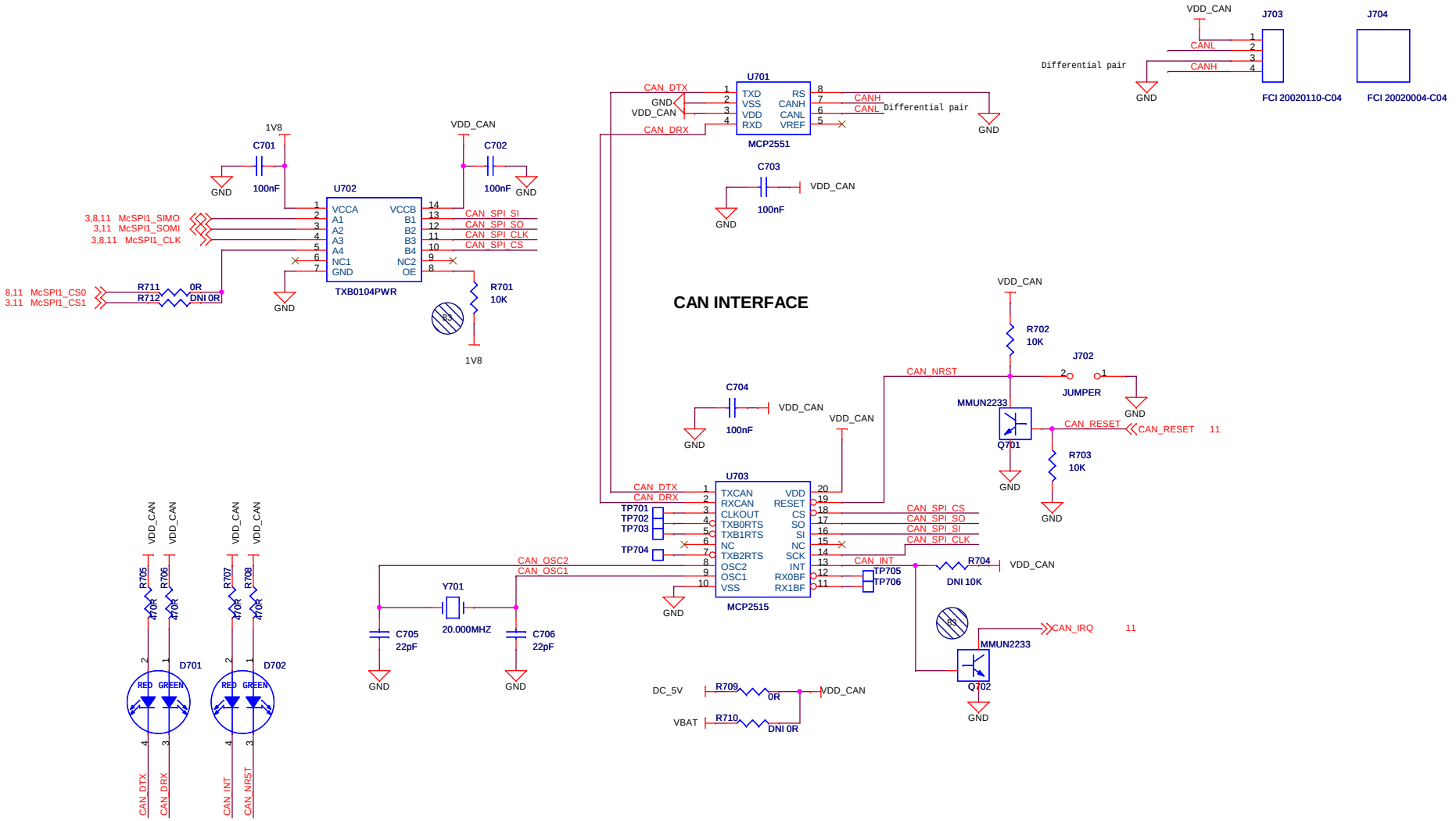

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CAN BUS INTERFACE

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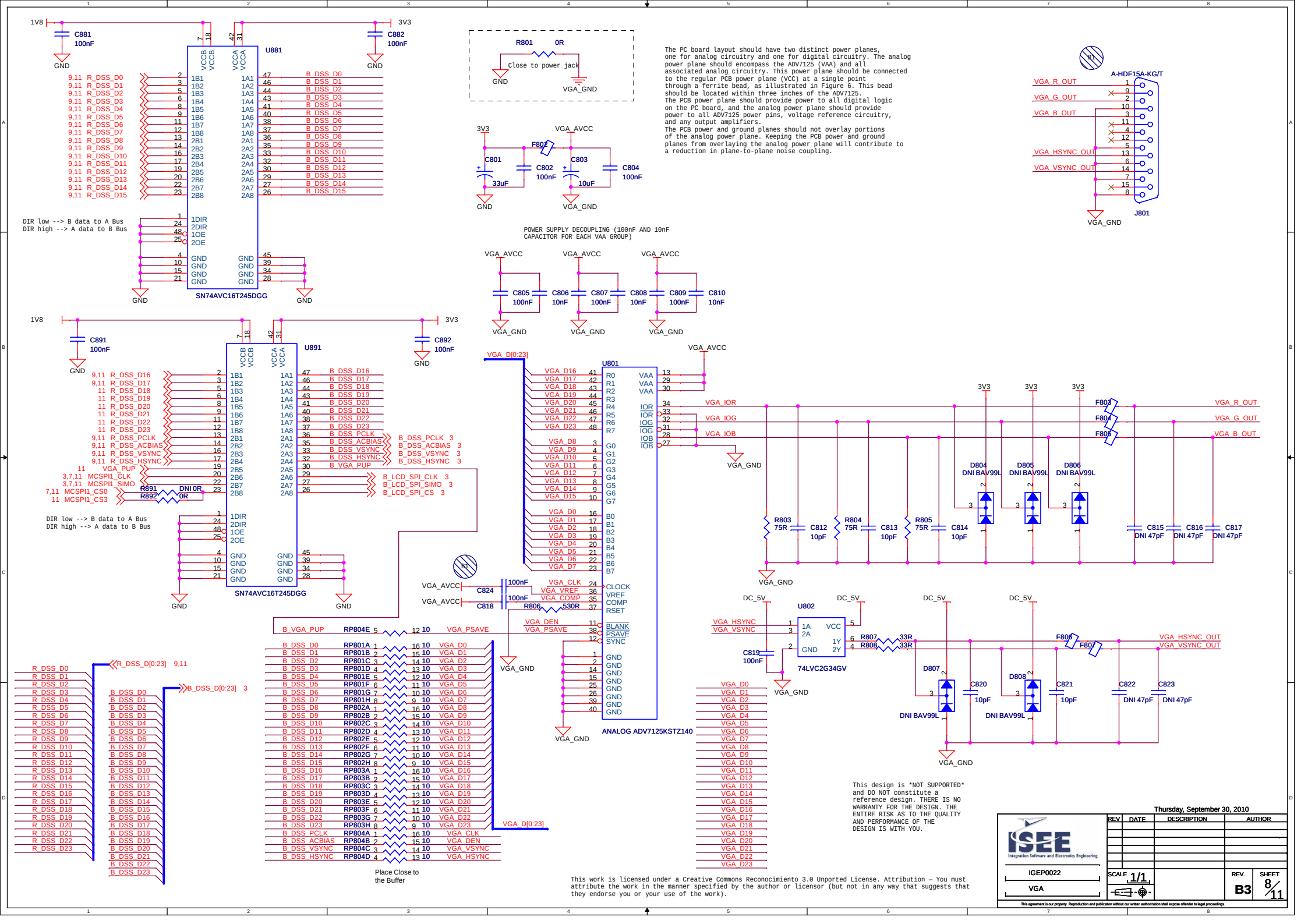
U881
SN74AVC16T245DGG
U891
SN74AVC16T245DGG
U801
ANALOG ADV7125KSTZ140
U802
74LVC2G34GV
J801
A-HDF15A-KG/T
R801 0R
Close to power jack
The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7125 (VAA) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 6. This bead should be located within three inches of the ADV7125. The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7125 power pins, voltage reference circuitry, and any output amplifiers. The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.
POWER SUPPLY DECOUPLING (100nF AND 10nF CAPACITOR FOR EACH VAA GROUP)
DIR low --> B data to A Bus
DIR high --> A data to B Bus
Place Close to the Buffer
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IGEP0022
VGA
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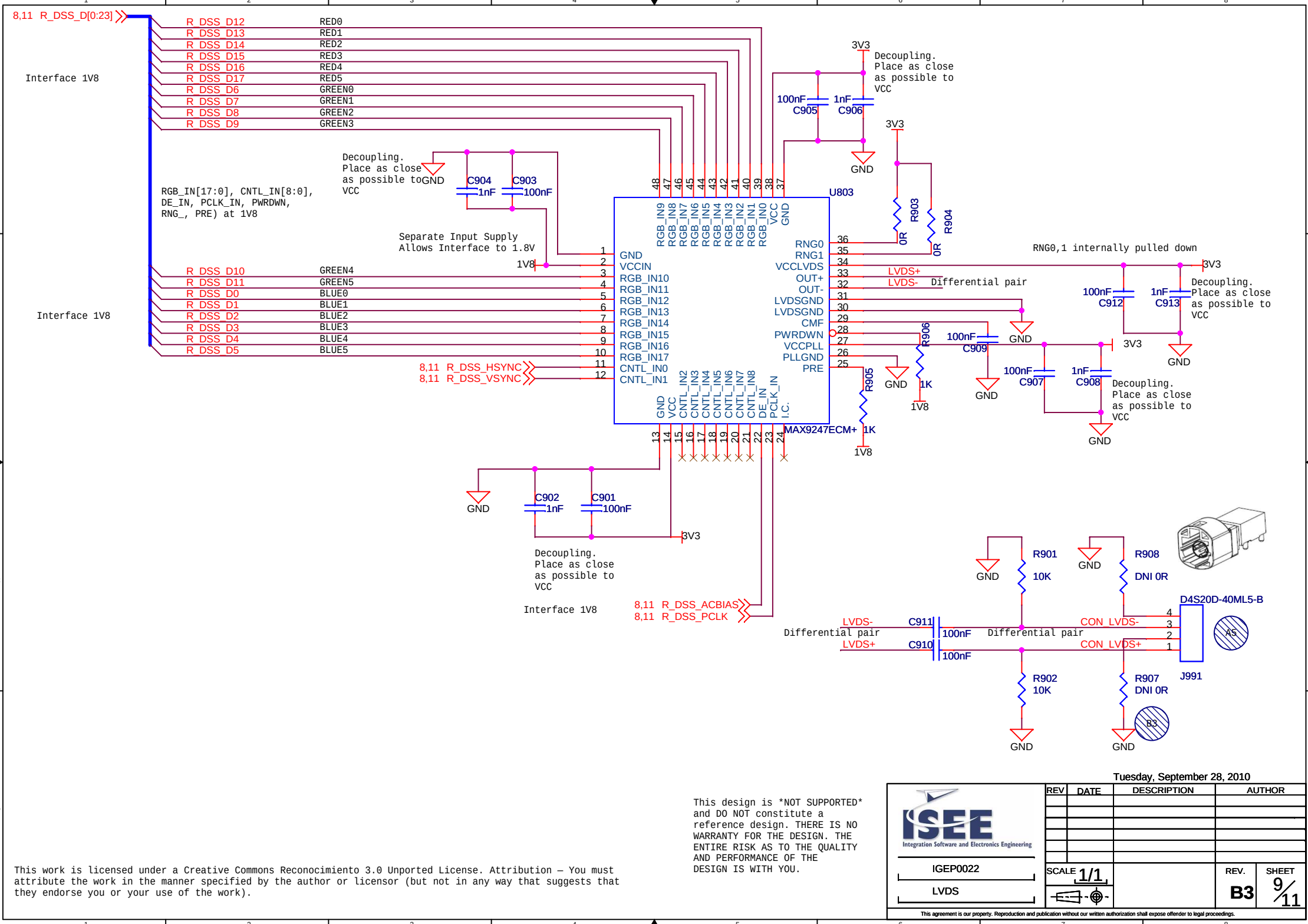

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LVDS

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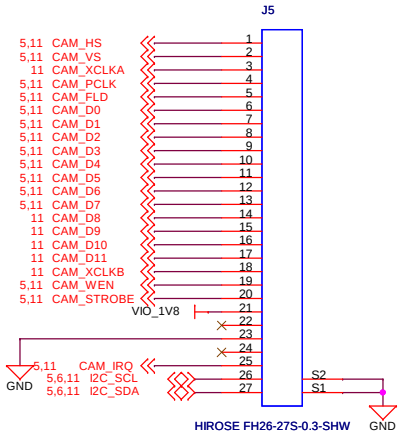
Camera connector.
27-pin connector J5
Camera interface



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IGEPv3 Connectors

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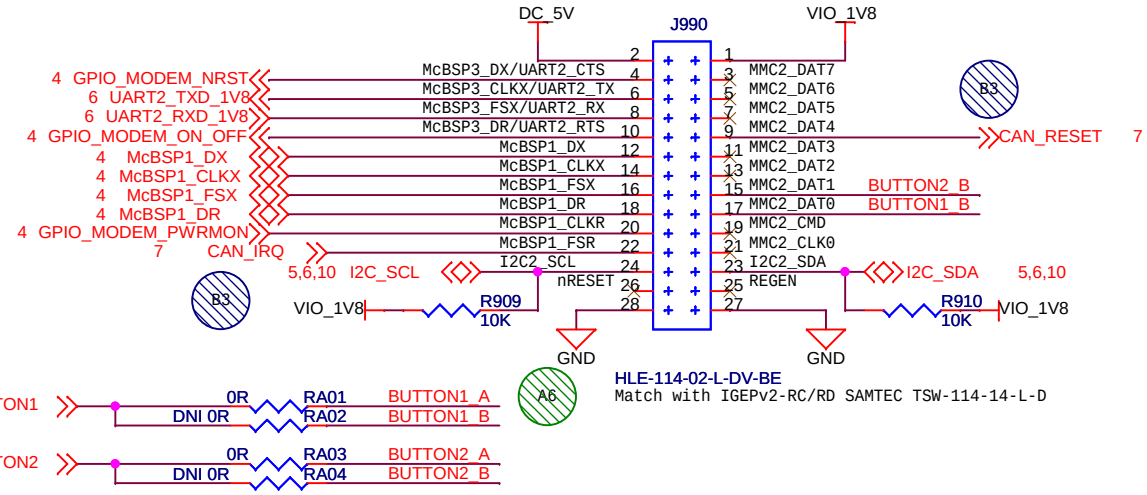
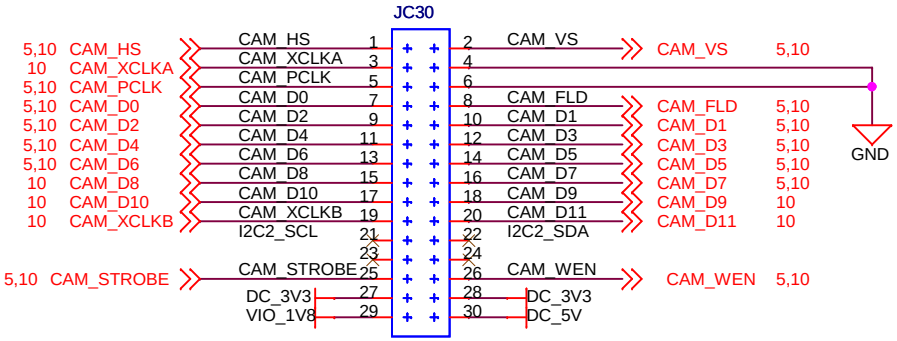
IGEPv2
EXPANSION CONNECTOR



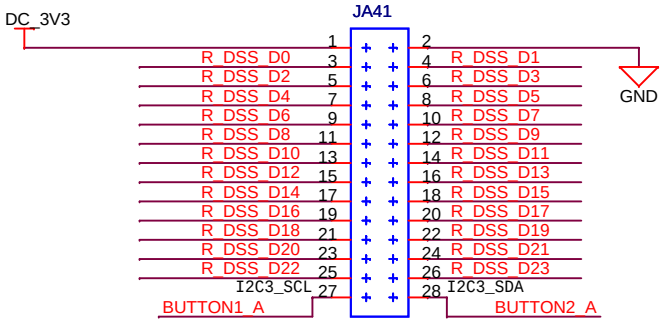
HLE-114-02-L-DV-BE
Match with IGEPv2-RC/RD SAMTEC TSW-114-14-L-D

IGEPv2
CAM CONNECTOR

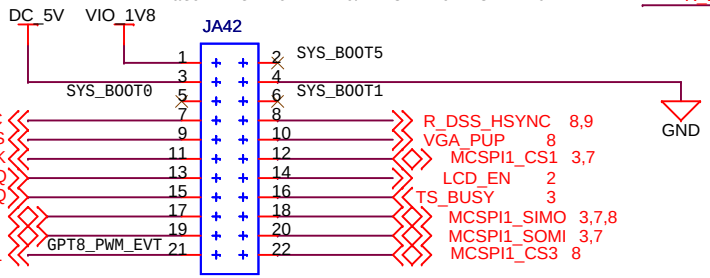


SFMC-115-01-L-D
Match with IGEPv2-RC SAMTEC FTS-114-01-L-D
Match with IGEPv2-RD SAMTEC FTS-115-01-L-D

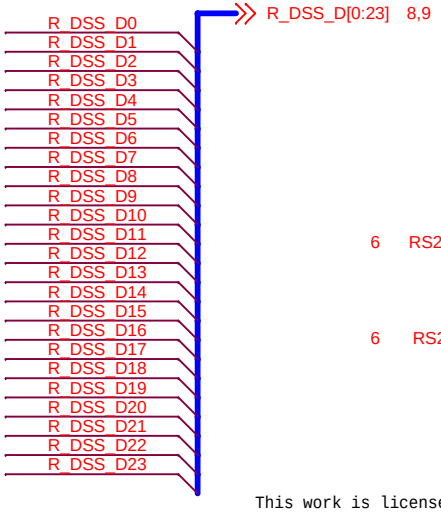
IGEPv2
TFT CONNECTOR



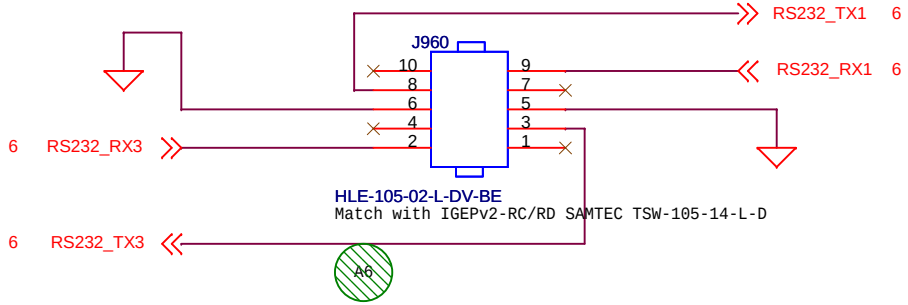
SFMC-114-01-L-D
Match with IGEPv2-RC/RD SAMTEC FTS-114-01-L-D



SFMC-111-01-L-D
Match with IGEPv2-RC SAMTEC FTS-110-01-L-D
Match with IGEPv2-RD SAMTEC FTS-111-01-L-D



IGEPv2
RS232 CONNECTOR



HLE-105-02-L-DV-BE
Match with IGEPv2-RC/RD SAMTEC TSW-105-14-L-D

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IGEPv2 CONNECTORS

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