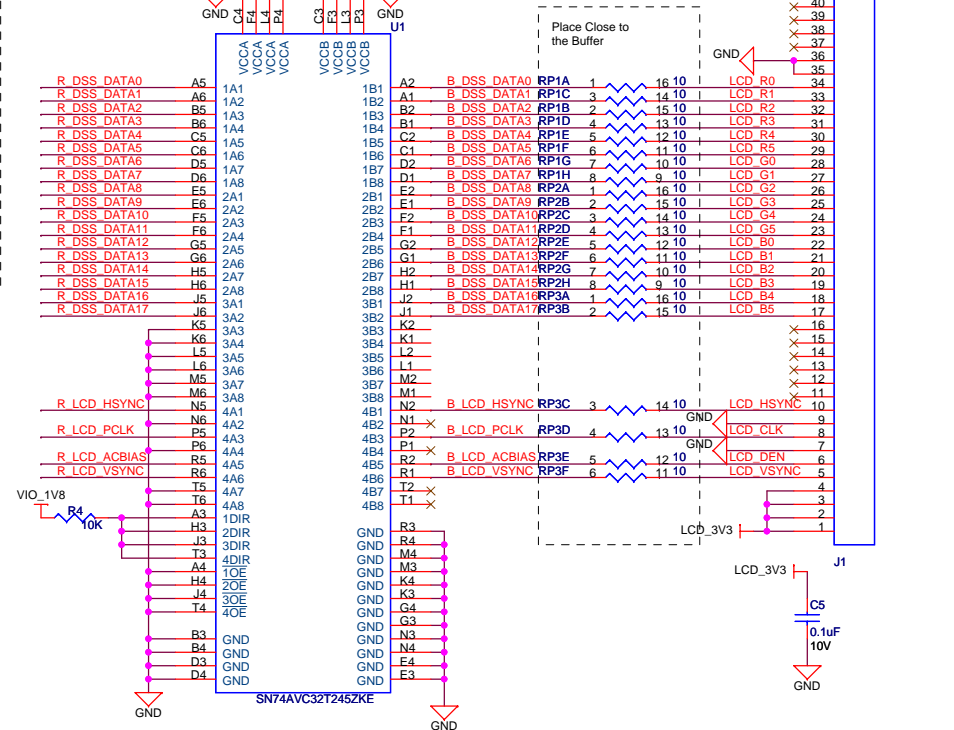


**3V3**

JA1	
1	R_DSS_DATA0
2	R_DSS_DATA1
3	R_DSS_DATA2
4	R_DSS_DATA3
5	R_DSS_DATA4
6	R_DSS_DATA5
7	R_DSS_DATA6
8	R_DSS_DATA7
9	R_DSS_DATA8
10	R_DSS_DATA9
11	R_DSS_DATA10
12	R_DSS_DATA11
13	R_DSS_DATA12
14	R_DSS_DATA13
15	R_DSS_DATA14
16	R_DSS_DATA15
17	R_DSS_DATA16
18	R_DSS_DATA17
19	
20	

**JA2**

JA2	
1	VIO_1V8
2	DC_5V
3	
4	
5	R_LCD_VSYNC
6	R_LCD_HSYNC
7	R_LCD_ACBIAS
8	
9	R_LCD_PCLK
10	
11	
12	TS_nPEN_IRQ
13	R_LCD_EN
14	
15	
16	MCSP11_CLK
17	MCSP11_SIMO
18	MCSP11_CS0
19	MCSP11_SOMI
20	



# LCD BACKLIGHT DRIVER

DC 5V

LCD EN

R1 100K

C4 4.7uF

R2 0R

U2A

VIN

EN

FSW

SS

PGND

GND

SW

OUT

FB

L1

TDK VLF5020T-4R7N1R7-1

LCD LED+

LCD LED-

R3 1R

C3 4.7uF

J2

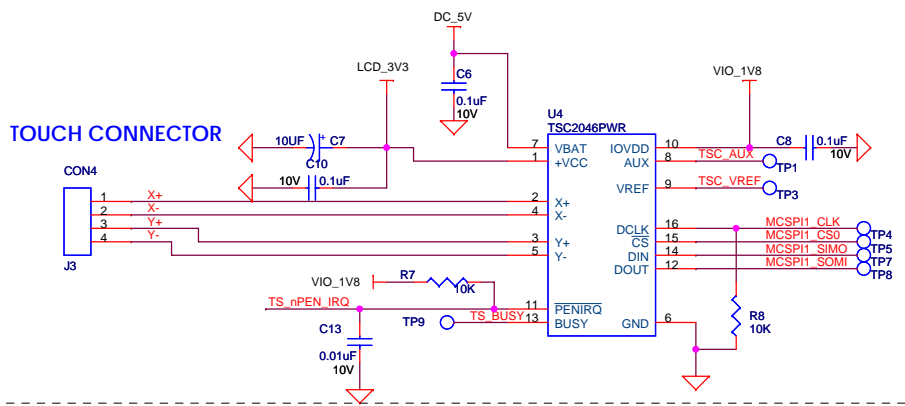
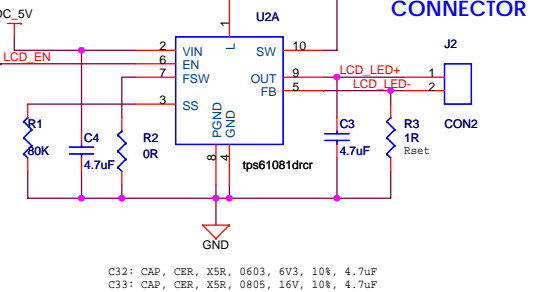
CON2

tpsg61081drcr

GND

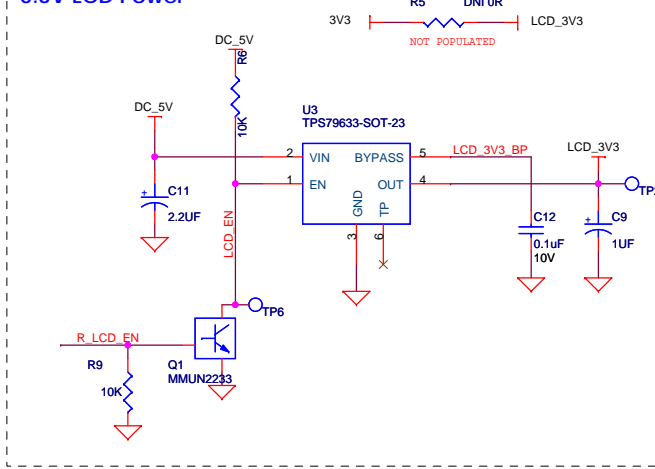
C32: CAP, CER, X5R, 0603, 6V3, 10%, 4.7uF

C33: CAP, CER, X5R, 0805, 16V, 10%, 4.7uF



### 3.3V LCD Power

The schematic diagram illustrates the 3.3V LCD Power circuit. It features a 3V3 input connected to a resistor R5 (DNI 0R, not populated) and then to LCD\_3V3. A DC\_5V input is connected to a 10K resistor R2, which then connects to the VIN pin of the U3 TPS79633-SOT-23 regulator. The EN pin of U3 is connected to a 2.2uF capacitor C11 to ground and to the LCD\_EN signal. The OUT pin of U3 is connected to the LCD\_3V3\_BP signal, which is then connected to LCD\_3V3 through a 0.1uF capacitor C12 to ground. A 1uF capacitor C9 is connected to LCD\_3V3 to ground. The LCD\_EN signal is also connected to the base of a PNP transistor Q1 (MMUN2233) through a 10K resistor R9. The emitter of Q1 is connected to ground, and the collector is connected to TP6.



This design is \*NOT SUPPORTED\* and DO NOT constitute a reference design. THERE IS NO WARRANTY FOR THE DESIGN. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN IS WITH YOU.