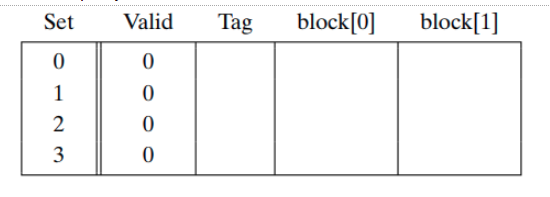
* Fully Associative cache is used for small set of caches such as TLB’s in virtual memory.
* tag bits = t = m - (s + b)
* Let us assume, (S, E, B, m) = (4, 1, 2, 4), In other words, the cache has four sets, one line per set, 2 bytes per block, and 4-bit addresses. Initially, the cache is empty (i.e., each valid bit is zero). Based on the following figure: Each row in the table represents a cache line. The first column indicates the set that the line belongs to. Now Read word at address 0. Specify whether this is a Cache Miss



* Based on the above discussion, Read word at address 1, This is a Cache Hit
* Based on the above discussion, Read word at address 13. This is a

Cache Miss

* Based on the above discussion, Read word at address 8. This is a

Cache Miss

* Based on the above discussion, Read word at address 0. This is a

Conflict miss

* When E = 2, B = 4, and S = 8 and m = 13 (Two way set associative cache, What are the values of Cache Set Index (CI), the Cache block offset (CO) and the cache tag (CT) when the memory address is given 0x0E34 = 0X5,0X0,0X71
* When E = 2, B = 4, and S = 8 and m = 13 (Two way set associative cache, What are the values of Cache Set Index (CI), the Cache block offset (CO) and the cache tag (CT) when the memory address is given 0x1FE4 = 0x3, 0x1, 0xFF

|  |  |  |
| --- | --- | --- |
| DMC (Direct Mapped Cache) | Fully Associated Cache(FAC) | SAC(Set Associated cache) |
| Multiple set 1 line each | 1 set multiple lines | Multiple line & set |
| Hits less | Hits More | Balanced and depended |
| Miss MORE | Miss less | Balanced and depended |