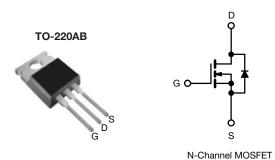
HALOGEN FREE



Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.077		
Q _g max. (nC)	72			
Q _{gs} (nC)	11			
Q _{gd} (nC)	32			
Configuration	Single			

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF540PbF
Lead (Pb)-free and halogen-free	IRF540PbF-BE3

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	100	V	
Gate-source voltage			V_{GS}	± 20	7 V	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C		28	А	
		T _C = 100 °C	I _D	20		
Pulsed drain current ^a			I _{DM}	110	1	
Linear derating factor				1.0	W/°C	
Single pulse avalanche energy b			E _{AS}	230	mJ	
Repetitive avalanche current a			I _{AR}	28	Α	
Repetitive avalanche energy ^a			E _{AR}	15	mJ	
Maximum power dissipation	T _C = 25 °C		P_D	150	W	
Peak diode recovery dV/dt ^c			dV/dt	5.5	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +175	• • • • • • • • • • • • • • • • • • • •	
Soldering recommendations (peak temperature) ^d	For	10 s		300	°C	
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 440 μ H, R_g = 25 Ω , I_{AS} = 28 A (see fig. 12)
- c. $I_{SD} \le 28$ A, $dI/dt \le 170$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 175$ °C
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62		
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	1.0		

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static					•	•	ļ
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$	100	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	-	0.13	-	V/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zara gata valtaga drain aurrant	1	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 150 \text{ °C}$		-	-	25	μΑ
Zero gate voltage drain current	I _{DSS}			-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 17 A ^b	-	-	0.077	Ω
Forward transconductance	9 _{fs}	V _{DS} = 50 V, I _D = 17 A b		8.7	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. } 5$		-	1700	-	pF
Output capacitance	C _{oss}			-	560	-	
Reverse transfer capacitance	C _{rss}			-	120	-	
Total gate charge	Qg			-	-	72	
Gate-source charge	Q _{gs}	$V_{GS} = 10 \text{ V}$ $I_D = 17 \text{ A, } V_{DS} = 80 \text{ V,}$ see fig. 6 and 13 b	-	-	11	nC	
Gate-drain charge	Q _{gd}		-	-	32		
Turn-on delay time	t _{d(on)}			-	11	-	
Rise time	t _r	V_{DD} = 50 V, I_{D} = 17 A R_{g} = 9.1 Ω , R_{D} = 2.9 Ω , see fig. 10 b		-	44	-	ns
Turn-off delay time	t _{d(off)}			-	53	-	
Fall time	t _f			-	43	-	
Gate input resistance	R_g	f = 1 MHz, open drain		0.5	-	3.6	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		_	-	28	A
Pulsed diode forward current ^a	I _{SM}			-	-	110	
Body diode voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 28 \text{A}, V_{GS} = 0 \text{V} ^{\text{b}}$		=	-	2.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 17 A, dl/dt = 100 A/µs b		-	180	360	ns
Body diode reverse recovery charge	Q _{rr}			-	1.3	2.8	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is			minated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

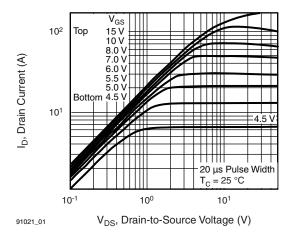


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

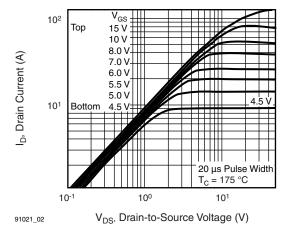


Fig. 2 - Typical Output Characteristics, $T_C = 175$ °C

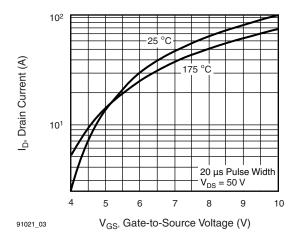


Fig. 3 - Typical Transfer Characteristics

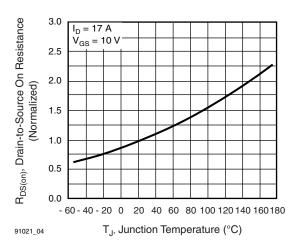


Fig. 4 - Normalized On-Resistance vs. Temperature

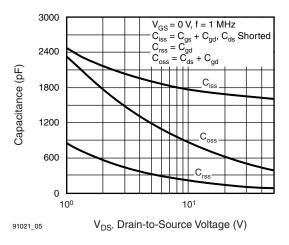


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

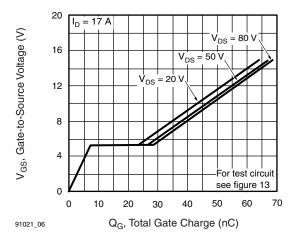


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



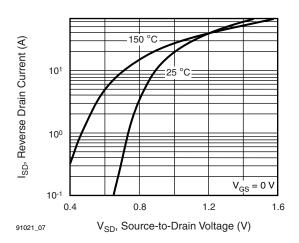


Fig. 7 - Typical Source-Drain Diode Forward Voltage

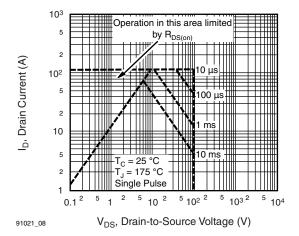


Fig. 8 - Maximum Safe Operating Area

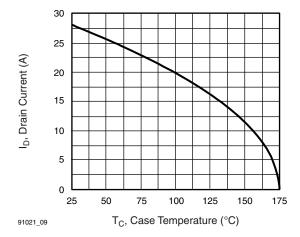


Fig. 9 - Maximum Drain Current vs. Case Temperature

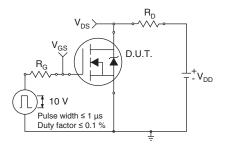


Fig. 10a - Switching Time Test Circuit

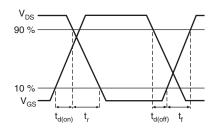


Fig. 10b - Switching Time Waveforms



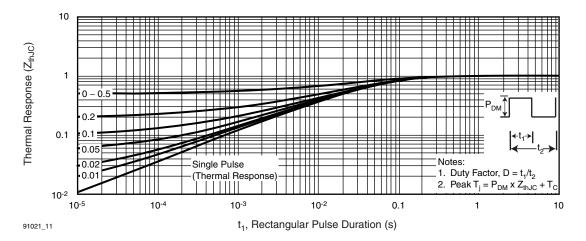


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

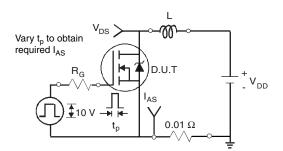


Fig. 12a - Unclamped Inductive Test Circuit

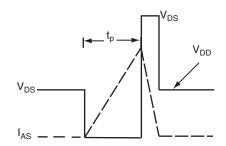


Fig. 12b - Unclamped Inductive Waveforms

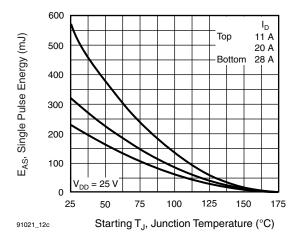


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



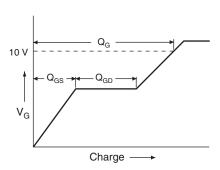


Fig. 13a - Basic Gate Charge Waveform

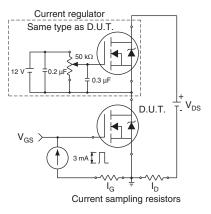
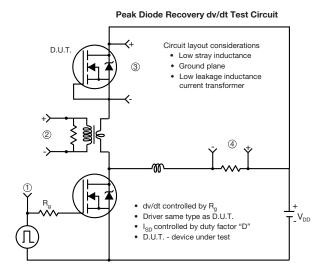


Fig. 13b - Gate Charge Test Circuit



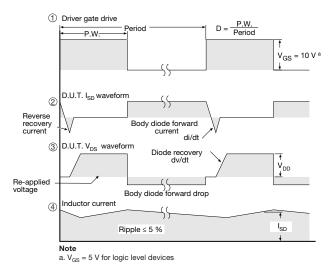


Fig. 14 - For N-Channel

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