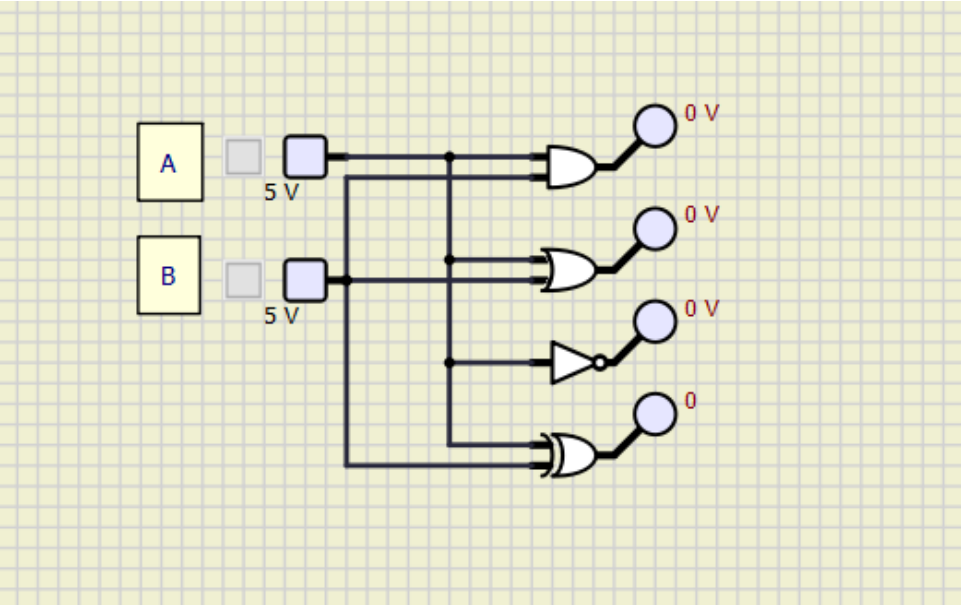
Kamil Kałwelis 16943/IT/2020/NS

ARCHITEKTURA KOMPUTERÓW

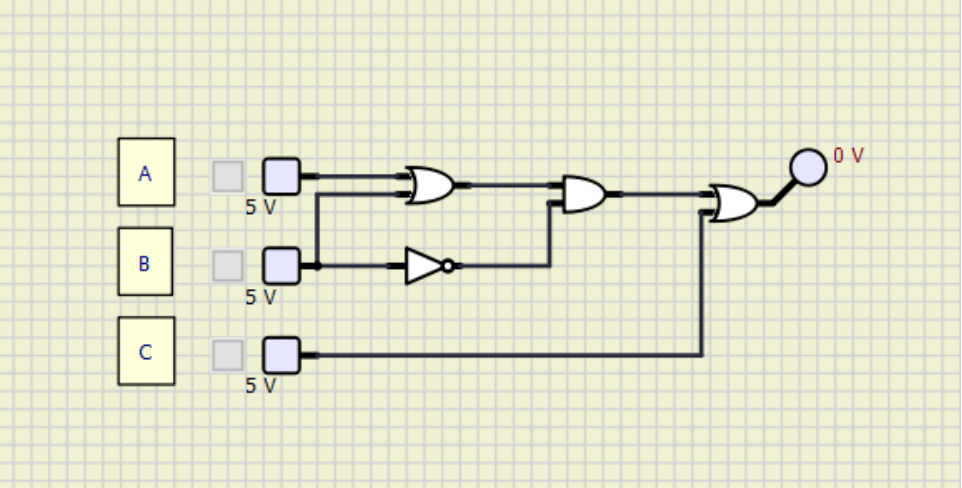
LAB2

Kamil Kałwelis 16943/IT/2020/NS

5.4.1.

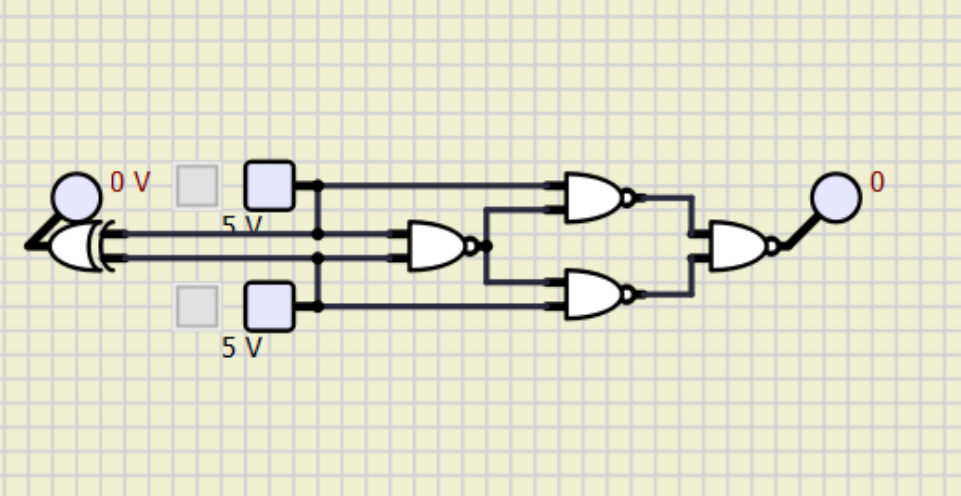


5.4.2.



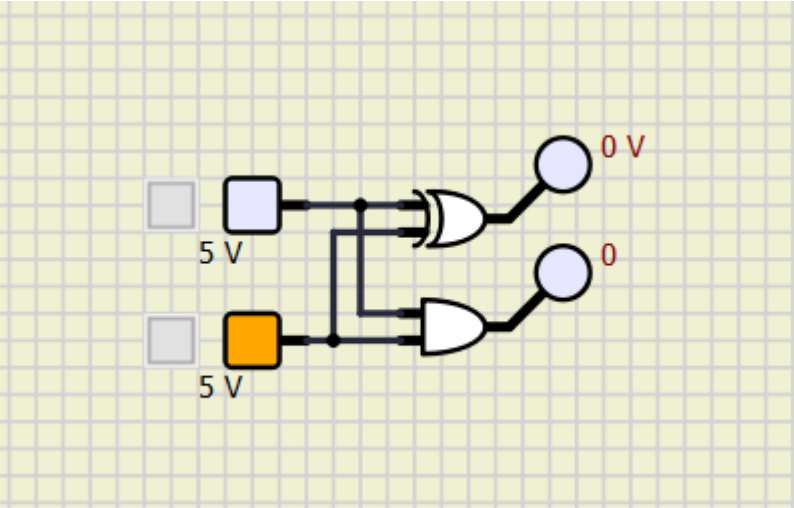
A	B	C	wynik
1	1	1	1
1	1	0	0
1	0	1	1
1	0	0	1
0	1	1	1
0	1	0	0
0	0	1	1
0	0	0	0

5.4.3.

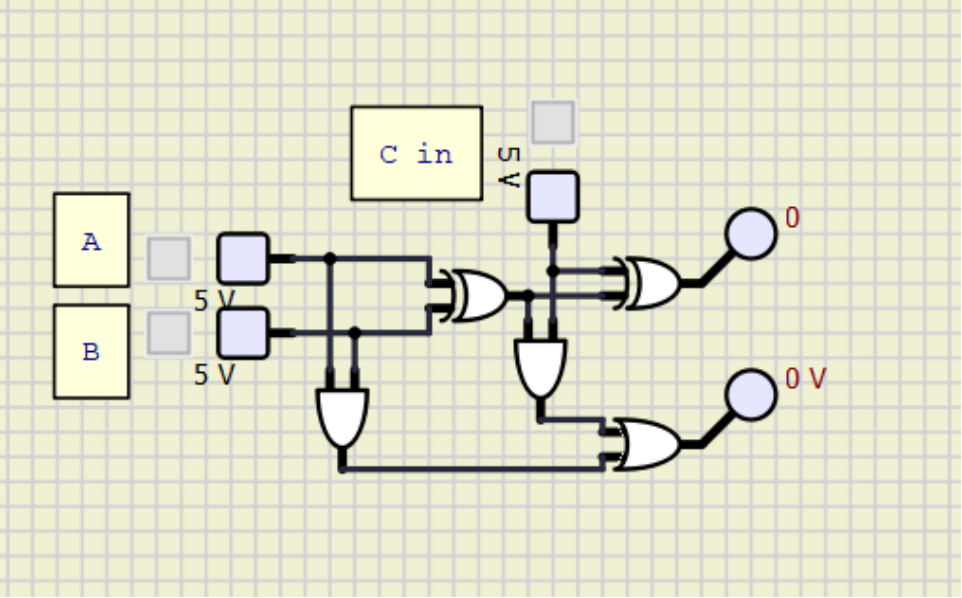


*bramka XOR po lewej stronie schematu, została dodana w celu zobrazowania identycznego sposobu działania, co układ zbudowany po prawej stronie

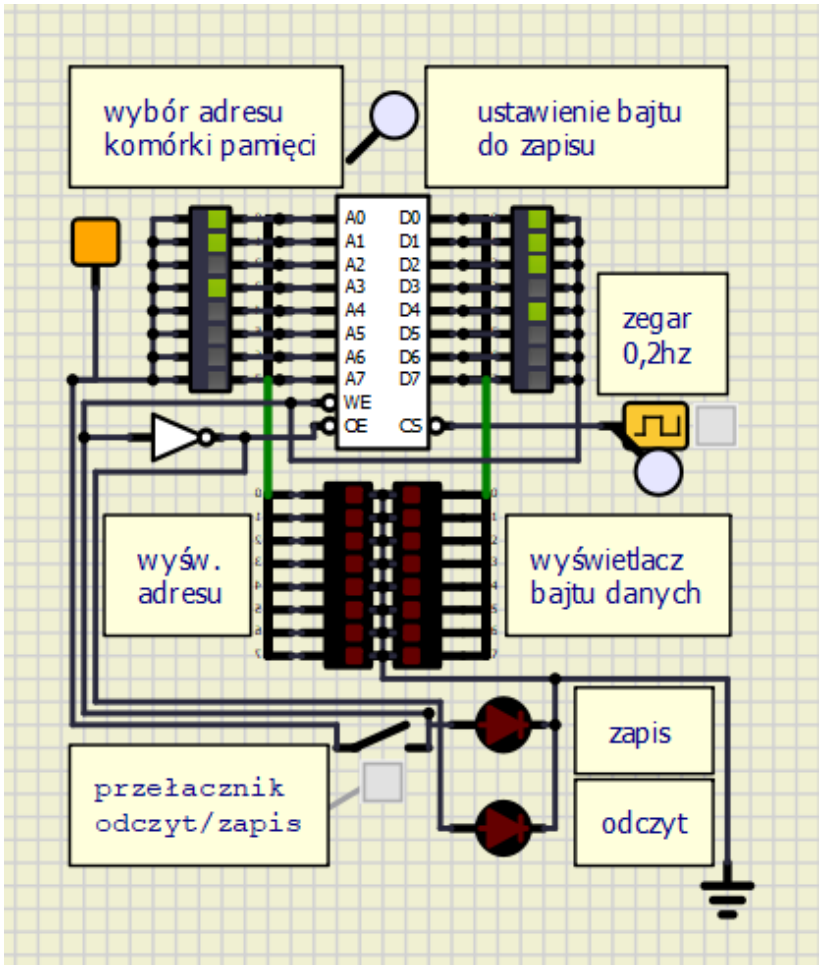
5.4.4.



5.4.5.

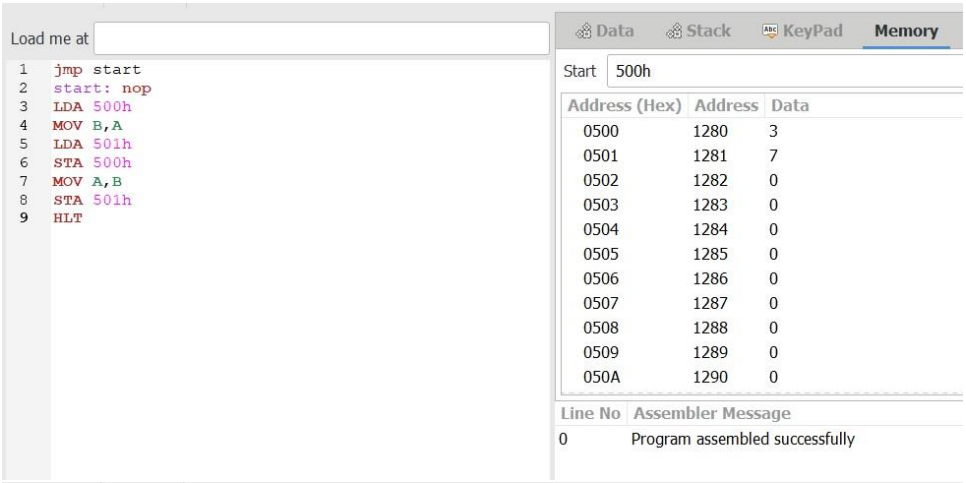


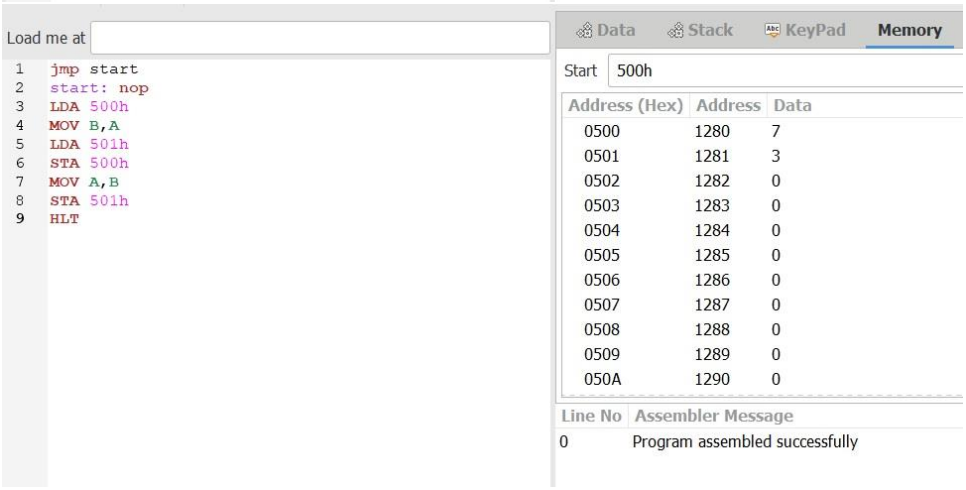
5.4.8.


wybór adresu komórki pamięci
ustawienie bajtu do zapisu
A0
A1
A2
A3
A4
A5
A6
A7
WE
OE
D0
D1
D2
D3
D4
D5
D6
D7
CS
zegar 0,2hz
wyśw. adresu
wyświetlacz bajtu danych
zapis
odczyt
przełacznik odczyt/zapis

ZADANIA Z ASEMBLERA

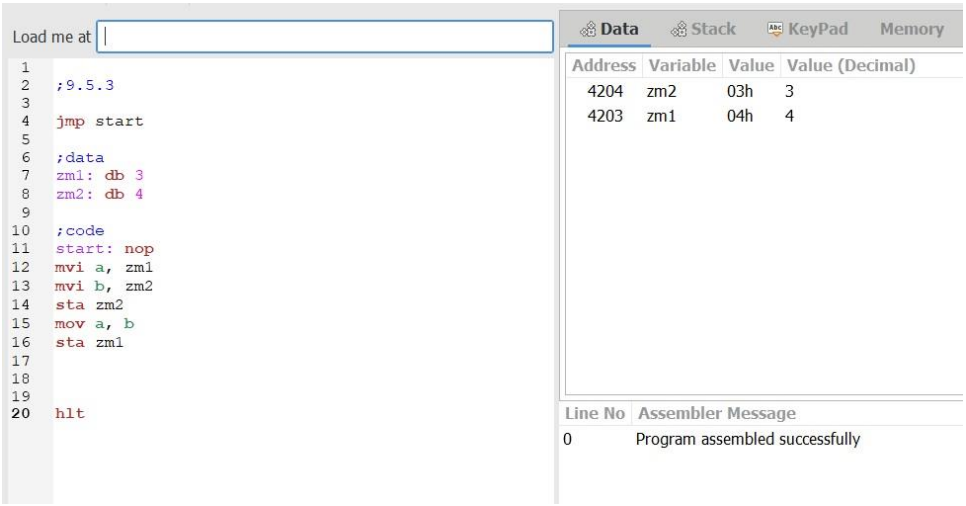
9.5.2





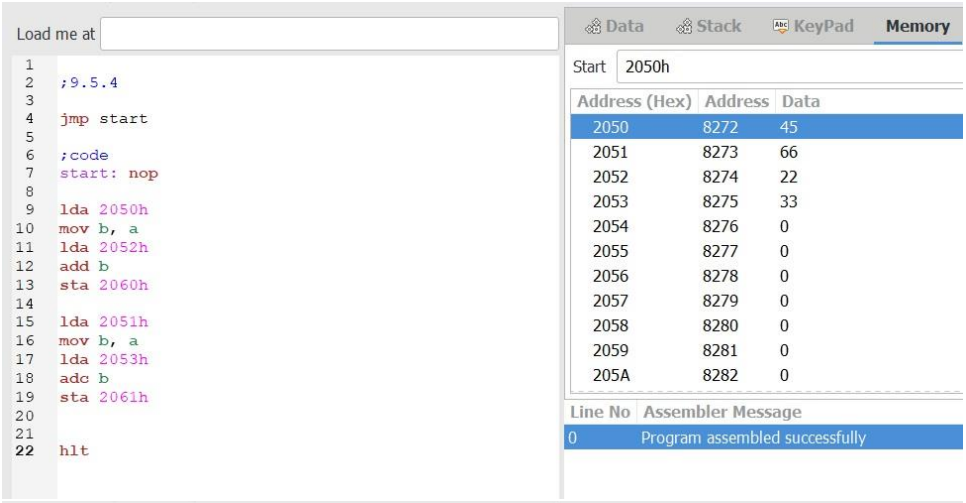

```
jmp start

start: nop

LDA 500h

MOV B,A

LDA 501h

STA 500h

MOV A,B

STA 501h

HLT
```

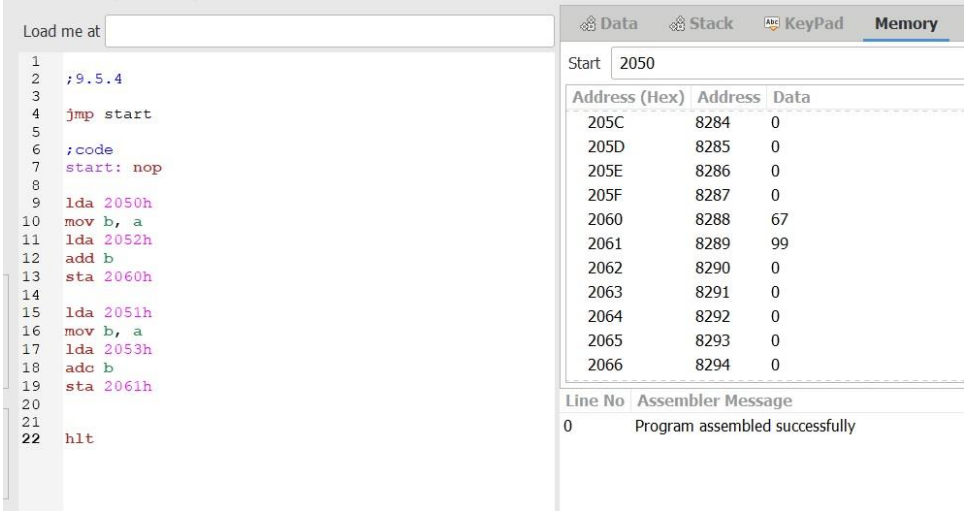
9.5.3




```
;9.5.3
jmp start

;data
zm1: db 3
zm2: db 4

;code
start: nop
mvi a, zm1
mvi b, zm2
sta zm2
mov a, b
sta zm1

hlt
```

9.5.4

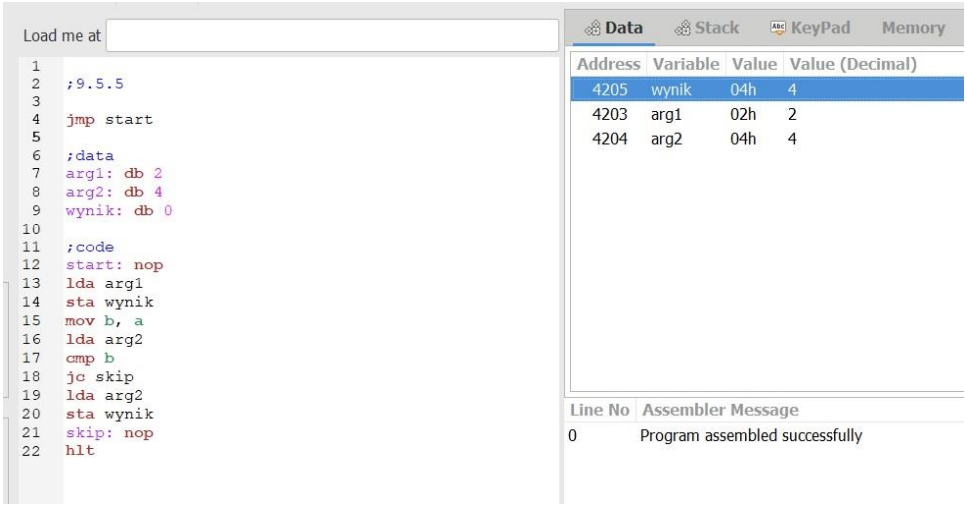





```
;9.5.4
jmp start
start: nop
lda 2050h
mov b, a
lda 2052h
add b
sta 2060h
lda 2051h
mov b, a
lda 2053h
```

```
adc b
sta 2061h
hlt
```

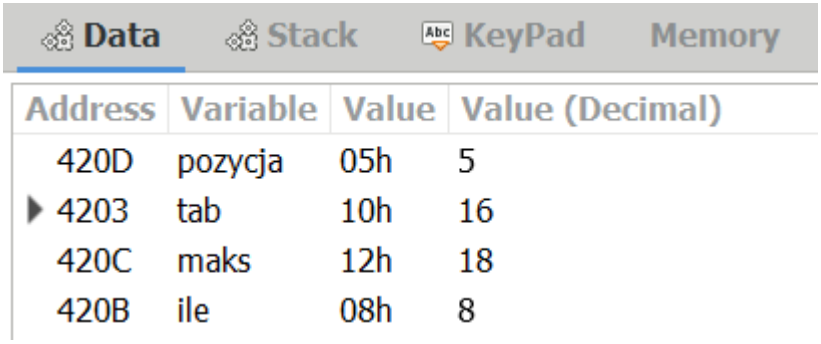
9.5.5




```
;9.5.5
jmp start
;data
arg1: db 2
arg2: db 4
wynik: db 0

;code
start: nop
lda arg1
sta wynik
mov b, a
lda arg2
cmp b
jc skip
lda arg2
sta wynik
```

```
skip: nop
Hlt
```

9.5.4



Address	Variable	Value	Value (Decimal)
420D	pozycja	05h	5
4203	tab	10h	16
420C	maks	12h	18
420B	ile	08h	8

```
;9.5.6

jmp start

;data
tab: db 16,10,2,3,18,5,6,0
ile: db 8
maks: db 0
pozycja: db 0
licznik: db 1

;code
start: nop
lxi h, tab
lda tab
sta maks
mov b, a
lda licznik
```

```
sta pozycja
back: inx h
lda licznik
inr a
sta licznik
mov a, m
cmp b
jc back
jz skip
jnc store
store: sta maks
mov b, a
lda licznik
sta pozycja
jnz back
skip: nop
hlt
```