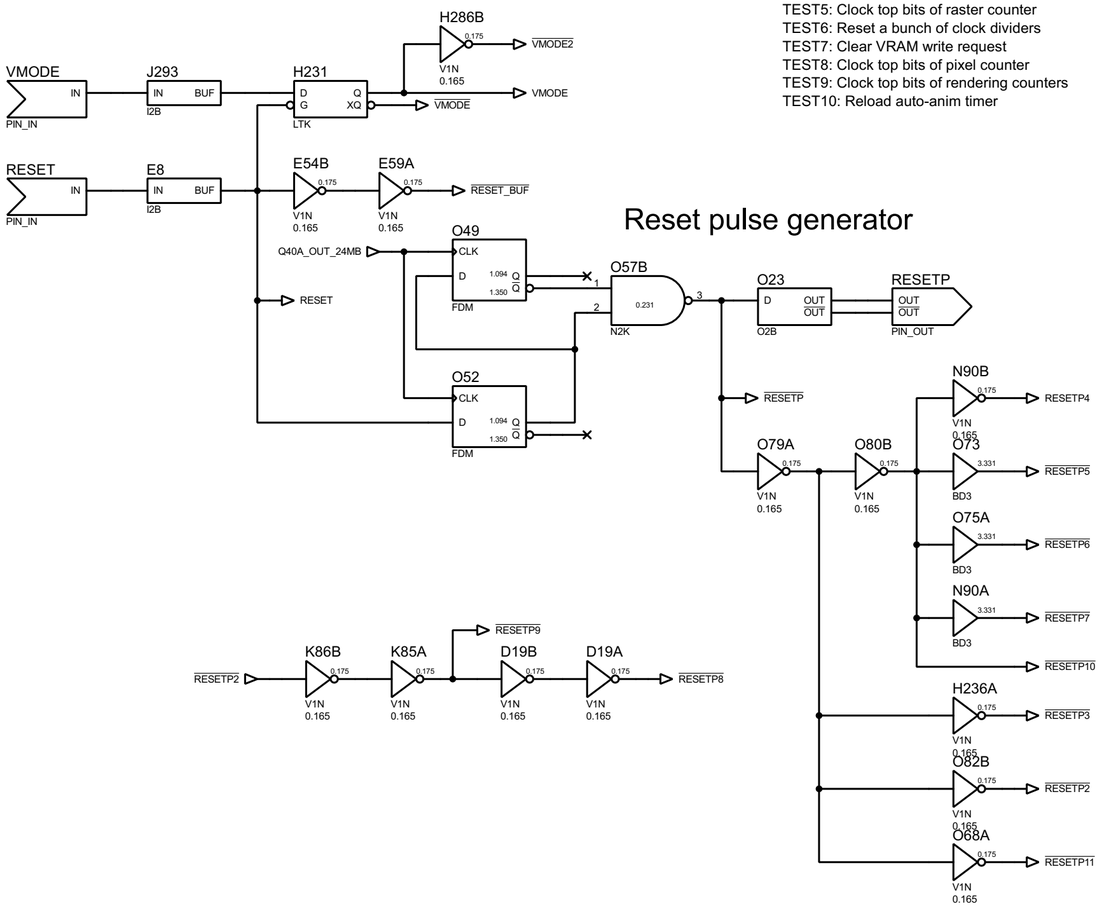
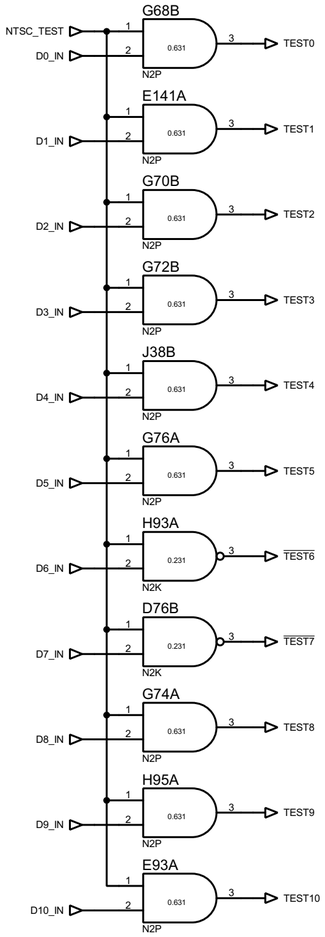
TEST0: Clock raster counter
TEST1: Clock auto-anim timer
TEST2: Clock top byte of REG_TIMERLOW
TEST3: Clock bottom byte of REG_TIMERHIGH
TEST4: Clock top byte of REG_TIMERHIGH
TEST5: Clock top bits of raster counter
TEST6: Reset a bunch of clock dividers
TEST7: Clear VRAM write request
TEST8: Clock top bits of pixel counter
TEST9: Clock top bits of rendering counters
TEST10: Reload auto-anim timer

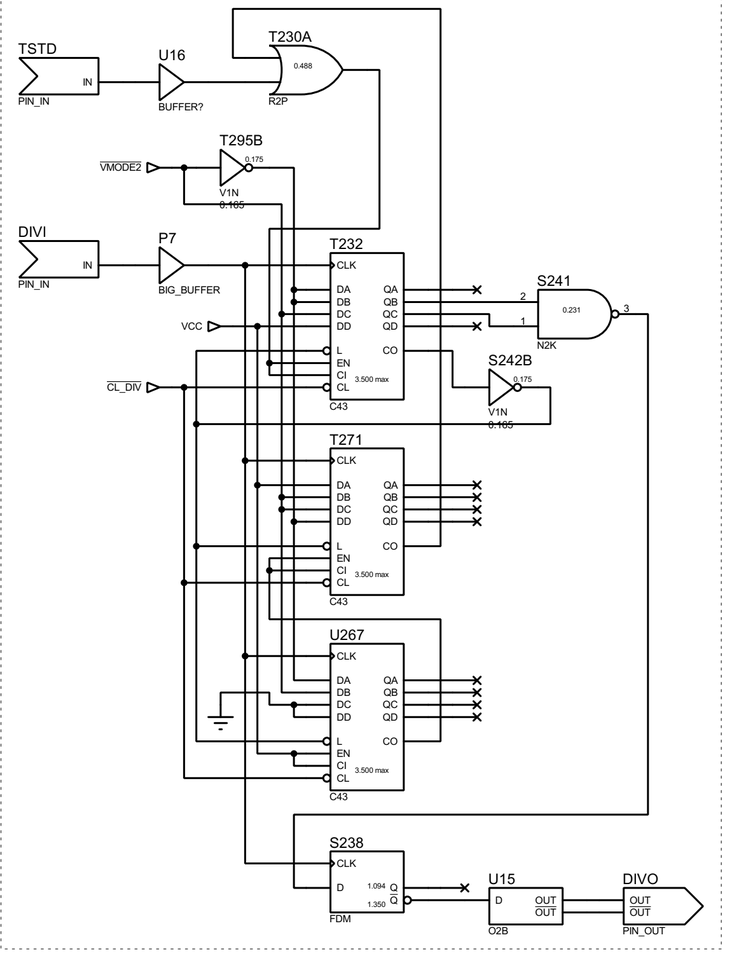
Test enables. Only active in NTSC and TEST mode (when TST=1 and VMODE=0)

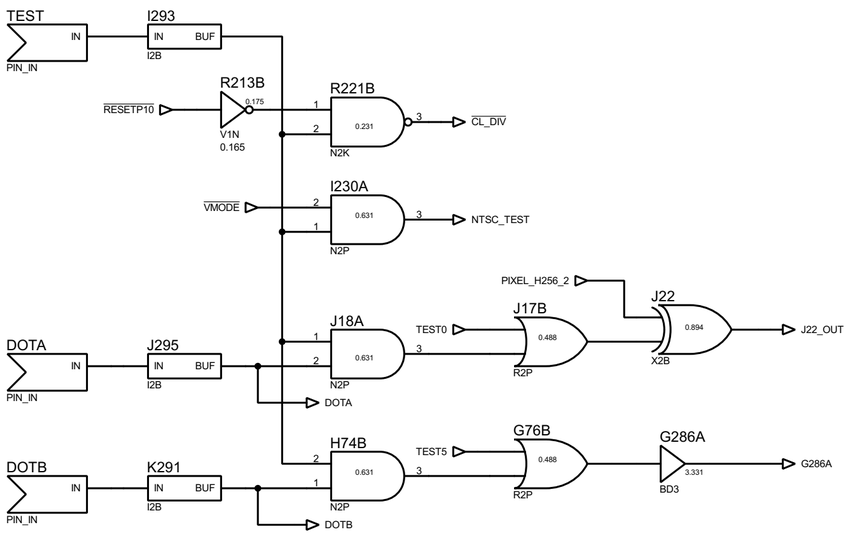
This part is completely independent from the rest.
It's the integrated version of the hack SNK used on NEO-AES boards: just a frequency divider used with an external PLL chip to enhance the composite video output.

Reset pulse generator



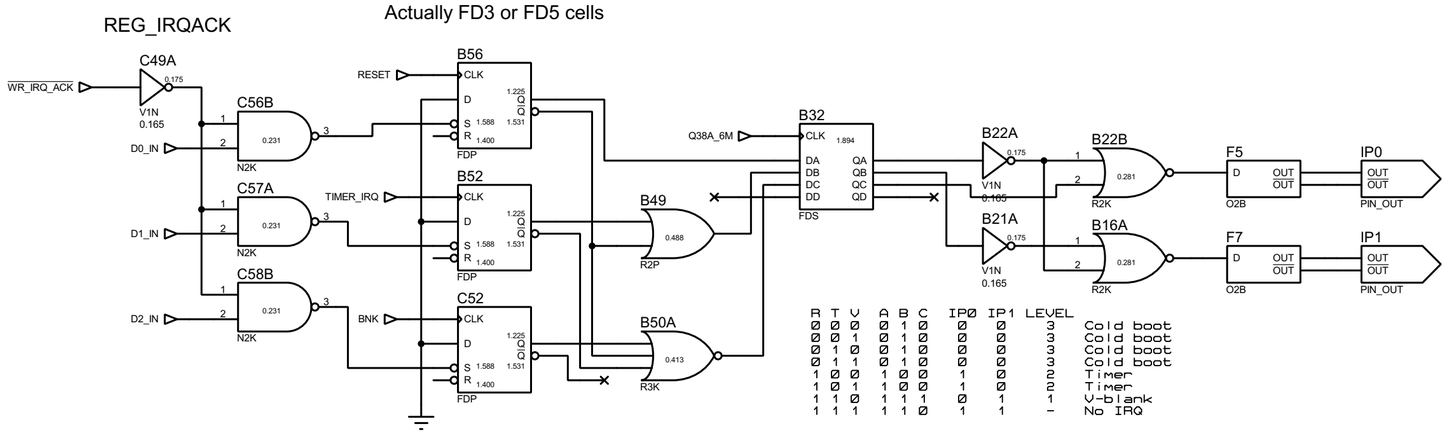






REG_IRQACK

Actually FD3 or FD5 cells



R	T	V	A	B	C	IPØ	IP1	LEVEL	
Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	3	Cold boot
Ø	Ø	1	Ø	1	Ø	Ø	Ø	3	Cold boot
Ø	1	Ø	Ø	1	Ø	Ø	Ø	3	Cold boot
Ø	1	1	Ø	1	Ø	Ø	Ø	3	Cold boot
1	Ø	Ø	1	Ø	Ø	1	Ø	2	Timer
1	Ø	1	1	Ø	Ø	1	Ø	2	Timer
1	1	Ø	1	1	1	Ø	1	1	V-blank
1	1	1	1	1	Ø	1	1	-	No IRQ

TITLE: LSPC2-A2 cells RESET & IRQs		DATE: 13/08/2021
BY: Sean Gonsalves	REV: B	PAGE: 1/17

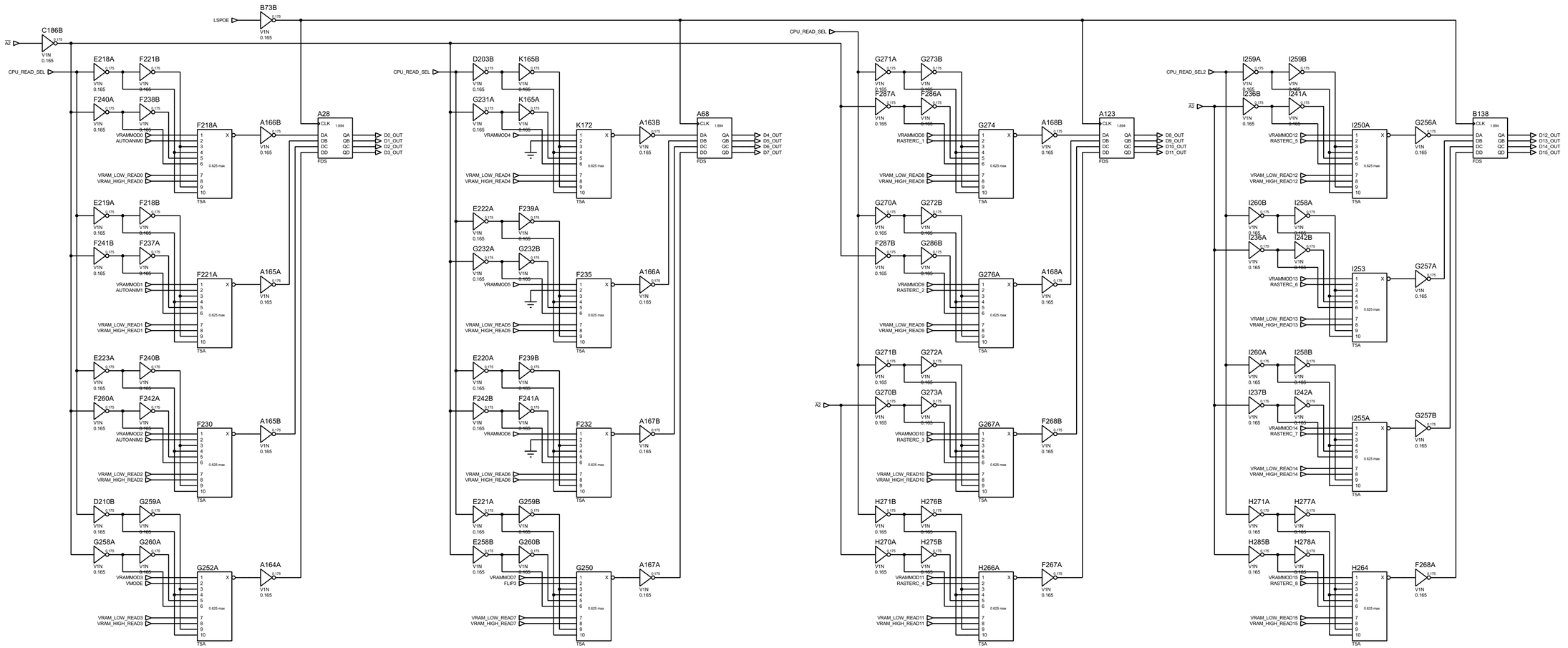
```
P bus can be:
HMS
--88:LO address      --------XXXXXXXXXXXXXXX
---:IO data          XXXXXXXX---------------
++--:Shrink index    --------XXXXXXXX-------
8---:Ser'lz palette  XXXXXXXX---------------
--88:X position      --------XXXXXXXXXXXXXXX
222:C address        XXXXXXXXXXXXXXXXXXXXXXX
777:S address        --------XXXXXXXXXXXXXXX
```

Shrunk tilemap index

Shrunk tile line number

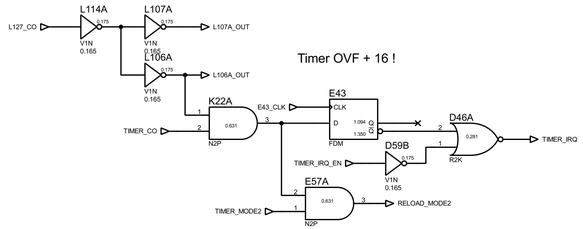
X = (XPOS >> 1) + LSB

CPU read data can be:
1: Read REG_VRAMMOD
2: Read REG_LSPCMODE (RASTER,000,VMODE,AA2~0)
7: Read REG_VRAMRW low buffer
8: Read REG_VRAMRW high buffer

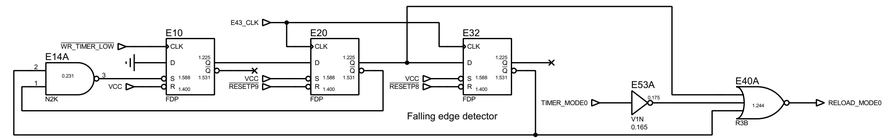


TITLE: LSPC2-A2 cells DATA OUT		DATE: 13/08/2021
BY: Sean Gonsalves	REV: B	PAGE: 3/17

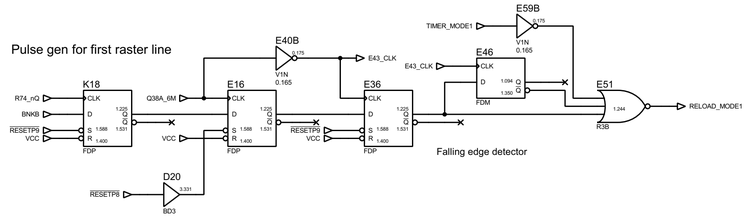
Timer OVF + 16 !



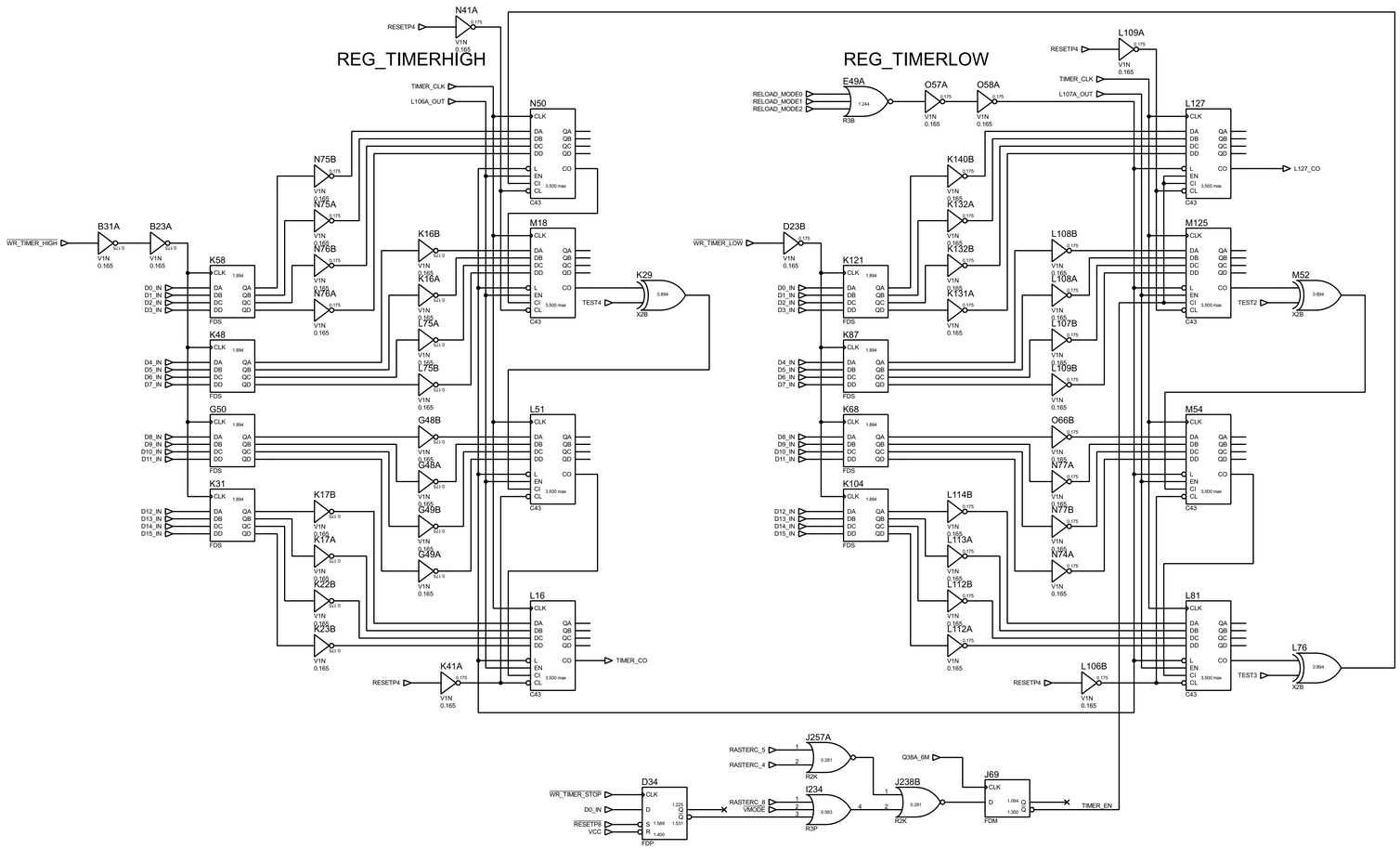
Pulse gen for write to REG_TIMERLOW



Pulse gen for first raster line

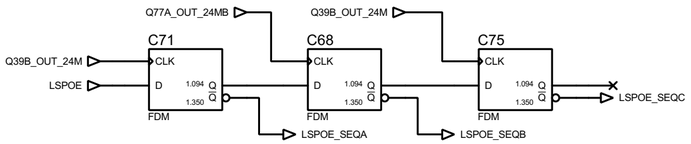


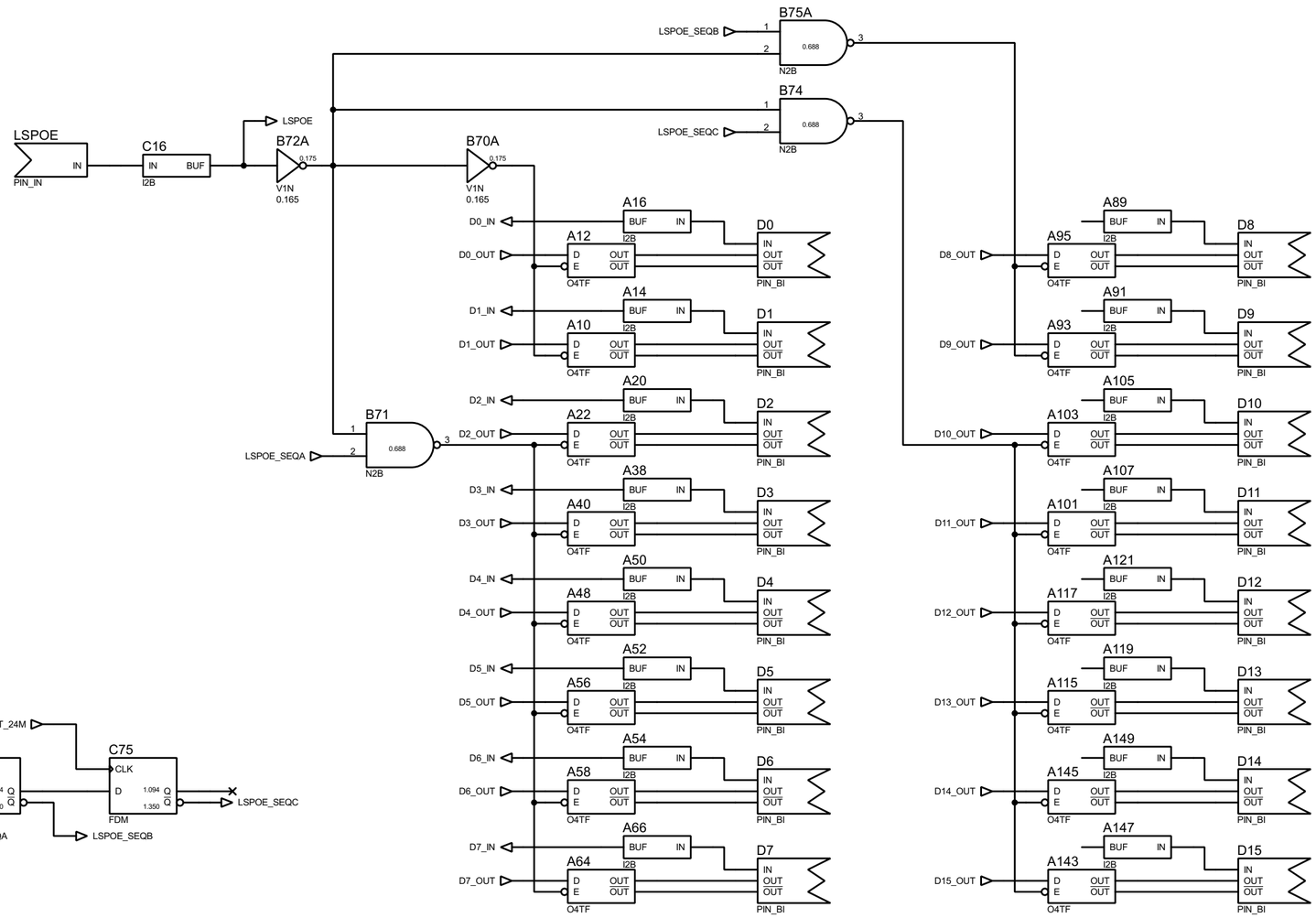
REG_TIMERHIGH

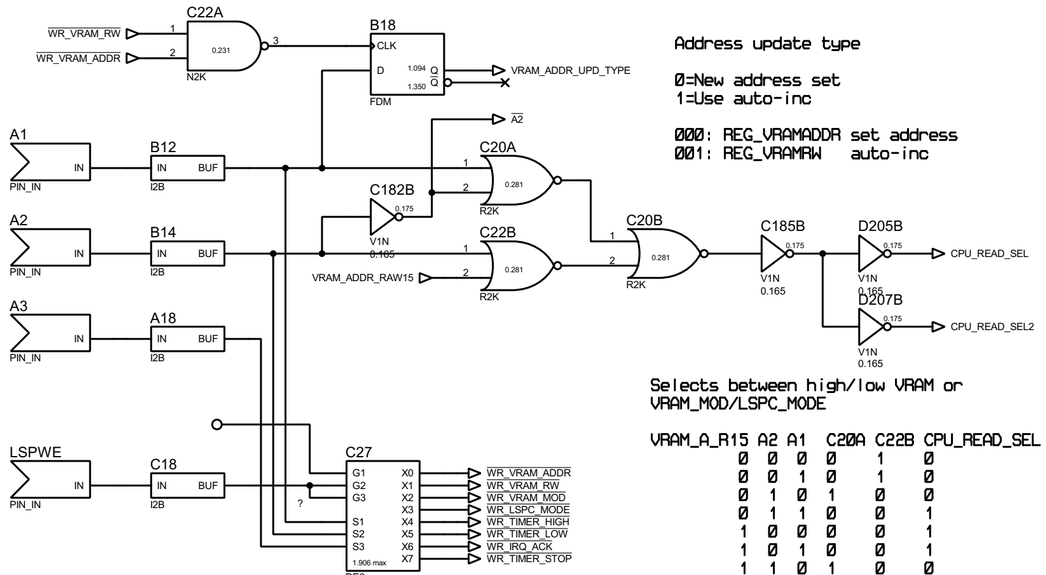


REG_TIMERLOW

TITLE: LSPC2-A2 cells TIMER REGISTERS	DATE: 13/08/2021
BY: Sean Gonsalves REV: B	PAGE: 4/17







Address update type

0=New address set
1=Use auto-inc

000: REG_VRAMADDR set address
001: REG_VRAMRW auto-inc

Selects between high/low VRAM or
VRAM_MOD/LSPC_MODE

VRAM_A_R15	A2	A1	C20A	C22B	CPU_READ_SEL	Read type
0	0	0	0	1	0	VRAM data low
0	0	1	0	1	0	VRAM data low
0	1	0	1	0	0	VRAM modulo
0	1	1	0	0	1	LSPC mode
1	0	0	0	0	1	VRAM data high
1	0	1	0	0	1	VRAM data high
1	1	0	1	0	0	VRAM modulo
1	1	1	0	0	1	LSPC mode

TITLE:	DATE:
LSPC2-A2 cells CPU I/O	13/08/2021
BY: Sean Gonsalves REV: B	PAGE: 5/17

VRAM low address can be:
1: CPU access
2: Fixmap read
7: Unused (20020)
8: Spritemap read

Q39B_OUT_24M
P210A_OUT
K166 CLK D Q FDM 1.094 1.350
P222A_OUT
SPRITEMAP_ADDR_MSB
O185 CLK D Q FDM 1.094 1.350
Q174B_OUT
Q174A_OUT
N169A R2K 0.281
N160 CLK D Q FDM 1.094 1.350
N165 CLK D Q FDM 1.094 1.350
N158A V1N 0.165 0.175
N159A V1N 0.165 0.175

K169A VRAM_ADDR0 RASTERC_3_BUF 0.625 max T5A
A171A V1N 0.165 0.175
A162 O2B
B0 PIN_OUT
K163B K164A K163A K164B V1N 0.165 0.175

N177 VRAM_ADDR4 RASTERC_7_BUF 0.625 max T5A
A186B V1N 0.165 0.175
A181 O2B
B4 PIN_OUT
N170B N185A N164B N172B V1N 0.165 0.175
SPR_TILEMAP3

H75A ACTIVE_RD2 VRAM_ADDR8 PIXEL_H64+16 0.625 max T5A
A185B V1N 0.165 0.175
A208 O2B
B8 PIN_OUT
H74A H72A H73A H73B V1N 0.165 0.175

F30A VRAM_ADDR12 VCC 0.625 max T5A
A187B V1N 0.165 0.175
A248 O2B
B12-PIN PIN_OUT
F38A F33A F36A F29A V1N 0.165 0.175
ACTIVE_RD6

N172A VRAM_ADDR1 RASTERC_4_BUF 0.625 max T5A
A170A V1N 0.165 0.175
A161 O2B
B1 PIN_OUT
N158B N164A N159B N168B V1N 0.165 0.175
SPR_TILEMAP0

E146A VRAM_ADDR5 PIXEL_H8_2 0.625 max T5A
A184B V1N 0.165 0.175
A198 O2B
B5 PIN_OUT
E96B E145B E146B E144A E145A V1N 0.165 0.175

H39A ACTIVE_RD3 VRAM_ADDR9 PIXEL_H128+16 0.625 max T5A
A185A V1N 0.165 0.175
A223 O2B
B9 PIN_OUT
H19A H20B H18A H19B V1N 0.165 0.175

F34 VRAM_ADDR13 VCC 0.625 max T5A
A187A V1N 0.165 0.175
A260 O2B
B13 PIN_OUT
F39B F29B F37B F30B V1N 0.165 0.175
ACTIVE_RD7

N182 VRAM_ADDR2 RASTERC_5_BUF 0.625 max T5A
A183B V1N 0.165 0.175
A172 O2B
B2 PIN_OUT
N168A N185B N163A N171B V1N 0.165 0.175
SPR_TILEMAP1

I75A VRAM_ADDR6 PIXEL_H16+16 0.625 max T5A
A184A V1N 0.165 0.175
A200 O2B
B6 PIN_OUT
I50B I49A I31A I48B V1N 0.165 0.175
ACTIVE_RD0

J31A VRAM_ADDR10 FIXMAP_ADDR_MSB 0.625 max T5A
A183A V1N 0.165 0.175
A229 O2B
B10 PIN_OUT
J35A J34B J20B J21B V1N 0.165 0.175
ACTIVE_RD4

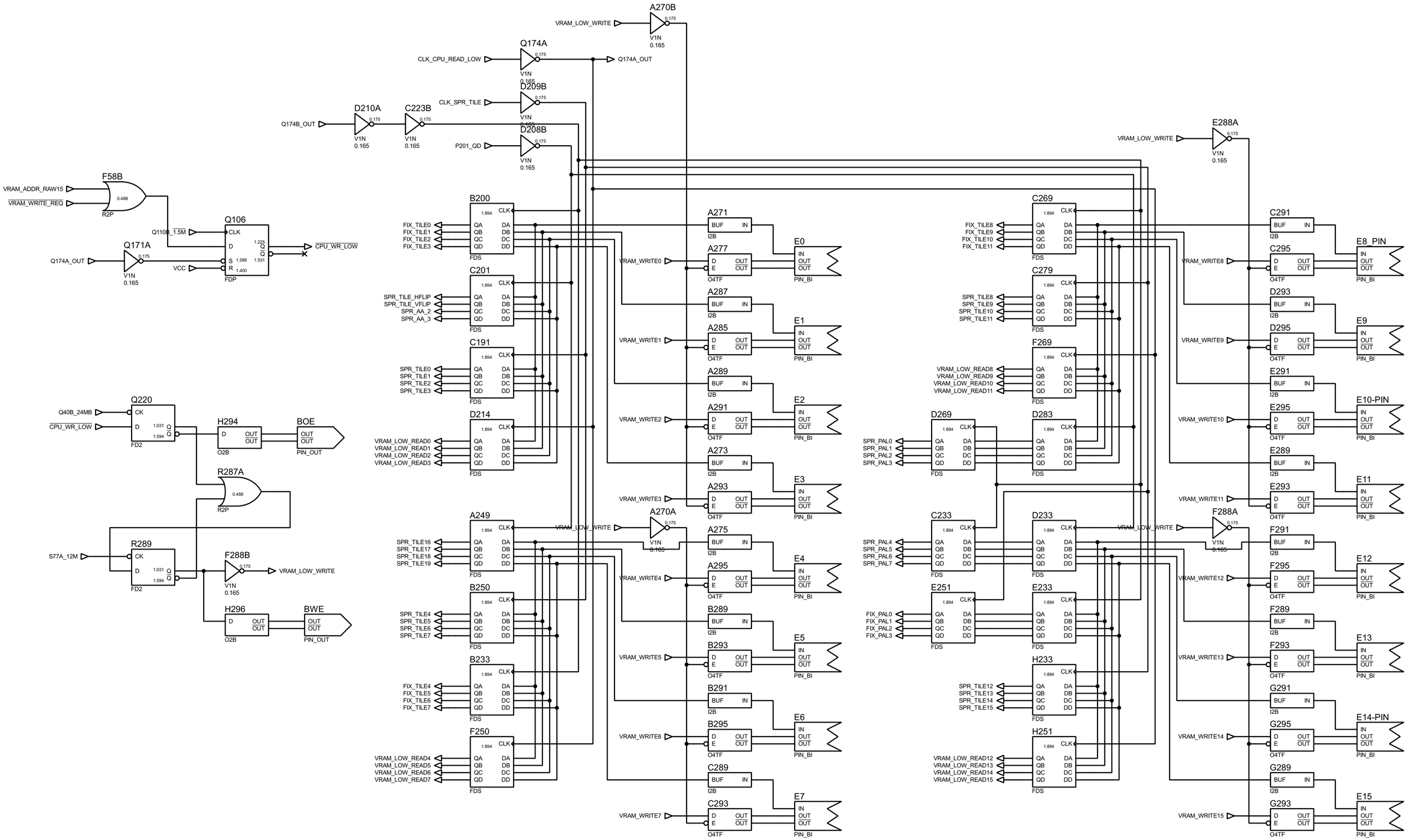
E54A VRAM_ADDR14 VCC 0.625 max T5A
A171B V1N 0.165 0.175
A268 O2B
B14-PIN PIN_OUT
E58B E53B E57B E52A V1N 0.165 0.175
ACTIVE_RD8

N179A VRAM_ADDR3 RASTERC_6_BUF 0.625 max T5A
A182A V1N 0.165 0.175
A174 O2B
B3 PIN_OUT
N169B N184A N163B N171A V1N 0.165 0.175
SPR_TILEMAP2

F206A VRAM_ADDR7 PIXEL_H32+16 0.625 max T5A
A202B V1N 0.165 0.175
A210 O2B
B7 PIN_OUT
F206B F210A G230A F238A V1N 0.165 0.175
ACTIVE_RD1

F39A FIXMAP VRAM_ADDR11 0.625 max T5A
A186A V1N 0.165 0.175
A231 O2B
B11 PIN_OUT
F38B F33B F37A F28A V1N 0.165 0.175
ACTIVE_RD5

TITLE: LSPC2-A2 cells VRAM LOW ADDRESS	DATE: 13/08/2021
BY: Sean Gonsalves REV: B	PAGE: 6/17



TITLE: LSPC2-A2 cells VRAM LOW DATA	DATE: 13/08/2021
BY: Sean Gonsalves REV: B	PAGE: 7/17

K131B_OUT
N98_QD
O98_Q
VRAM_HIGH_ADDR_S8
CLK_ACTIVE_RD
CLK_ACTIVE_RD_DELAY
H124B
H124A
H125A
M95B
L105A
K86A
L110A
L110B
L113B
K114A
O82A
R2K
V1N
0.165
0.175
0.281

C0_OUT
C1_OUT
C2_OUT
C3_OUT
C4_OUT
C5_OUT
C6_OUT
C7_OUT
C8_OUT
C9_OUT
C10_OUT
U296
U294
U293
U291
U266
U264
U260
U257
T258
U242
T229
C0
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
D
OUT
O2B
PIN_OUT

J217A
J198A
J221A
J199B
H222B
J199A
I213
I232A
I218A
ACTIVE_RD_PRE0
ACTIVE_RD_ADDR0
ACTIVE_WR_ADDR0
VRAM_ADDR0
PARSE_INDEX0
T44
1.350
0.231
N2K

F205A
G163B
G220B
G163A
F205B
G162A
G169A
G266B
G164
ACTIVE_RD_PRE1
ACTIVE_RD_ADDR1
ACTIVE_WR_ADDR1
VRAM_ADDR1
PARSE_INDEX1

G221B
G218B
G222B
G217B
F209B
G222A
G182A
G255B
G194A
ACTIVE_RD_PRE2
ACTIVE_RD_ADDR2
ACTIVE_WR_ADDR2
VRAM_ADDR2
PARSE_INDEX2

F210B
G221A
G223B
G219B
F209A
G223A
G200
G230B
G205A
ACTIVE_RD_PRE3
ACTIVE_RD_ADDR3
ACTIVE_WR_ADDR3
VRAM_ADDR3
PARSE_INDEX3

J176B
I181A
J175A
I182B
J177B
I181B
I175A
I232B
I182A
ACTIVE_RD_PRE4
ACTIVE_RD_ADDR4
ACTIVE_WR_ADDR4
VRAM_ADDR4
PARSE_INDEX4
A B /C
/A B C
A B C
A /B /C
/A B /C
/A /B C
/A B C
/A /B /C

Fast VRAM address can be:

ABC
000 SCB3 read for parsing 010
001 CPU access xxx
010 Active list write 110
011 CPU access xxx
100 Rendering read xxx
101 Active list read 110
110 Rendering read xxx
111 Active list read 110

10 9 8 7 6 5 4 3 2 1 0
B B N n n n n n n n n n

n = sprite # (0~511)
N = sprite # or active list select
B = bank ($000 $200 $400 $600)

NAND mux notes:
8-to-1 (3 select bits * 2 = 6 lines)
Made of 2x 16-input NANDs

Select lines:
1,2,3,5,6,7,9,10,11,13,14,15

Data inputs:
4,8,12,16

$600/$680 select

I50A
J61A
J72B
J68B
I75B
J61B
J62
J67A
J72A
ACTIVE_RD_PRE5
ACTIVE_RD_ADDR5
ACTIVE_WR_ADDR5
VRAM_ADDR5
PARSE_INDEX5
C5_OUT

I94A
I95A
I93B
I94B
I93A
I96A
I109A
I95B
I104
ACTIVE_RD_PRE6
ACTIVE_RD_ADDR6
ACTIVE_WR_ADDR6
VRAM_ADDR6
PARSE_INDEX6
C6_OUT

J222A
J220A
J223A
J219A
J218A
J223B
J200
J234B
J205A
ACTIVE_RD_PRE7
FLIP
FLIP3
VRAM_ADDR7
PARSE_INDEX7
C7_OUT

I48A
J47B
J48B
J46B
I49B
J46A
J49
J47A
J54A
ACTIVE_RD_PRE8
VRAM_ADDR8
PARSE_INDEX8
J36_OUT
VCC
C8_OUT

H20A
H21A
I31B
H23B
H21B
H22B
H28A
H22A
H34
VRAM_ADDR9
C9_OUT
N98_QC

I29A
I12B
I30A
I10A
I30B
I11B
I13
I11A
I18A
VRAM_ADDR10
C10_OUT

"Backwards" delay for shift stages
to work correctly

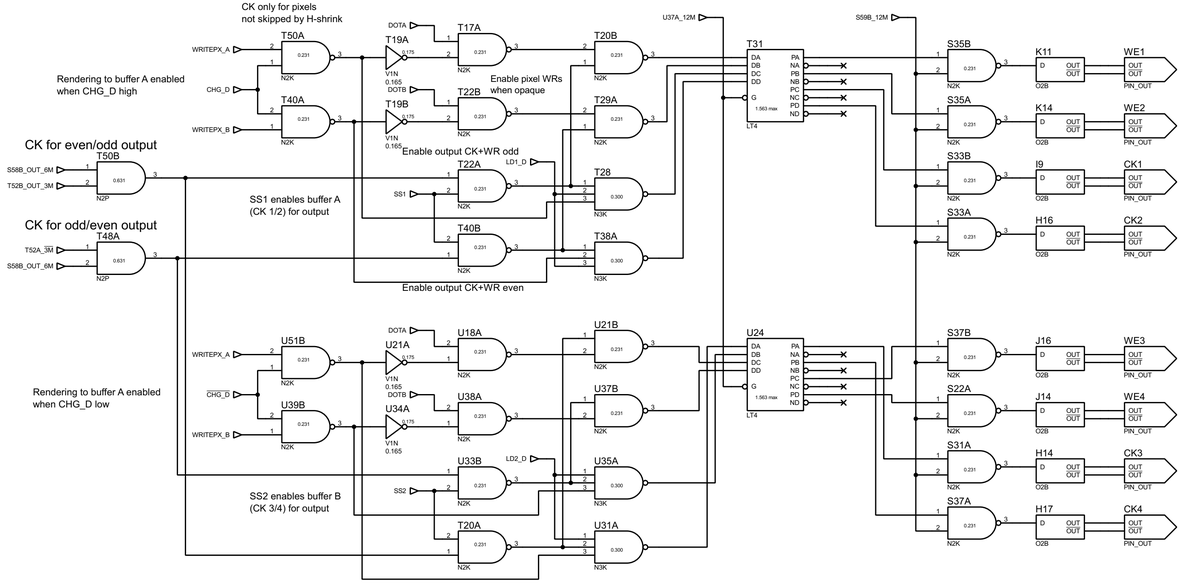
Selects data to write between
CPU or active list

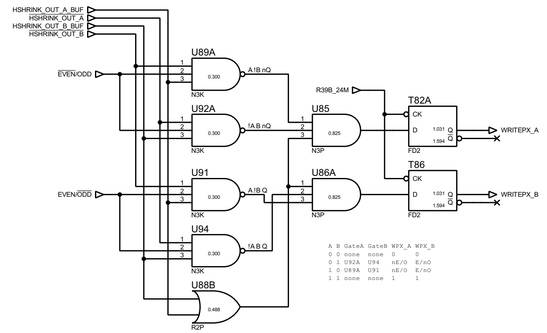
Write 00's to active list when
parsing is done (clear up to end)

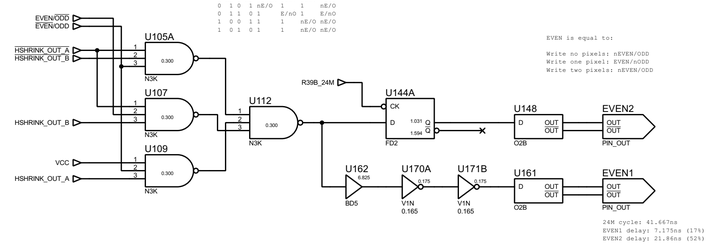
Chain

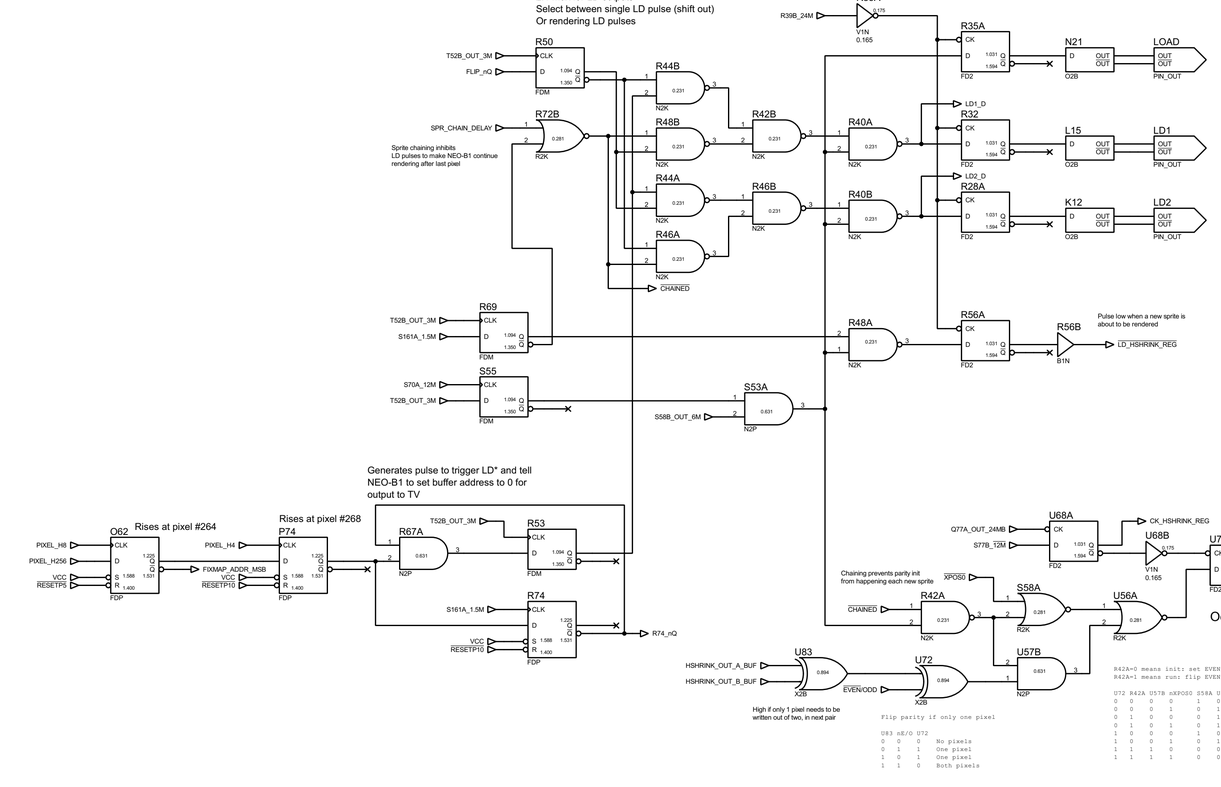
Active list sprite # -> Sprite tilemap address

TITLE: LSPC2-A2 cells VRAM HIGH DATA	DATE: 13/08/2021
BY: Sean Gonsalves REV: B	PAGE: 9/17









TITLE: LSPC2-A2 cells NEO-B1 CONTROL	DATE: 13/08/2021
BY: Sean Gonsalves REV: B	PAGE: 10/17

"Writing" pulses

CPU_WR_HIGH
CPU_WR_LOW
O108B
N2K
E164B
E164A
V1N 0.165

REG_VRAMRW

For writes only

Set when CPU writes to VRAM
Reset when write is done or when CPU sets a new VRAM address

WR_VRAM_RW
C50A
D38
VCC
D32A
TEST7
N2P
VRAM_WRITE_REQ
D28
FDP

E154 E196 D121 D141 D131 D178 F155 F165
D0_IN D1_IN D2_IN D3_IN D4_IN D5_IN D6_IN D7_IN D8_IN D9_IN D10_IN D11_IN D12_IN D13_IN D14_IN D15_IN
VRAM_WRITE0 VRAM_WRITE1 VRAM_WRITE2 VRAM_WRITE3 VRAM_WRITE4 VRAM_WRITE5 VRAM_WRITE6 VRAM_WRITE7 VRAM_WRITE8 VRAM_WRITE9 VRAM_WRITE10 VRAM_WRITE11 VRAM_WRITE12 VRAM_WRITE13 VRAM_WRITE14 VRAM_WRITE15
FDS

To write Writing

Internal, last written value by CPU

REG_VRAMADDR

WR_VRAM_ADDR
C51B
C123 A79 D87 F47
Clocked by falling edge of nWR_VRAM_ADDR
VRAM_ADDR_RAW15
F91

VRAM_ADDR_UPD_TYPE
C74A C149A B73A A113A D23A D114B D22A F11B

Block B
D112B
C51A
C56A
0.631 total

Block A
0.594 total
C144A C142A C140B C138B A112B A111A A109A A110B D110B D106B D108B D85A F10A F12A F26A F12B
C160A C159A C159B C160B B125A B125B A114A A114B D59A D58A D58B D77A F10B F27B F28B F9A
D24

Muxes used to select new VRAM address:
0: Set by CPU
1: Current address + VRAM_MOD

Latch new VRAM address
Clocked by rising edge of nWR_VRAM_ADDR or nCPU_WR_HIGH or nCPU_WR_LOW

C164 C105 D48 F14
VRAM_ADDR3 VRAM_ADDR2 VRAM_ADDR1 VRAM_ADDR0 VRAM_ADDR7 VRAM_ADDR6 VRAM_ADDR5 VRAM_ADDR4 VRAM_ADDR11 VRAM_ADDR10 VRAM_ADDR9 VRAM_ADDR8 VRAM_ADDR14 VRAM_ADDR13 VRAM_ADDR12

REG_VRAMMOD

WR_VRAM_MOD
F57A
G123 F81 G105 H105
D0_IN D1_IN D2_IN D3_IN D4_IN D5_IN D6_IN D7_IN D8_IN D9_IN D10_IN D11_IN D12_IN D13_IN D14_IN D15_IN
VRAMMOD0 VRAMMOD1 VRAMMOD2 VRAMMOD3 VRAMMOD4 VRAMMOD5 VRAMMOD6 VRAMMOD7 VRAMMOD8 VRAMMOD9 VRAMMOD10 VRAMMOD11 VRAMMOD12 VRAMMOD13 VRAMMOD14 VRAMMOD15
F127 F91 G81 G18
A4H

Outputs of these adders go back to the D24's here on same sheet

Note that A15 is used but that VRAM bank selection is done with A15_RAW, which is only set by the CPU.

REG_LSPCMODE

To check: only one ?

WR_LSPC_MODE
C50B C59A
E61
RESET_BUF
D3_IN D4_IN D5_IN D6_IN
TIMER_IRQ_EN TIMER_MODE0 TIMER_MODE1
AA_DISABLE
C180A
C184A C186A B180B
SPR_AA_3 SPR_AA_2
AUTOANIM3_EN AUTOANIM2_EN
E74
D7_IN
TIMER_MODE2

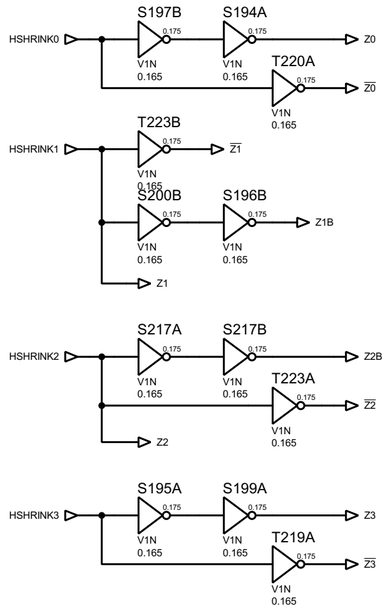
DISBL AA_3 AA_2 3_EN 2_EN
0 0 0 0 0
0 0 1 0 1
0 1 0 0 1
0 1 1 1 1
1 0 0 0 0
1 0 1 0 0
1 1 0 0 0
1 1 1 1 0

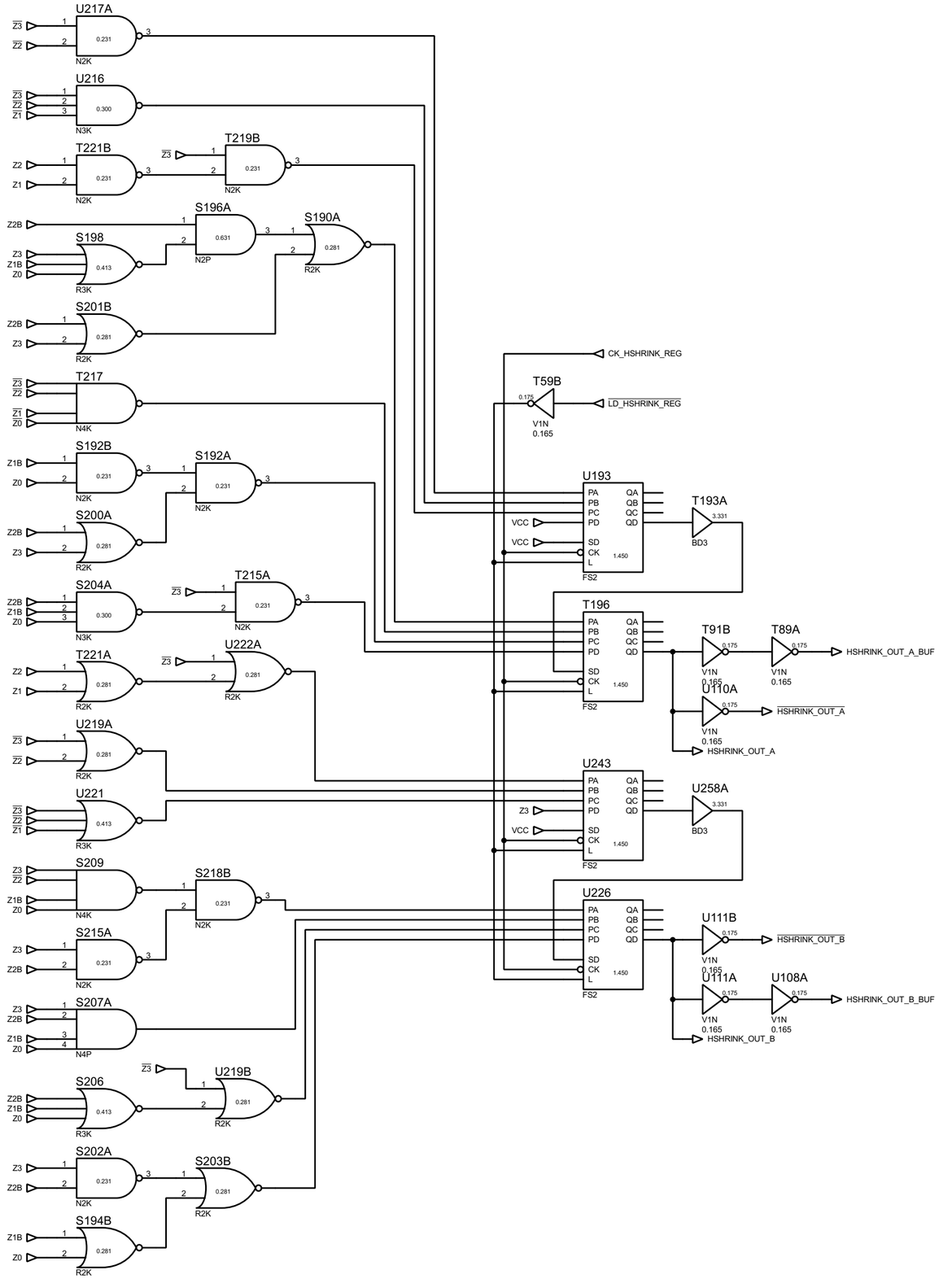
Auto-anim speed

B77A B77B B90A B90B
C87
D8_IN D9_IN D10_IN D11_IN
B91
Auto-anim timer
E105
D12_IN D13_IN D14_IN D15_IN
E143A E143B E144B E104A
E117
C43
E149
X1B
TEST1 RASTERC_8
TEST10
E95A
D151
AUTOANIM0 AUTOANIM1 AUTOANIM2
RESETP2

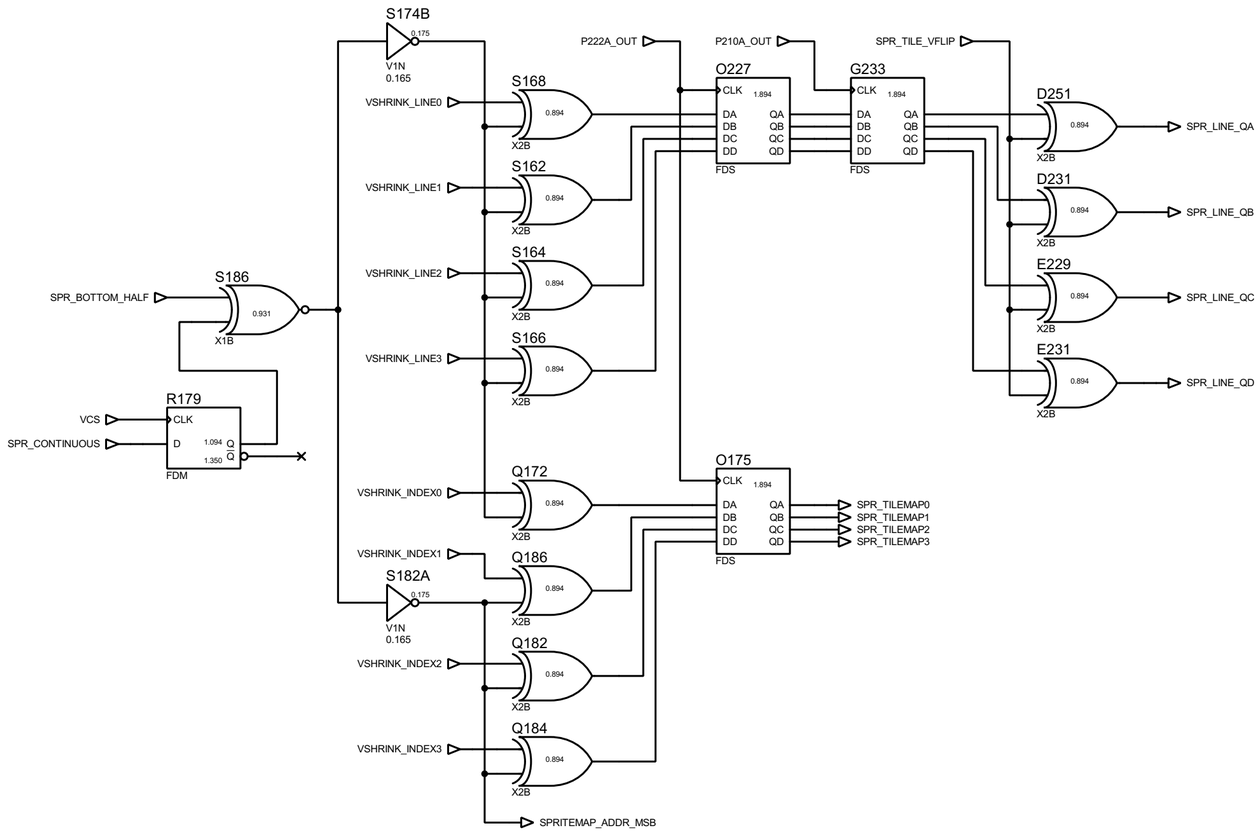
Auto-anim counter

Horizontal shrink "lookup"





Vertical shrink



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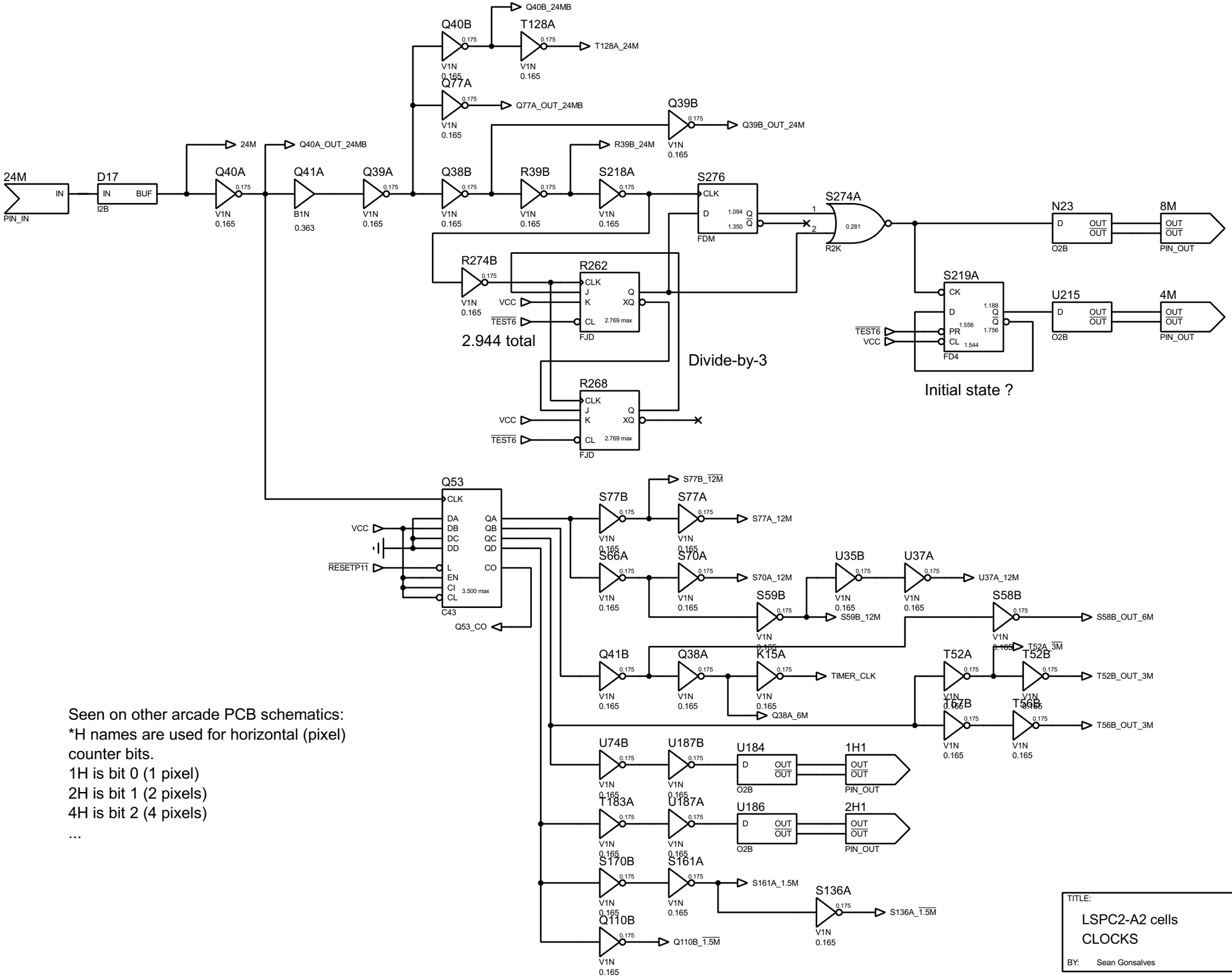

Seen on other arcade PCB schematics:
*H names are used for horizontal (pixel) counter bits.
1H is bit 0 (1 pixel)
2H is bit 2 (4 pixels)
...

TITLE: LSPC2-A2 cells CLOCKS	DATE: 13/08/2021
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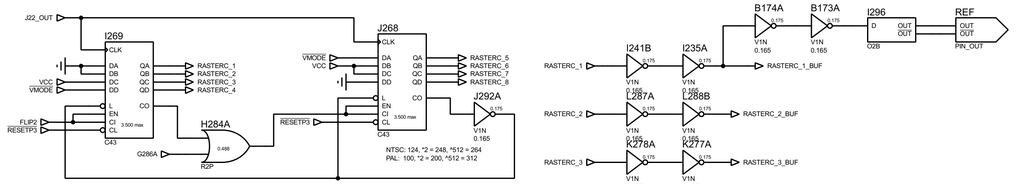
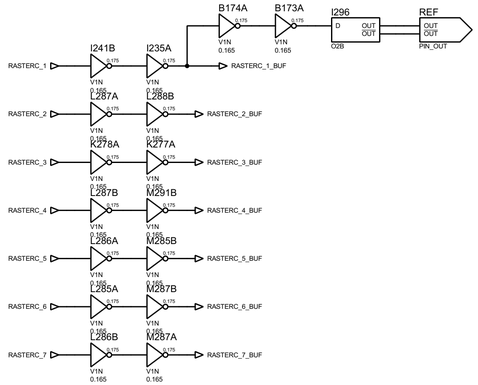
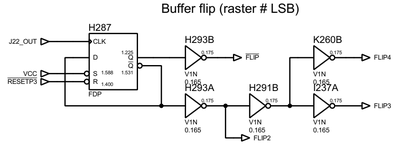
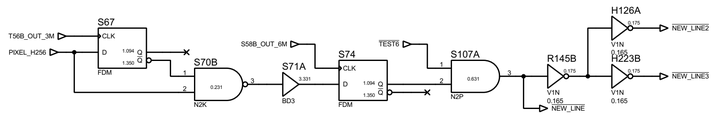
RASTER COUNTER



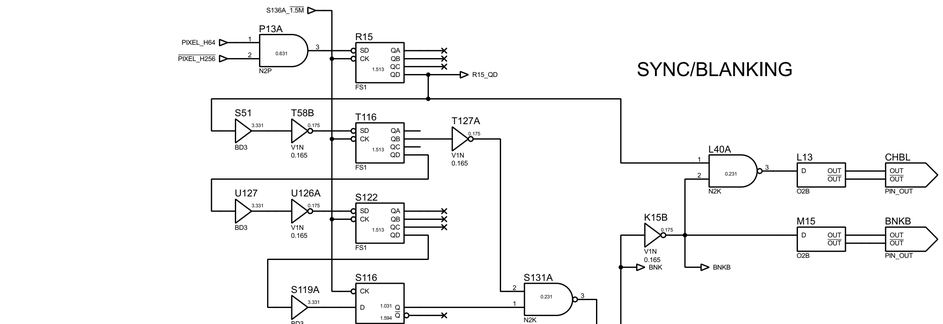


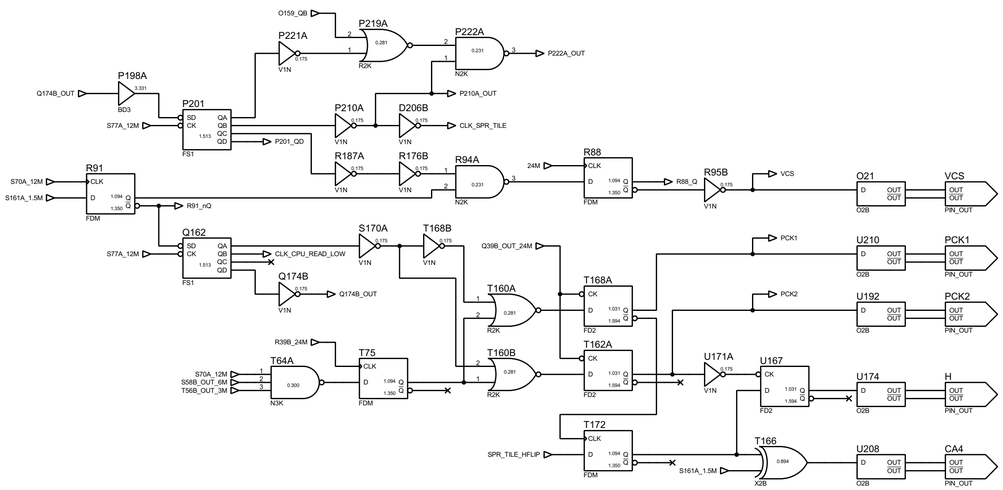
Buffer flip (raster # LSB)





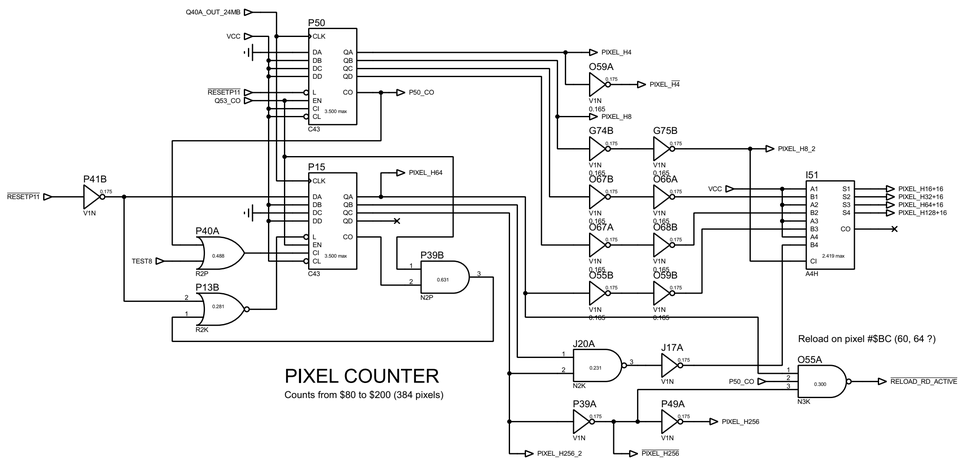
SYNC/BLANKING





PIXEL COUNTER

Counts from $80 to $200 (384 pixels)



TITLE:	DATE:
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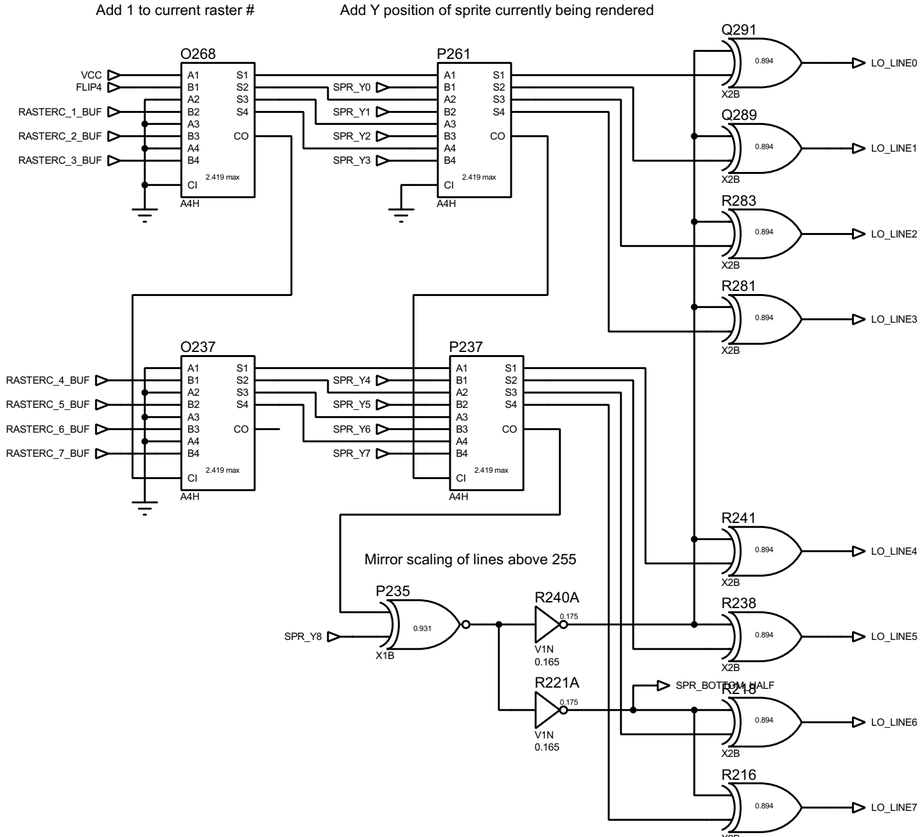
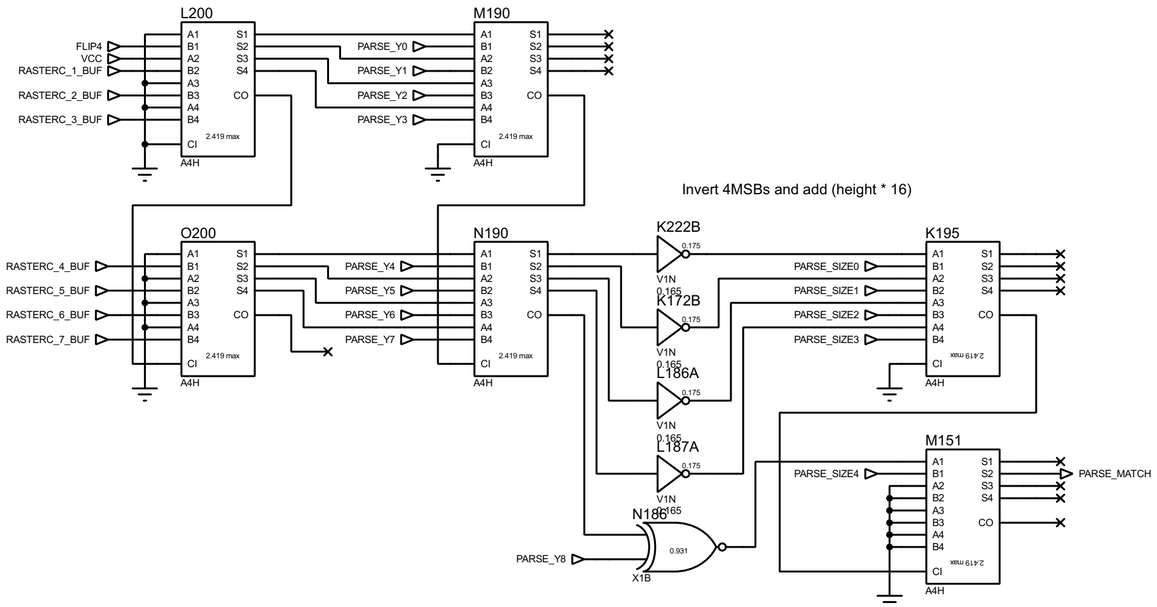
Add 1 to current raster #

Add Y position of sprite currently being rendered

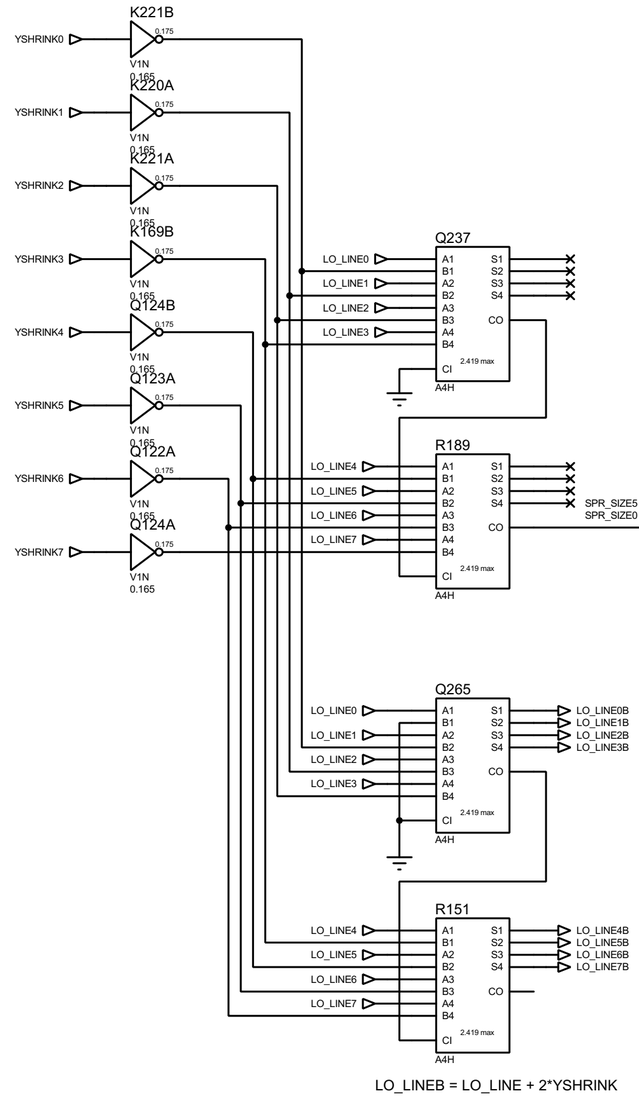


Add 2 to current raster #

Add Y position of sprite currently being parsed



8.188 total



LO_LINEB = LO_LINE + 2*YSHRINK

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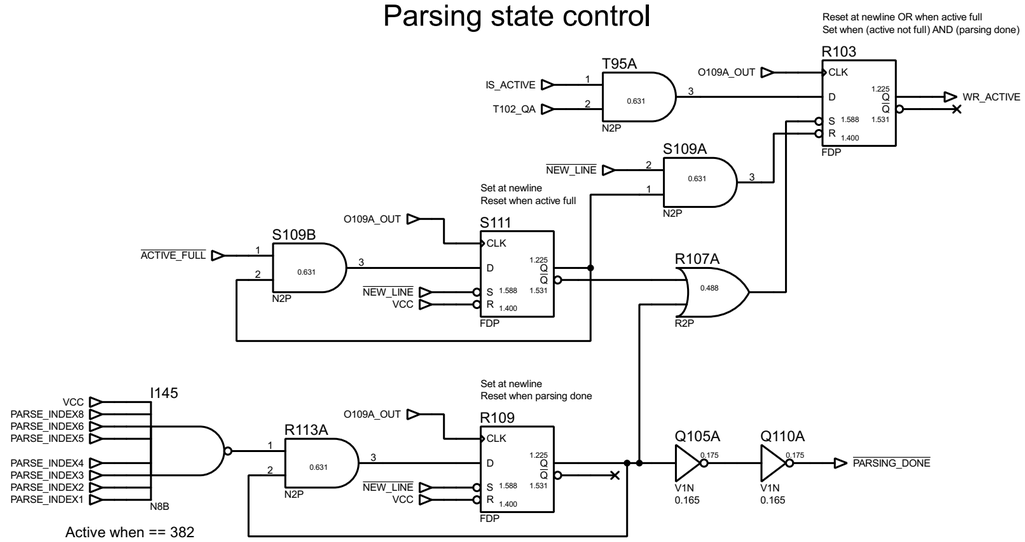
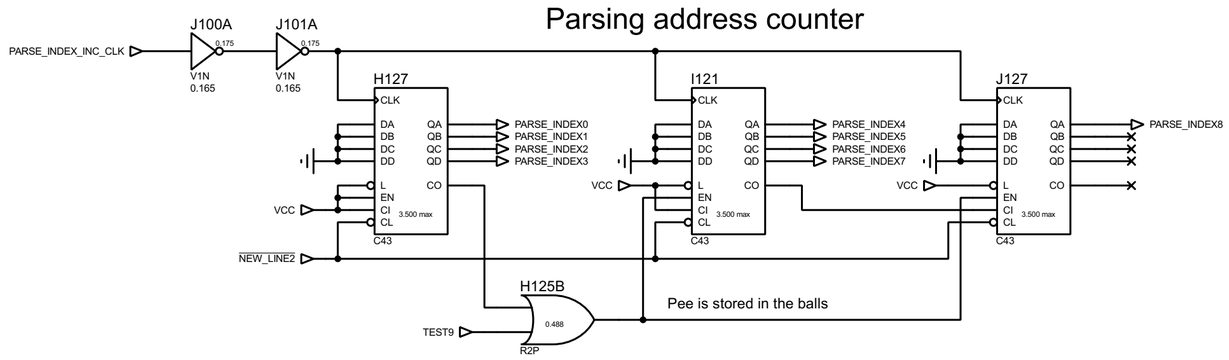
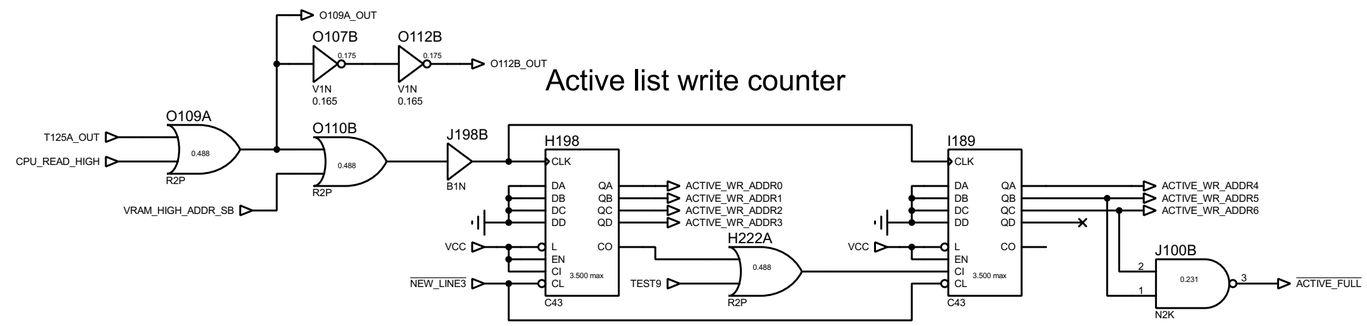
Parsing state control



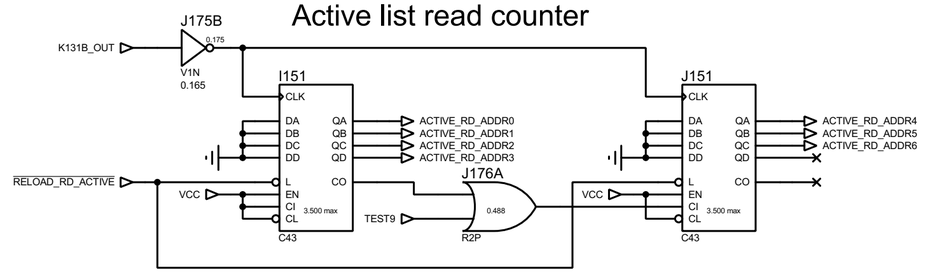
Parsing address counter



Active list write counter



Active list read counter



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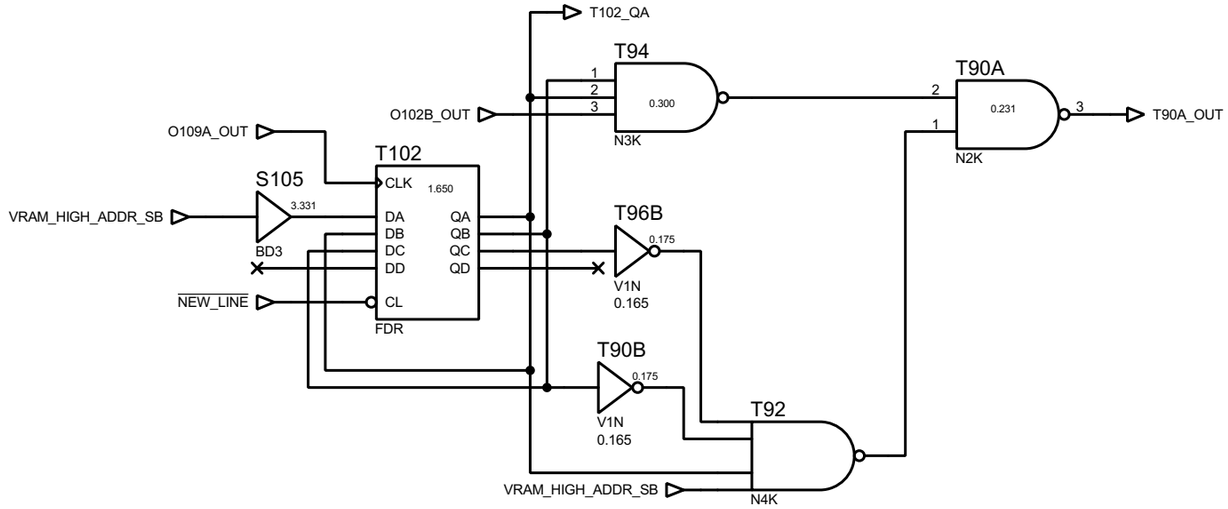

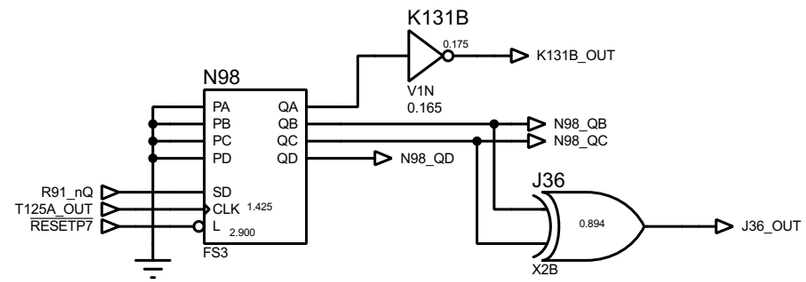

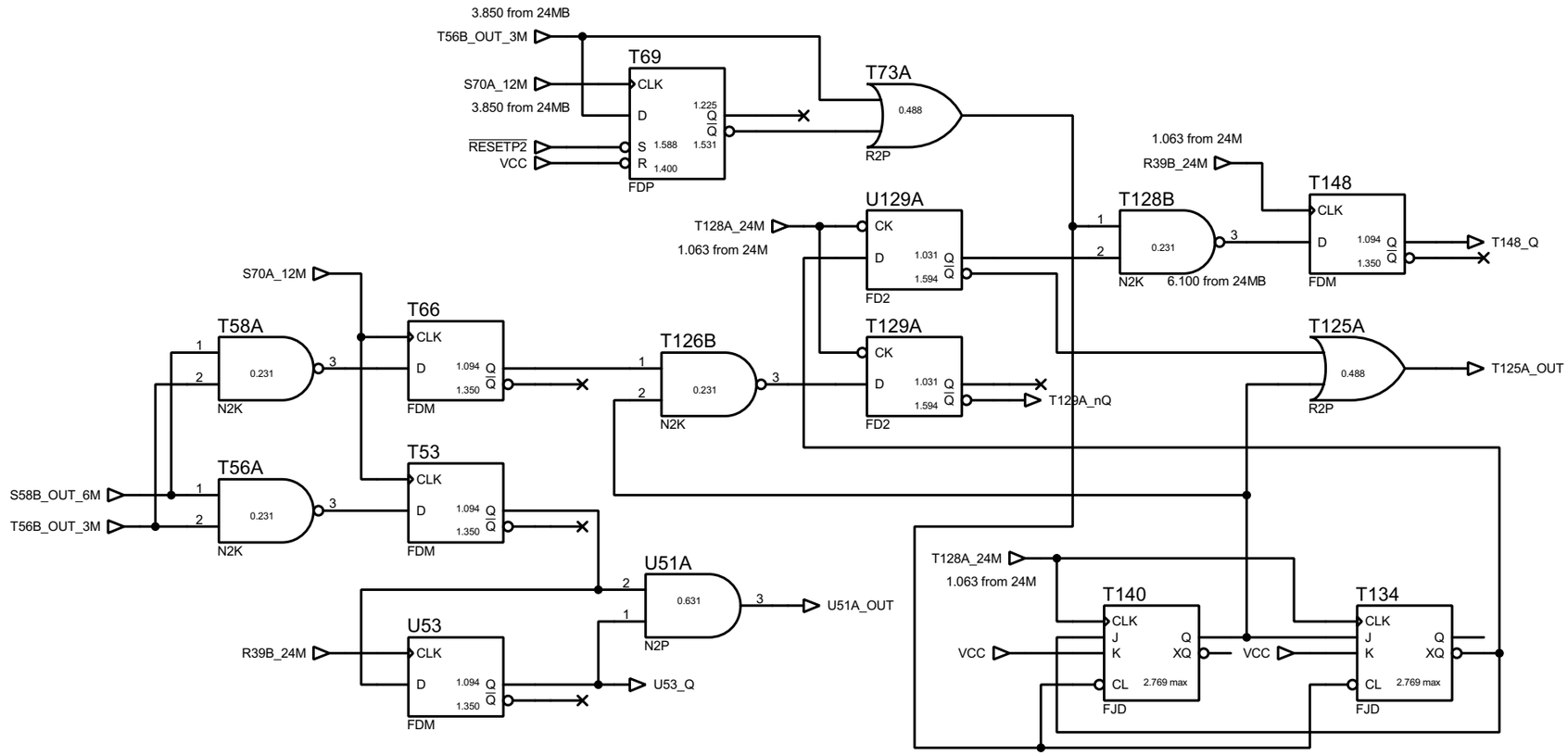

TITLE: LSPC2-A2 cells SEQUENCING	DATE: 13/08/2021
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