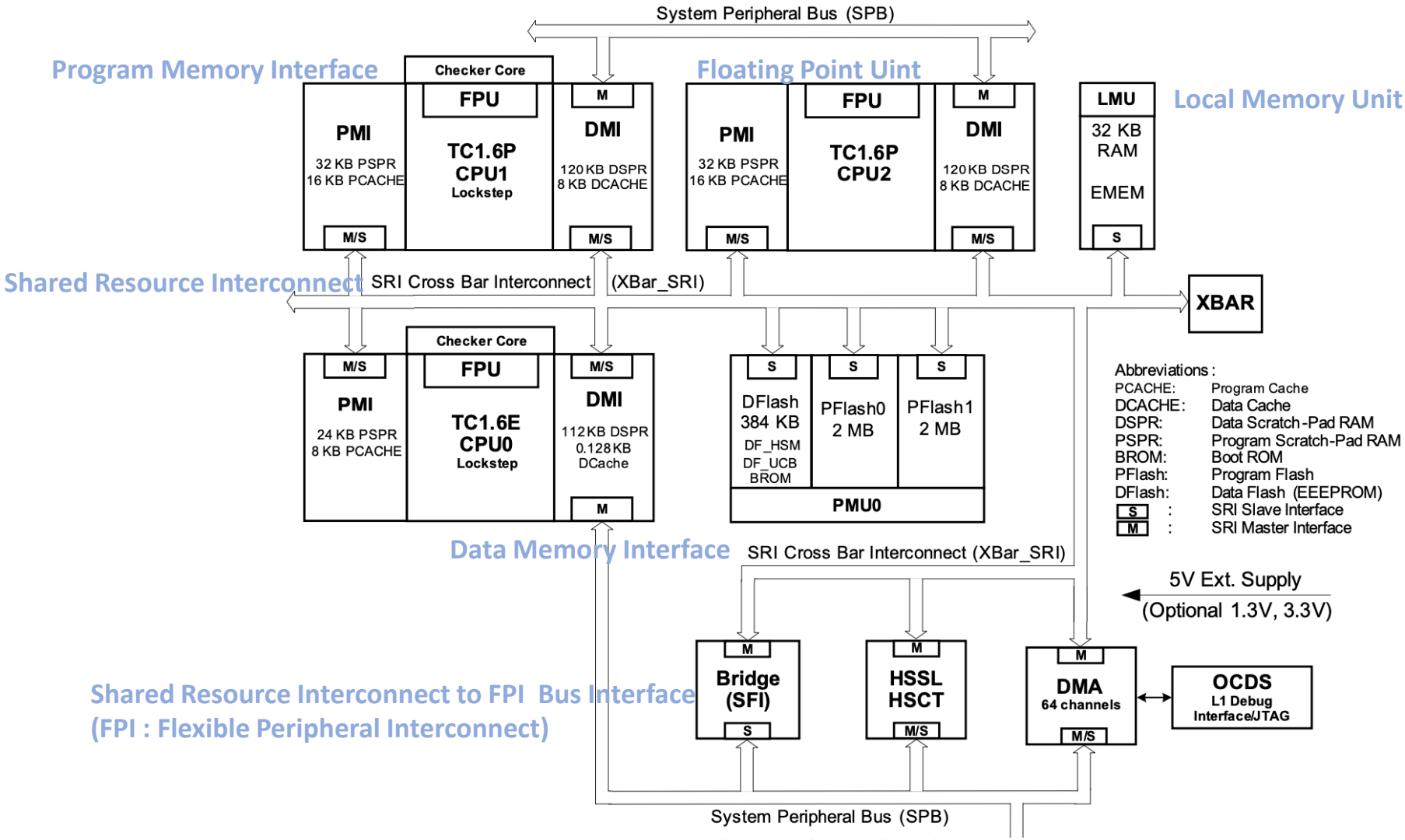
TC275 Core Overview

User's Manual V2.2 2014-12

ACE Lab.

KNU

1. TC27x Introduction



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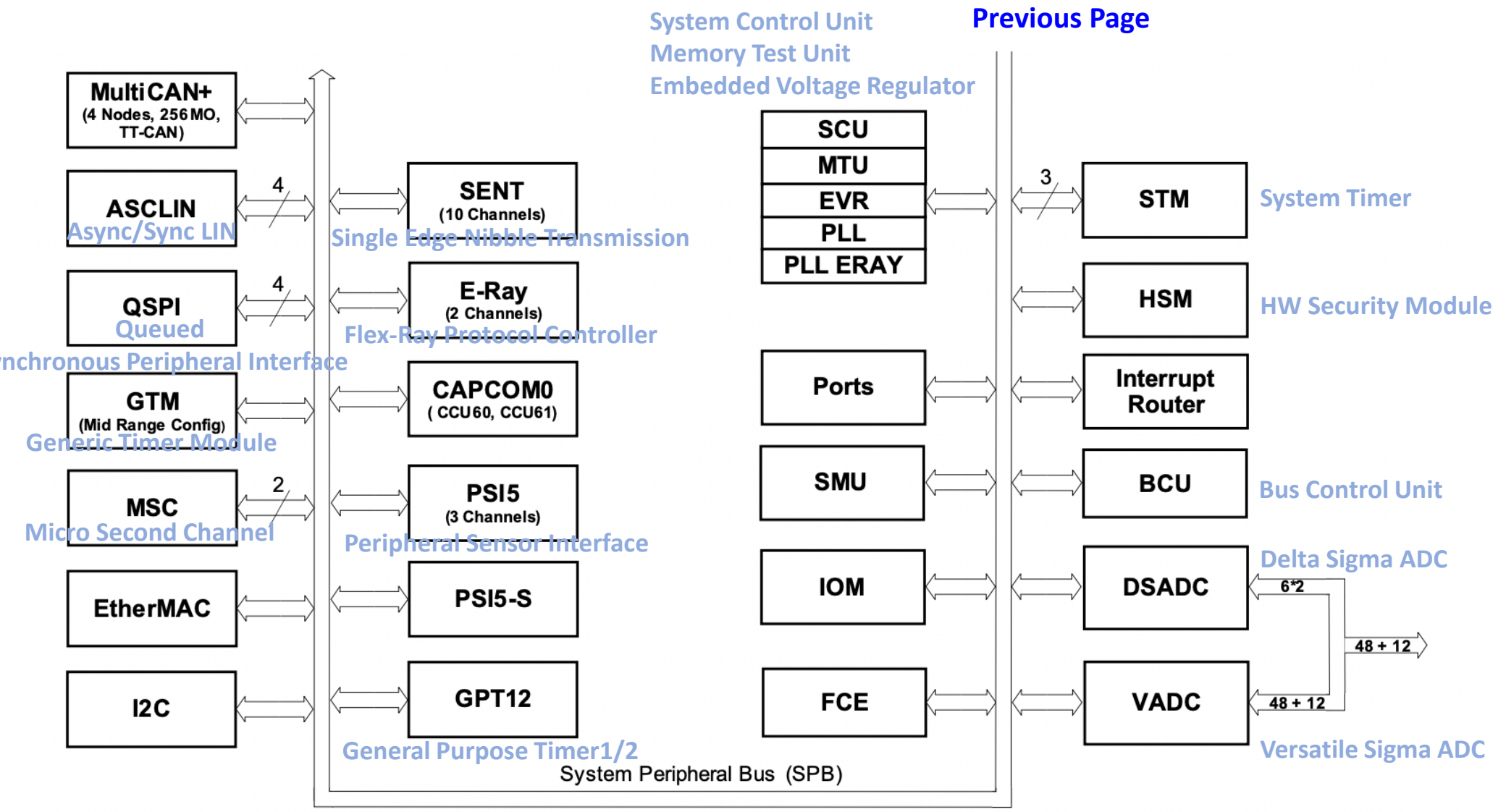
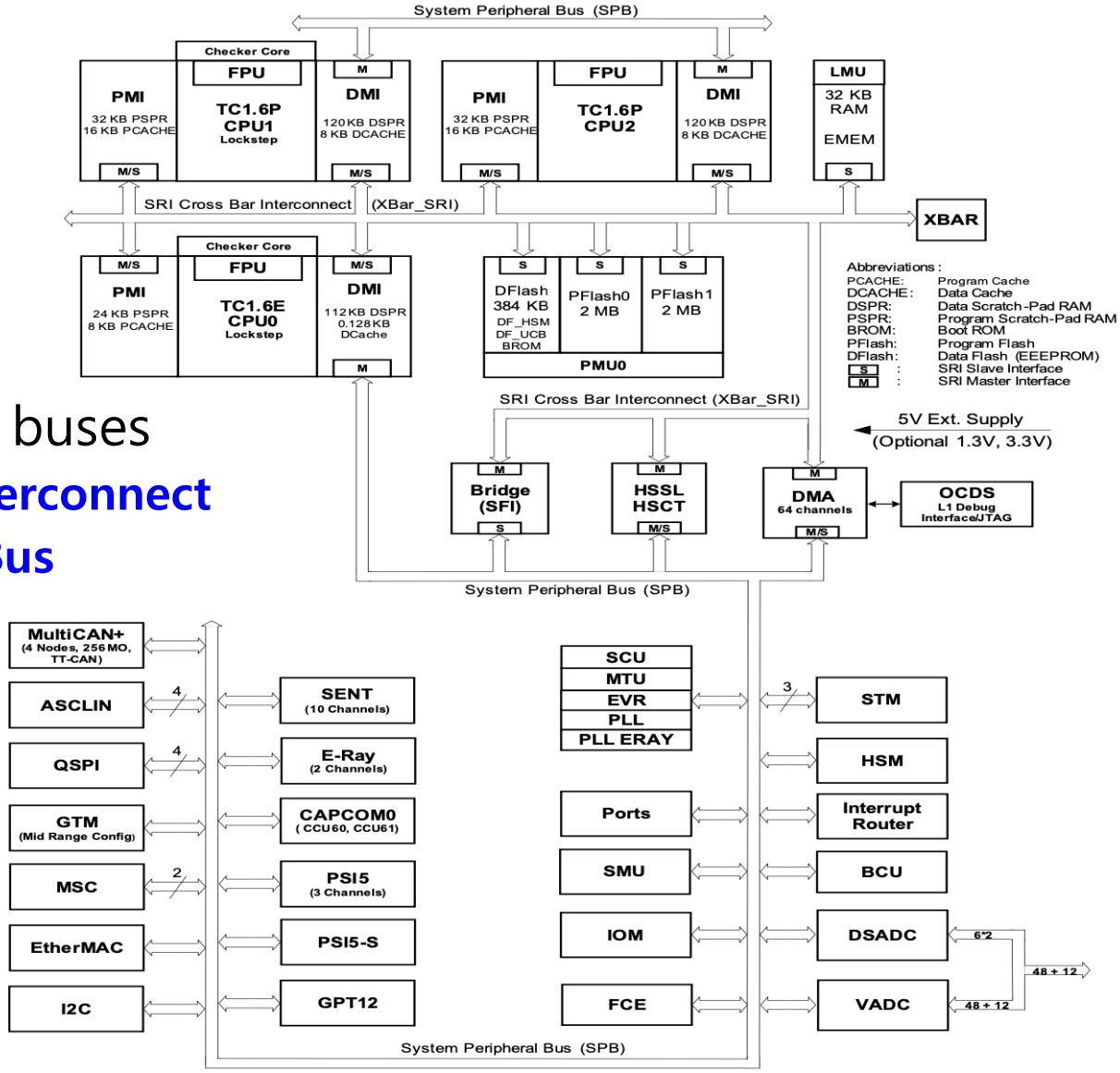
1. TC27x Introduction



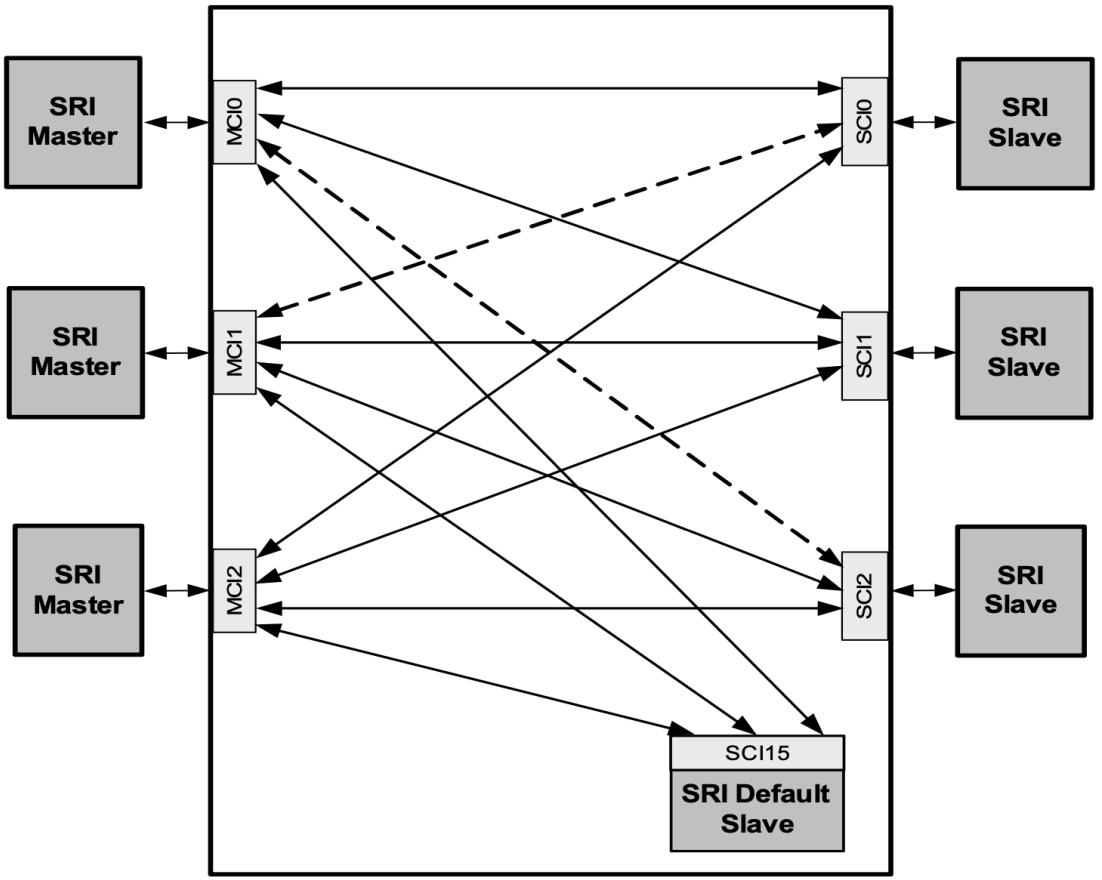
2. On-Chip System Buses and Bus Bridges

- Two independent on-chip buses
  - **SRI: Shared Resource Interconnect**
  - **SPB: System Peripheral Bus**



2. On-Chip System Buses and Bus Bridges

- SRI Crossbar (XBar_SRI)



XBar_SRI point to point connection scheme

3. Memory Maps

- Program Memory Unit (PMU0)
  - 4 MB of Program Flash Memory (PFLASH)
  - Data Flash Memory (DF_EEPROM)
  - User Configuration Blocks (DF_UCB)
  - 32 KB of Boot ROM (BROM)
- CPU0
  - 24 KB of Program Scratch-Pad SRAM (PSPR)
  - 112 KB of Data Scratch-Pad SRAM (DSPR)
  - 8 KB of Program Cache (PCache)
- CPU1 & CPU2
  - 32 KB of Program Scratch-Pad SRAM (PSPR)
  - 120 KB of Data Scratch-Pad SRAM (DSPR)
  - 16 KB of Program Cache (PCache)
  - 8 KB of Data Cache (DCache)
- LMU: 32 KB SRAM (LMURAM)

Address Map of the On Chip Bus System

Segment	Address Ragne	Size	Description
0-4	0000 0000h - 4FFF FFFFh	-	Reserved
5	5000 0000h - 5FFF FFFFh	-	CPU2 Area
6	6000 0000h - 6FFF FFFFh	-	CPU1 Area
7	**7000 0000h - 7001 BFFFh**	**112 KB**	**CPU0 Data Scratch-Pad SRAM (CPU0.DSPR)**
	7010 0000h - 7010 5FFFh	24 KB	CPU0 Program Scratch-Pad SRAM (CPU0.PSPR)
	7010 6000h - 7010 7FFFh	8 KB	CPU0 Program Cache SRAM (CPU0.PCache)
	701C 0000h - 701C 0BFFh		CPU0 Program Cache TAG SRAM (CPU0.PTAG)
8	**8000 0000h - 801F FFFFh**	**2 MB**	**Program Flash 0 (PF0)**
	8020 0000h - 803F FFFFh	2 MB	Program Flash 1 (PF1)
	8FFF 80000h - 8FFF FFFFh	32 KB	Boot ROM (BROM)
9	9000 0000h - 9000 7FFFh	32 KB	LMU SRAM (LMUSRAM)

Reserved 제외, User's Manual Table 3-2 참조

4. TC27x BootROM Content

- BOOT_TC27X
  - Startup software (SSW)
  - Software modules implementing additional functions (Bootstrap Loaders)
  - Test Firmware

Startup Software (SSW)

- SSW는 칩이 리셋 된 후 실행되는 첫 번째 소프트웨어임
- SSW는 CPU0에서 실행
  - 다른 CPU는 부팅 동안 Halt-state 유지하다 사용자 SW에 의해 시작됨
  - BootROM의 SSW 시작 주소는 CPU0의 PC 레지스터의 리셋 값임. 이 위치에서 명령어를 가져오며 장치가 시작된 후 실행되는 첫 번째 명령어임
  - 진입점 직후 펌웨어는 테스트 모드를 체크하고, 만약 선택되어 있다면 테스트 펌웨어로 점프가 실행됨
  - 마지막 SSW 명령어는 첫 번째 사용자 코드 명령어로 점프를 수행함. 첫 번째 사용자 명령어는 사용자가 선택한 스타트업 설정에 따라 다른 위치에서 가져올 수 있음
- SSW는 다음 중 하나 이상에 따라 장치를 초기화 절차를 포함함
  - 전용 플래시 위치에 저장된 이전 정보
  - 전용 레지스터/메모리 위치에 특수 비트/필드의 현재 상태
  - SSW 실행을 트리거한 이벤트 유형 (마지막 리셋 이벤트)
  - 외부(구성)핀에 적용된 값 (옵션)

5. CPU Subsystem

- Key CPU Features
  - 32-bit load store architecture
  - 4 GB address range
  - 16-bit & 32-bit instructions for reduced code size
  - Data types
    - Boolean, integer with saturation, bit array, signed fraction, character, double-word integers, signed integer, unsigned integer, IEEE-754 single-precision floating point
  - Data formats
    - Bit, byte (8-bit), half-word (16-bit), word (32-bit), double-word (64-bit)
  - Byte and bit addressing
  - **Little-endian** byte ordering for data, memory and CPU registers
  - Multiply and Accumulate (MAC) instructions: Dual 16x16, 16x32, 32x32
  - Saturation integer arithmetic
  - Packed data

5. CPU Subsystem

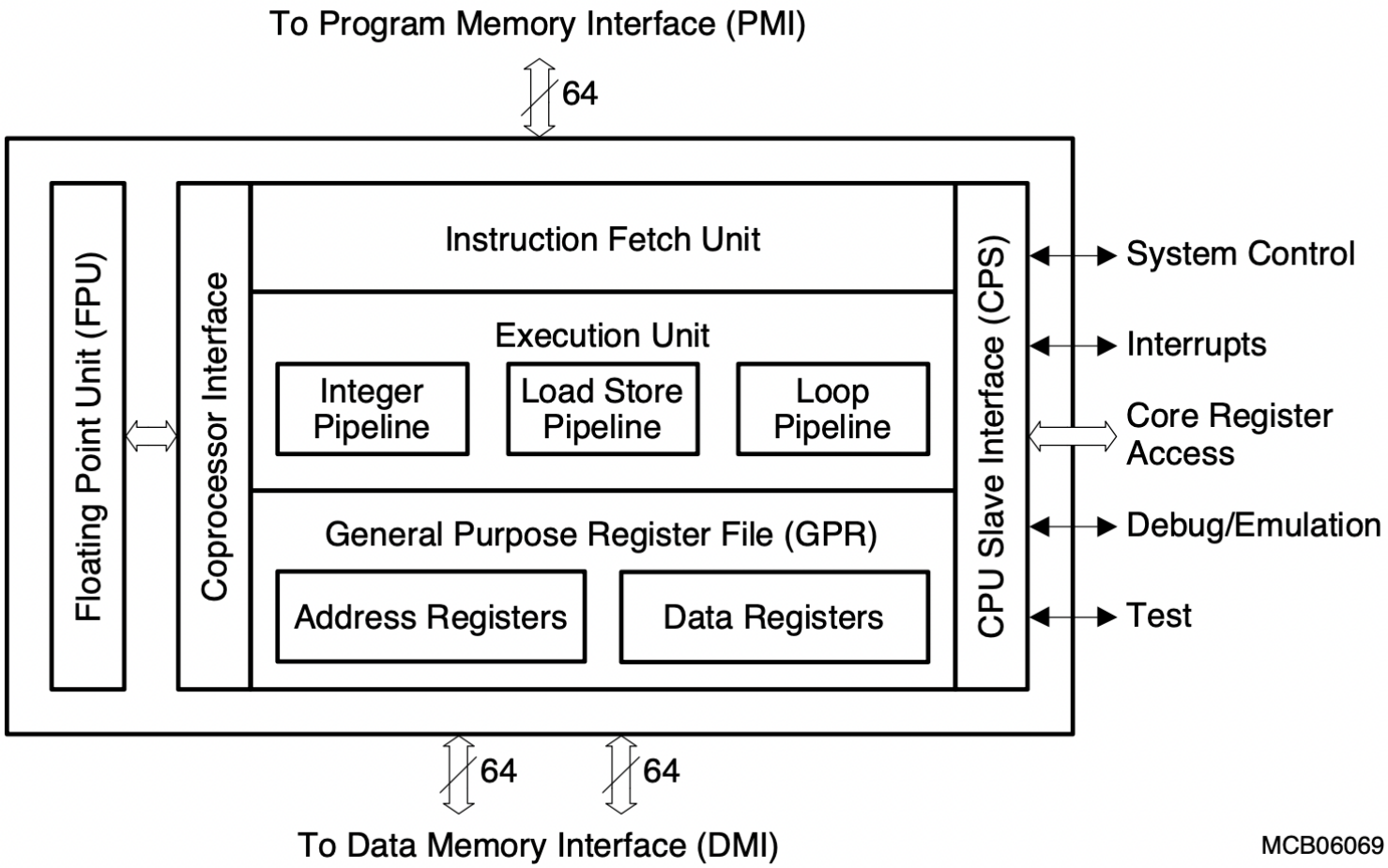
- Key CPU Features
  - **Addressing modes**
    - Absolute, circular, bit reverse, long + short, base + offset with pre- and post-update
  - Instruction types
    - Arithmetic, address arithmetic, comparison, address comparison, logical, MAC, shift, coprocessor, bit logical, branch, bit field, load/store, packed data
  - General Purpose Register Set (GPRS)
    - Sixteen 32-bit data registers (D0 - D15)
    - **Sixteen 32-bit address registers (A0 - A15)**
    - Three 32-bit status and program counter registers (PSW, PC, **PCXI**)
  - Flexible memory protection system providing multiple protection sets with multiple protection ranges per set
  - Temporal protection system allowing time bounded real time operation

5. CPU Subsystem

- Key CPU Features
  - Most instructions executed in 1 cycle
  - Branch instructions in 1, 2, or 3 cycles (using dynamic branch prediction)
  - Wide memory interface for fast context switch
  - Automatic context save-on-entry and restore-on-exit for: subroutine, interrupt, trap
  - Four memory protection register sets
  - **Dual instruction issuing** (in parallel into Integer Pipeline and Load/Store Pipeline)
  - Third pipeline for loop instruction only (zero overhead loop)
  - Single precision Floating Point Unit (IEEE-754 Compatible)
  - Dedicated integer divide unit
  - Implementation optimized for performance
  - 16 data protection ranges, 8 code protection ranges

TC1.6P Implementation Overview

- CPU block diagram



Registers

- Program Status Word Register

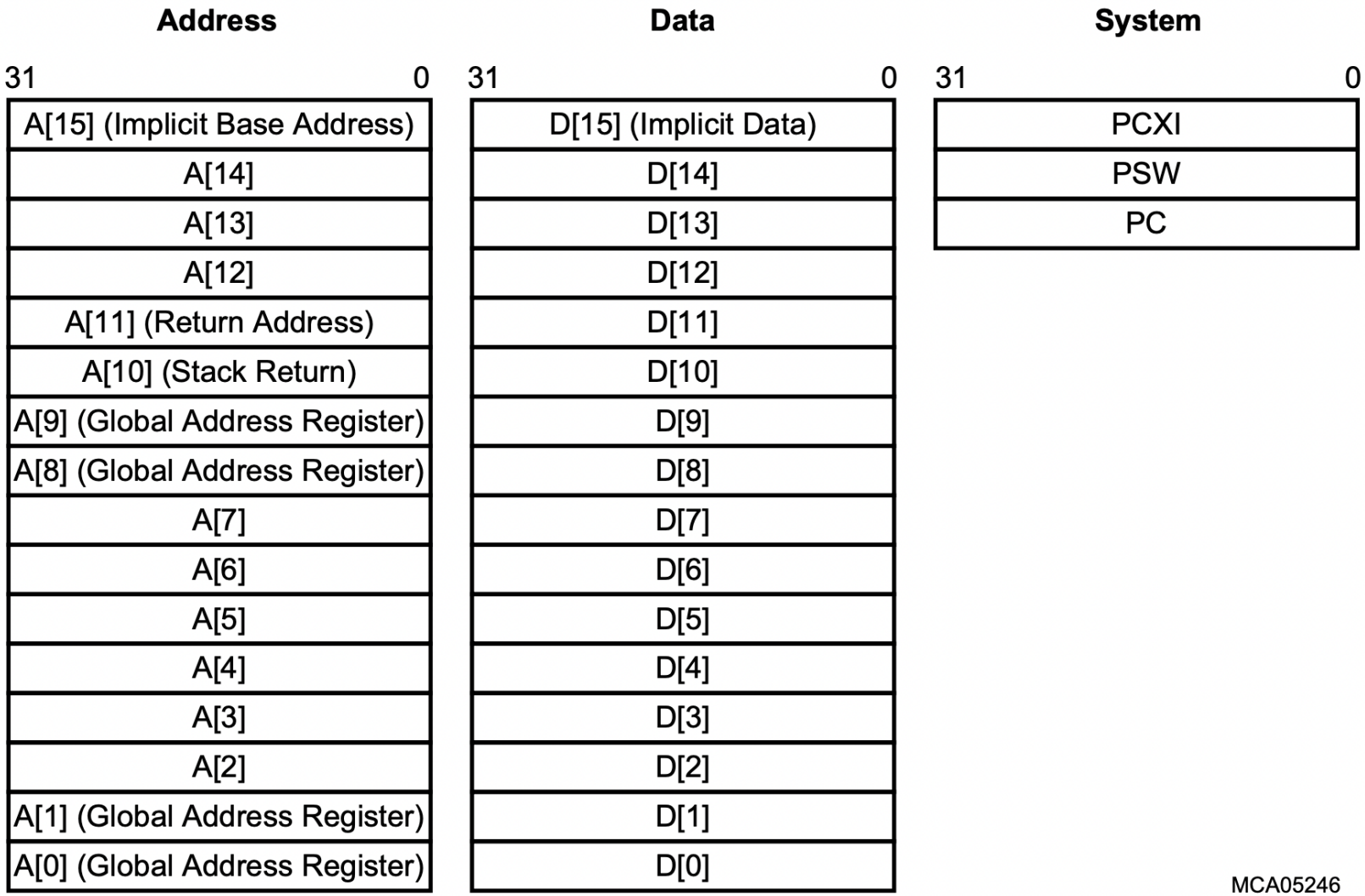
PSW

Program Status Word Register (CSFR_Base + $FE04_H$) **Reset Value: 0000 $0B80_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C or FS	V or FI	SV or FV	AV or FZ	SAV or FU	FX	RM		0							
rwh	rwh	rwh	rwh	rwh	rwh	rw		r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	S	PRS		IO		IS	GW	CDE	CDC						
r	rwh	rwh		rwh		rwh	rwh	rwh	rwh						

Registers



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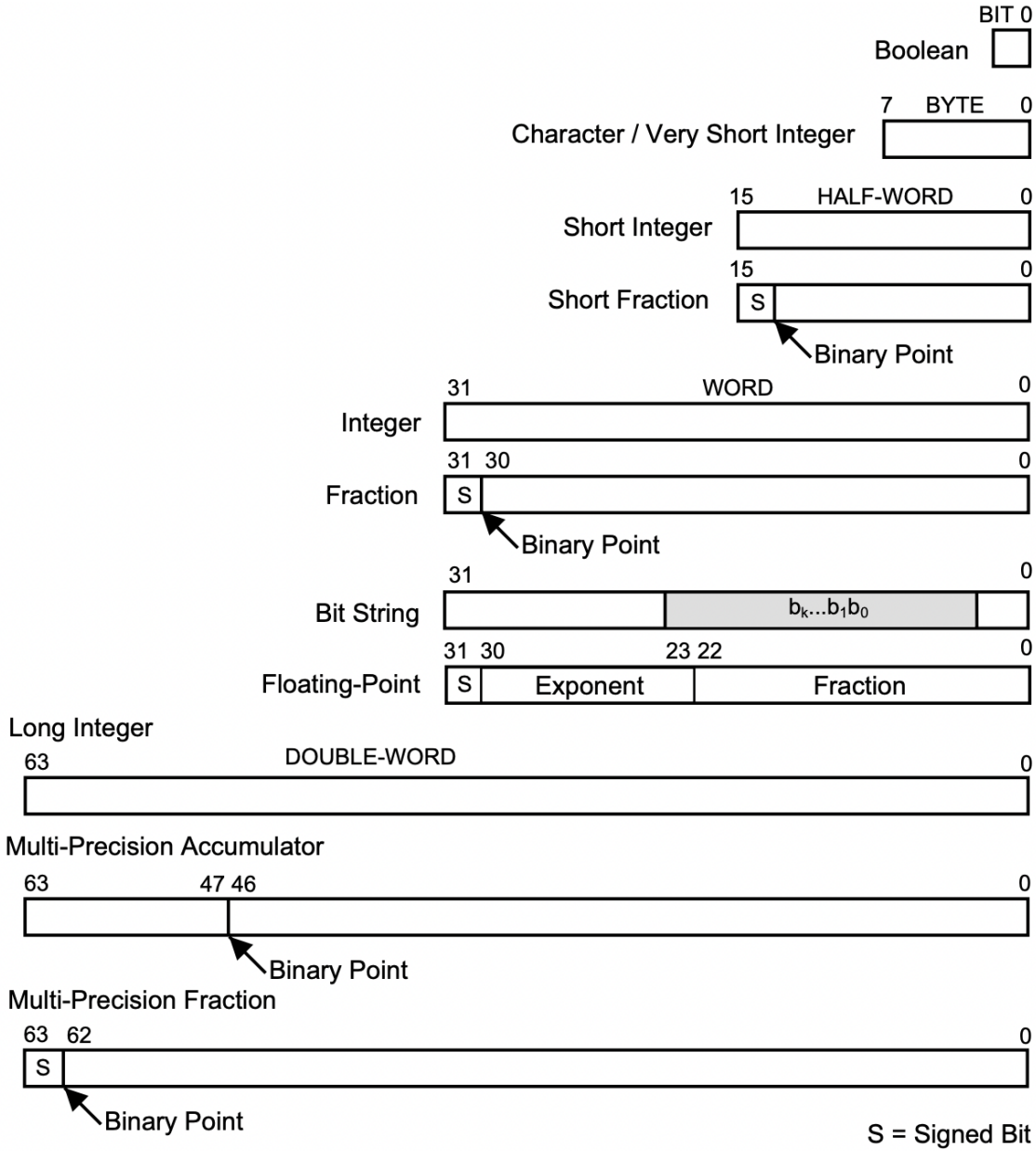
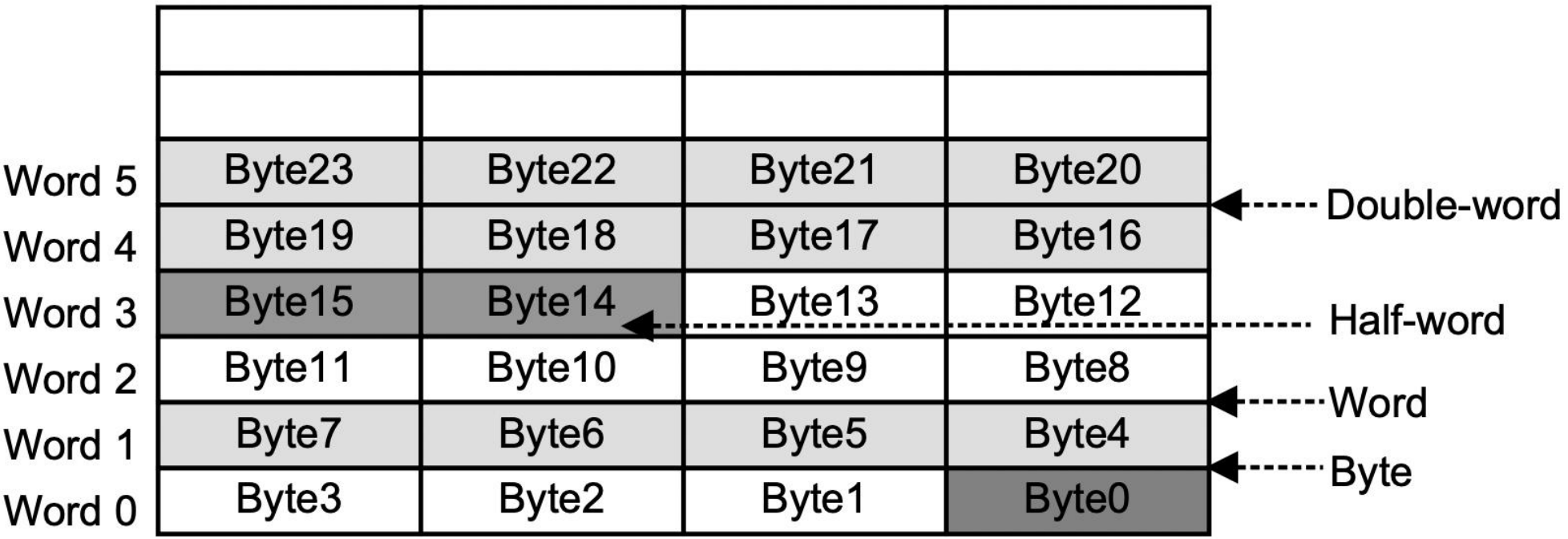
Supported Data Formats



Alignment Rules

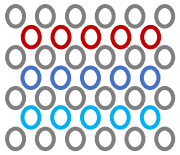
Access type	Access size	Alignment of address in memory
Load, Store Data Register	Byte	Byte (1_H)
	Half-Word	2 bytes (2_H)
	Word	2 bytes (2_H)
	Double-Word	2 bytes (2_H)
Load, Store Address Register	Word	4 bytes (4_H)
	Double-Word	4 bytes (4_H)
SWAP.W, LDMST	Word	4 bytes (4_H)
ST.T	Byte	Byte (1_H)
Context Load / Store / Restore / Save	16 x 32-bit registers	64 bytes (40_H)

Byte Ordering



Q & A

Thank you for your attention



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