PCA

DRN BY	NR
DATE	20Mar2015
CHKD BY	SIVA REDDY
DATE	20Mar2015
APPD BY	
DATE	

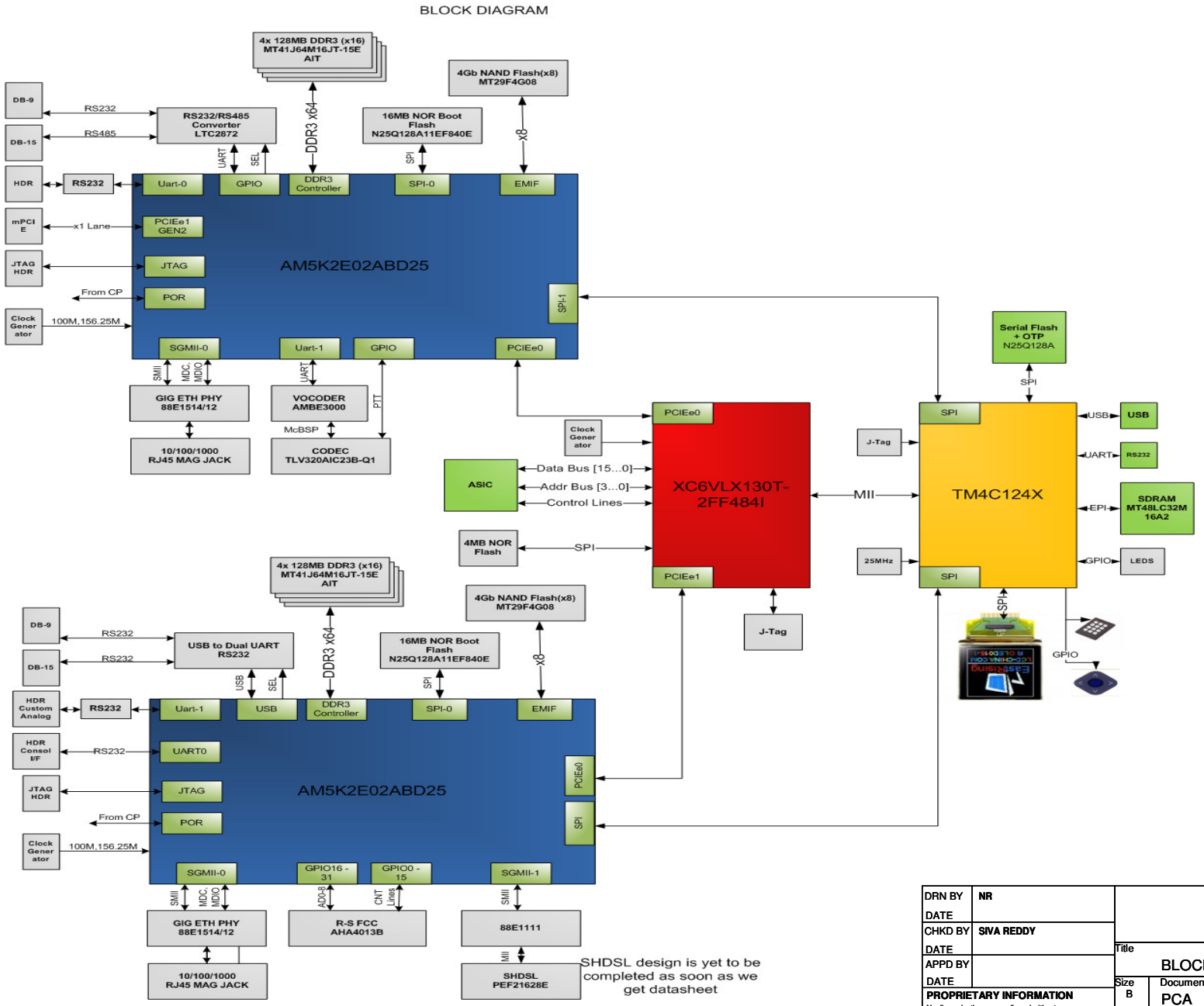
Ronanki Infotech Pvt Ltd

Title: COVER PAGE

Size	Document Number	Rev
B	PCA	1.0

Date: Sunday, March 22, 2015 Sheet 1 of 46

BLOCK DIAGRAM



DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION

No dissemination or use allowed without prior written permission

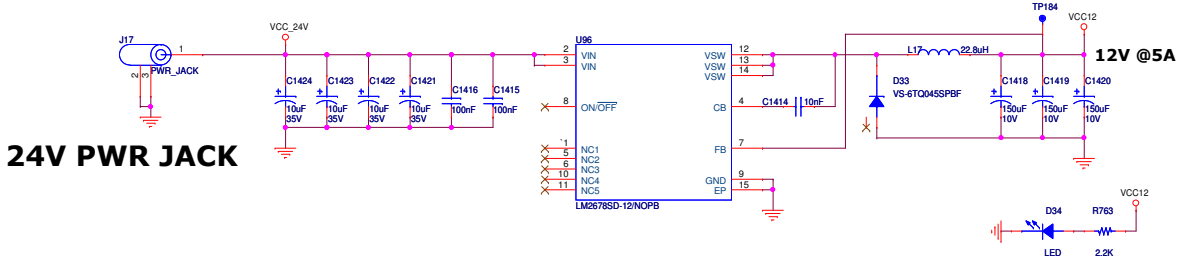
Ronanki Infotech Pvt Ltd

Title: BLOCK DIAGRAM

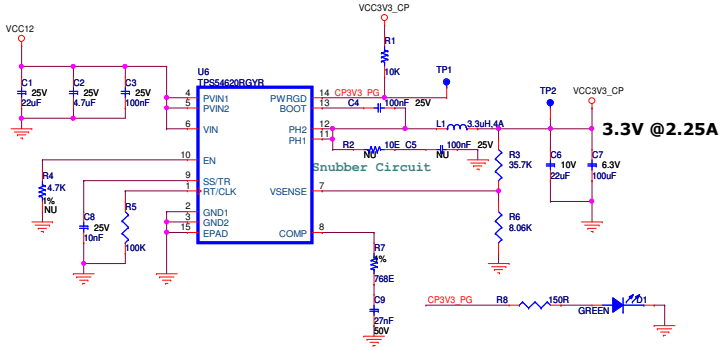
Size	Document Number	Rev
B	PCA	1.0

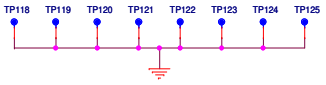
Date: Monday, March 23, 2015 Sheet 2 of 46

24V to 12V Generation



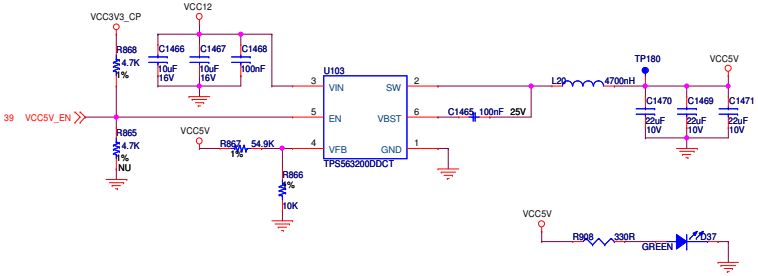
12V to 3.3V Generation for Controll Processor



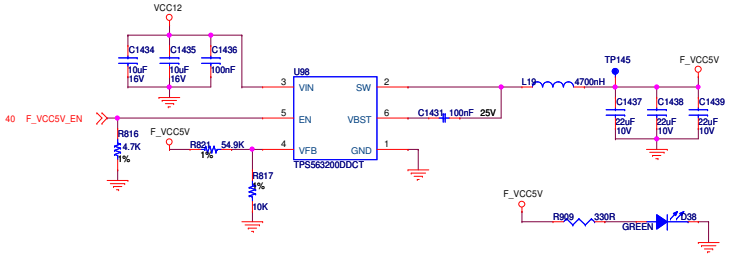


Distribute these TPs in board

12V to 5V Generation



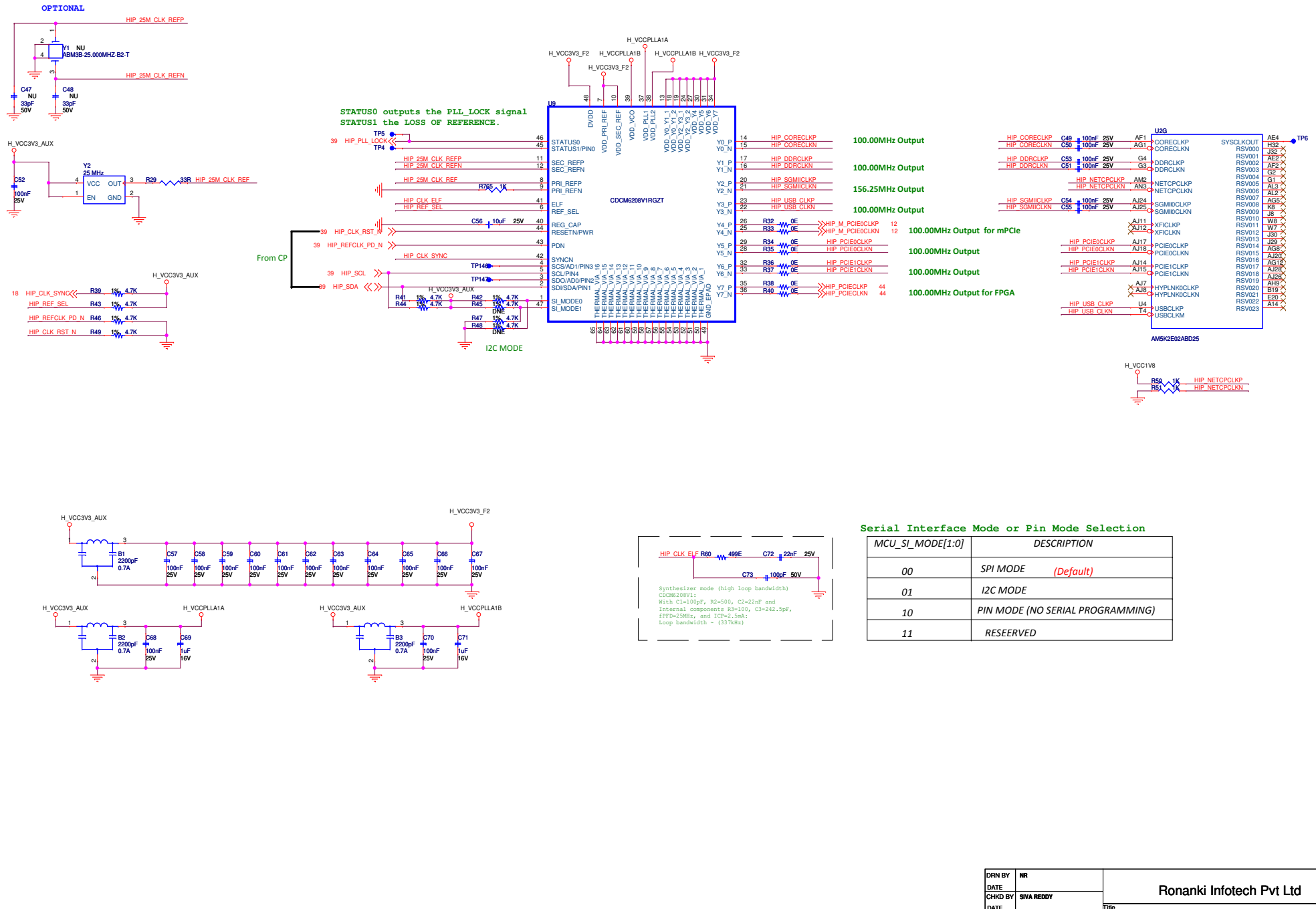
12V to 5V Generation For ASIC



DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY		
DATE		Title	MAIN & MISC PWR
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 3 of 46

No dissemination or use allowed without prior written permission

HIP CLOCK SOURCE

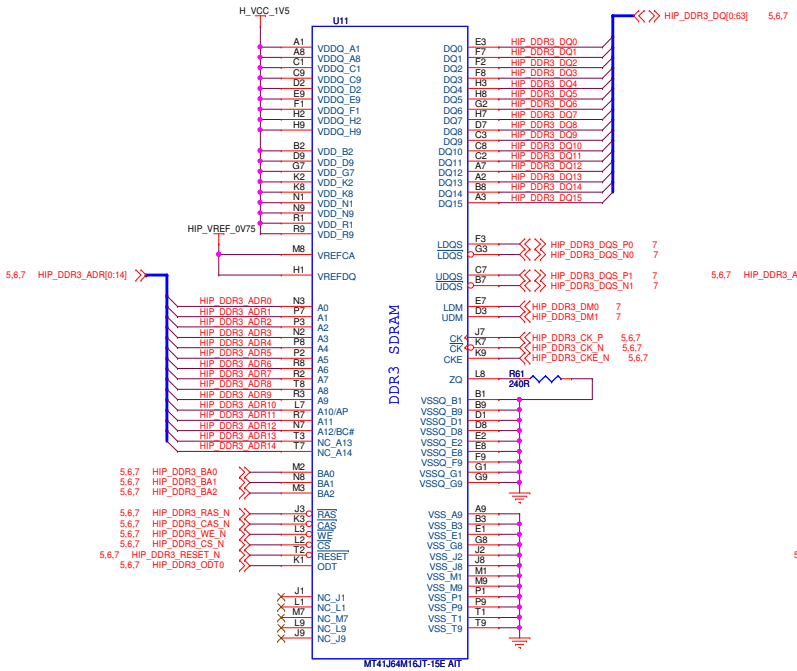


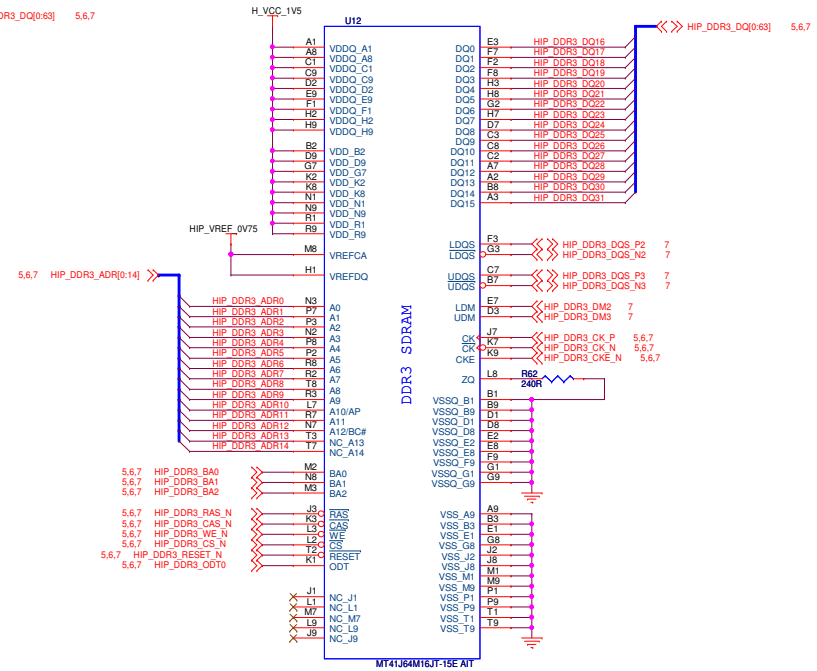
Serial Interface Mode or Pin Mode Selection

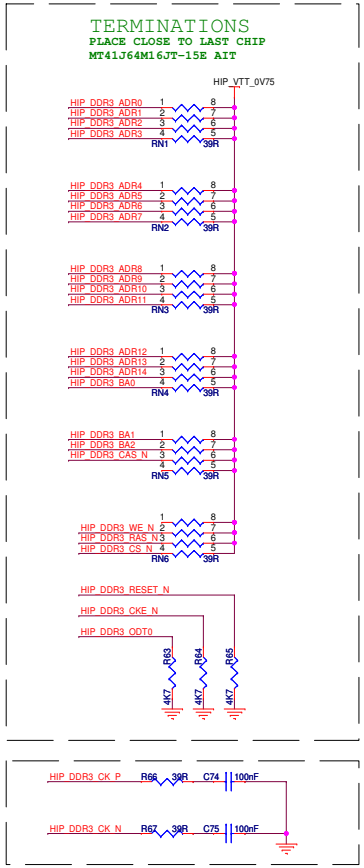
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

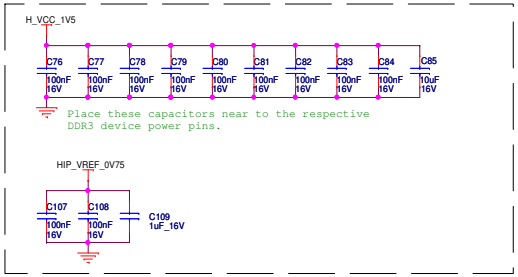
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_CLK
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 4 of 46

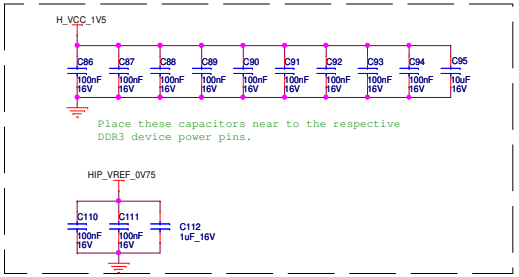
DDR3_MEMORY_HIP

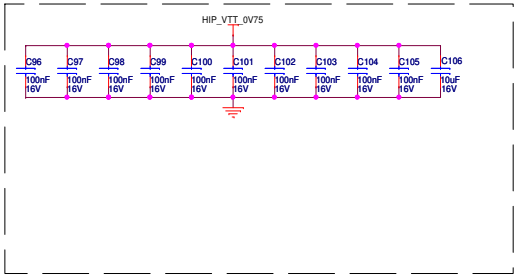












DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

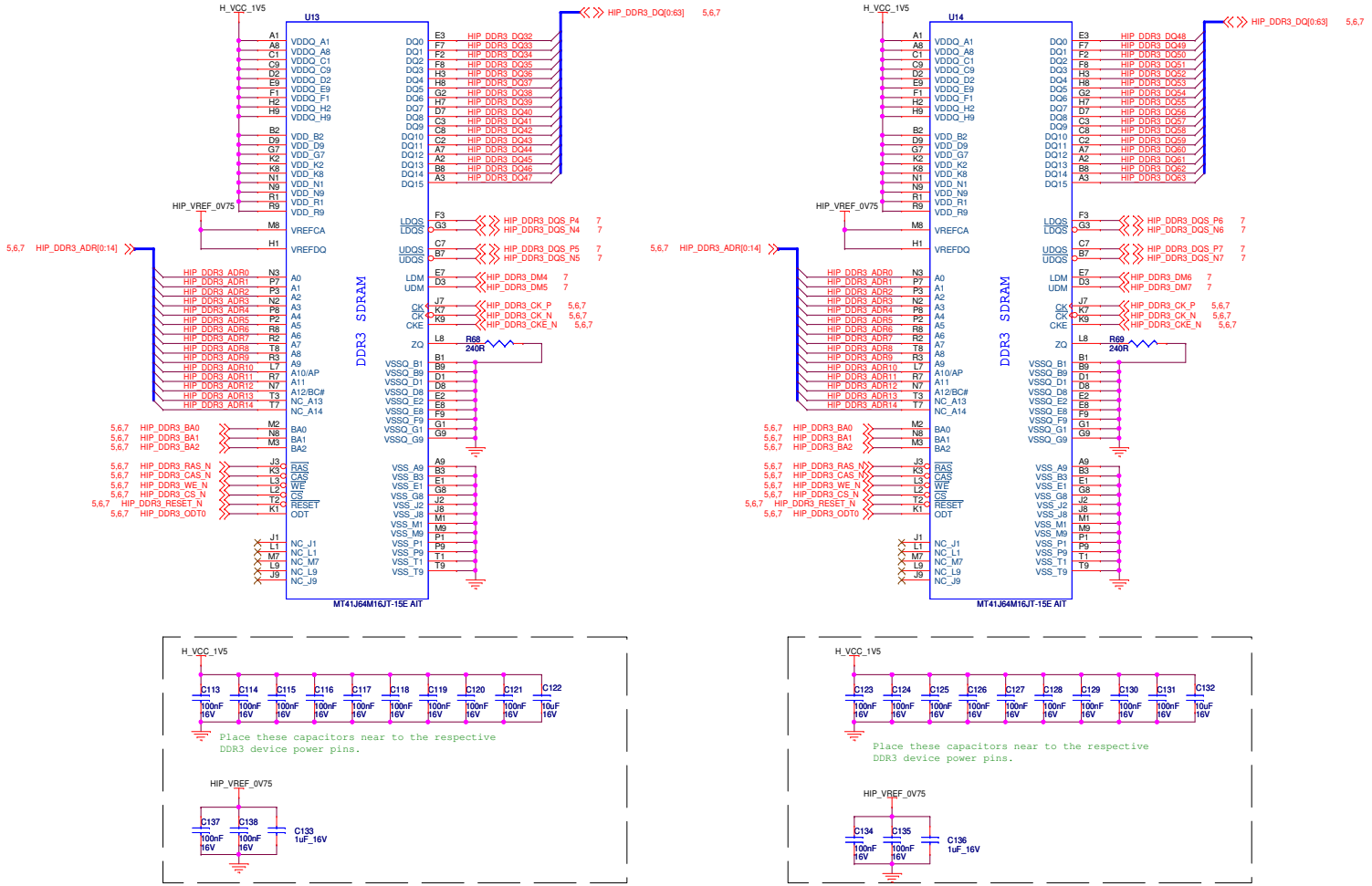
Ronanki Infotech Pvt Ltd

Title: HIP_DDR3_0-31

Size: C | Document Number: PCA | Rev: 1.0

Date: Sunday, March 22, 2015 | Sheet 5 of 46

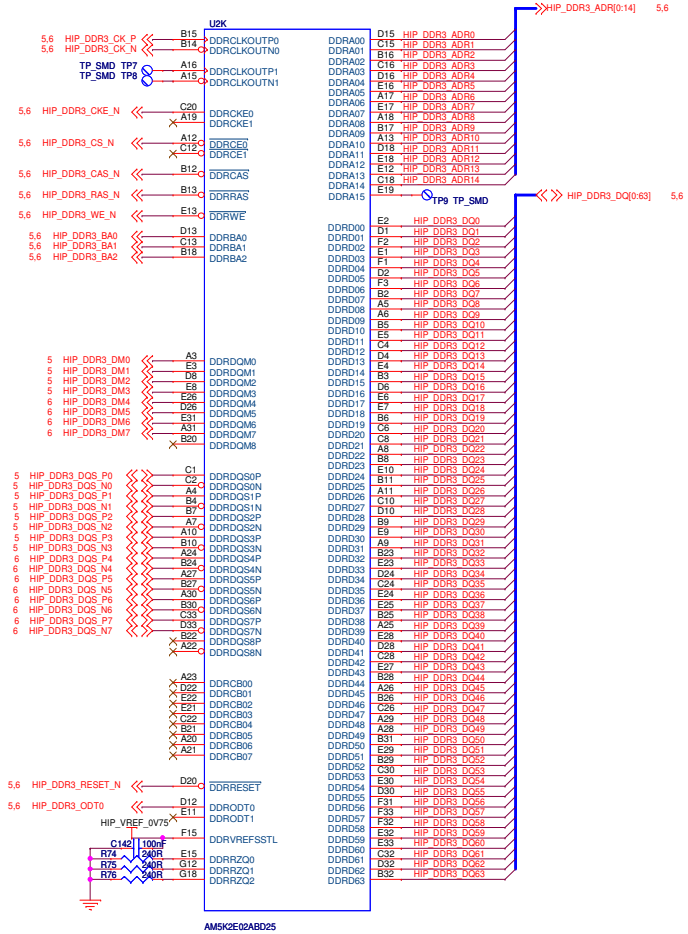
DDR3_MEMORY_HIP

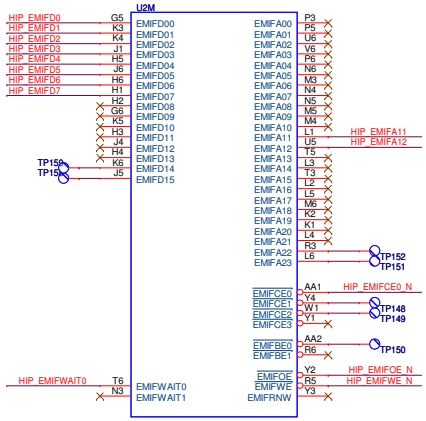


DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_DDR3_32-63
DATE		Size C	Document Number PCA
APPD BY			Rev 1.0
DATE		Date: Sunday, March 22, 2015	Sheet 6 of 46

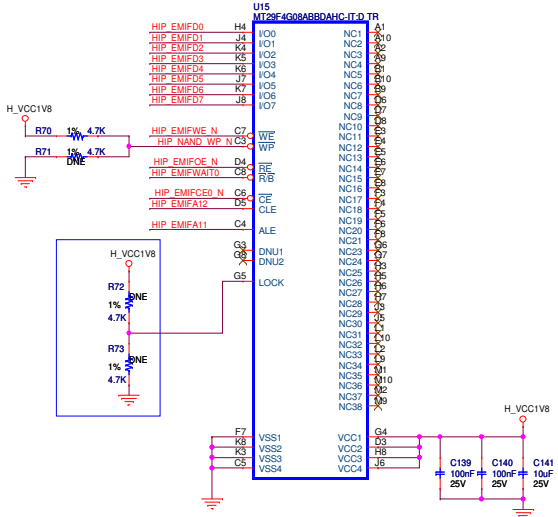
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

HIP DDR3 AND NAND INTERFACE

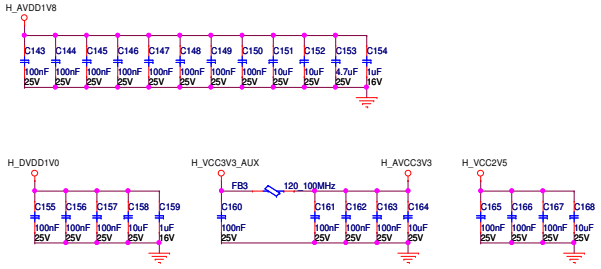




NAND FLASH



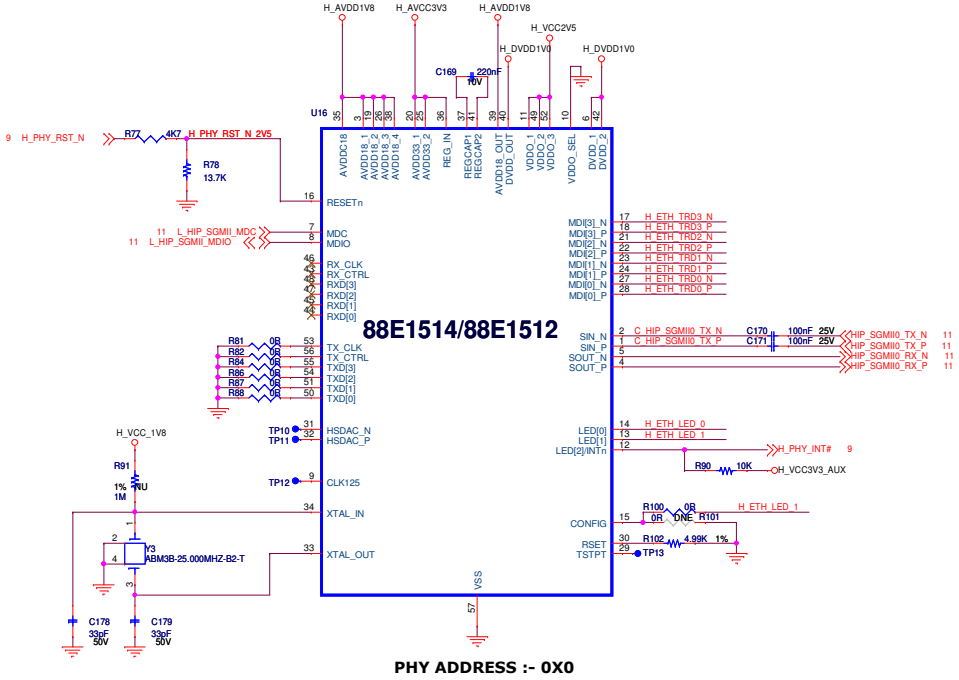
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_DDR3_NAND
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 7 of 46



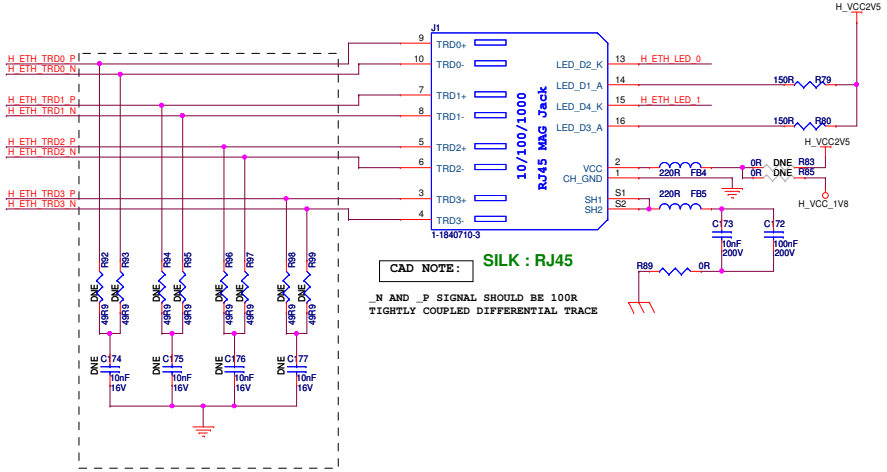
CONFIGURATION MAPPING

PIN	BIT 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

PIN	CONFIG Bit1	CONFIG Bit0	Value Assignment
CONFIG	0	0	PHY Address[0] = 0 VDDO_LEVEL = 3.3V
CONFIG	1	1	PHY Address[0] = 1 VDDO_LEVEL = 3.3V
CONFIG	1	0	PHY Address[0] = 0 VDDO_LEVEL = 2.5V
CONFIG	0	1	PHY Address[0] = 1 VDDO_LEVEL = 2.5V



PHY ADDRESS :- 0X0



DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

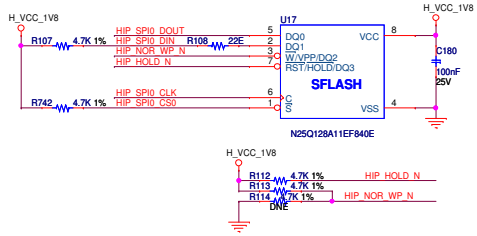
Ronanki Infotech Pvt Ltd

Title: HIP_GIG_88E1512/14

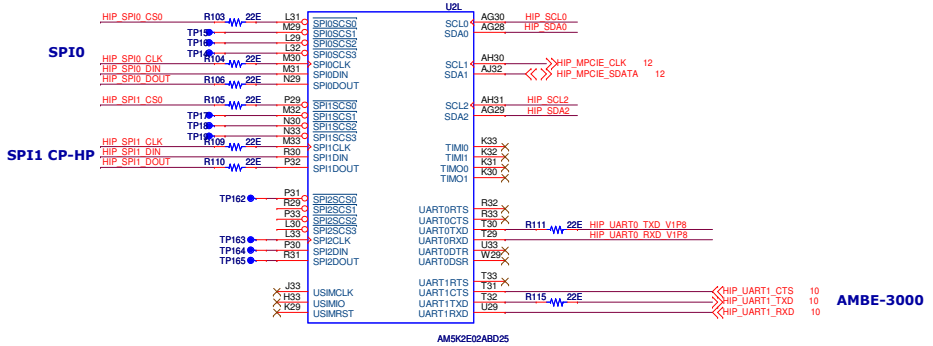
Size: C | Document Number: PCA | Rev: 1.0

Date: Sunday, March 22, 2015 | Sheet 8 of 46

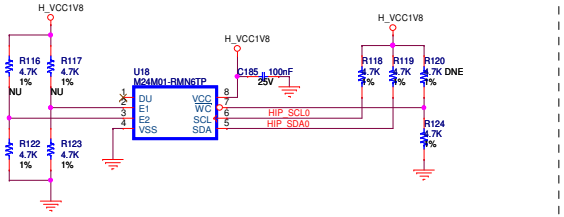
128Mb SPI NOR Flash



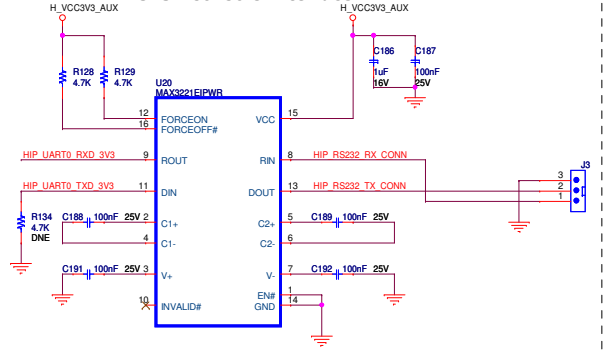
SPI0 / SPI1 CP-HP / AMBE-3000



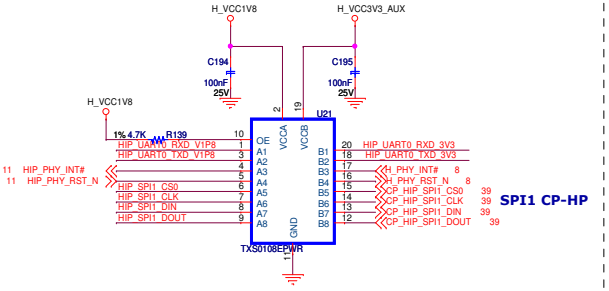
I2C EEPROM



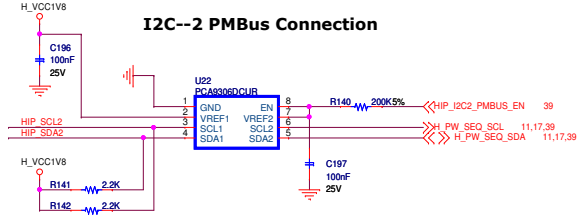
RS232 Console Interface

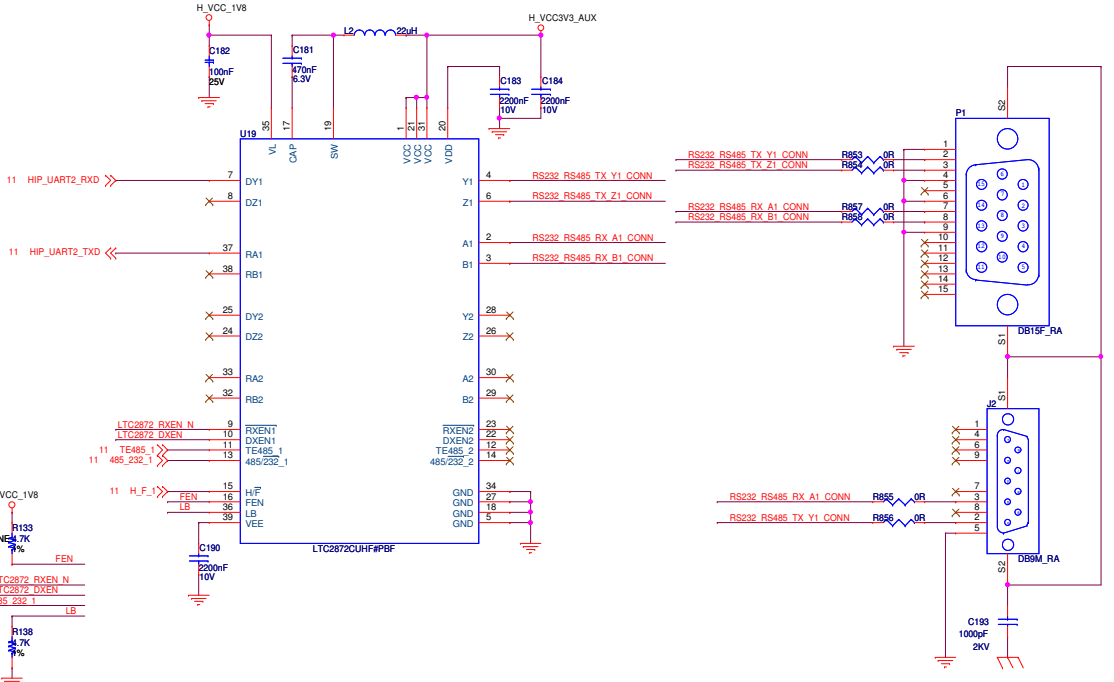


UART,SPI & MISC 1V8 to 3V3 CONVERTER



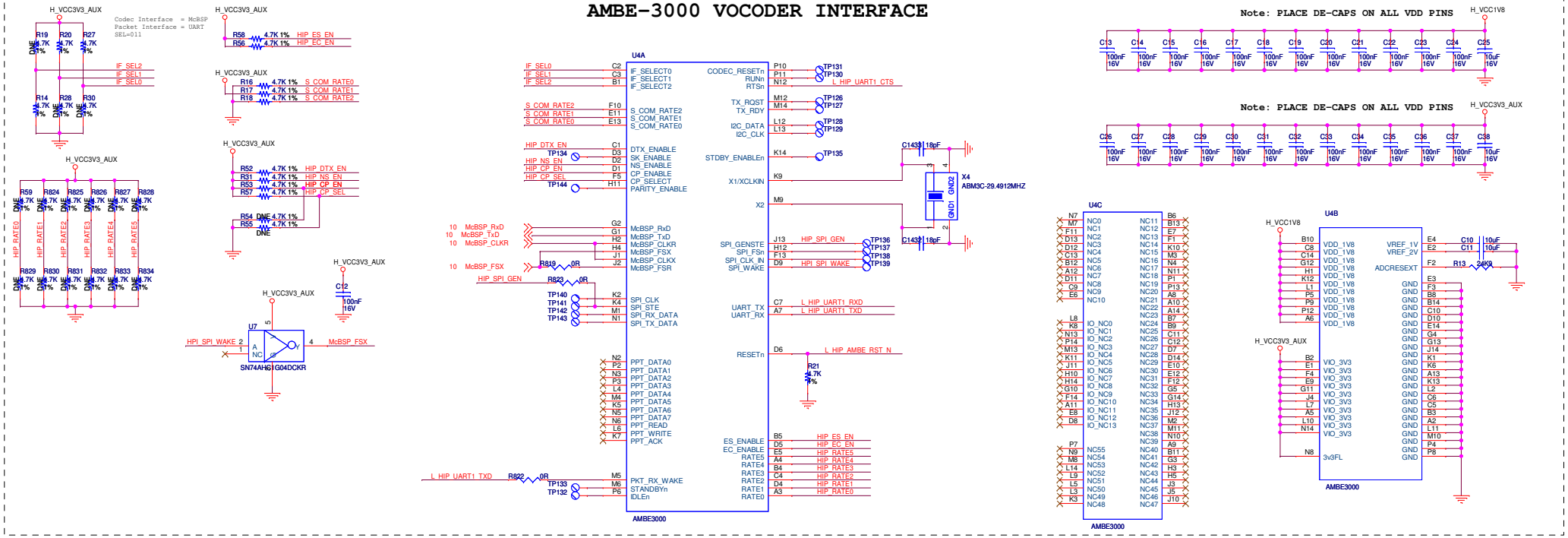
I2C--2 PMBus Connection



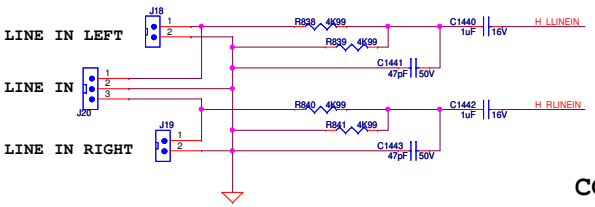


DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_NOR_EEPROM_UART_485_SPI
DATE			
APPD BY		Size C	Document Number PCA — Rev 1.0
DATE			
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 9 of 46

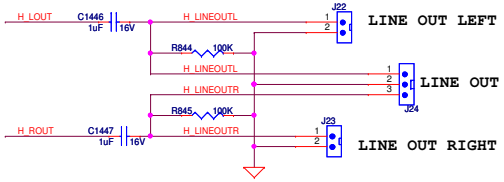
AMBE-3000 VOCODER INTERFACE



LINE IN

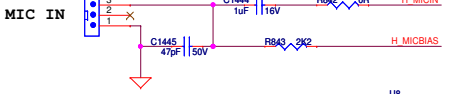


LINE OUT

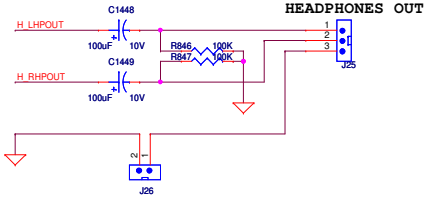


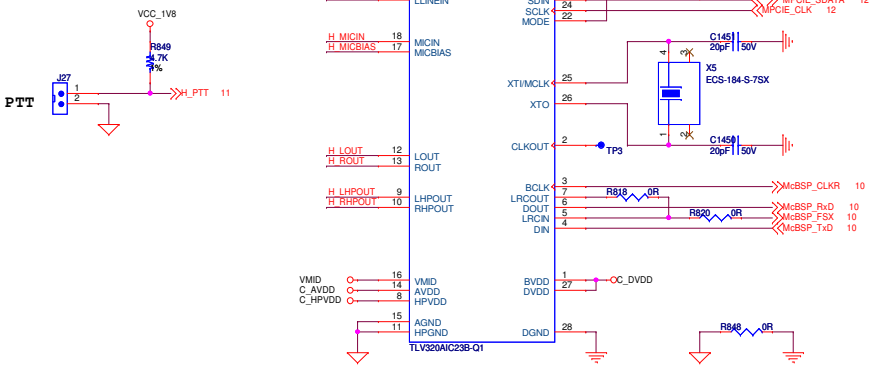
CODEC INTERFACE

MIC IN

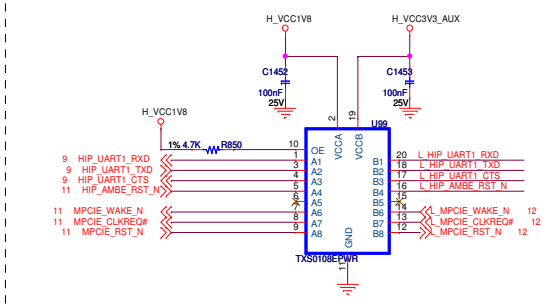


HEADPHONES OUT

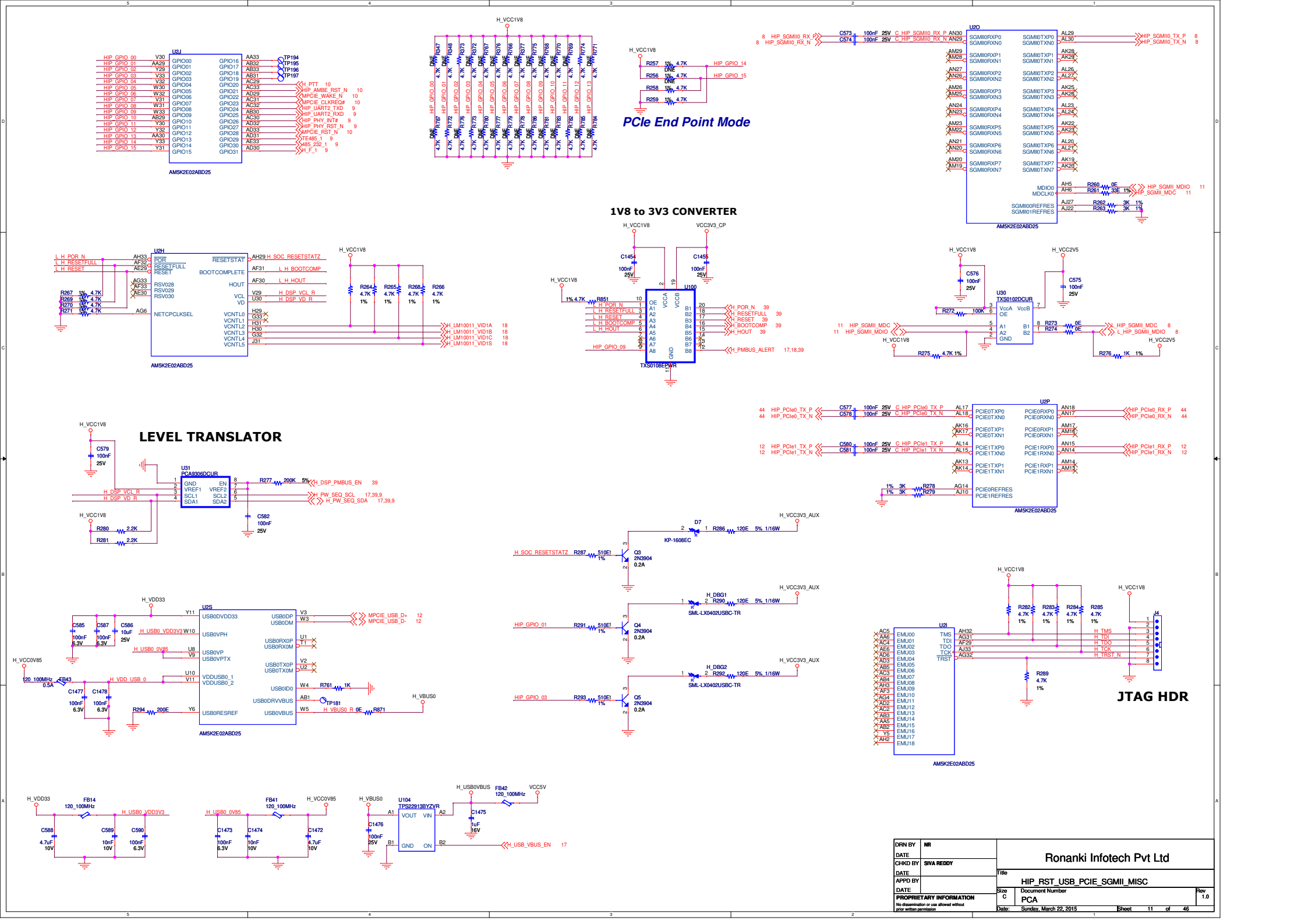




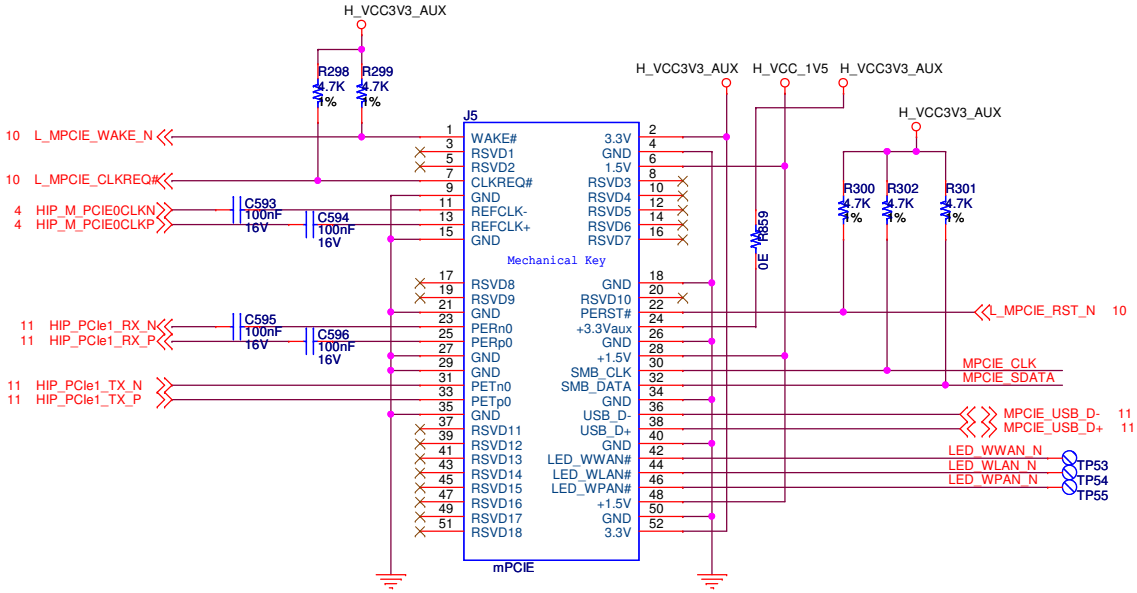
1V8 to 3V3 CONVERTER

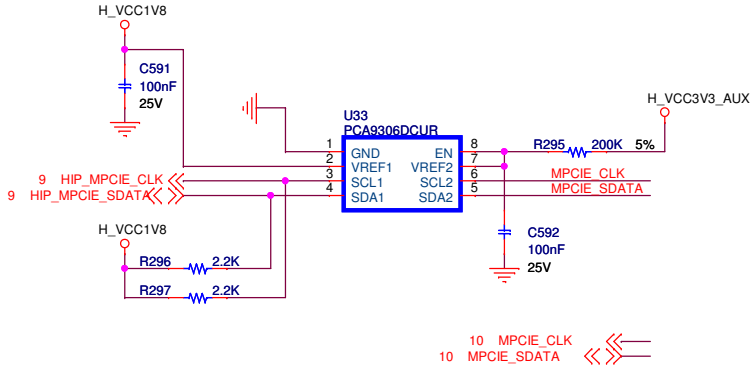


DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_AMBE3000_CODEC
DATE			
APPD BY		Size C	Document Number PCA — Rev 1.0
DATE			
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 10 of 46


PCIe End Point Mode
1V8 to 3V3 CONVERTER
LEVEL TRANSLATOR
JTAG HDR
AM5K2E02ABD25
TXS0106EPWR
TXS0102DCUR
PCA9306DCUR
KP-1608EC
SML-LX0402USBC-TR
TPS22913BYZVR
Ronanki Infotech Pvt Ltd
HIP_RST_USB_PCIE_SGMII_MISC
PCA
Sunday, March 22, 2015
PROPRIETARY INFORMATION

Mini PCIe INTERFACE





SELECT PART BASED ON MECHANICAL CONSTRAINTS

Product Selector Right angle MOLEX
SMT with pegs0.80mm (.031") pitch

Part Number	Height mm (in.)
538-48338-0040	4.00 (.157)
538-48338-0052	5.20 (.220)
538-48338-0056	5.60 (.220)
538-48338-0057	5.75 (.226)
538-48338-0065	6.50 (.256)
538-48338-0068	6.80 (.268)
538-48338-0070	7.00 (.276)
538-48338-0075	7.50 (.295)
538-48338-0080	8.00 (.315)
538-48338-0085	8.50 (.335)
538-48338-0099	9.90 (.390)

DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

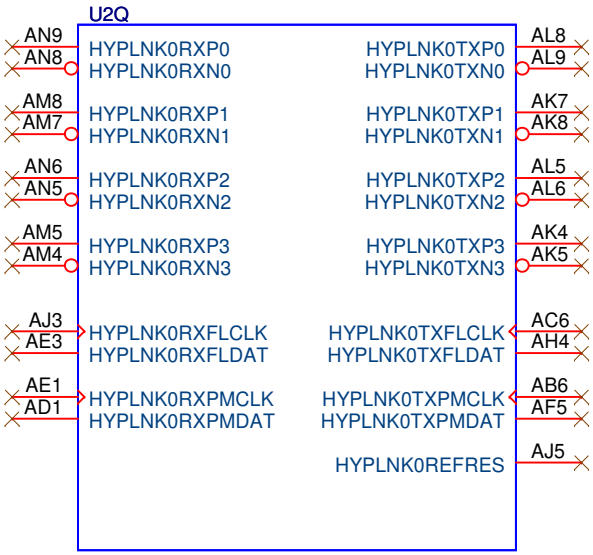
Ronanki Infotech Pvt Ltd

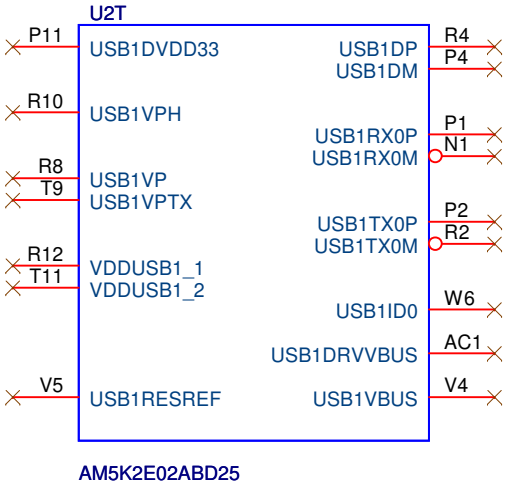
Title: HP_MINI_PCIE

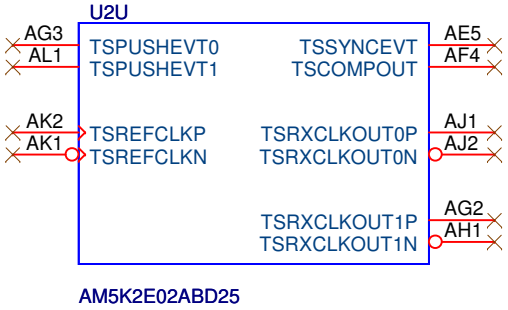
Size: B | Document Number: PCA | Rev: 1.0

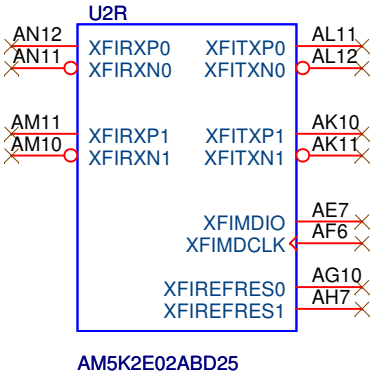
Date: Sunday, March 22, 2015 | Sheet 12 of 46

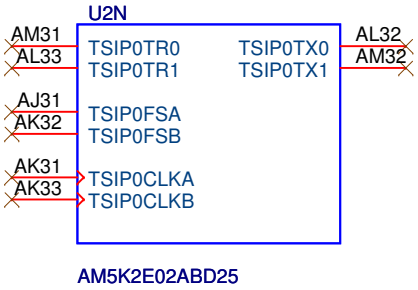
UNUSED











DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

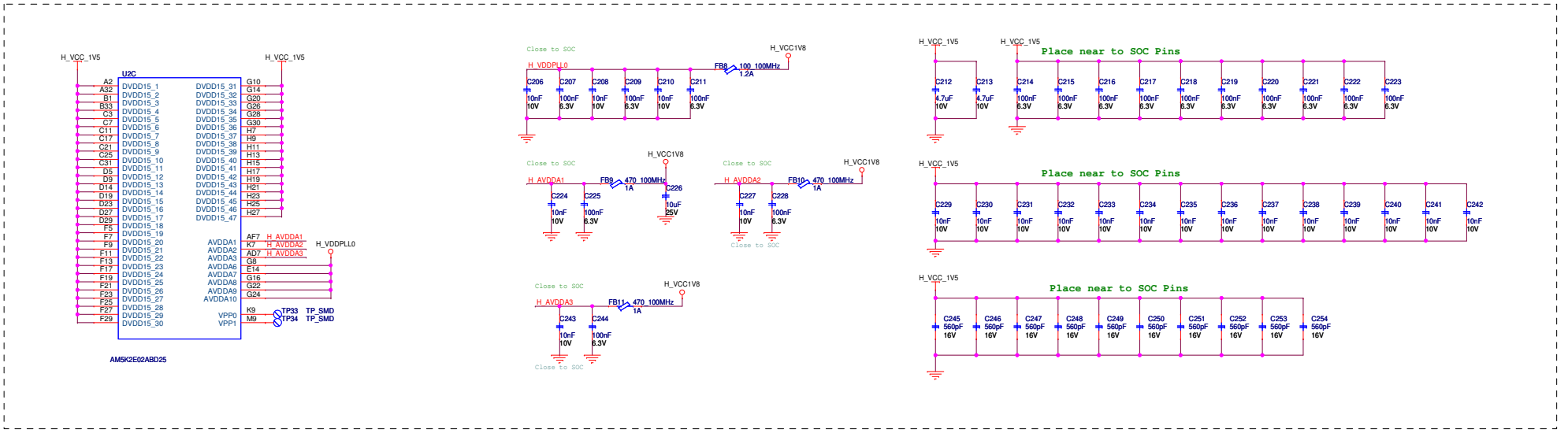
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

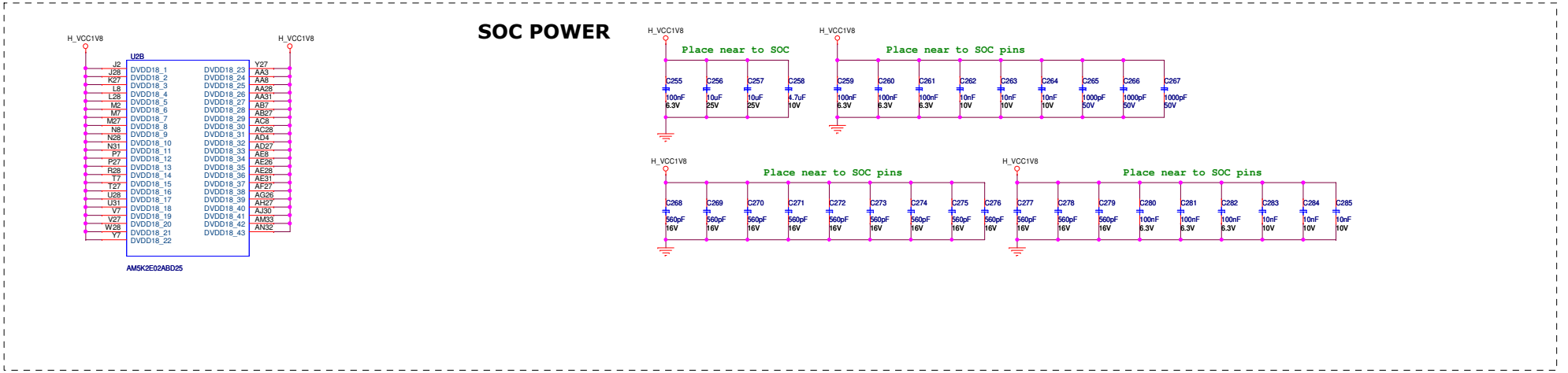
Ronanki Infotech Pvt Ltd

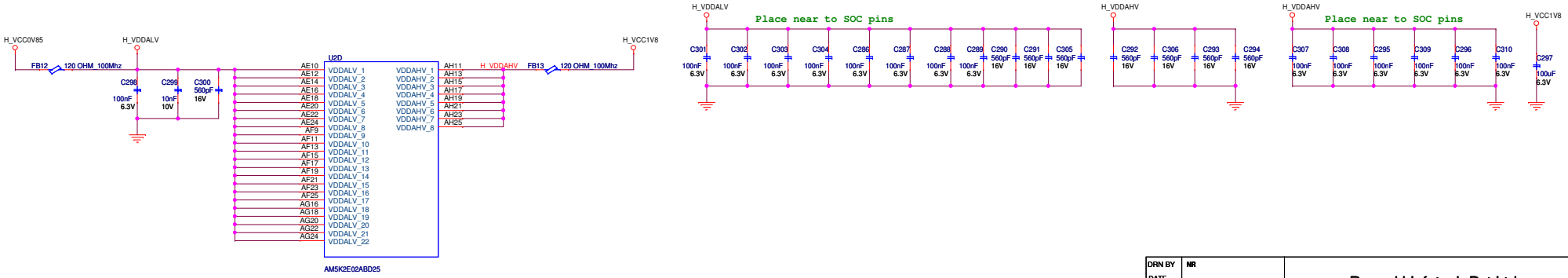
Title: HIP_UNUSED

Size	Document Number	Rev
A	PCA	1.0

Date: Sunday, March 22, 2015 Sheet 13 of 46



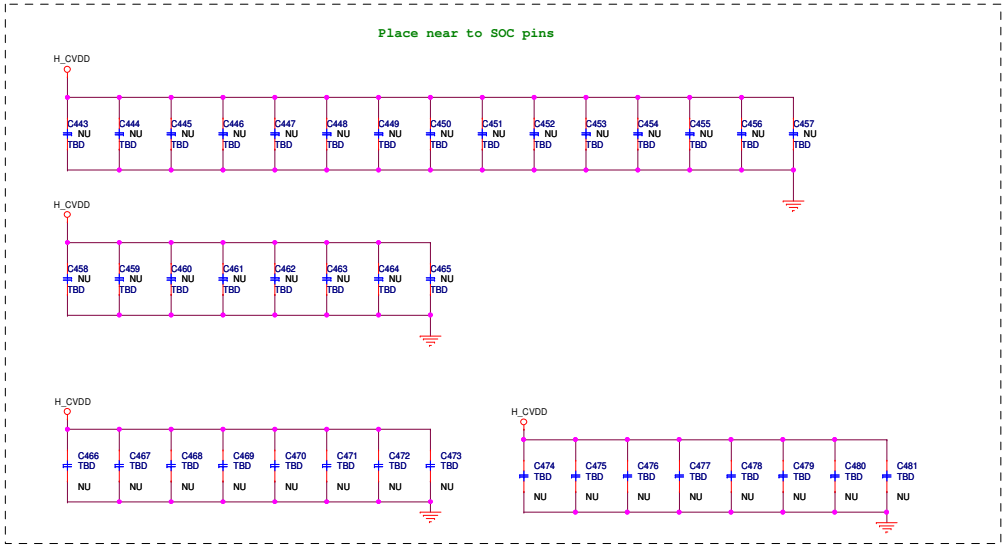




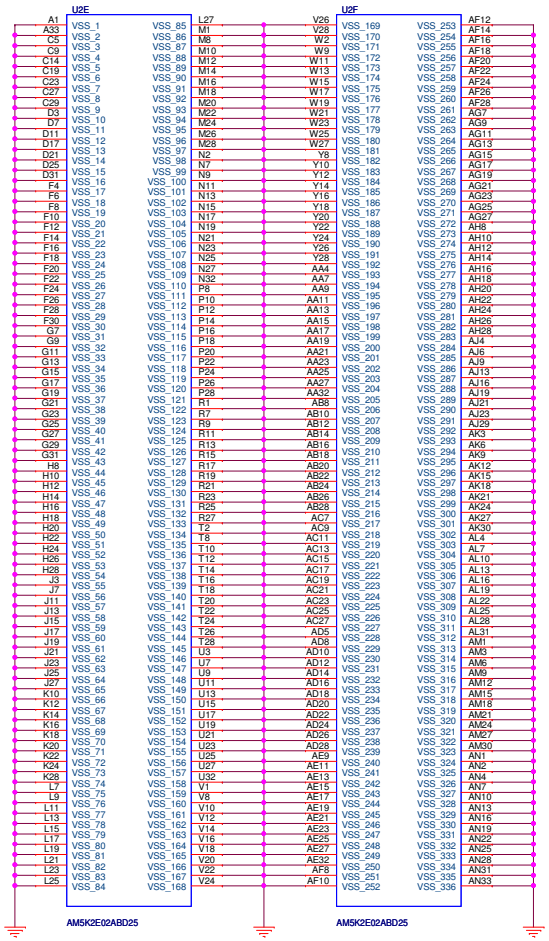
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_POWERA
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 14 of 46

0.85V - 1.05V (CVDD) (Smart Reflex)

SOC POWER

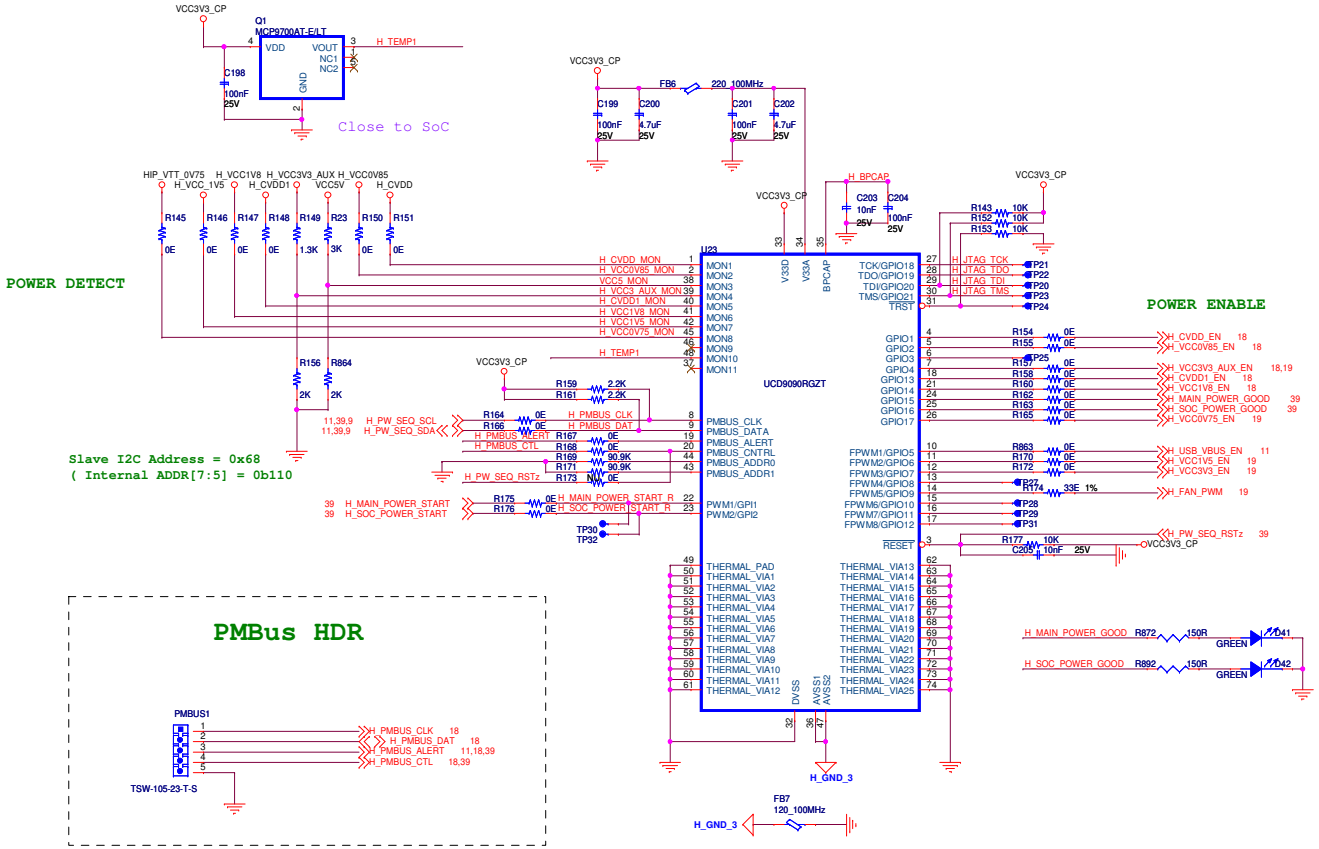


DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_POWERB
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 15 of 46



DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_PWR GND
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 16 of 46

Power Sequencing (UCD9090)



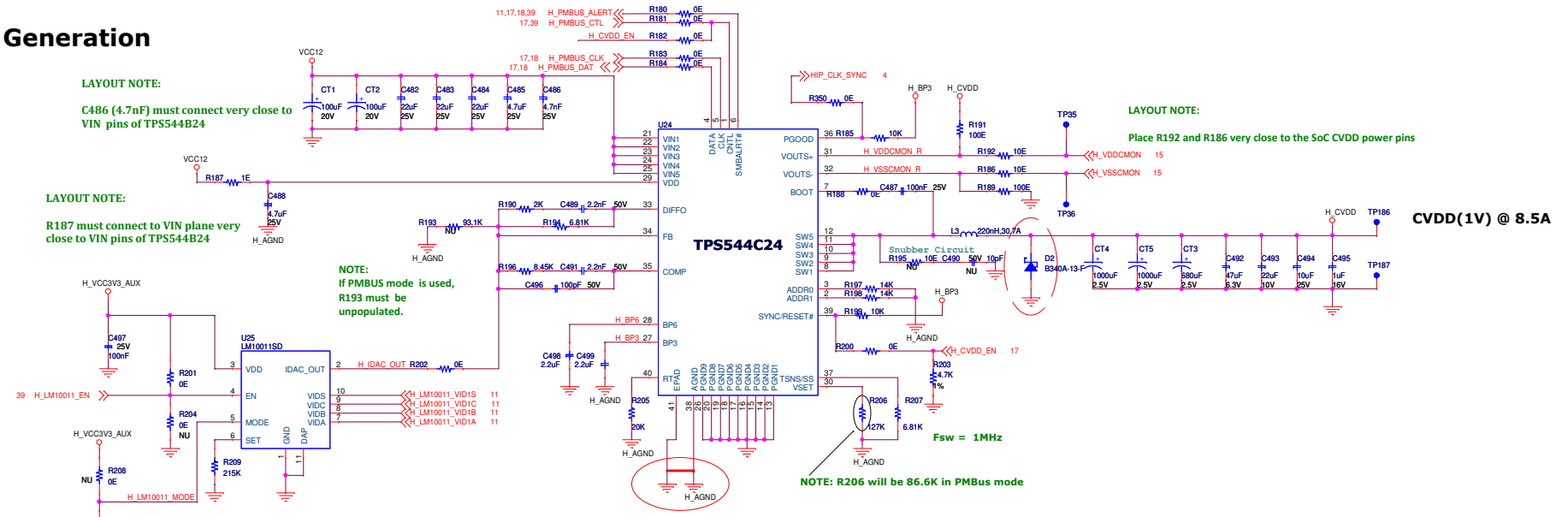
PMBus Address Pins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

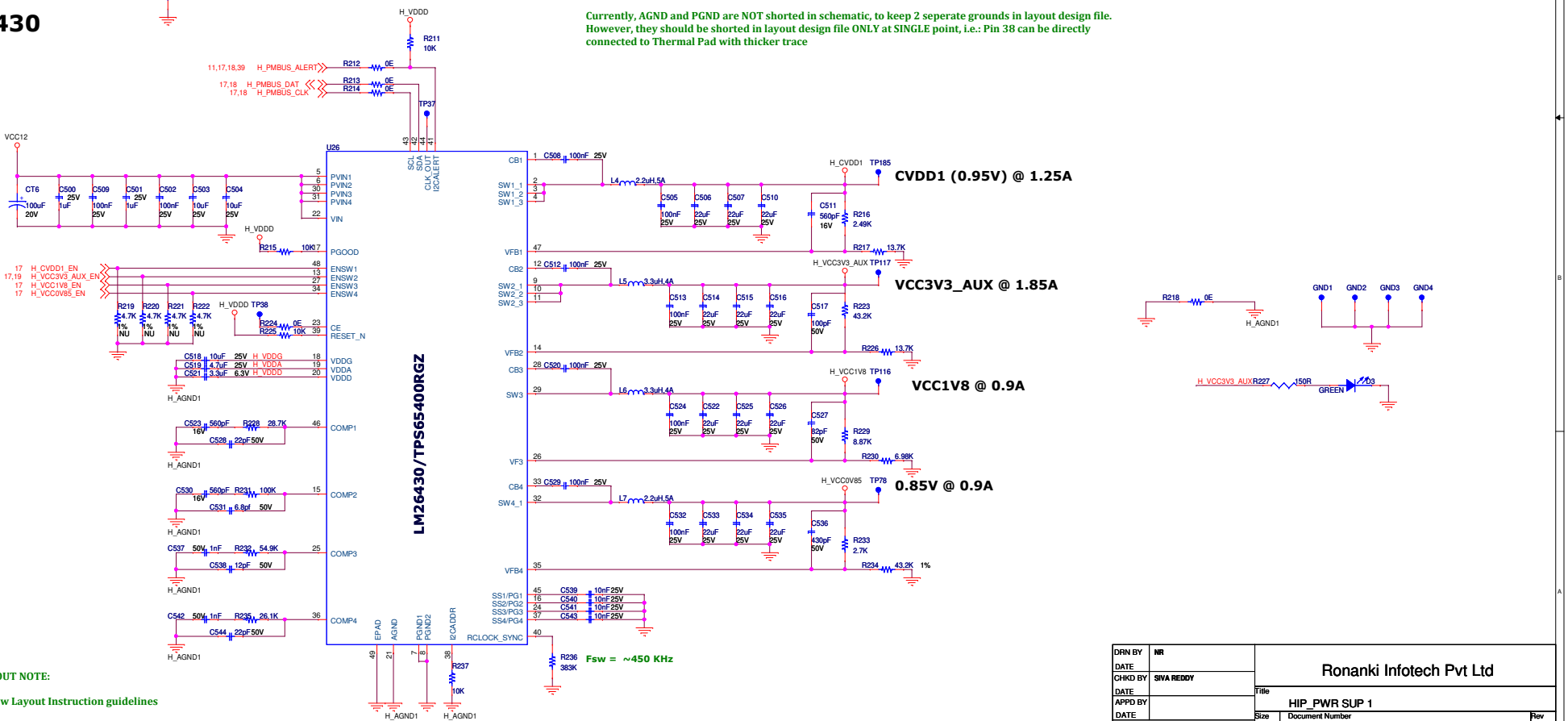
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_POWER_SEQ
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 17 of 46

No dissemination or use allowed without prior written permission

12V to CVDD Generation

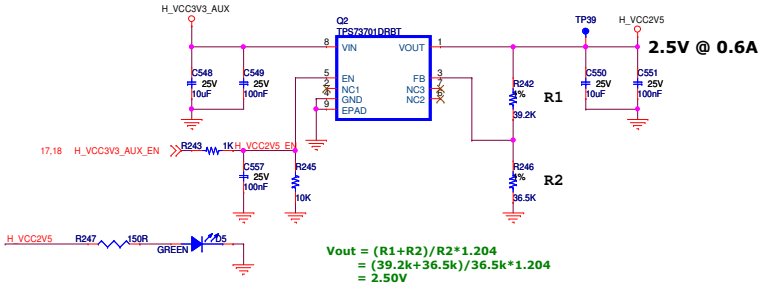


LM26430



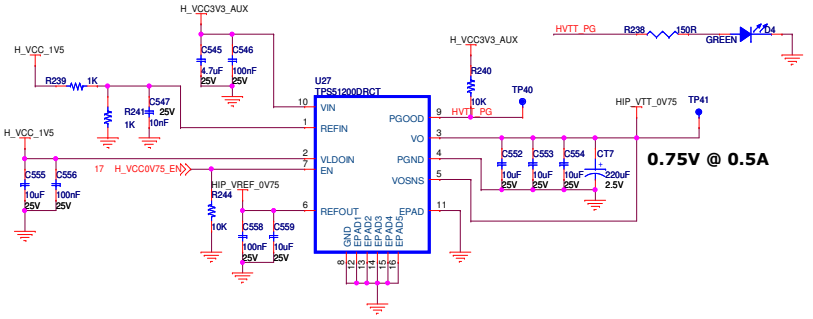
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	HIP_PWR SUP 1
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 18 of 46

3.3V_AUX to 2.5V Generation



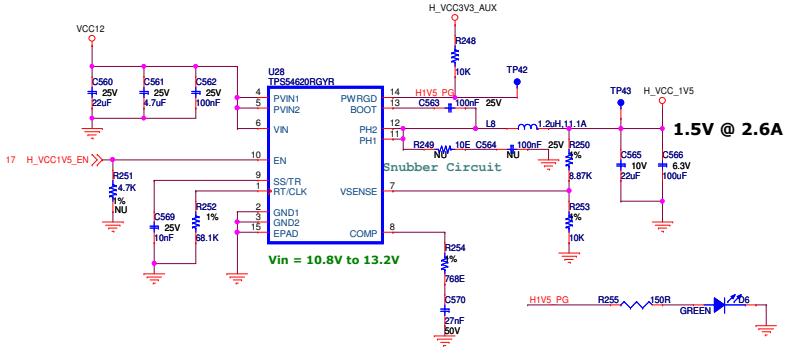
Vout = (R1+R2)/R2*1.204
= (39.2k+36.5k)/36.5k*1.204
= 2.50V

1.5V to 0.75V Generation



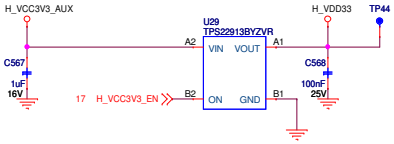
Place near DDR3 VTT Terminations

12V to 1.5V Generation



Vin = 10.8V to 13.2V

3V3_AUX to VDD33 Generation



VOUT = 0.8 * (R1/R2 + 1)
= 0.8 * (8.87/10 + 1)
= ~1.5V

Rrt=48000 * Fsw(kHz)^(-0.997) - 2
=48000 * 700^(-0.997) - 2
=~68 Kohms

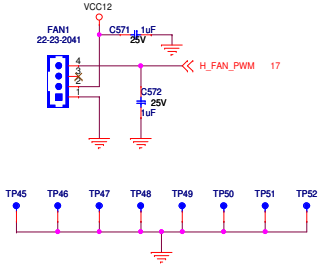
OUTPUT CAPACITOR CALCULATION
Cout= 2 * delta(Iout) / (Fsw*delta(Vout)
= 2 * 1 / (700kHz*0.125)
= ~38uF

REFERENCE CAPACITOR = 100uF

INDUCTOR CALCULATION
L= (Vin - Vout)/(Iout * Kind) *(Vout / (Vin * Fsw))
= (12 - 1.5)/(4.5 * 0.3) * (1.5 / (12 * 700KHz))
= 7.78 * 0.18u
= ~ 1.38uH

REFERENCE CAPACITOR = 1.2uH

DC FAN Connector for SOC



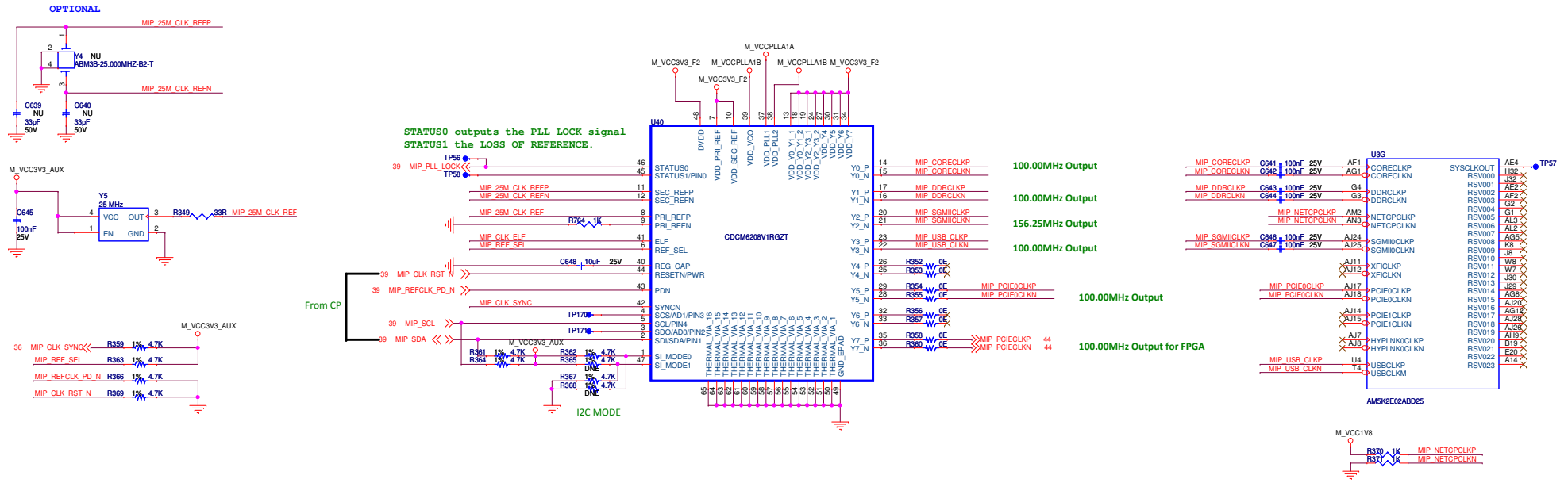
Distribute these TP in board

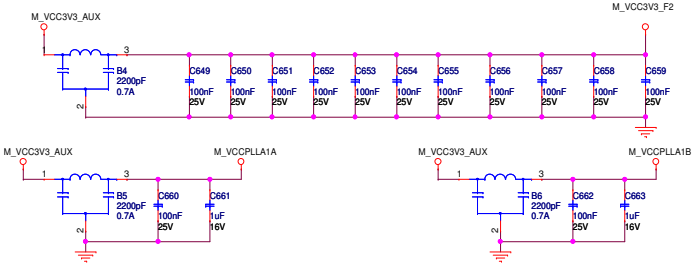
DRN BY	NR	Ronanki Infotech Pvt Ltd
DATE		
CHKD BY	SIVA REDDY	Title: HIP_PWR SUP 2
DATE		
APPD BY		Size: C — Document Number: PCA — Rev: 1.0
DATE		

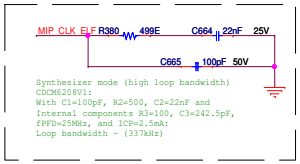
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

Date: Sunday, March 22, 2015 Sheet 19 of 46

MIP CLOCK SOURCE







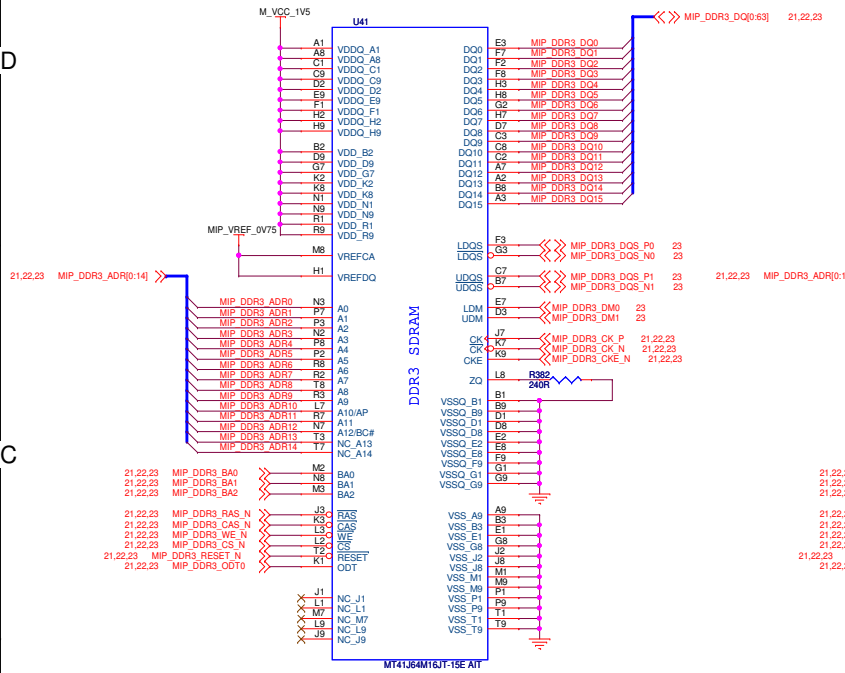
Serial Interface Mode or Pin Mode Selection

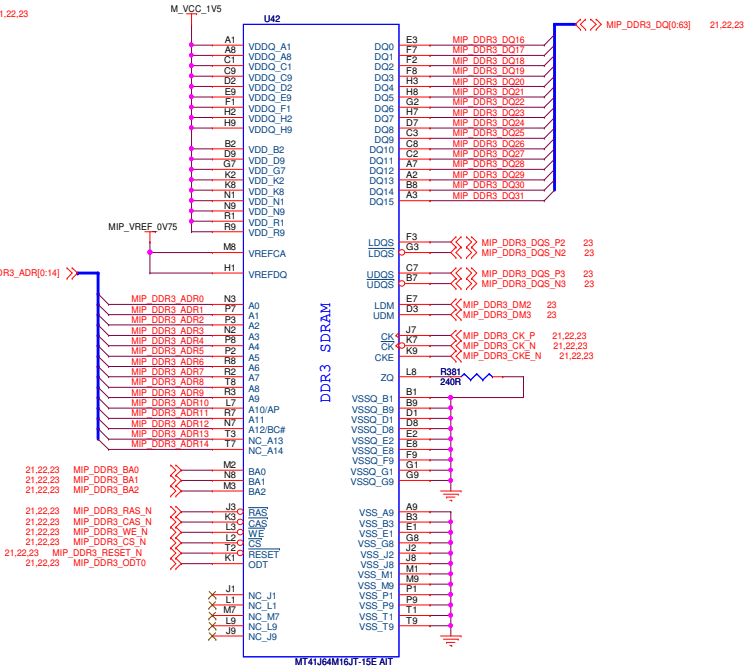
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

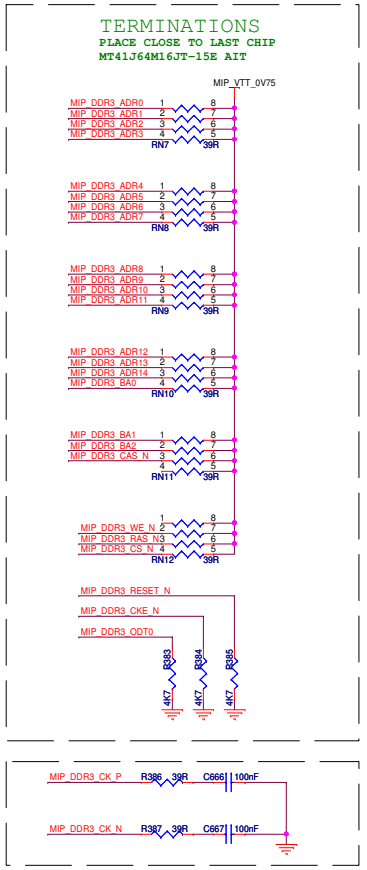
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_CLK
DATE		Size C	Document Number PCA
APPD BY			Rev 1.0
DATE		Date: Sunday, March 22, 2015	Sheet 20 of 46

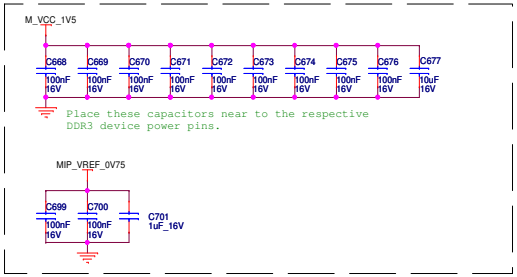
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

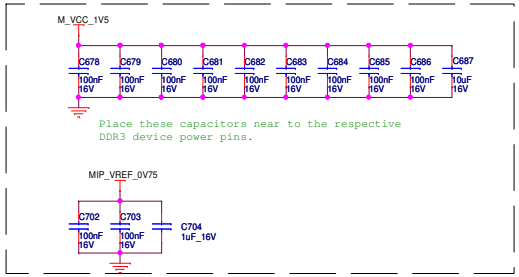
DDR3_MEMORY_MIP

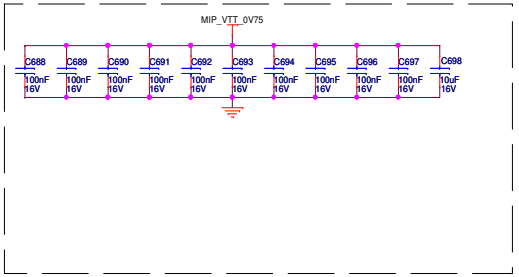












DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

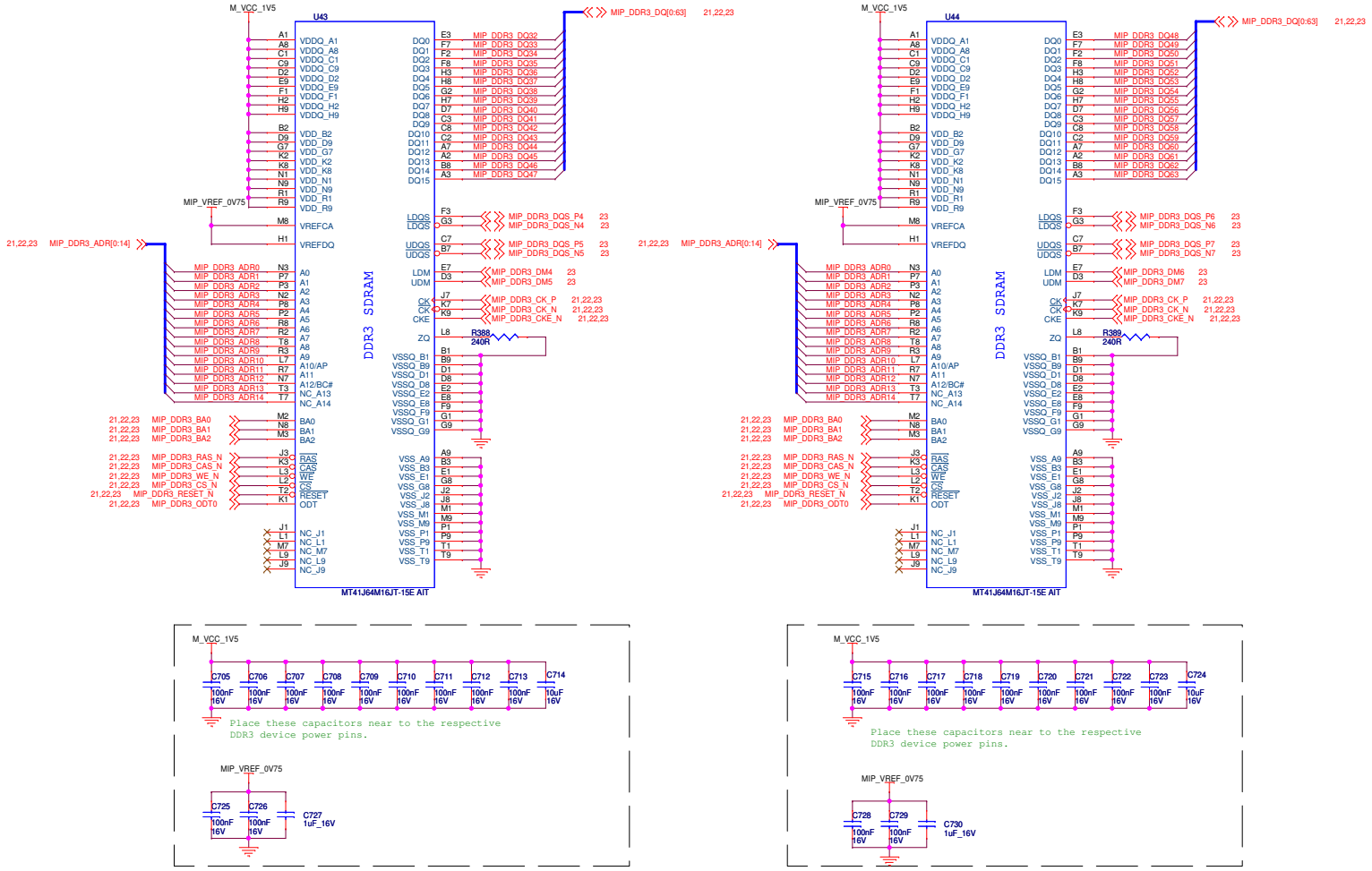
Ronanki Infotech Pvt Ltd

Title: MIP_DDR3_0-31

Size: C | Document Number: PCA | Rev: 1.0

Date: Sunday, March 22, 2015 | Sheet 21 of 46

DDR3_MEMORY_MIP



DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

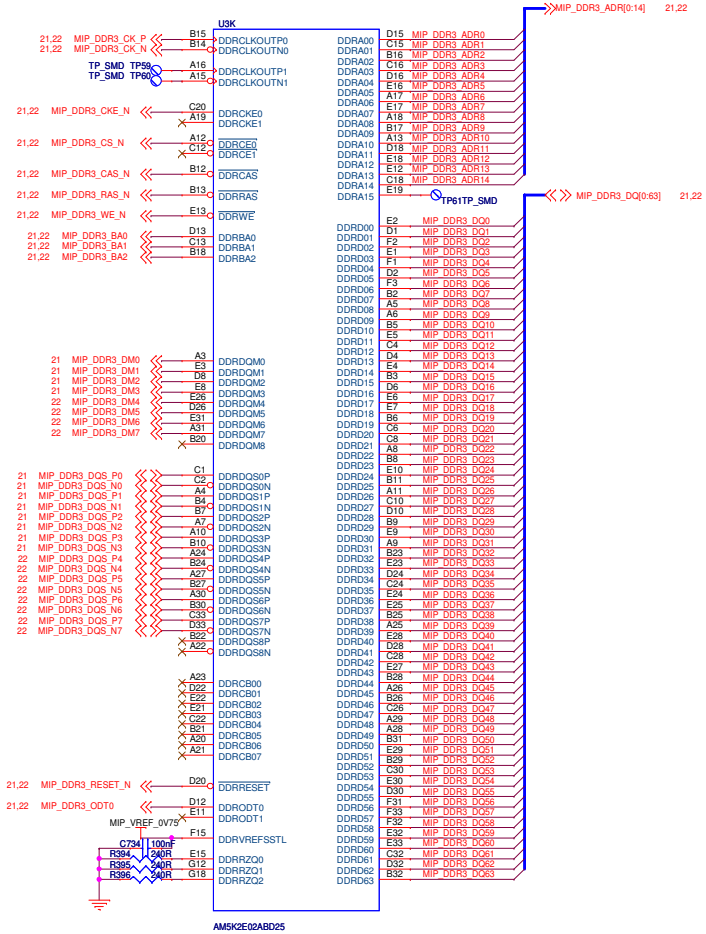
Ronanki Infotech Pvt Ltd

Title: MIP_DDR3_32-63

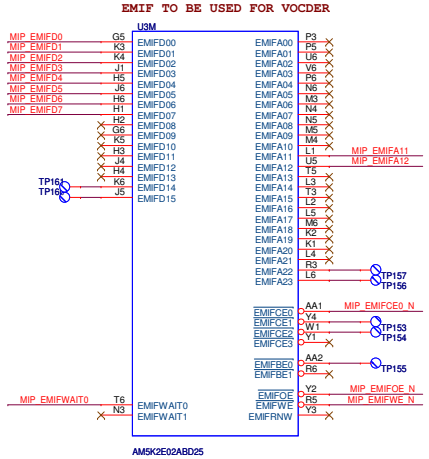
Size: C | Document Number: PCA | Rev: 1.0

Date: Sunday, March 22, 2015 | Sheet 22 of 46

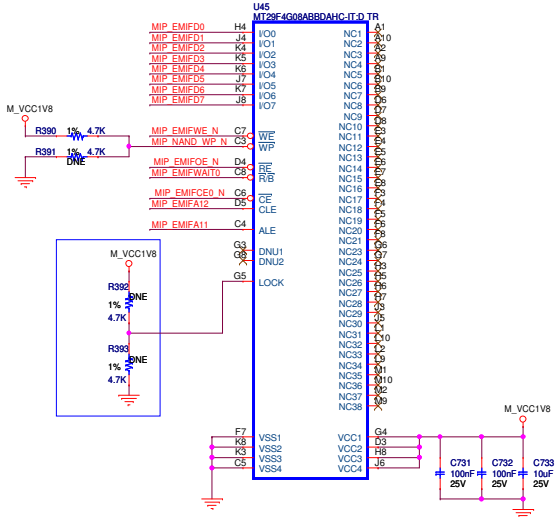
MIP DDR3 AND NAND INTERFACE



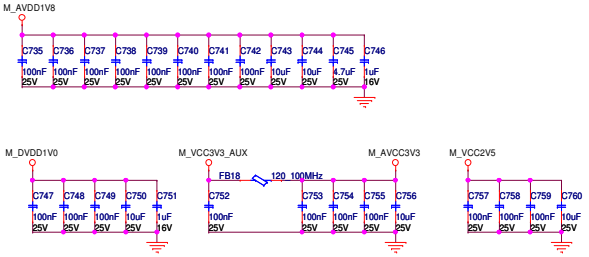
EMIF TO BE USED FOR VOCDER



NAND FLASH



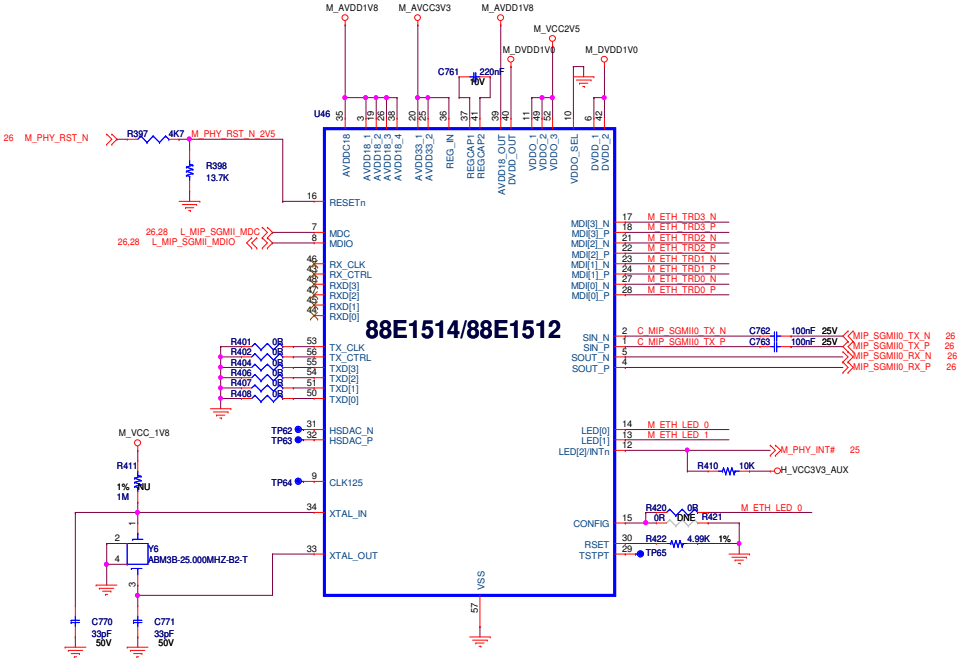
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_DDR3_NAND
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 23 of 46



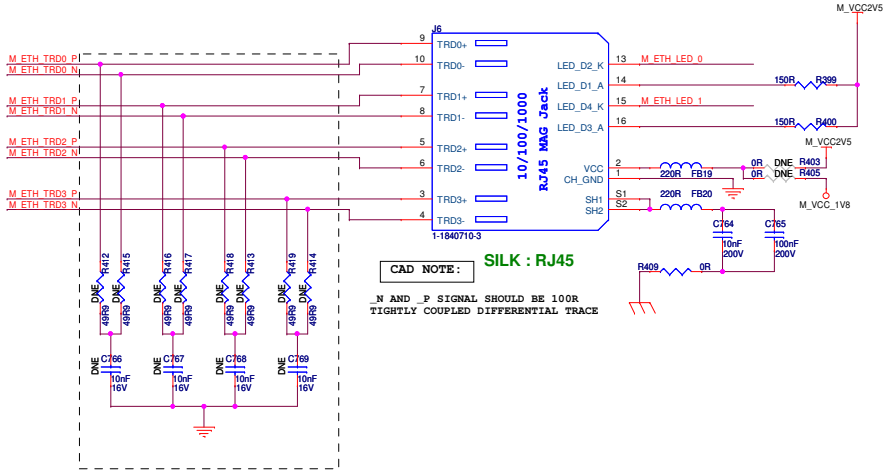
CONFIGURATION MAPPING

PIN	BIT 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

PIN	CONFIG Bit1	CONFIG Bit0	Value Assignment
CONFIG	0	0	PHY Address[0] = 0 VDDO_LEVEL = 3.3V
CONFIG	1	1	PHY Address[0] = 1 VDDO_LEVEL = 3.3V
CONFIG	1	0	PHY Address[0] = 0 VDDO_LEVEL = 2.5V
CONFIG	0	1	PHY Address[0] = 1 VDDO_LEVEL = 2.5V



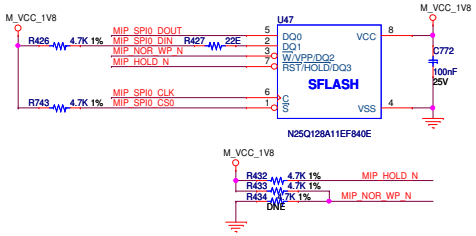
PHY ADDRESS :- 0X1



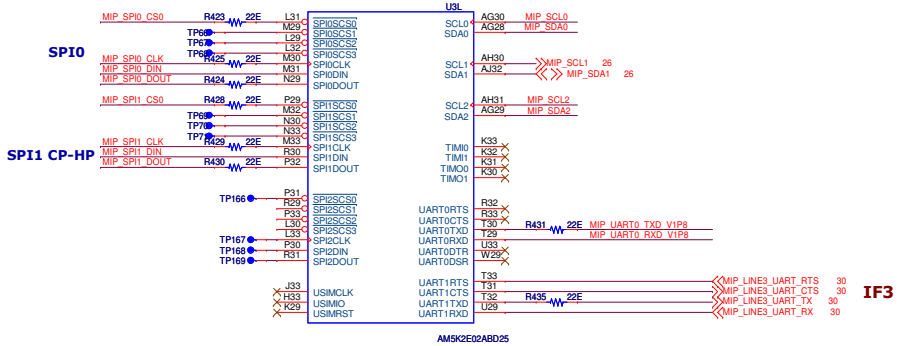
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_GIG_88E1512/14
DATE		Size C	Document Number PCA
APPD BY			Rev 1.0
DATE		Date: Sunday, March 22, 2015	Sheet 24 of 46

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

128Mb SPI NOR Flash

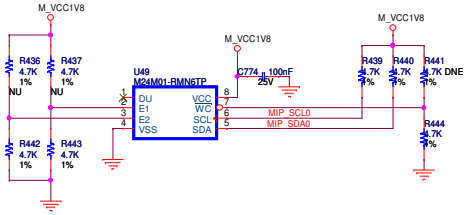


SPI0 / SPI1 CP-HP

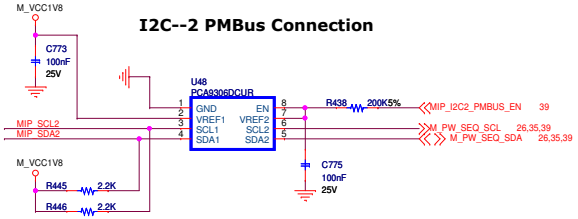


IF3

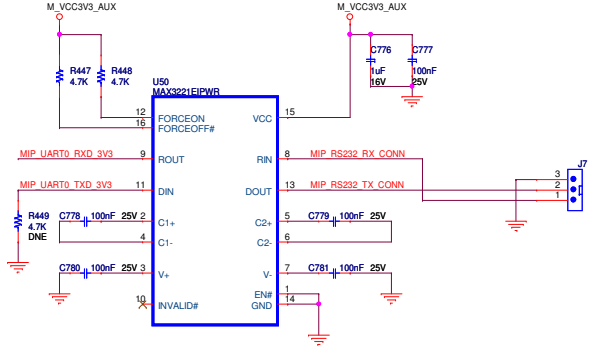
I2C EEPROM



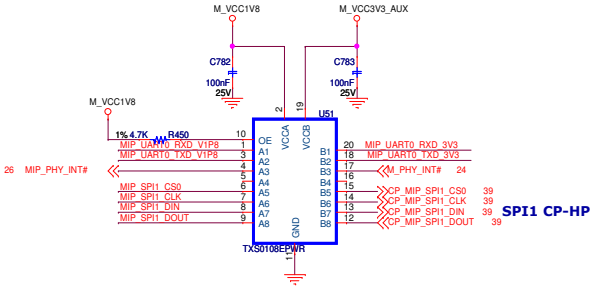
I2C--2 PMBus Connection



RS232 Console Interface

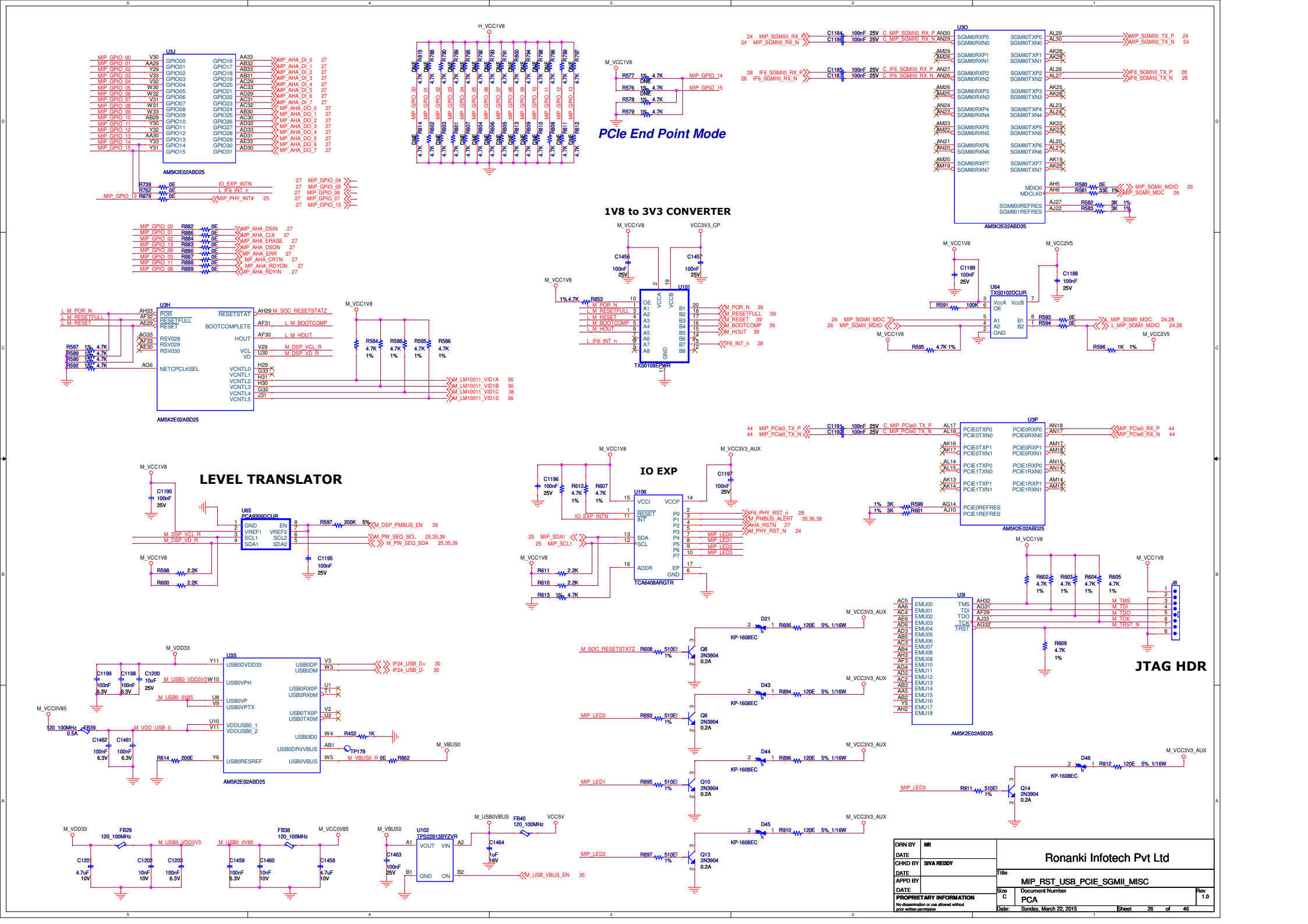


UART 1V8 to 3V3 CONVERTER

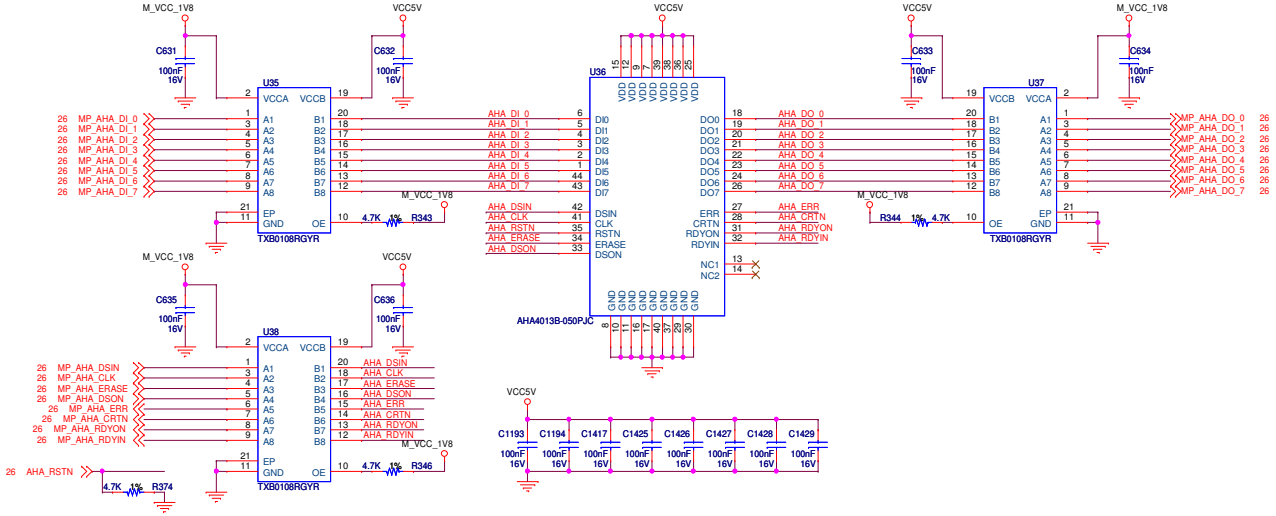


SPI1 CP-HP

DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_NOR_EEPROM_UART_SPI
DATE			
APPD BY		Size C	Document Number PCA — Rev 1.0
DATE			
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 25 of 46

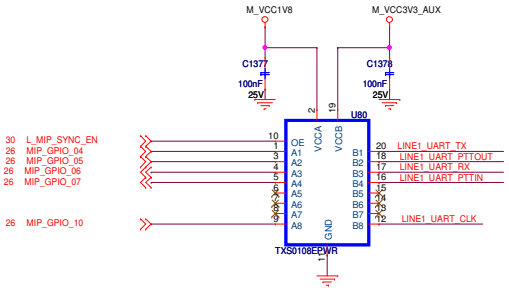

PCIe End Point Mode
1V8 to 3V3 CONVERTER
LEVEL TRANSLATOR
IO EXP
JTAG HDR
U3J
AM5K2E02ABD25
U3O
U3H
U3P
U3I
U3S
U65
PCA9306DCUR
U106
TCA6408ARGTR
U101
TXS0108EPWR
U64
TXS0102DCUR
U102
TPS22913BYZVR
KP-1608EC
2N3904
Ronanki Infotech Pvt Ltd
MIP_RST_USB_PCIE_SGMII_MISC
PCA
Sunday, March 22, 2015
Sheet 26 of 46

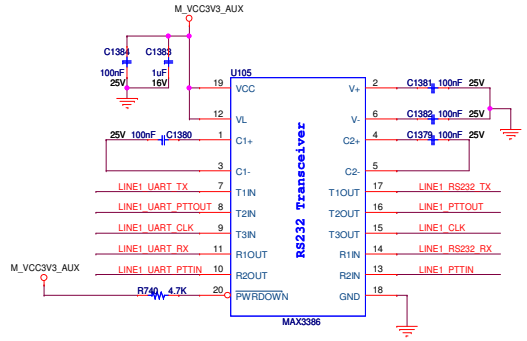
AHA4013B INTERFACE



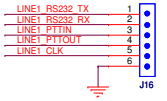
SYNC I/F-1 FOR RADIO 1

UART 1V8 to 3V3 CONVERTER



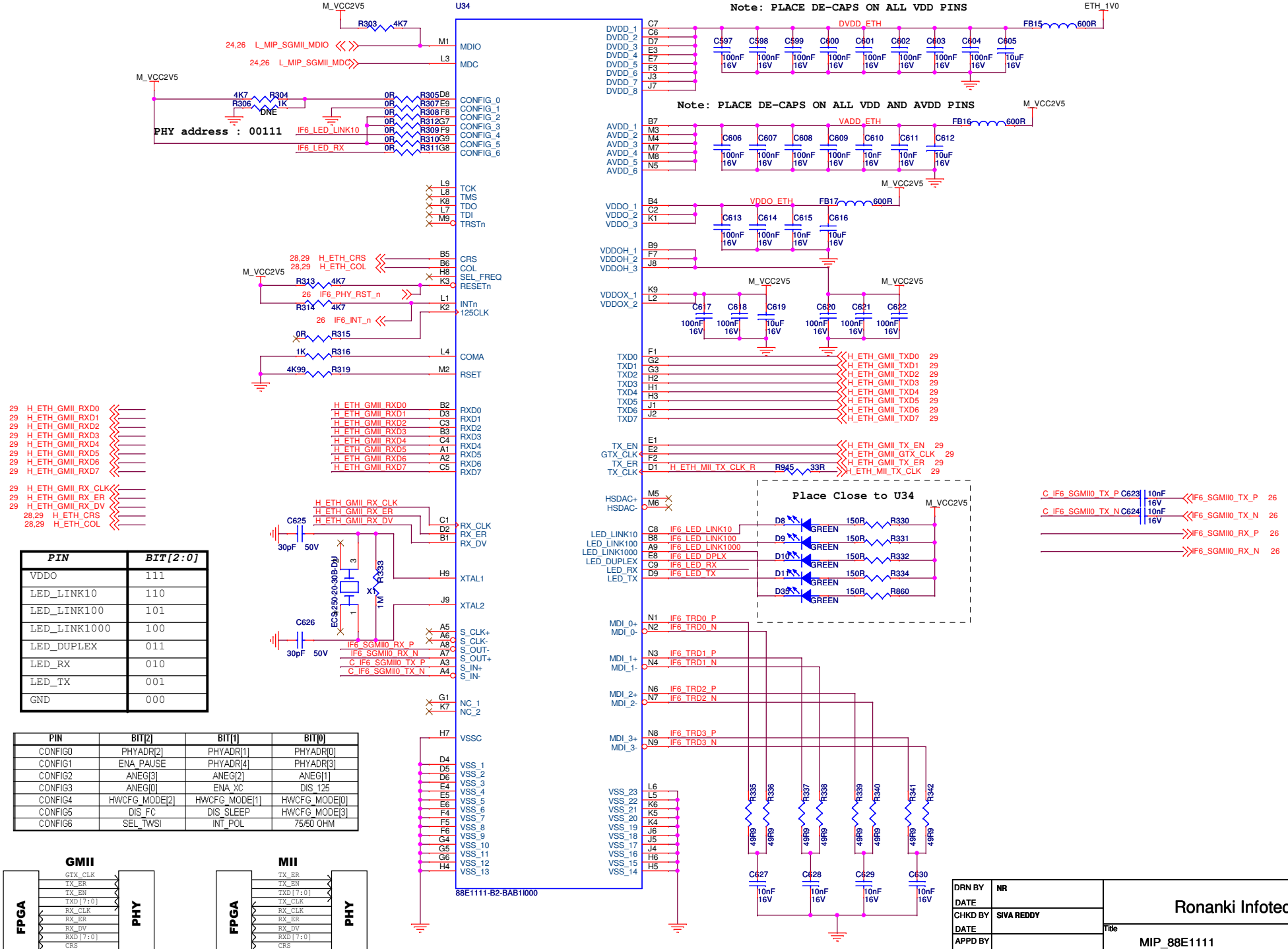


SYNC I/F-1 FOR RADIO 1



DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_AHA4013B_RIF_1
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 27 of 46

MII TO SGMII INTERFACE

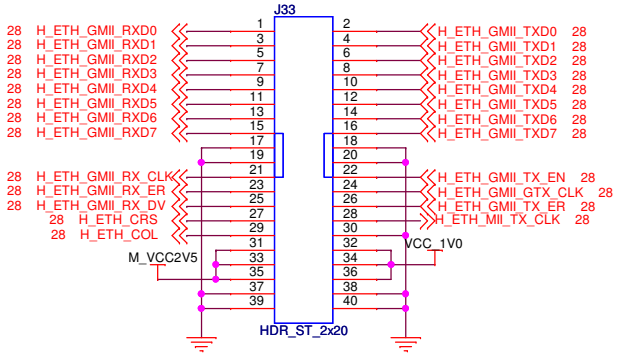


PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

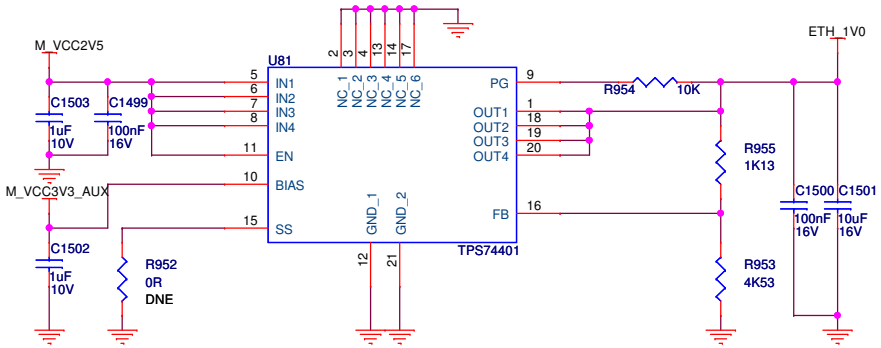
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	
DATE		MIP_88E1111	
APPD BY		Size A3	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 28 of 46
No dissemination or use allowed without prior written permission			

SHDSL HEADER INTERFACE



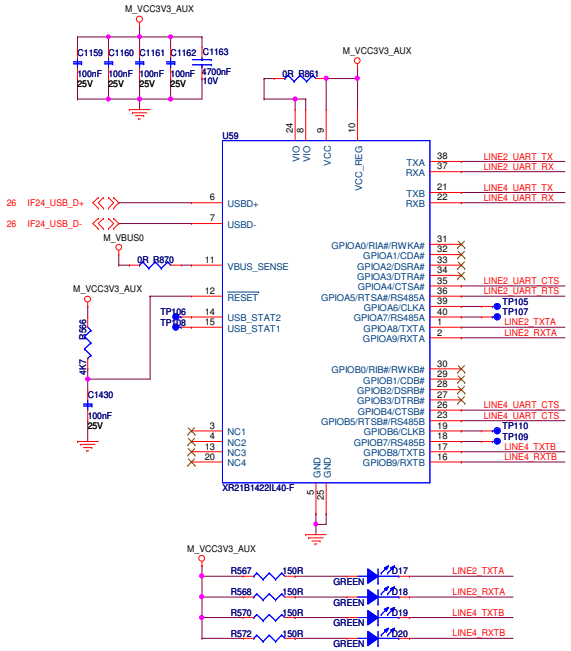
1V0 GENERATION FOR 88E1111

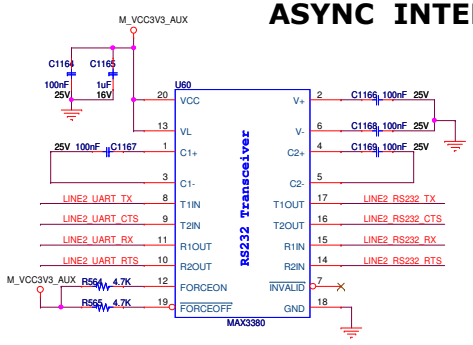


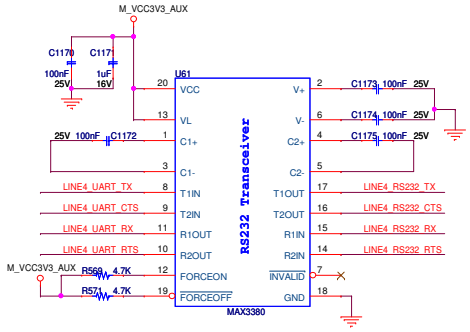
Vout=0.8X(1+R1/R2)

DRN BY	NR	Ronanki Infotech Pvt Ltd
DATE		
CHKD BY	SIVA REDDY	Title: MIP_SHDSL
DATE		
APPD BY		Size: B — Document Number: PCA — Rev: 1.0
DATE		
PROPRIETARY INFORMATION No dissemination or use allowed without prior written permission		Date: Sunday, March 22, 2015 — Sheet 29 of 46

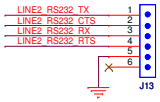
ASYNC INTERFACE



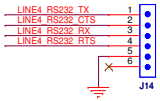




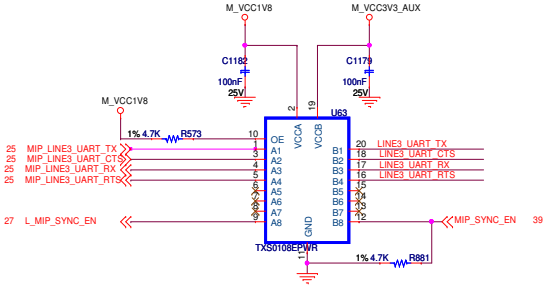
ASYNC I/F-2 FOR RADIO 1

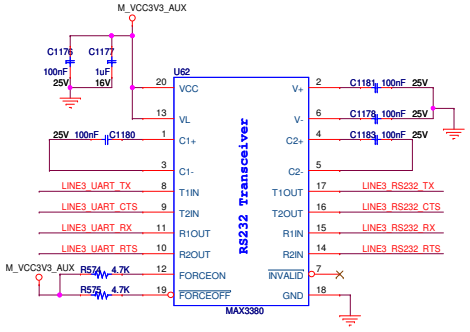


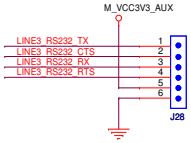
ASYNC I/F-4 FOR RADIO 2



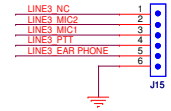
UART 1V8 to 3V3 CONVERTER





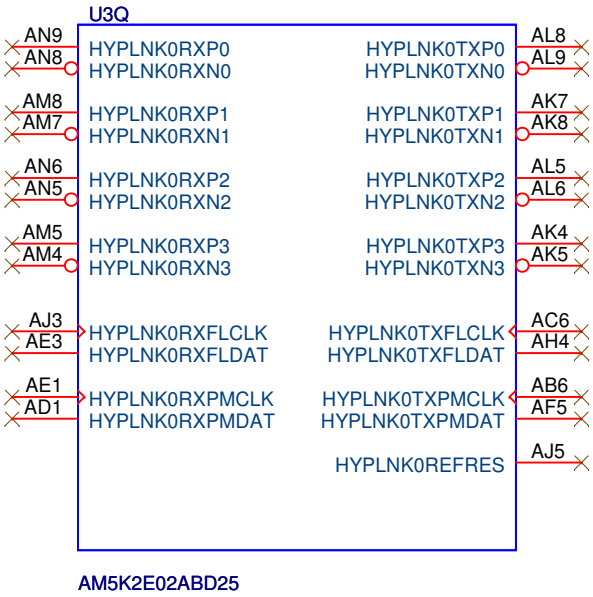


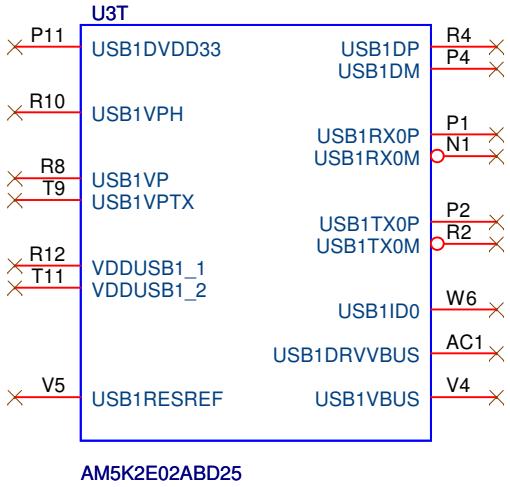
ASYNC I/F-3 FOR RADIO 1

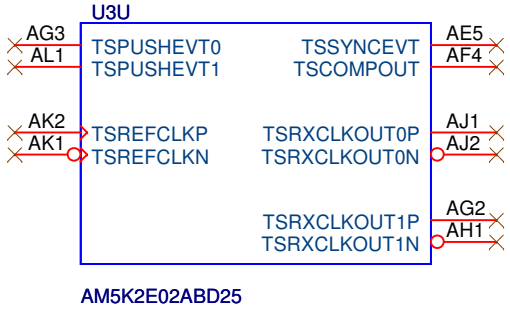


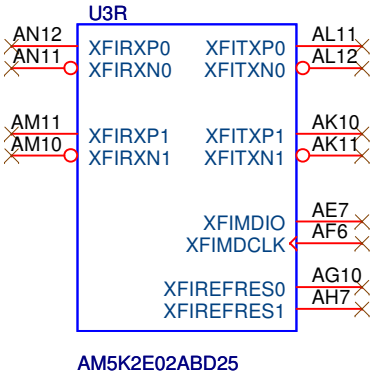
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_RIF_234
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 30 of 46

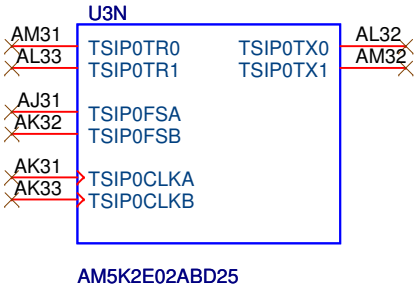
UNUSED











DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

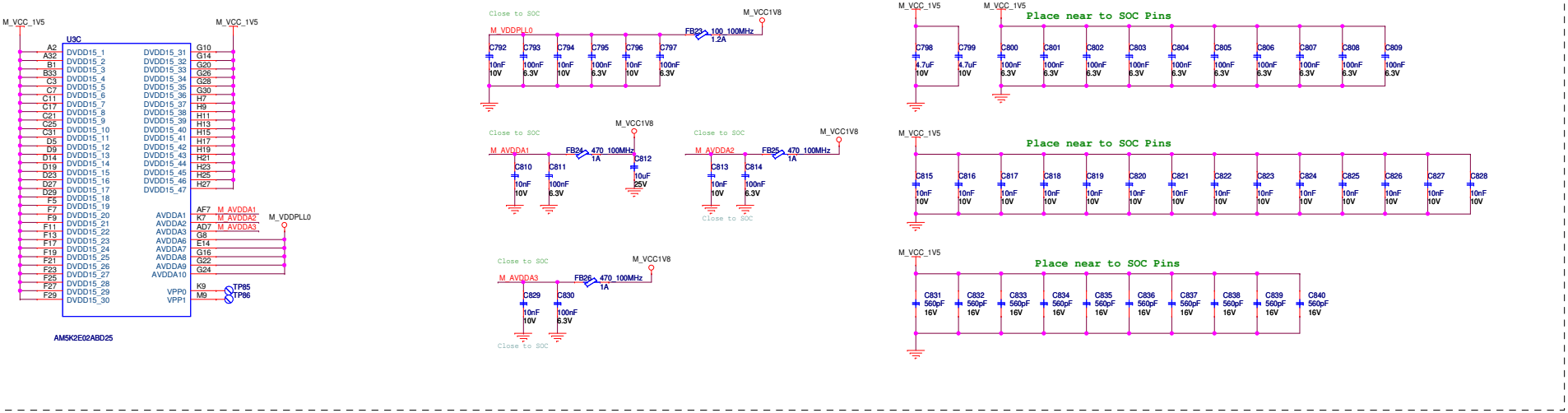
Ronanki Infotech Pvt Ltd

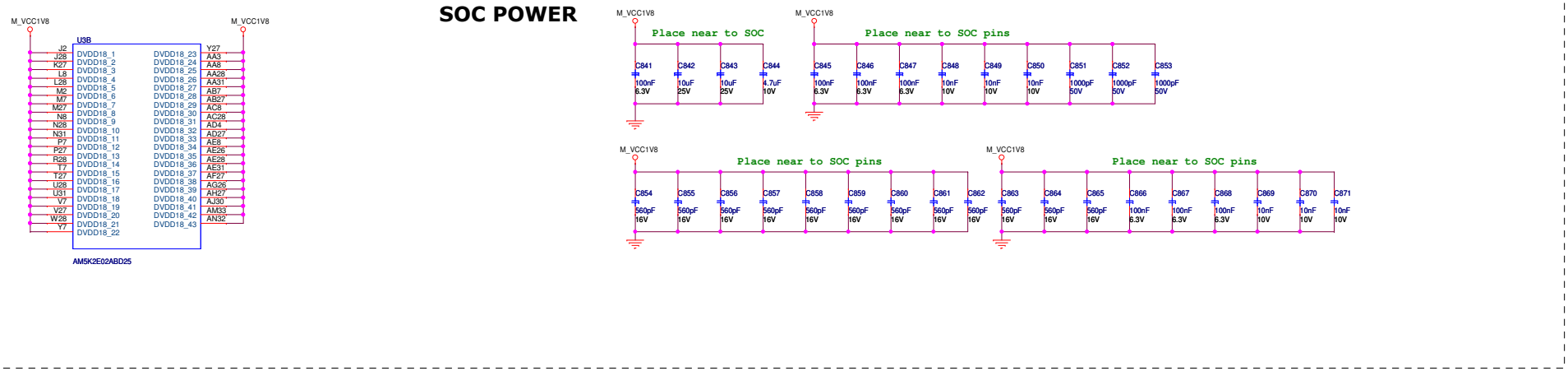
Title: MIP_UNUSED

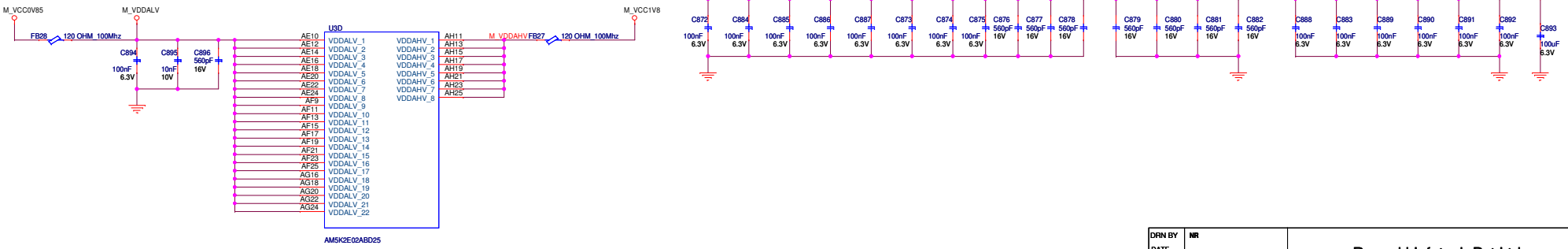
Size	Document Number	Rev
A	PCA	1.0

Date: Sunday, March 22, 2015 Sheet 31 of 46

SOC POWER



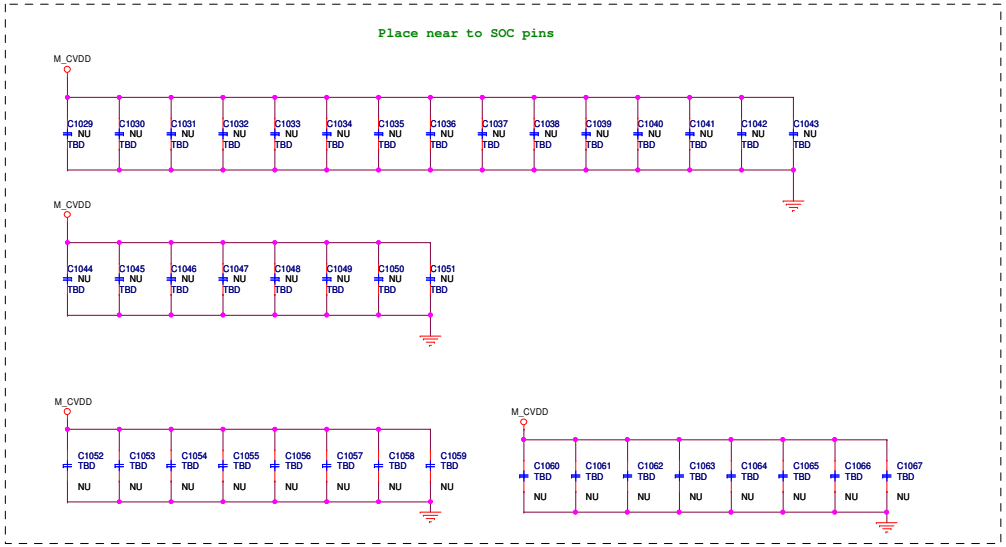




DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY		
DATE		Title	MIP_POWERA
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 32 of 46

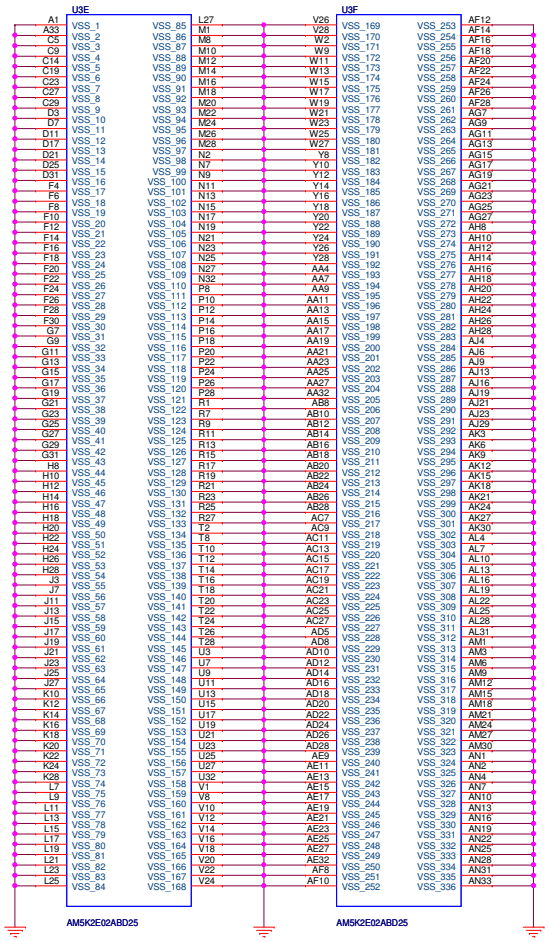
0.85V - 1.05V (CVDD) (Smart Reflex)

SOC POWER



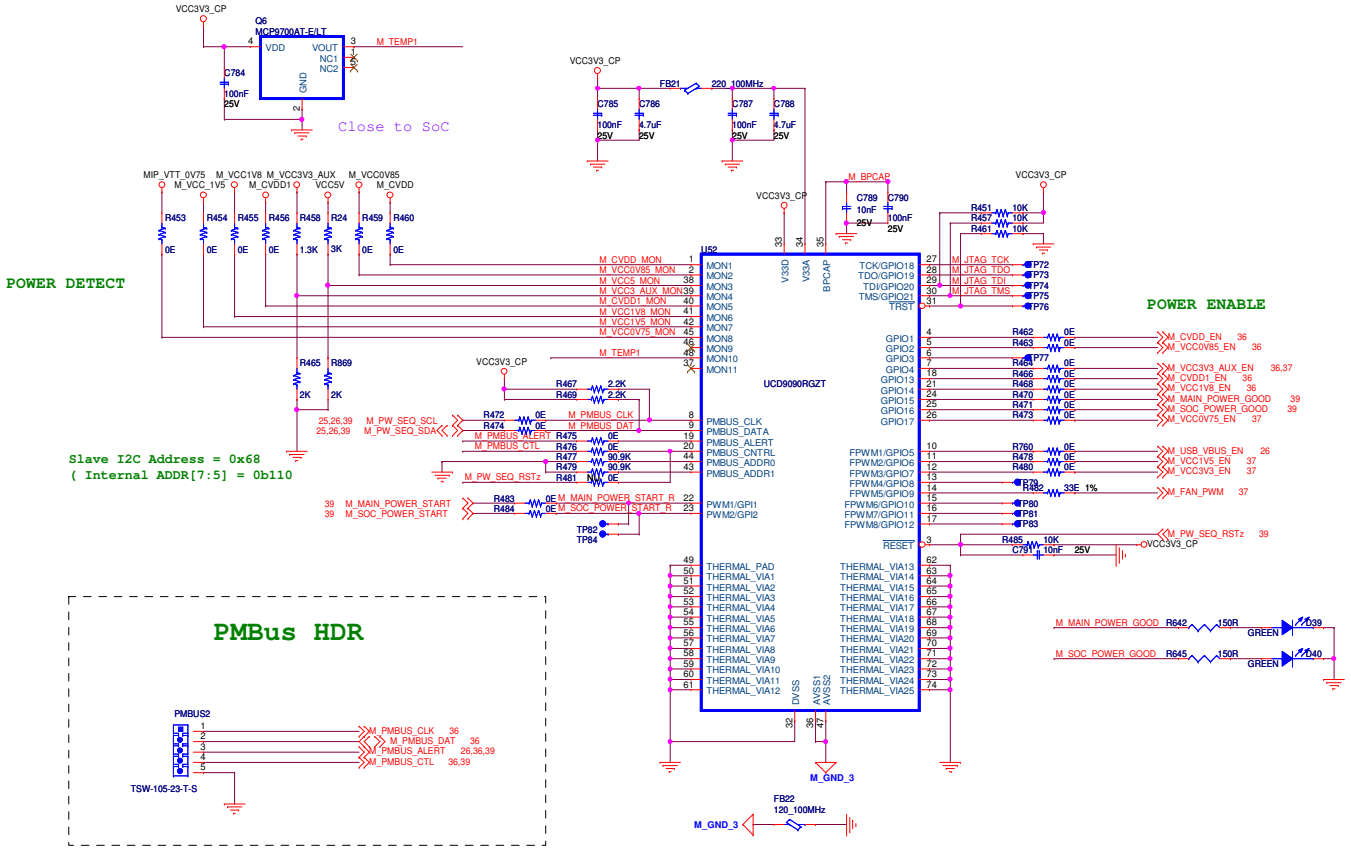
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_POWERB
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 33 of 46

No dissemination or use allowed without prior written permission



DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_PWR GND
DATE		Size C	Document Number PCA
APPD BY		Date: Sunday, March 22, 2015	Sheet 34 of 46
DATE			Rev 1.0

Power Sequencing (UCD9090)



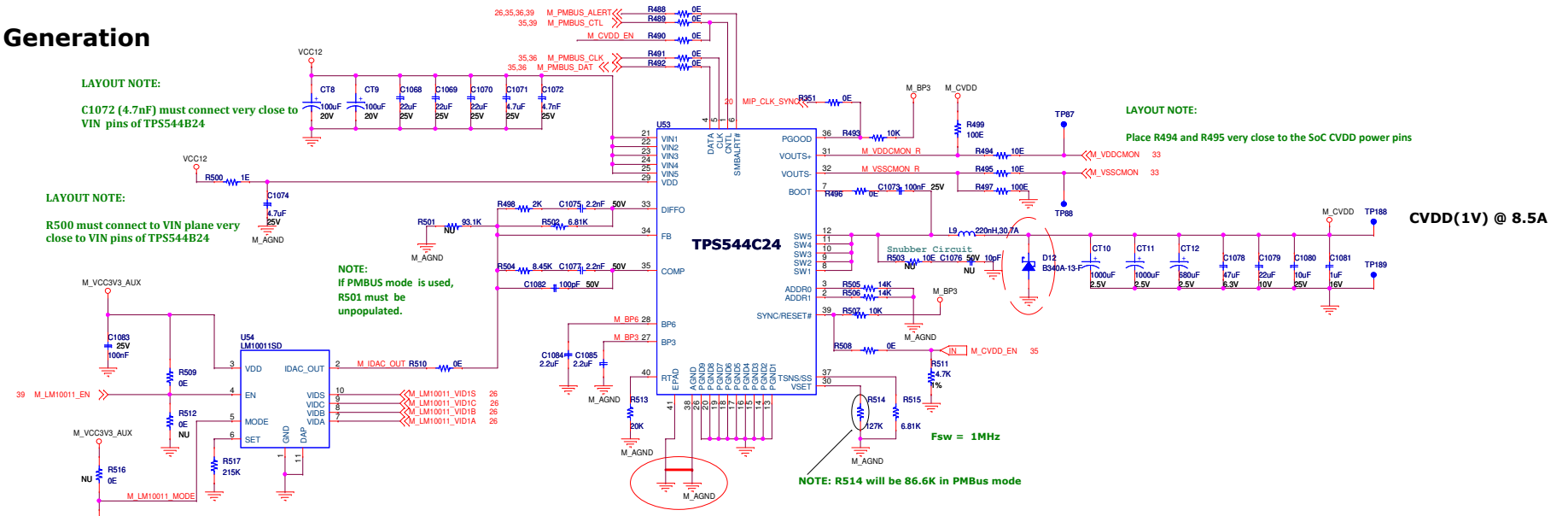
PMBus Address Pins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

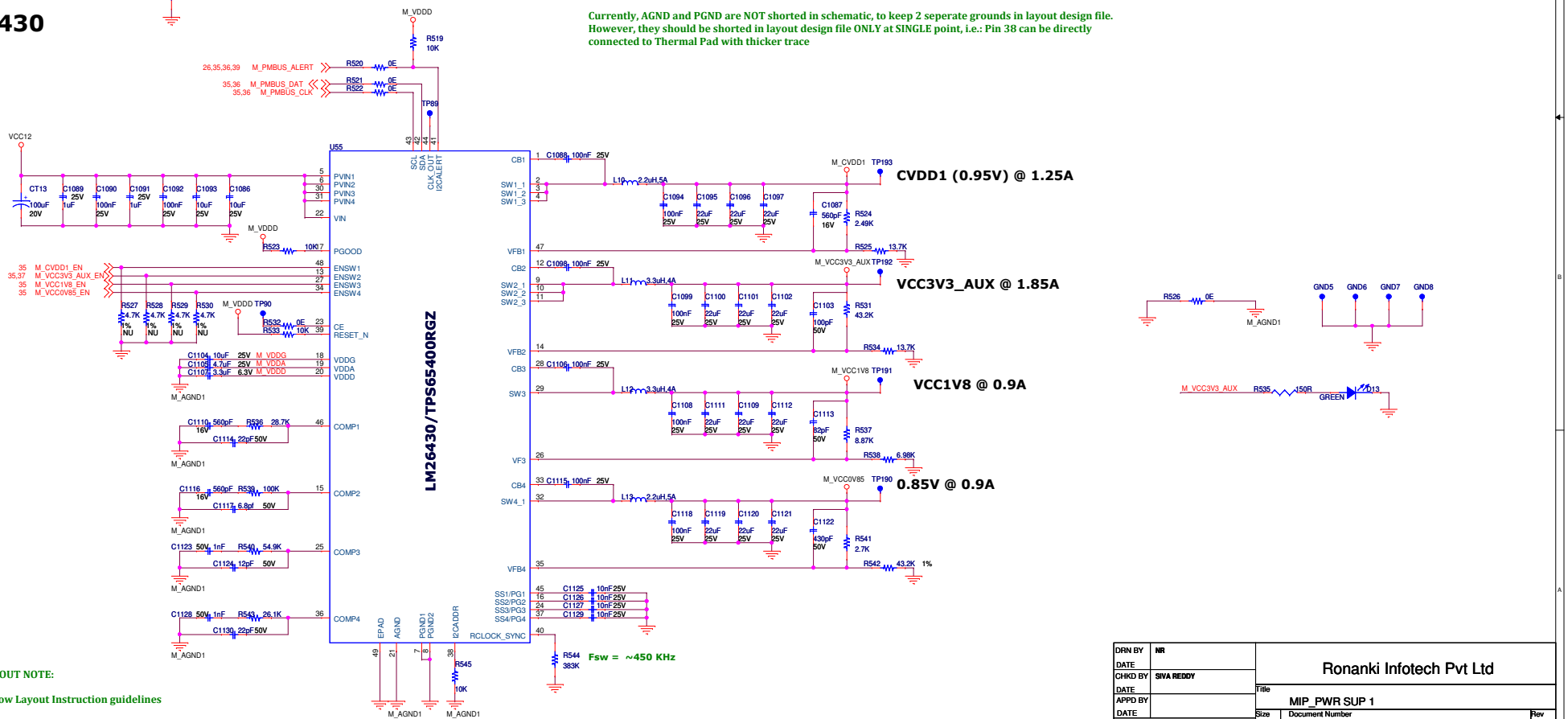
DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_POWER_SEQ
DATE		Size C	Document Number PCA
APPD BY			Rev 1.0
DATE		Date: Sunday, March 22, 2015	Sheet 35 of 46

PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

12V to CVDD Generation

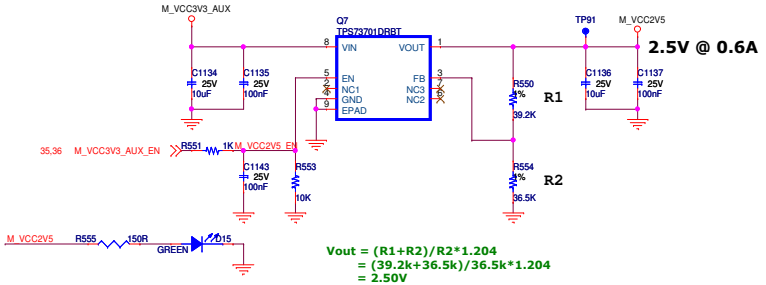


LM26430

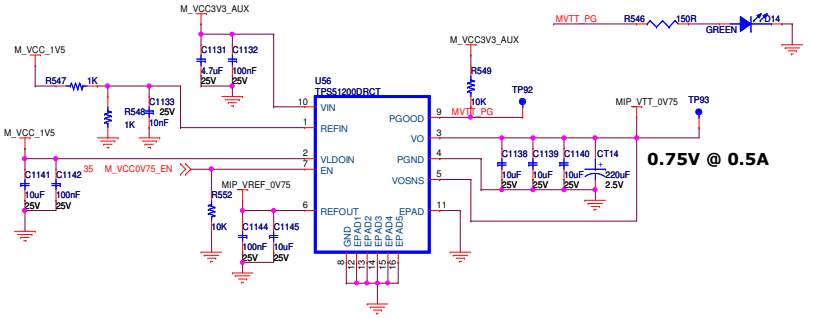


DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	MIP_PWR SUP 1
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015	Sheet 36 of 46

3.3V_AUX to 2.5V Generation

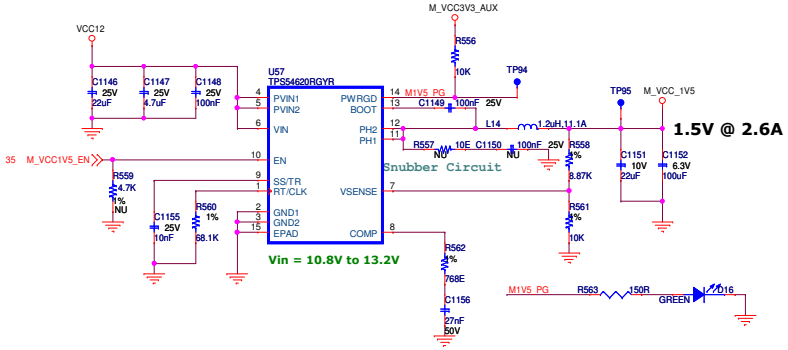


1.5V to 0.75V Generation

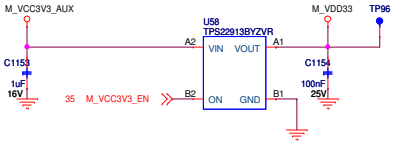


Place near DDR3 VTT Terminations

12V to 1.5V Generation



3V3_AUX to VDD33 Generation



VOUT = 0.8 * (R1/R2 + 1)
= 0.8 * (8.87/10 + 1)
= ~1.5V

Rrt=48000 * Fsw(kHz)^(-0.997) - 2
=48000 * 700^(-0.997) - 2
=~68 Kohms

OUTPUT CAPACITOR CALCULATION
Cout= 2 * delta(Iout) / (Fsw*delta(Vout)
= 2 * 1 / (700kHz*0.125)
= ~38uF

REFERENCE CAPACITOR = 100uF

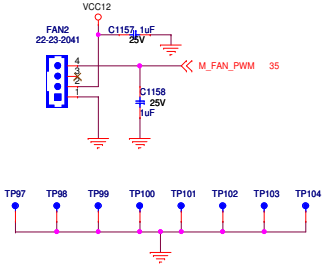
INDUCTOR CALCULATION
L= (Vin - Vout)/(Iout * Kind) *(Vout / (Vin * Fsw))
= (12 - 1.5)/(4.5 * 0.3) * (1.5 / (12 * 700KHz))
= 7.78 * 0.18u
= ~ 1.38uH

REFERENCE CAPACITOR = 1.2uH

chk pwr req for ambe3000 if any other

24 to 12v?

DC FAN Connector for SOC



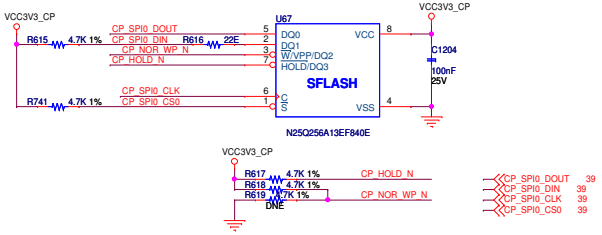
Distribute these TP in board

DRN BY	NR	Ronanki Infotech Pvt Ltd
DATE		
CHKD BY	SIVA REDDY	Title: MIP_PWR SUP 2
DATE		
APPD BY		Size: C — Document Number: PCA — Rev: 1.0
DATE		

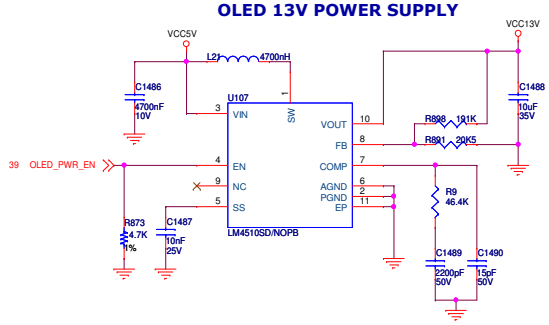
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

Date: Sunday, March 22, 2015 Sheet 37 of 46

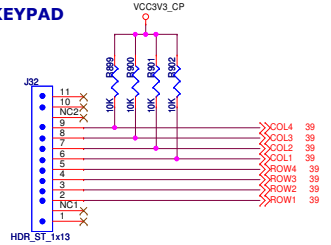
128Mb SPI NOR Flash



OLED 13V POWER SUPPLY

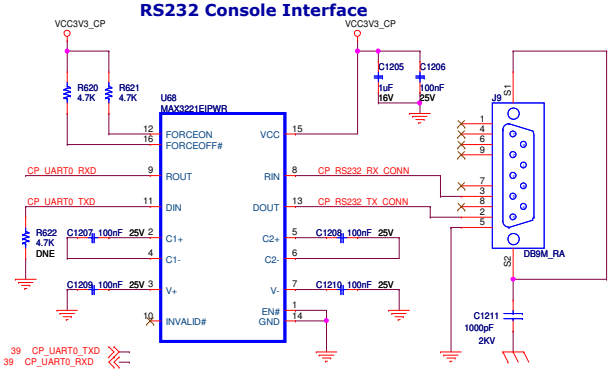


4X4 KEYPAD

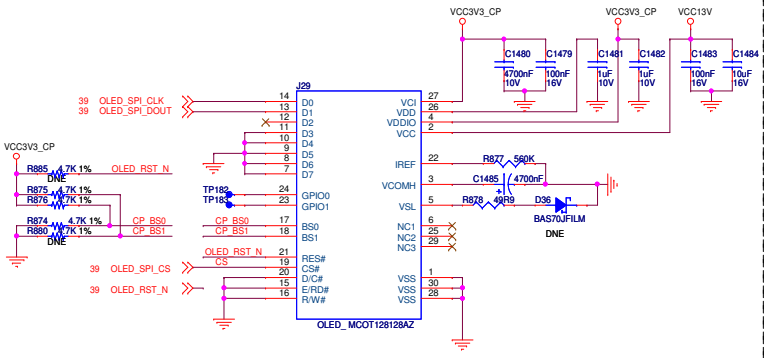


CAD :REFER DATASHEET FOR ACTUAL MECHANICAL CONSTRAINTS

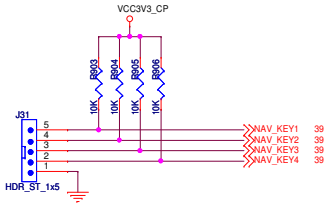
RS232 Console Interface



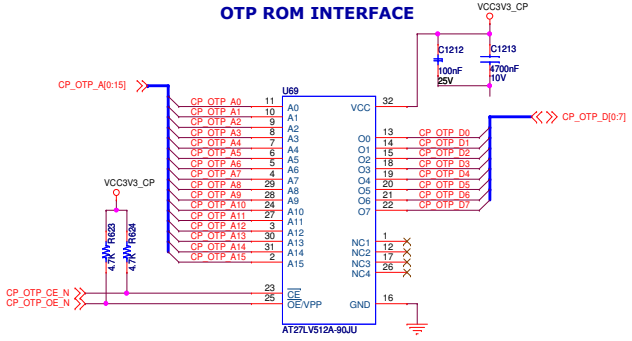
OLED INTERFACE



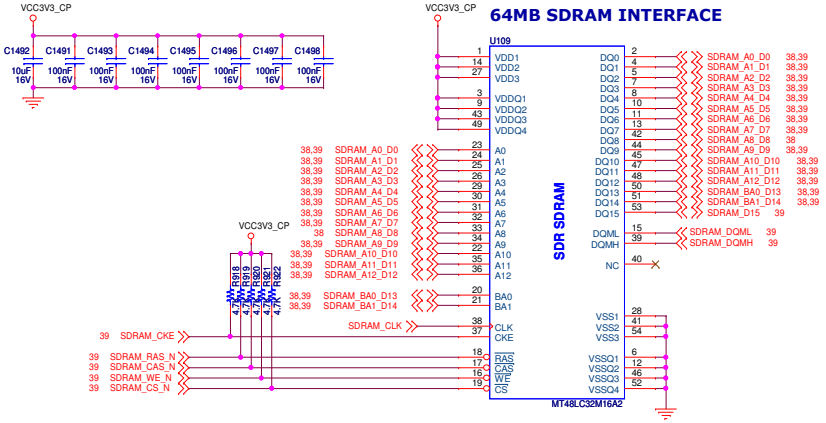
NAVIGATION KEYPAD



OTP ROM INTERFACE



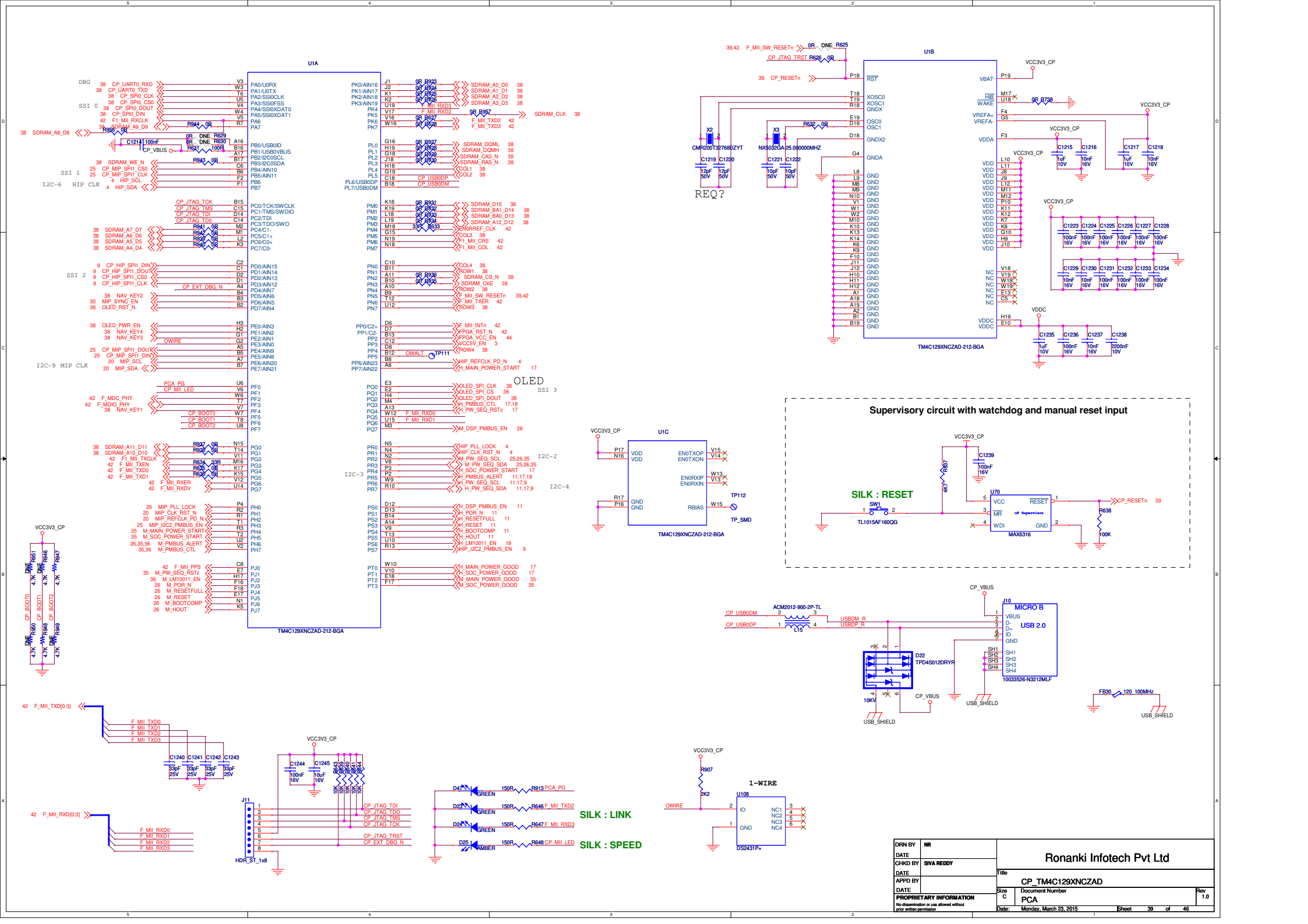
64MB SDRAM INTERFACE



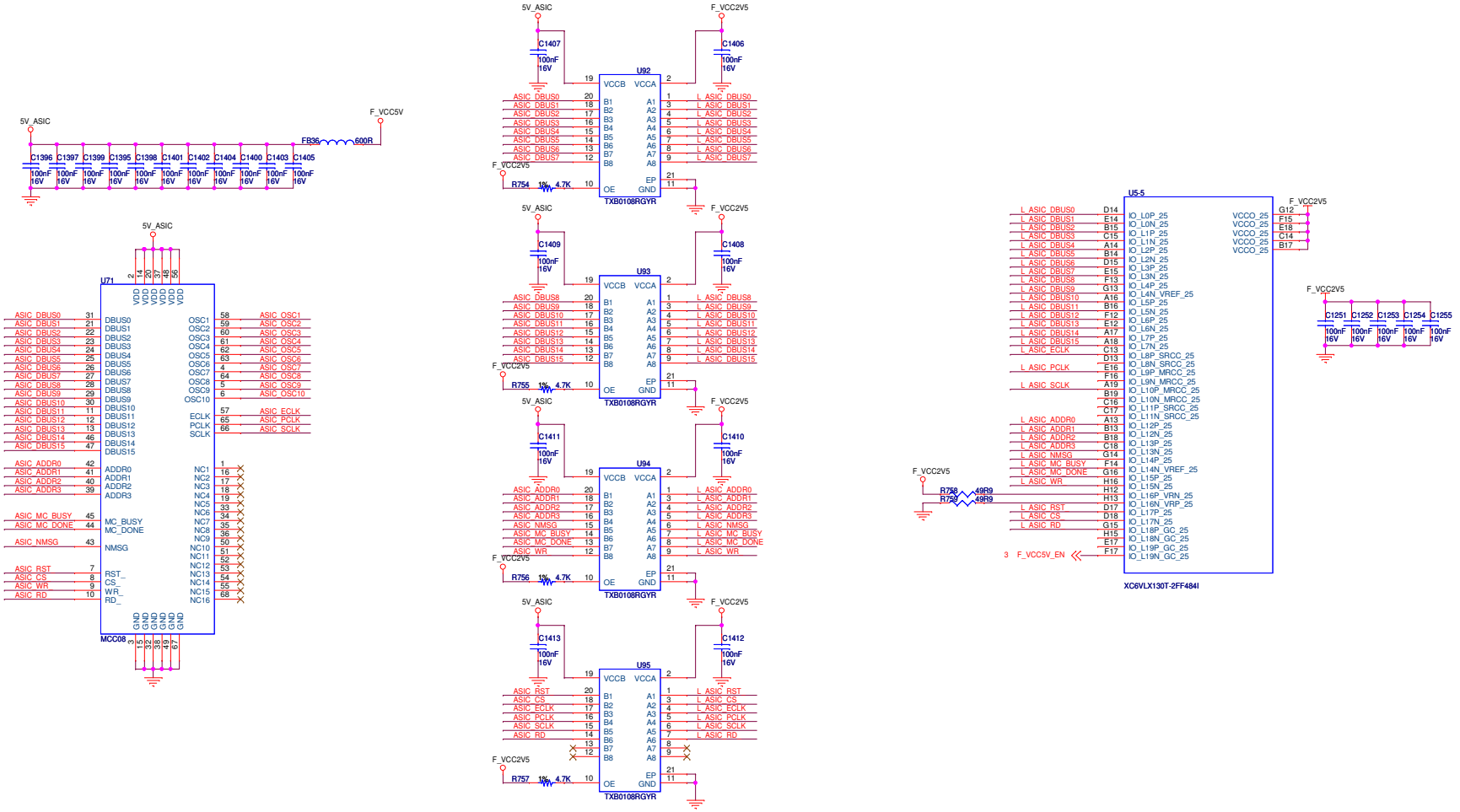
DRN BY	NR	Ronanki Infotech Pvt Ltd
DATE		
CHKD BY	SIVA REDDY	Title: CP_NOR_RS232_OTP
DATE		
APPD BY		Size: C — Document Number: PCA — Rev: 1.0
DATE		

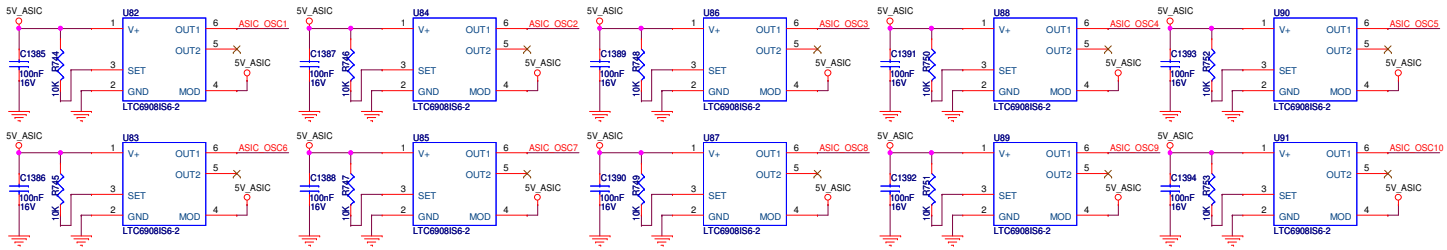
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

Date: Sunday, March 22, 2015 — Sheet 38 of 46


U1A
TM4C129XNCZAD-212-BGA
U1B
TM4C129XNCZAD-212-BGA
U1C
TM4C129XNCZAD-212-BGA
REQ?
OLED
SSI 3
SILK : RESET
SILK : LINK
SILK : SPEED
Supervisory circuit with watchdog and manual reset input
1-WIRE
MICRO B
USB 2.0
Ronanki Infotech Pvt Ltd
CP_TM4C129XNCZAD
PCA
Monday, March 23, 2015

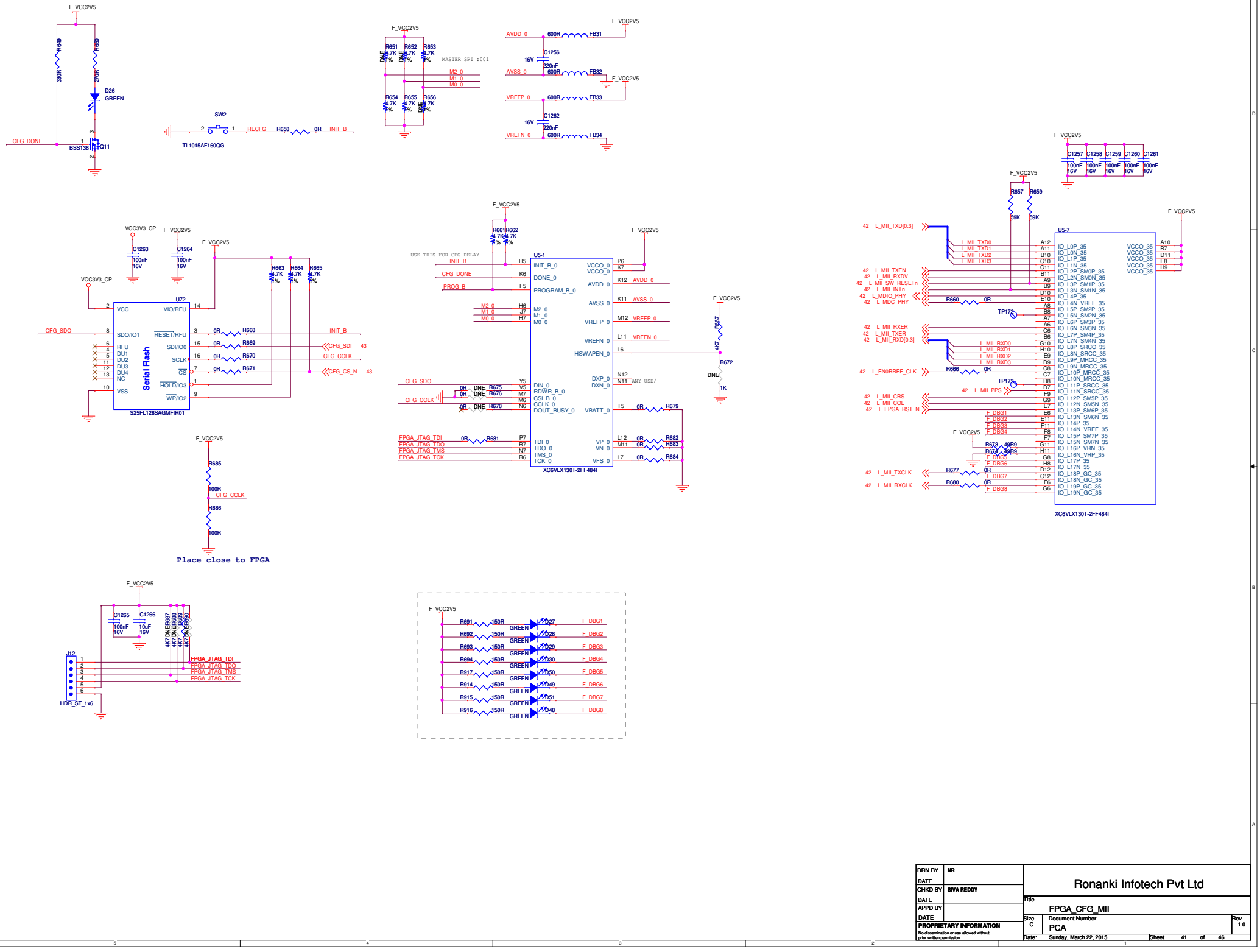
ASIC INTERFACE



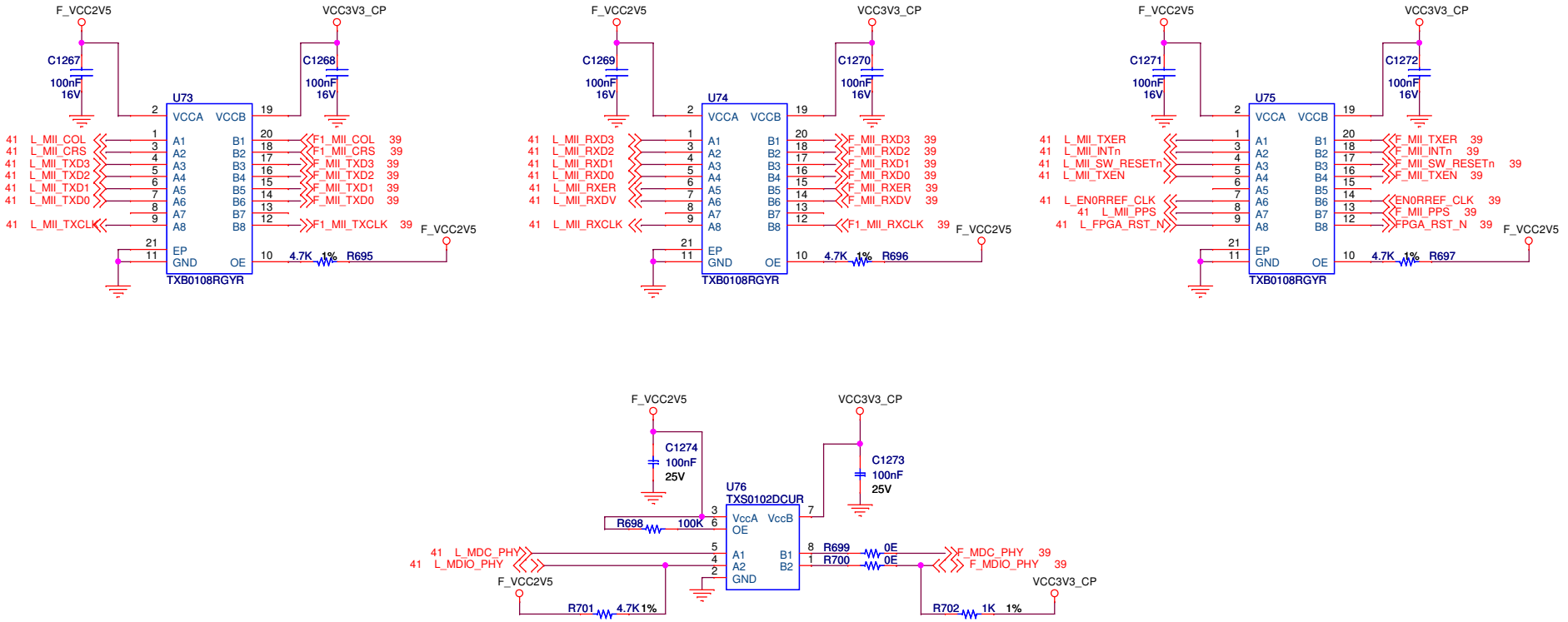


DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	FPGA_ASIC
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 40 of 46

No dissemination or use allowed without prior written permission



DRN BY	NR	Ronanki Infotech Pvt Ltd	
DATE			
CHKD BY	SIVA REDDY	Title	FPGA_CFG_MII
DATE			
APPD BY		Size C	Document Number PCA
DATE			Rev 1.0
PROPRIETARY INFORMATION		Date: Sunday, March 22, 2015	Sheet 41 of 46



DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

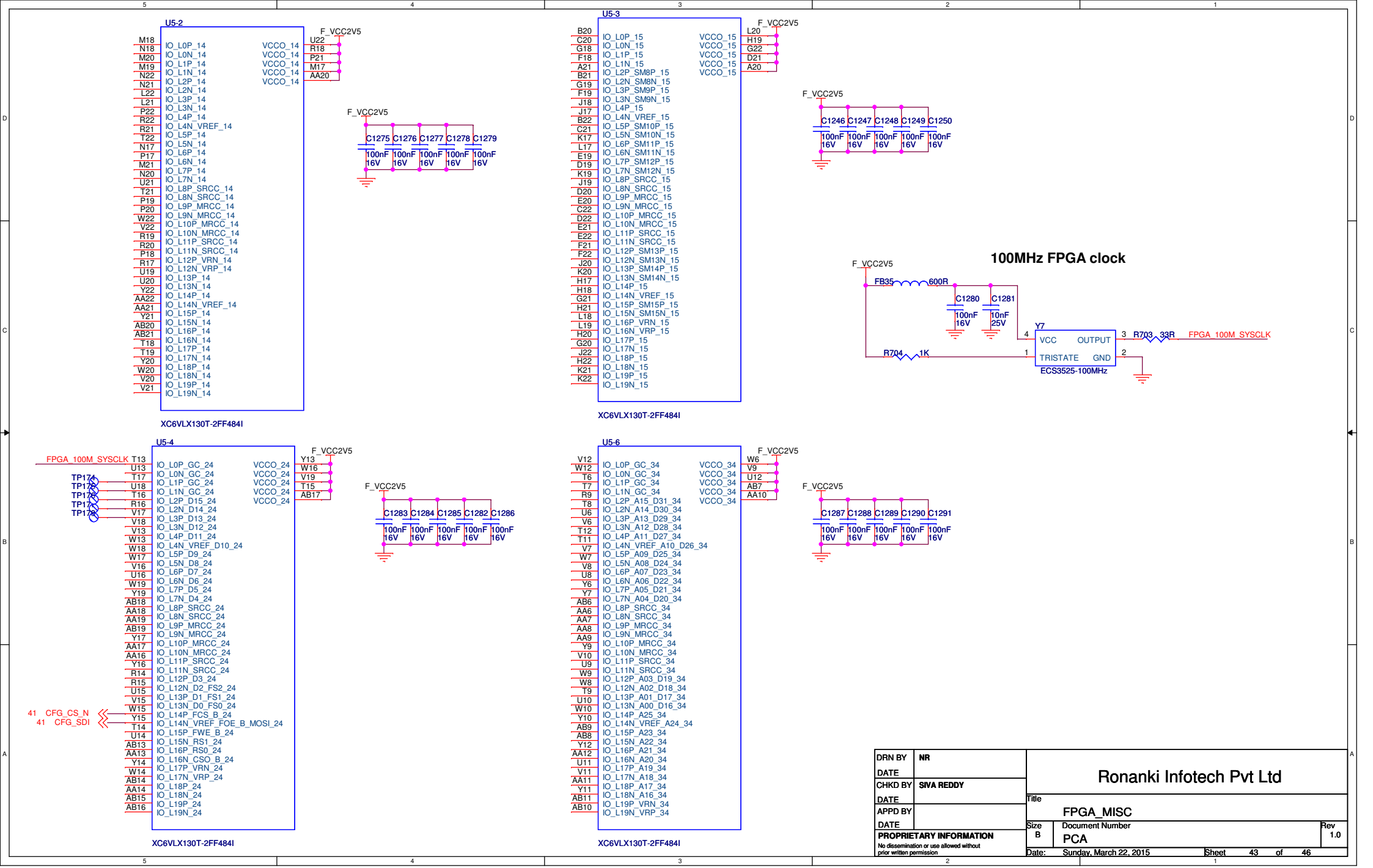
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission

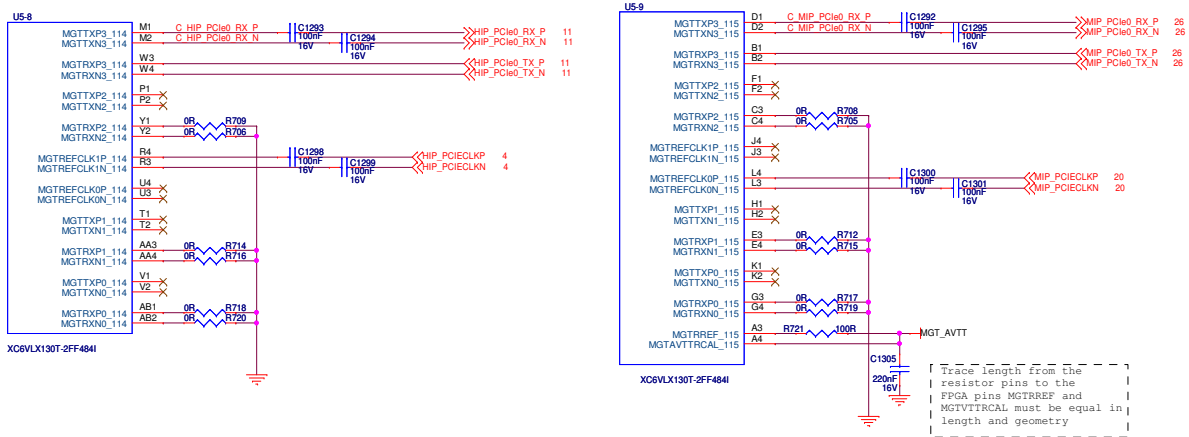
Ronanki Infotech Pvt Ltd

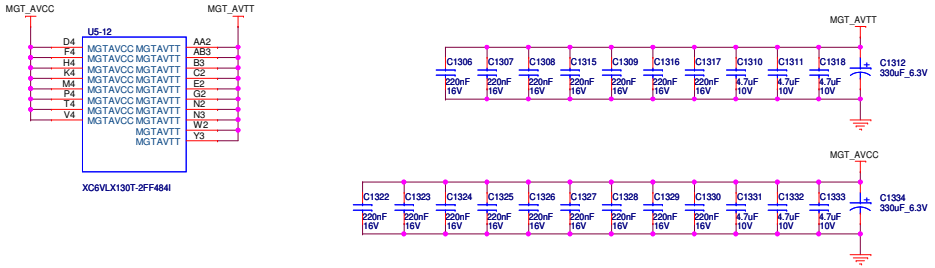
Title: FPGA_MII_TRANSLATORS

Size	Document Number	Rev
B	PCA	1.0

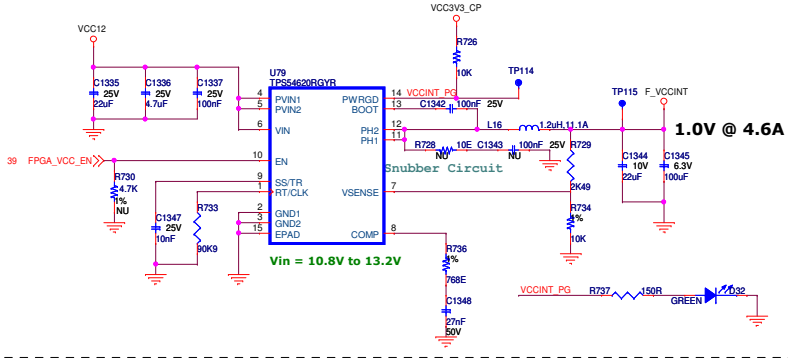
Date: Sunday, March 22, 2015 Sheet 42 of 46

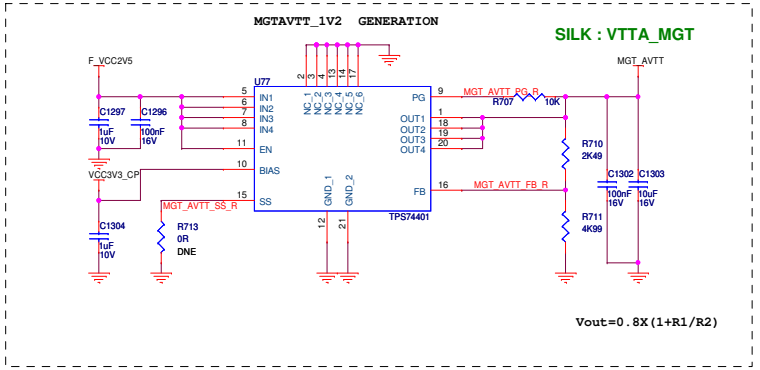

U5-2
M18 N18 M20 M19 N22 N21 L22 L21 P22 R22 R21 T22 N17 P17 M21 N20 U21 T21 P19 P20 W22 V22 R19 R20 P18 R17 U19 U20 Y22 AA22 AA21 Y21 AB20 AB21 T18 T19 Y20 W20 V20 V21
IO_L0P_14 IO_L0N_14 IO_L1P_14 IO_L1N_14 IO_L2P_14 IO_L2N_14 IO_L3P_14 IO_L3N_14 IO_L4P_14 IO_L4N_VREF_14 IO_L5P_14 IO_L5N_14 IO_L6P_14 IO_L6N_14 IO_L7P_14 IO_L7N_14 IO_L8P_SRCC_14 IO_L8N_SRCC_14 IO_L9P_MRCC_14 IO_L9N_MRCC_14 IO_L10P_MRCC_14 IO_L10N_MRCC_14 IO_L11P_SRCC_14 IO_L11N_SRCC_14 IO_L12P_VRN_14 IO_L12N_VRP_14 IO_L13P_14 IO_L13N_14 IO_L14P_14 IO_L14N_VREF_14 IO_L15P_14 IO_L15N_14 IO_L16P_14 IO_L16N_14 IO_L17P_14 IO_L17N_14 IO_L18P_14 IO_L18N_14 IO_L19P_14 IO_L19N_14
VCCO_14 VCCO_14 VCCO_14 VCCO_14 VCCO_14
F_VCC2V5
U22 R18 P21 M17 AA20
C1275 C1276 C1277 C1278 C1279
100nF 16V
XC6VLX130T-2FF484I
U5-3
B20 C20 G18 F18 A21 B21 G19 F19 J18 J17 B22 C21 K17 L17 E19 D19 K19 J19 D20 E20 C22 D22 E21 E22 F21 F22 J20 K20 H17 H18 G21 H21 L18 L19 H20 G20 J22 H22 K21 K22
IO_L0P_15 IO_L0N_15 IO_L1P_15 IO_L1N_15 IO_L2P_SM8P_15 IO_L2N_SM8N_15 IO_L3P_SM9P_15 IO_L3N_SM9N_15 IO_L4P_15 IO_L4N_VREF_15 IO_L5P_SM10P_15 IO_L5N_SM10N_15 IO_L6P_SM11P_15 IO_L6N_SM11N_15 IO_L7P_SM12P_15 IO_L7N_SM12N_15 IO_L8P_SRCC_15 IO_L8N_SRCC_15 IO_L9P_MRCC_15 IO_L9N_MRCC_15 IO_L10P_MRCC_15 IO_L10N_MRCC_15 IO_L11P_SRCC_15 IO_L11N_SRCC_15 IO_L12P_SM13P_15 IO_L12N_SM13N_15 IO_L13P_SM14P_15 IO_L13N_SM14N_15 IO_L14P_15 IO_L14N_VREF_15 IO_L15P_SM15P_15 IO_L15N_SM15N_15 IO_L16P_VRN_15 IO_L16N_VRP_15 IO_L17P_15 IO_L17N_15 IO_L18P_15 IO_L18N_15 IO_L19P_15 IO_L19N_15
VCCO_15 VCCO_15 VCCO_15 VCCO_15 VCCO_15
F_VCC2V5
L20 H19 G22 D21 A20
C1246 C1247 C1248 C1249 C1250
100nF 16V
XC6VLX130T-2FF484I
100MHz FPGA clock
F_VCC2V5
FB35 600R
C1280 100nF 16V
C1281 10nF 25V
Y7
VCC OUTPUT TRISTATE GND
ECS3525-100MHz
R703 33R
FPGA_100M_SYSCLK
R704 1K
U5-4
FPGA_100M_SYSCLK T13
U13 T17 U18 T16 R16 V17 V18 V13 W13 W18 W17 V16 U16 W19 Y19 AB18 AA18 AA19 AB19 Y17 AA17 AA16 Y16 R14 R15 U15 V15 W15 Y15 T14 U14 AB13 AA13 Y14 W14 AB14 AA14 AB15 AB16
IO_L0P_GC_24 IO_L0N_GC_24 IO_L1P_GC_24 IO_L1N_GC_24 IO_L2P_D15_24 IO_L2N_D14_24 IO_L3P_D13_24 IO_L3N_D12_24 IO_L4P_D11_24 IO_L4N_VREF_D10_24 IO_L5P_D9_24 IO_L5N_D8_24 IO_L6P_D7_24 IO_L6N_D6_24 IO_L7P_D5_24 IO_L7N_D4_24 IO_L8P_SRCC_24 IO_L8N_SRCC_24 IO_L9P_MRCC_24 IO_L9N_MRCC_24 IO_L10P_MRCC_24 IO_L10N_MRCC_24 IO_L11P_SRCC_24 IO_L11N_SRCC_24 IO_L12P_D3_24 IO_L12N_D2_FS2_24 IO_L13P_D1_FS1_24 IO_L13N_D0_FS0_24 IO_L14P_FCS_B_24 IO_L14N_VREF_FOE_B_MOSI_24 IO_L15P_FWE_B_24 IO_L15N_RS1_24 IO_L16P_RS0_24 IO_L16N_CSO_B_24 IO_L17P_VRN_24 IO_L17N_VRP_24 IO_L18P_24 IO_L18N_24 IO_L19P_24 IO_L19N_24
VCCO_24 VCCO_24 VCCO_24 VCCO_24 VCCO_24
TP174 TP175 TP176 TP177 TP178
41 CFG_CS_N
41 CFG_SDI
F_VCC2V5
Y13 W16 V19 T15 AB17
C1283 C1284 C1285 C1282 C1286
100nF 16V
XC6VLX130T-2FF484I
U5-6
V12 W12 T6 T7 R9 T8 U6 V6 T12 T11 V7 W7 V8 U8 Y6 Y7 AB6 AA6 AA7 AA8 AA9 Y9 V10 U9 W9 W8 T9 U10 W10 Y10 AB9 AB8 Y12 AA12 U11 V11 AA11 Y11 AB11 AB10
IO_L0P_GC_34 IO_L0N_GC_34 IO_L1P_GC_34 IO_L1N_GC_34 IO_L2P_A15_D31_34 IO_L2N_A14_D30_34 IO_L3P_A13_D29_34 IO_L3N_A12_D28_34 IO_L4P_A11_D27_34 IO_L4N_VREF_A10_D26_34 IO_L5P_A09_D25_34 IO_L5N_A08_D24_34 IO_L6P_A07_D23_34 IO_L6N_A06_D22_34 IO_L7P_A05_D21_34 IO_L7N_A04_D20_34 IO_L8P_SRCC_34 IO_L8N_SRCC_34 IO_L9P_MRCC_34 IO_L9N_MRCC_34 IO_L10P_MRCC_34 IO_L10N_MRCC_34 IO_L11P_SRCC_34 IO_L11N_SRCC_34 IO_L12P_A03_D19_34 IO_L12N_A02_D18_34 IO_L13P_A01_D17_34 IO_L13N_A00_D16_34 IO_L14P_A25_34 IO_L14N_VREF_A24_34 IO_L15P_A23_34 IO_L15N_A22_34 IO_L16P_A21_34 IO_L16N_A20_34 IO_L17P_A19_34 IO_L17N_A18_34 IO_L18P_A17_34 IO_L18N_A16_34 IO_L19P_VRN_34 IO_L19N_VRP_34
VCCO_34 VCCO_34 VCCO_34 VCCO_34 VCCO_34
F_VCC2V5
W6 V9 U12 AB7 AA10
C1287 C1288 C1289 C1290 C1291
100nF 16V
XC6VLX130T-2FF484I
DRN BY NR
DATE
CHKD BY SIVA REDDY
DATE
APPD BY
DATE
PROPRIETARY INFORMATION
No dissemination or use allowed without prior written permission
Ronanki Infotech Pvt Ltd
Title
FPGA_MISC
Size B
Document Number
PCA
Rev 1.0
Date: Sunday, March 22, 2015
Sheet 43 of 46

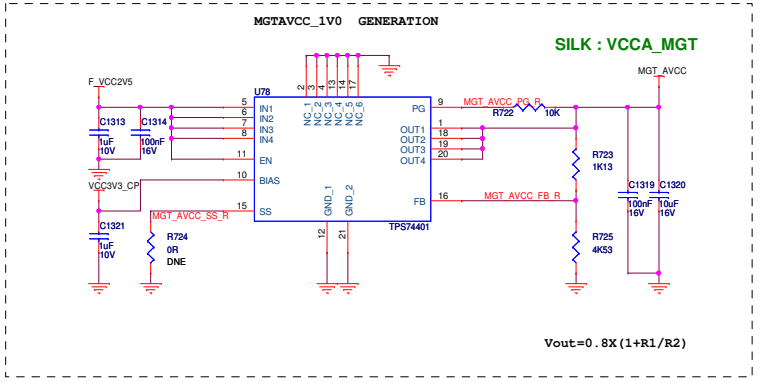




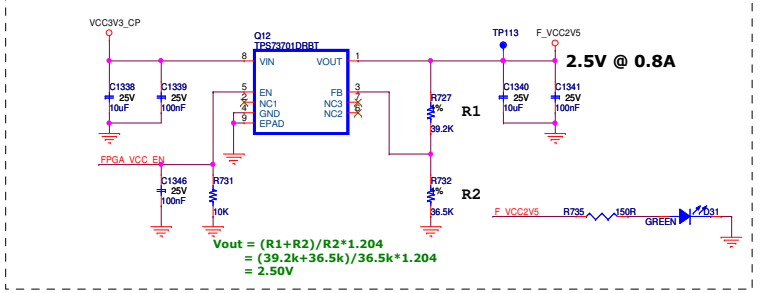
12V to 1.0V Generation



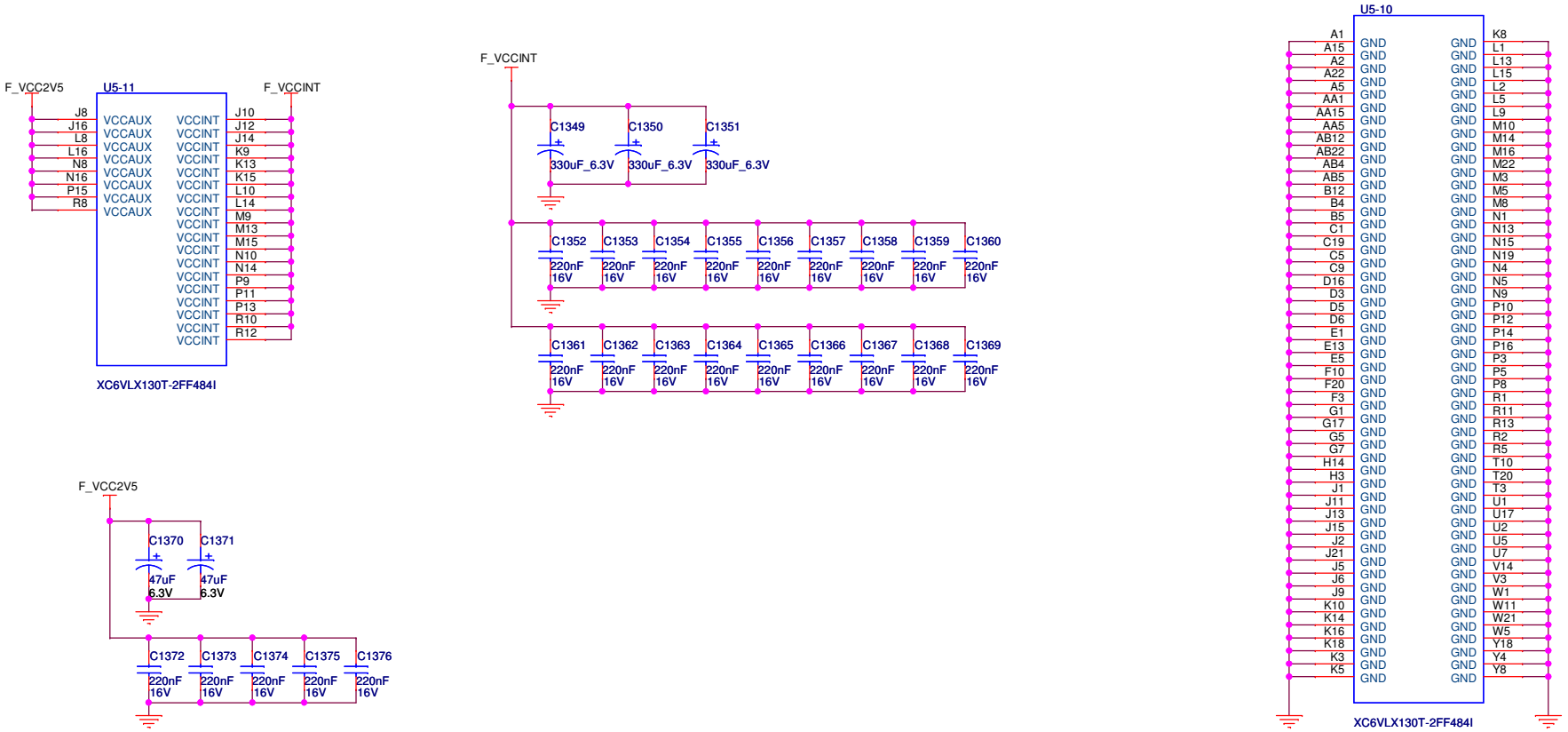




3.3V_CP to 2.5V Generation



DRN BY	NR	Ronanki Infotech Pvt Ltd
DATE		
CHKD BY	SIVA REDDY	Title: FPGA_PCIE
DATE		
APPD BY		Size: C — Document Number: PCA — Rev: 1.0
DATE		
PROPRIETARY INFORMATION	No dissemination or use allowed without prior written permission	Date: Sunday, March 22, 2015 — Sheet 44 of 46



DRN BY	NR
DATE	
CHKD BY	SIVA REDDY
DATE	
APPD BY	
DATE	

PROPRIETARY INFORMATION

No dissemination or use allowed without prior written permission

Ronanki Infotech Pvt Ltd

Title: FPGA_POWER

Size: B | Document Number: PCA | Rev: 1.0

Date: Sunday, March 22, 2015 | Sheet 45 of 46

DRN BY DATE	**NR**
CHKD BY DATE	**SIVA REDDY**
APPD BY DATE	
PROPRIETARY INFORMATION No dissemination or use allowed without prior written permission	

Ronanki Infotech Pvt Ltd

Title

HISTORY

Size	Document Number	Rev
A	PCA	1.0

Date: Sunday, March 22, 2015 Sheet 46 of 46