Técnicas de reducción de consumo

Niveles de abstracción de un diseño

- Sistema
- Algoritmos
- Arquitectura
- Diseño del circuito
- Tecnología de fabricación

Co-funded by the Erasmus+ Programme of the European Union

Circuit-Level Techiques

- Dynamic-power optimization
  - Multiple supply voltages
  - Transistor sizing
  - Technology mapping
- Static-power optimization
  - Multiple thresholds
  - Transistor stacking

Source: Rabaey, Jan. Low power design essentials. Springer Science & Business Media, 2009.

Reducing Active Energy

$$E_{\text{active}} \sim \alpha \cdot C_{\text{L}} \cdot V_{\text{swing}} \cdot V_{\text{DD}}$$

$$P_{\text{active}} \sim \alpha \cdot C_{\text{L}} \cdot V_{\text{swing}} \cdot V_{\text{DD}} \cdot f$$

- Reducing voltages
  - Lowering the supply voltage (VDD) at the expense of clock speed
  - Lowering the logic swing (Vswing)
- Reducing transistor sizes (CL)
  - Slows down logic
- Reducing activity (α)
  - Reducing switching activity through transformations
  - Reducing glitching by balancing logic

Multiple Supply Voltages

- Block-level supply assignment
  - Higher-throughput/lower-latency functions are implemented in higher VDD
  - Slower functions are implemented with lower VDD
  - This leads to so-called voltage islands with separate supply grids
  - Level conversion performed at block boundaries
- Multiple supplies inside a block
  - Non-critical paths moved to lower supply voltage
  - Level conversion within the block
  - Physical design challenging

Multiple Supply Voltages

- Two supply voltages per block are optimal
- Optimal ratio between the supply voltages is 0.7
- Level conversion is performed on the voltage boundary, using a level-converting flip-flop (LCFF)
- An option is to use an asynchronous level converter
  - More sensitive to coupling and supply noise

Practical Transistor Sizing

- Continuous sizing of transistors only an option in custom design
- In ASIC design flows, options set by available library
- Discrete sizing options made possible in standard-cell design methodology by providing multiple options for the same cell
  - Leads to larger libraries (> 800 cells)
  - Easily integrated into technology mapping

Technology Mapping

Example: four-input AND

- (a) Implemented using four-input NAND + INV
- (b) Implemented using two-input NAND + two-input NOR

			Library 1: High-Speed	**Library 2: Low-Power**
Gate type	Area (cell unit)	Input cap. (fF)	Average delay (ps)	Average delay (ps)
INV	3	1.8	$7.0 + 3.8C_L$	$12.0 + 6.0C_L$
NAND2	4	2.0	$10.3 + 5.3C_L$	$16.3 + 8.8C_L$
NAND4	5	2.0	$13.6 + 5.8C_L$	$22.7 + 10.2C_L$
NOR2	3	2.2	$10.7 + 5.4C_L$	$16.7 + 8.9C_L$

(delay formula: C_L in fF)

(numbers calibrated for 90 nm)

Technology Mapping

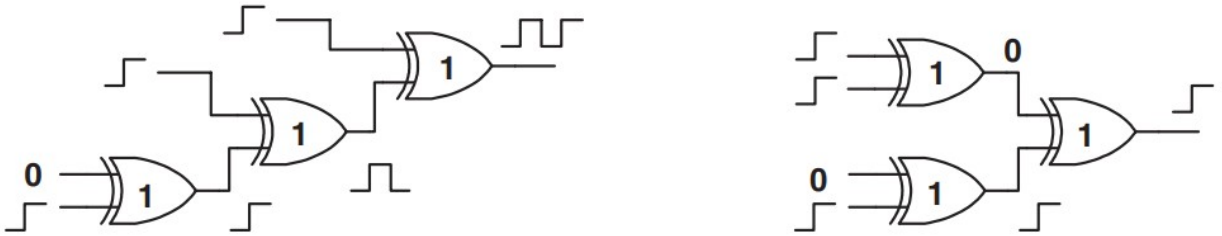
four-input AND	(a) NAND4 + INV	(b) NAND2 + NOR2
Area	8	11
HS: Delay (ps)	$31.0 + 3.8C_L$	$32.7 + 5.4C_L$
LP: Delay (ps)	$53.1 + 6.0C_L$	$52.4 + 8.9C_L$
Sw Energy (fF)	$0.1 + 0.06C_L$	$0.83 + 0.06C_L$

- Area
  - Four-input more compact than two-input (two gates vs three gates)
- Timing
  - Both implementations are two-stage realizations
  - Second-stage INV (a) is better driver than NOR2 (b)
  - For more complex blocks, simpler gates will show better performance
- Energy
  - Internal switching increases energy in the two-input case
  - Low-power library has worse delay, but lower leakage (see later)

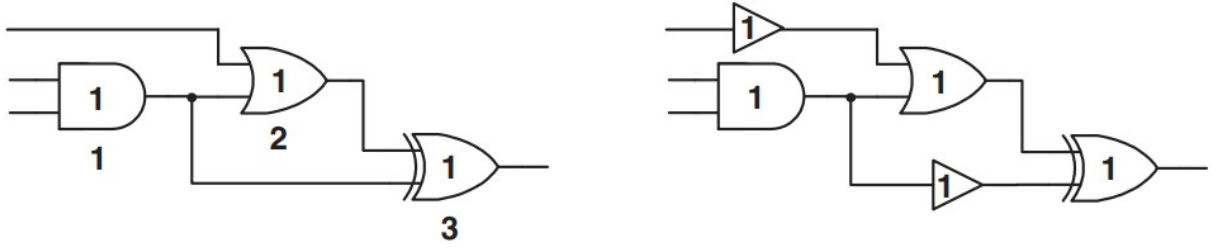
Gate-Level Trade-offs for Power

- Technology mapping
  - Gate selection
  - Sizing
  - Pin assignment
- Logical Optimizations
  - Factoring
  - Restructuring
  - Buffer insertion/deletion
  - Don’t - care optimization

Logic Restructuring



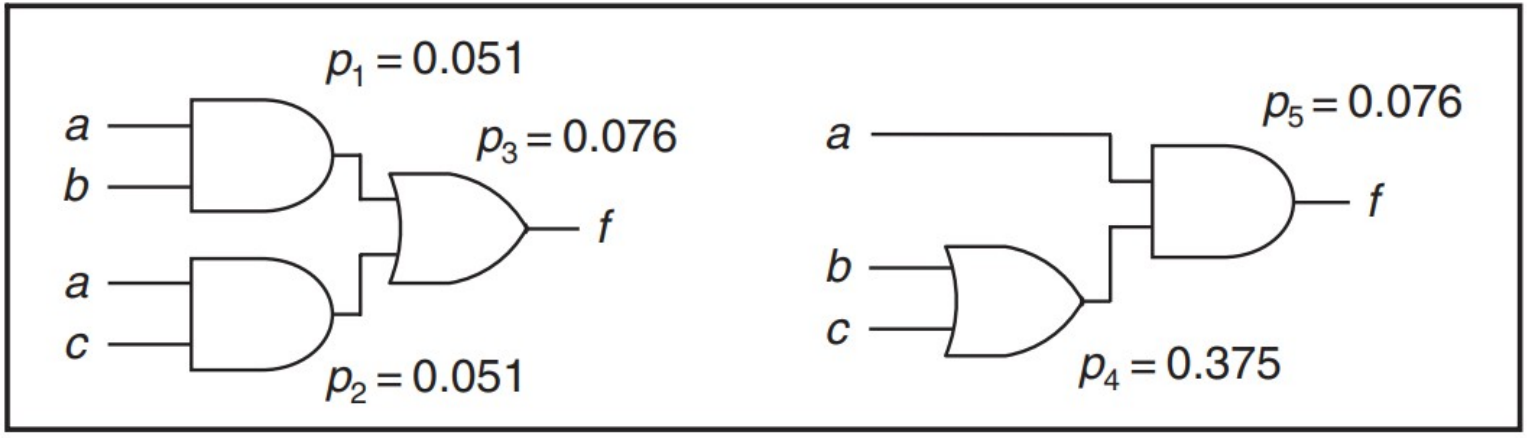
Logic restructuring to minimize spurious transitions



Buffer insertion for path balancing

Algebraic Transformations Factoring

Idea: Modify network to reduce capacitance



$p_a = 0.1; p_b = 0.5; p_c = 0.5$

Caveat: This may increase activity!