Estimación de consumo

- Ecuación del consumo

$$P_{tot} = \alpha\, f_{ck}\, C_L V_{DD}^2/2 + \alpha\, f_{ck}\, V_{DD}\, I_{sc} + V_{DD}\, I_{leakage}$$

- ¿Dónde está la incertidumbre?

Co-funded by the
Erasmus+ Programme
of the European Union

Estimación de consumo

- Ecuación del consumo

$$P_{tot} = \alpha\, f_{ck}\, C_L V_{DD}^2/2 + \alpha\, f_{ck}\, V_{DD}\, I_{sc} + V_{DD}\, I_{leakage}$$

- ¿Dónde está la incertidumbre?

α = activity factor

Capacitancias

- Input gate: 0.042 pF (ES2 1u), 0.003 (Atmel 0.25u)
- Local wire: 0.3 pF
- Global wire: 2.5 pF
- Output pin: 3 pF
- PCB wire: several pF
- Wire: hundred of pF

Cálculo de potencia (orden de magnitud)

P = 0.1pF x 1V x 100 MHz x 10 millones de gates = 100 watts!!!

Activity rate

- Toggle Rates
  - How often a signal changes relative to a given clock
  - Percentage between 0–100%.
    - 12.5% (default) logic-intensive designs
    - 20% worst case (toggle rates greater than 20% are not very common)
    - 50% absolute worst case (arithmetic-intensive modules)

Switching Activity Computation

- Delay Model
  - Zero-delay model
  - Real delay model
    - Post synthesis,
    - Post technology mapping
    - Post Place&Route
- Functional activity
  - steady-state transitions
- Spurious activity
  - Glitches considered

The switching activity is the most difficult factor to obtain in the power consumption equation.

Power Estimation Techniques

- Complete circuit simulation (~Spice)
- Statistical Approaches
- Probabilistic Approaches

- Sequential Circuits (FSM)

E. Todorovich, “Estimación estadística de consumo en FPGAs,” Ph.D dissertation, Dep. Ing. Infor., Univ. Autónoma de Madrid, 2006. Accessed on: Sept 7, 2021. [Online].
Available: https://repositorio.uam.es/bitstream/handle/10486/3656/25461_todorovich_elias.pdf

Complete circuit simulation (~Spice)

- Problems
  - Size of the stimulus vector set necessary to calculate accurately the activity
  - Efficiency: memory and execution time

Complete circuit simulation (~Spice)

- Timing Simulators
  - Transistor level power simulator, applies an event-driven timing simulation algorithm to increase the speed by two to three orders of magnitude over SPICE
- Switch Simulators
  - Transistor model simplified to a simple resistive switch using a discrete data representation (0, 1, X, for example).
- Gate Level Simulators
  - Use the macromodels built for the gates in the ASIC library
- Hierarchical Simulation
  - Use a hierarchy of power simulators (for example, at architectural, gate-level and circuit-level) to achieve a reasonable accuracy and efficiency tradeoff

Statistical Approaches

- Monte Carlo
  - Random input patterns
- Total Power (McPower)
  - Iteration, combines statistical estimation and measures (slow convergence problem)
- Power of Individual Gates
  - direct extension of McPower
  - provides both the total and individual-gate power estimates
- Improvements in Statistical Methods
  - Better execution time

Probabilistic Approaches

- Statistics-based strategies
  - the circuit under test is simulated with a number of patterns and after that, the resulting waveforms are processed
- If an appropriate probability characterization for circuit inputs is provided
  - The circuit can be simulated just once
  - Some processing must be done somehow before the simulation run to compute the required probability values at the inputs
  - A single run of a probability analysis tool replaces a number of conventional circuit simulation runs.
  - The user must specify the typical behavior at the circuit inputs

Probabilistic Approaches

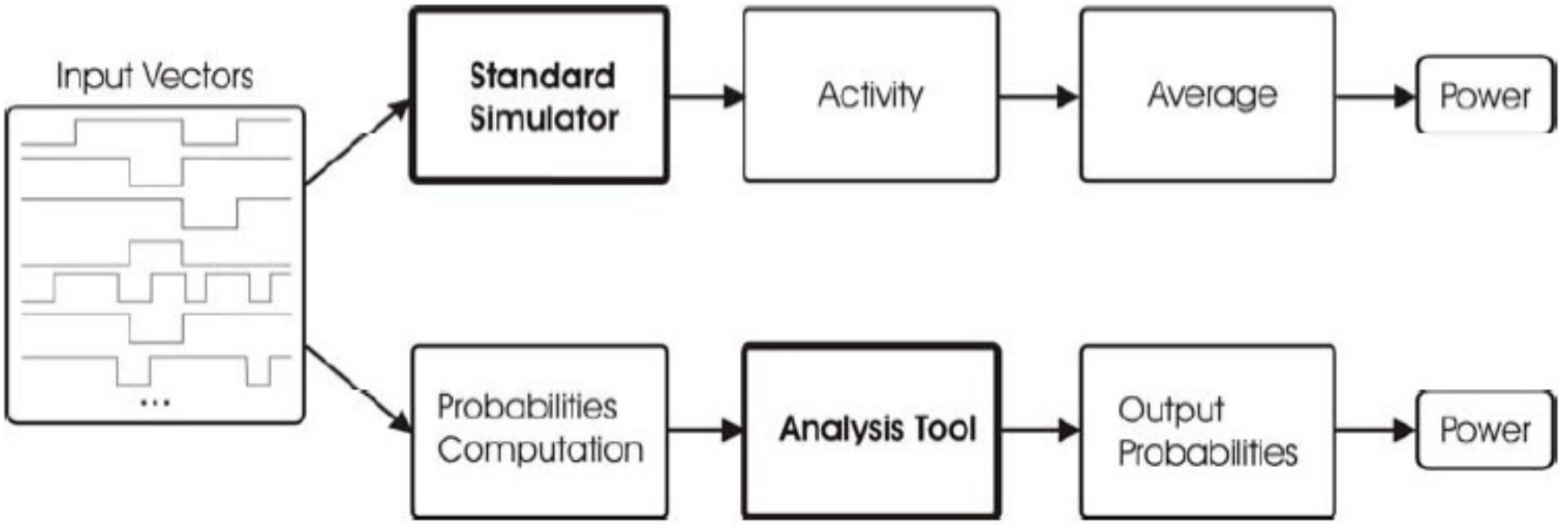


Fig. 3.1: Probabilistic (bottom) vs. Statistic approach (top)

Sequential Circuits

- Accurate average switching activity estimation for FSMs is considerably more difficult for two reasons:

  1. The probability of the circuit being in each of its possible states has to be calculated (maybe indirectly)

  2. The present state line inputs of the FSM are strongly correlated

     - Temporally correlated due to the machine behavior, as represented in its state transition graph
     - Spatially correlated because of the given state encoding.

Sequential Circuits

- Statistical Approaches
  - Power Consumption of the Sequential Circuit Combinational Part
  - Sequential Circuits with Multimodal Distributions in Power Consumption
  - A Technique to Generate a Random Sample in Sequential Circuits
  - Block Sampling in large Sequential Circuits

Herramientas en FPGAs

- Etapa temprana del diseño
  - Sirve para tener una estimación muy gruesa del consumo del diseño terminado
  - Planillas Excel (Altera, Xilinx)
- Final
  - Simuladores que usan información interna del chip
  - Altera: PowerPlay
  - Xilinx: XPower

Power Analysis Tools in FPGAs

- Xilinx Announces XPower Power Analysis Software for FPGA Design, San Jose, CA, Nov. 21, 2000, Xilinx Inc.

  http://investor.xilinx.com/phoenix.zhtml?c=75919&p=irol-wsArticle&ID=134100&highlight=

  - Xilinx was founded in 1984. AMD announced its acquisition of Xilinx in October 2020 and the deal was completed on February 14, 2022

- Altera's Quartus II Version 4.2 Delivers FPGA and CPLD Performance Leadership, San Jose, CA, December 6, 2004, Altera Corporation

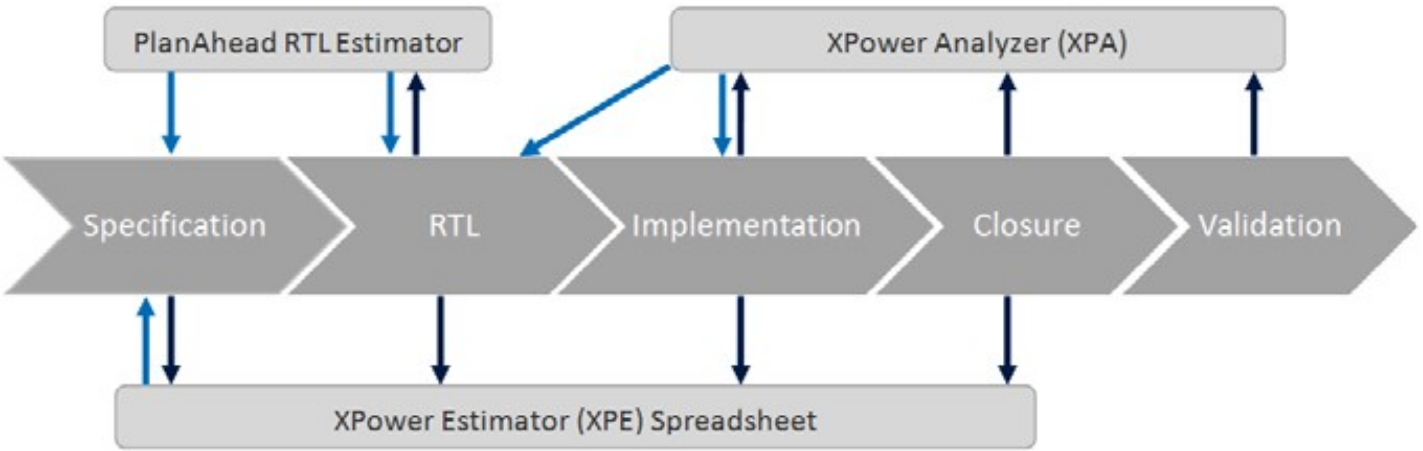
  http://www.altera.com/corporate/news_room/releases/releases_archive/2004/products/nr-quartusii_biz.html

  - Altera was founded in 1983 and acquired by Intel in 2015.

Xilinx Power Tools

- XPower Estimator (XPE)
  - Excel spreadsheet
  - Early phases of the project (predesign, pre-implementation)
- RTL Power Estimation
  - PlanAhead
  - RTL level
  - Early estimation
- XPower Analyzer (XPA)
  - ISE or PlanAhead
  - Post implementation
  - Most accurate tool

- Real measurements
  - Power measurements
  - Thermal measurements

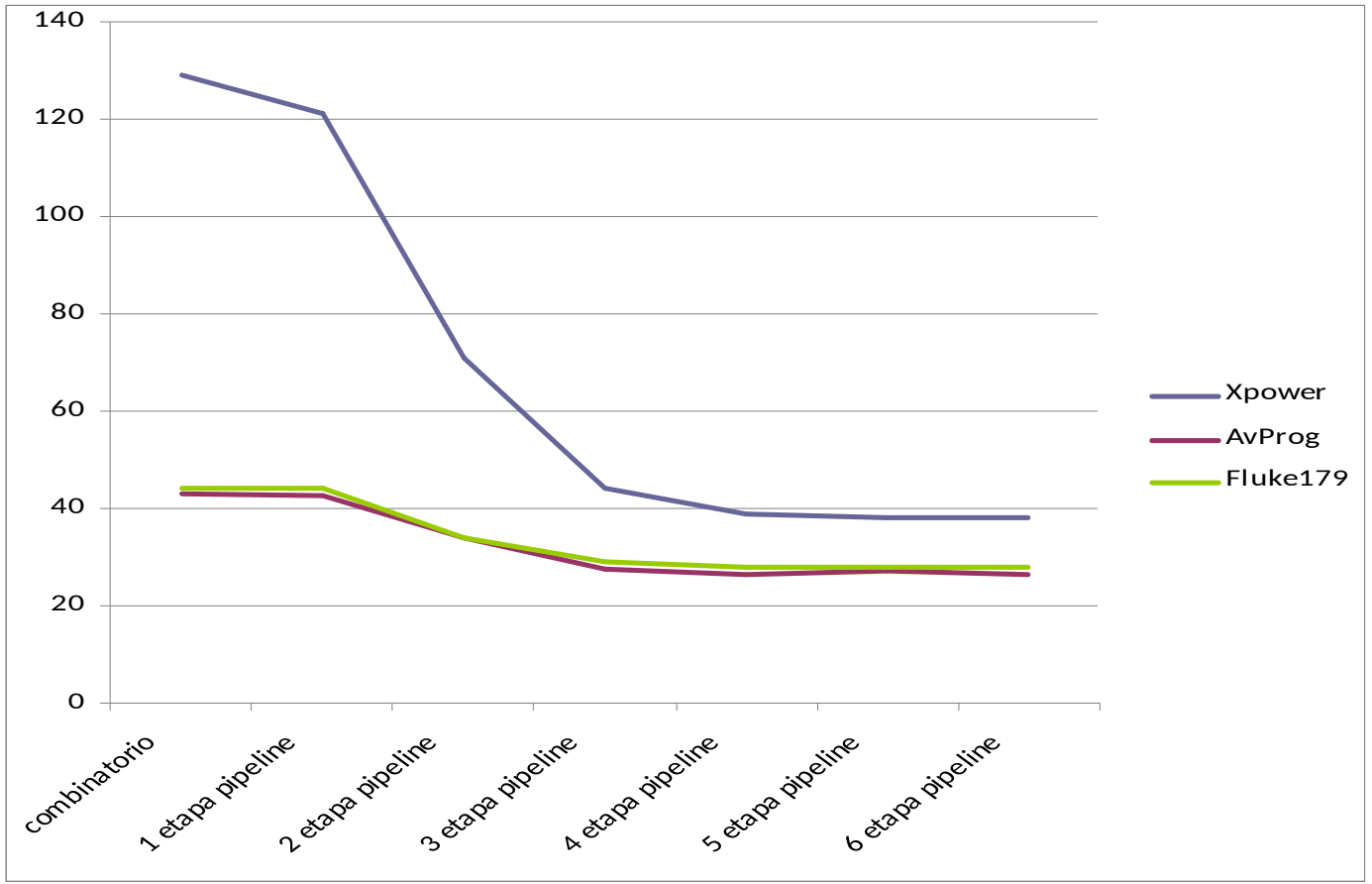


Source: Xilinx UG786 Power Methodology Guide

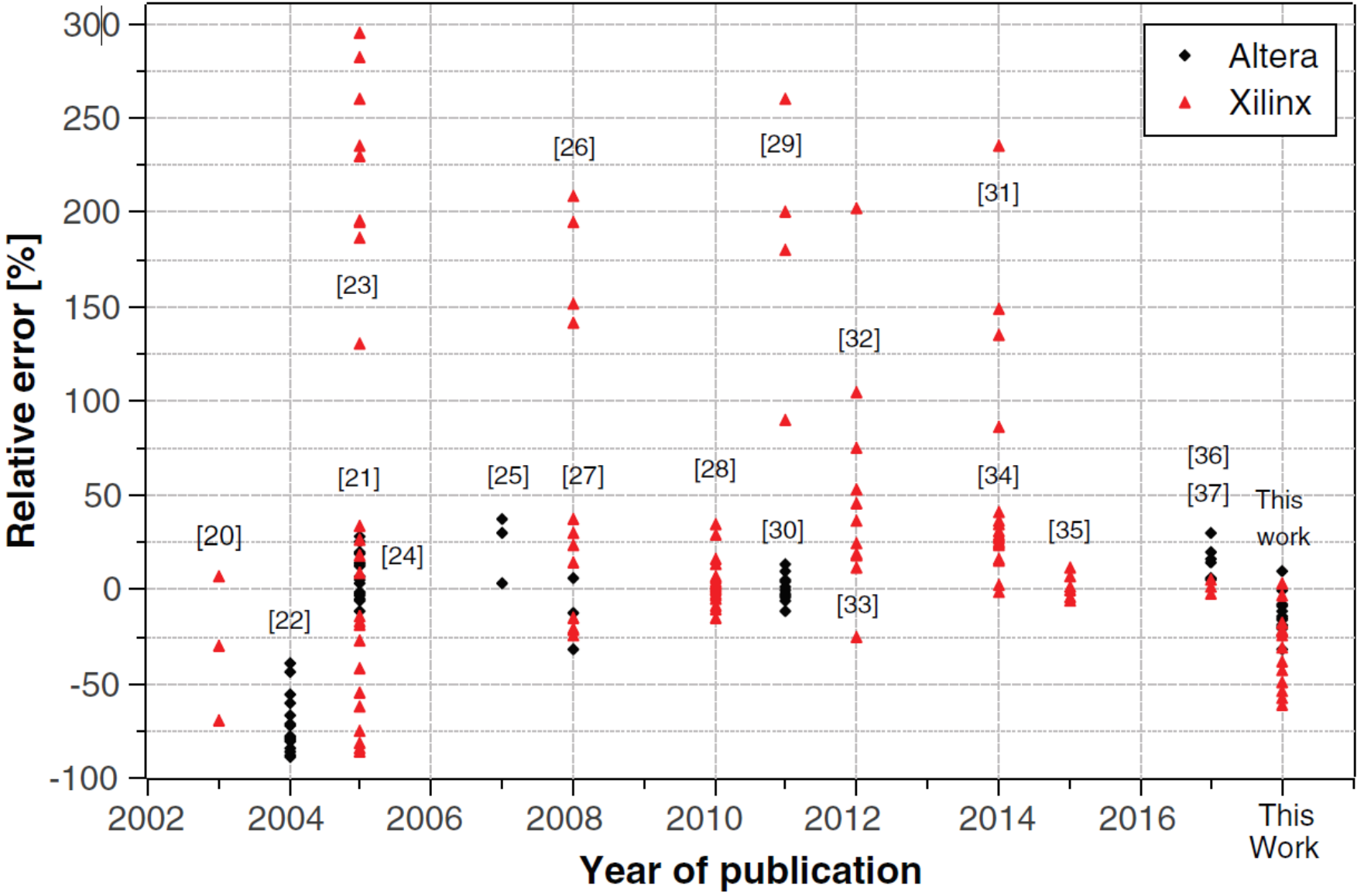
Estimación: Altera PowerPlay

		32x32			64x64	
Type of circuit	Measured (mA)	Estimated (mA)	Error (%)	Measured (mA)	Estimated (mA)	Error (%)
LUT	52,91	55,35	4,61	164,33	185,73	13,02
LUT 1 pipeline	39,22	38,65	-1,44	149,60	148,53	-0,72
LUT 2 pipeline	37,43	41,90	11,93	116,03	120,34	3,71
LUT 3 pipeline	40,12	43,90	9,43	102,26	103,19	0,91
LUT 4 pipeline	40,47	39,37	-2,71	110,78	108,34	-2,20
LUT 5 pipeline	41,93	39,61	-5,54	110,73	108,89	-1,66
LUT 6 pipeline	54,17	51,05	-5,75	111,50	107,08	-3,96
Embedded mult	16,78	17,53	4,47	39,45	34,85	-11,66
Embedded mult 1 pipeline	17,42	16,45	-5,57	33,57	33,19	-1,12
Embedded mult 2 pipeline	18,81	17,98	-4,41	37,57	36,25	-3,50
Embedded mult 3 pipeline	21,76	21,33	-1,98	39,20	37,10	-5,36

Xilinx Xpower



- Xpower: Error mayor con mayor profundidad de lógica


Altera
Xilinx
Relative error [%]
300
250
200
150
100
50
0
-50
-100
2002
2004
2006
2008
2010
2012
2014
2016
This Work
Year of publication
[20]
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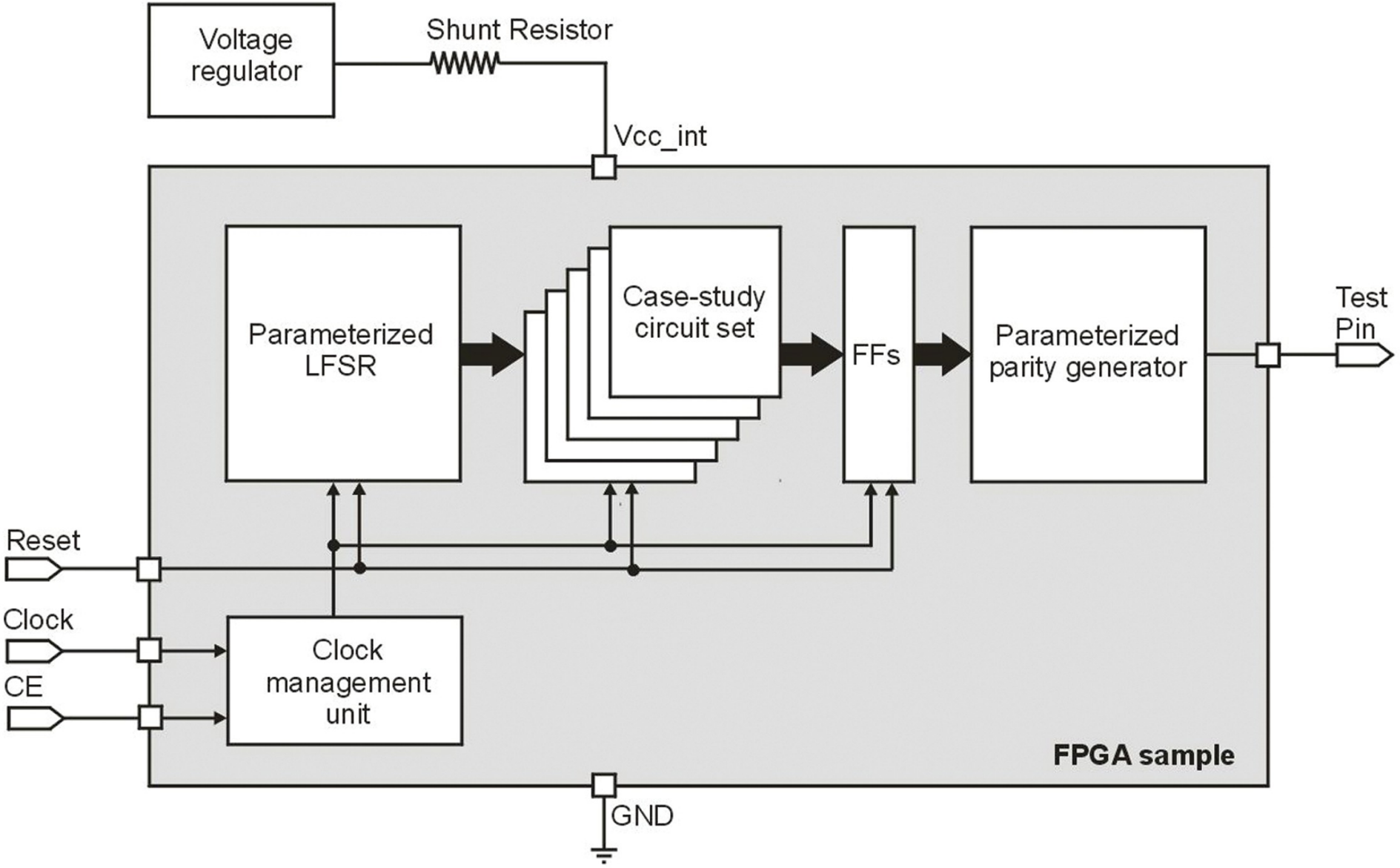
[35]
[36]
[37]
This work

Estimación “best-case”

- Simular circuito con entradas “reales” un tiempo “suficientemente” largo
- Generar y grabar el “activity file”
  - Resume la actividad de cada linea y FF
  - Hay dos formatos:
    - Guarda todo
    - Guarda % de actividad
- Usar simulador de consumo
  - Post place & route
  - Usar información del “activity file”

Oliver, J.P., Favaro, F. and Boemo, E., 2019. A framework to compare estimated and measured power consumption on FPGAs. Journal of Low Power Electronics, 15(4), pp.329-337. Accessed on: Sept 7, 2021. [Online]. Available:DOI: https://doi.org/10.1166/jolpe.2019.1622


Voltage regulator
Shunt Resistor
Vcc_int
Parameterized LFSR
Case-study circuit set
FFs
Parameterized parity generator
Test Pin
Reset
Clock
CE
Clock management unit
FPGA sample
GND

A Standarized Framework to Evaluate Power Estimation Tools

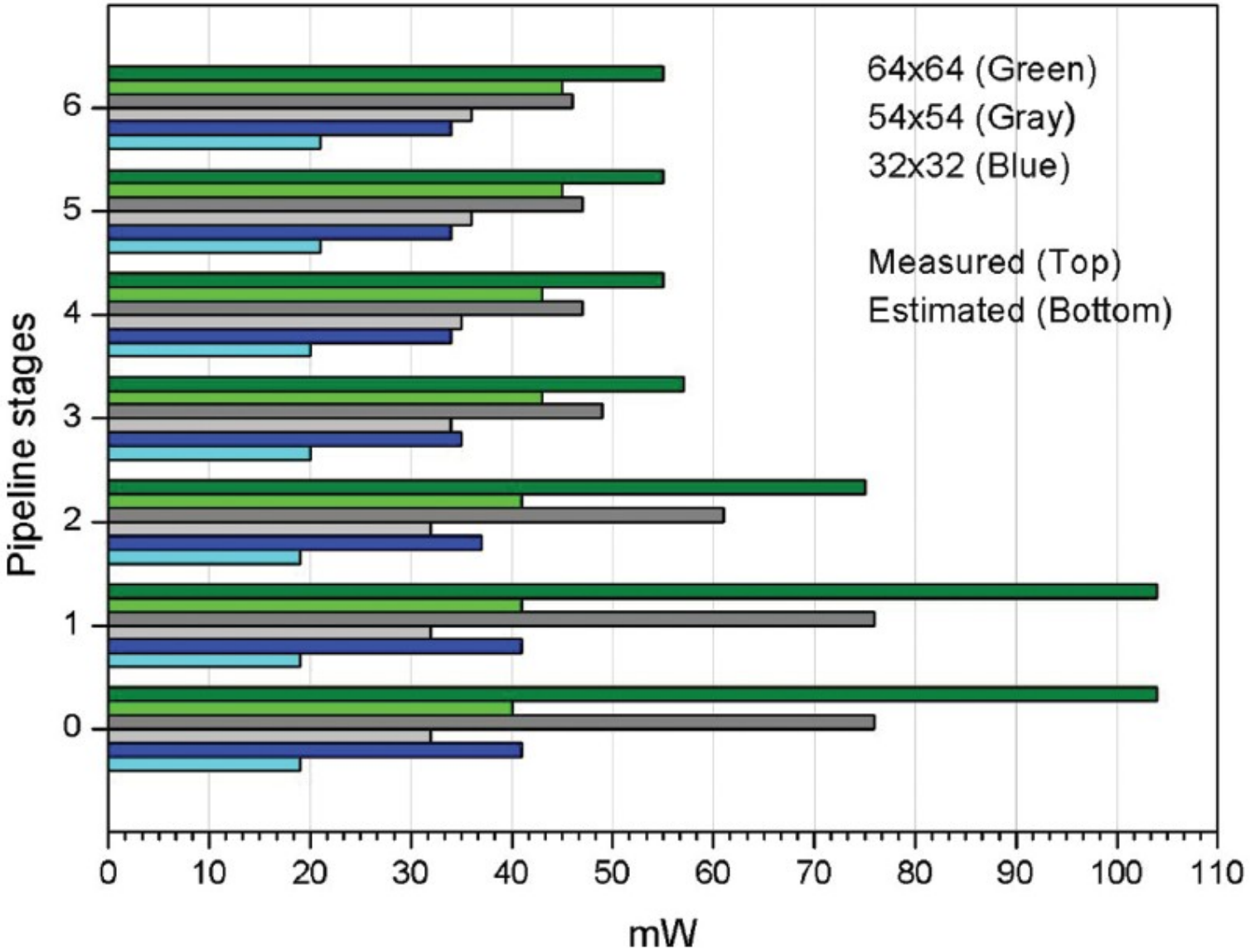
1) A set of IP cores is selected as benchmark circuits. (include diverse real-life applications, fully synthesizable.
2) For each circuit, a post place and route simulation is done using predefined patterns of input data.
3) The switching activity information of all circuit nodes is extracted from the simulation.

   SAIF (Simulation Activity File) in Xilinx

   VCD (Value Change Dump) in Intel.
4) The switching activity file is loaded into the power estimation tool (adjust temperature)
5) Each benchmark circuit is loaded into a FPGA and the power consumption during normal operation is measured.
6) Finally, the estimated power consumption is compared with the measured one and the relative error is computed.

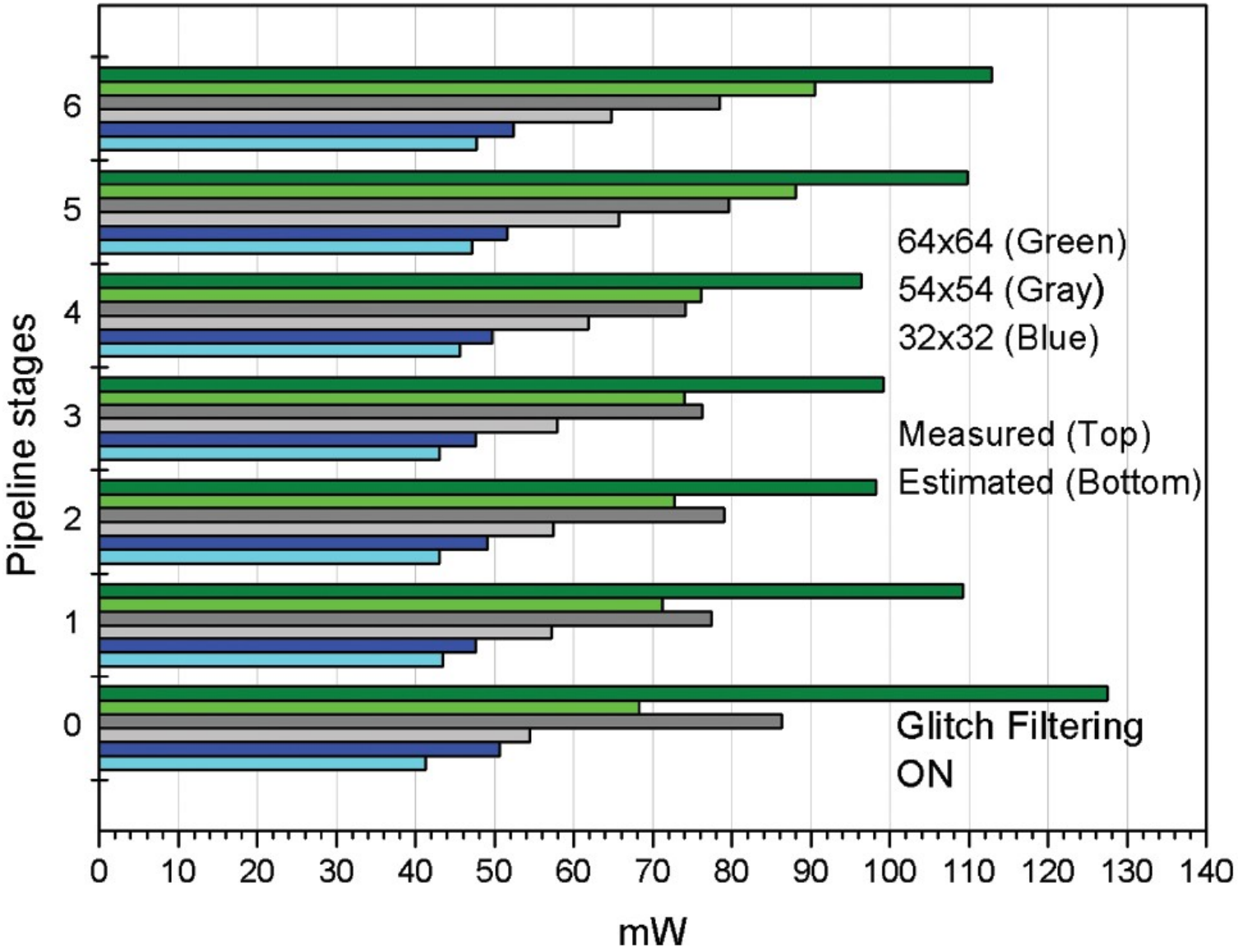
Estimation Flow

- First, the complete system (after place and route stage) is simulated.
- During the simulation, the tool must be configured to register the activity of each node in a file.
- Finally, the power estimation tool uses this data to perform the calculation, taking into account the laboratory room temperature.

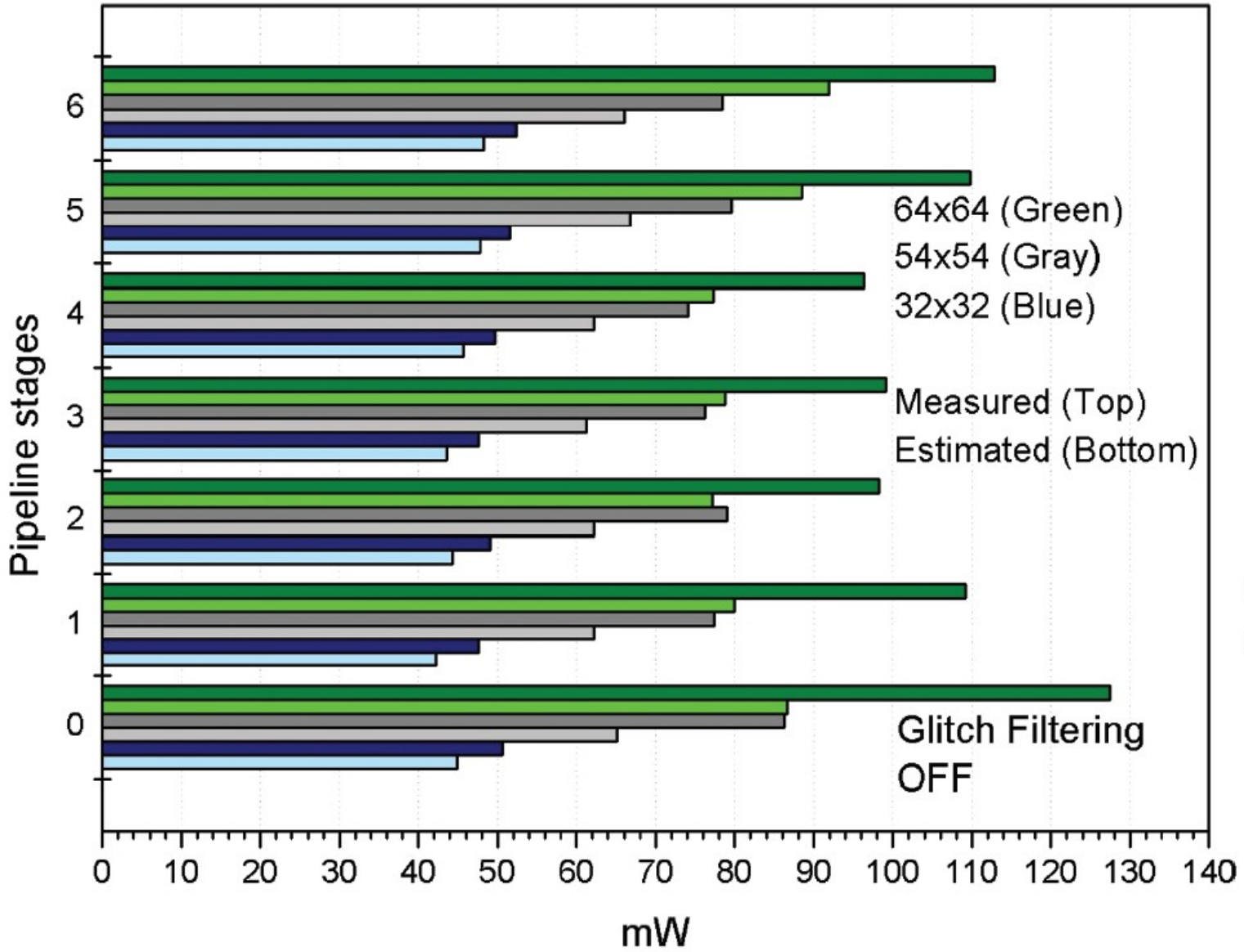


Results Xilinx

Arty 7 Multipliers



Results Altera
Cyclone V



Results Altera

Cyclone V

Table II. Benchmark IP cores characteristics for Xilinx.

Type of circuit	LUTs	Registers	RAM kbits	DSPs	MHz
AES	1832	1115	0	0	100
FFT	3260	5034	90	0	100
IEEE802154	777	376	0	0	8
openMSP430	1754	822	54	1	50
Mult 32×32	1103	0	0	0	25
Mult 54×54	3065	0	0	0	25
Mult 64×64	4290	0	0	0	25

Table III. Power consumption of benchmark IP cores in Artix-7.

Type of circuit	Estimation (mW)	Measurement (mW)	Relative error (%)
AES	71.3	69.1	3.1
FFT	117.8	121.2	−2.8
IEEE802154	10.5	20.6	−49.4
openMSP430	22.8	29.5	−22.8
Mult 32×32	18.1	39.0	−53.7
Mult 54×54	30.4	72.2	−57.9
Mult 64×64	38.0	98.8	−61.5

Table IV. Benchmark IP cores characteristics for Intel.

Type of circuit	ALUTs	Registers	RAM kbits	DSPs	MHz
AES	1991	2030	2.05	0	100
FFT	3242	5282	42.66	4	100
IEEE802154	1883	395	0.04	2	8
openMSP430	1755	1000	40.96	1	50
Mult 32×32	818	0	0	0	50
Mult 54×54	2113	0	0	0	50
Mult 64×64	3175	0	0	0	50

Table V. Power consumption of Benchmark IP cores in Cyclone V.

Type of cicuit	Glitch filtering (ON/OFF)	Estimation (mW)	Measurement (mW)	Relative error (%)
AES	ON	83.8	105.6	−20.7
	OFF	89.3	105.6	−15.4
FFT	ON	135.4	166.3	−18.6
	OFF	142.2	166.3	−14.5
IEEE802154	ON	37.8	39.2	−3.7
	OFF	39.1	39.2	−0.5
openMSP430	ON	45.2	44.3	2.1
	OFF	48.3	44.3	9.2
Mult 32×32	ON	45.4	55.7	−18.5
	OFF	49.4	55.7	−11.3
Mult 54×54	ON	60.0	94.9	−36.8
	OFF	71.6	94.9	−24.6
Mult 64×64	ON	75.1	140.2	−46.4
	OFF	95.5	140.2	−31.9

¿Entonces?

- ¿Cómo trabajar con consumo?
  - Medidas
  - Estimaciones

Power Measurements

- Pros
  - Real data of power consumption!!
- Cons
  - Is not the “worst case”
    - Differences between samples
    - Thermal influence
  - Stimulus pattern generation
  - Lab equipment
  - Boards with measurement capabilities

Conclusiones

- Medir
  - Da resultados reales
  - Pero tiene varios problemas
- Estimar
  - Error de estimación
  - Hay que “calibrar” resultados

Medir + Estimar + Analizar resultados