

E. Parimalasundar, R. Senthil Kumar, V.S. Chandrika, K. Suresh

## Fault diagnosis in a five-level multilevel inverter using an artificial neural network approach

**Introduction.** Cascaded H-bridge multilevel inverters (CHB-MLI) are becoming increasingly used in applications such as distribution systems, electrical traction systems, high voltage direct conversion systems, and many others. Despite the fact that multilevel inverters contain a large number of control switches, detecting a malfunction takes a significant amount of time. In the fault switch configurations diode included for freewheeling operation during open-fault condition. During short circuit fault conditions are carried out by the fuse, which can reveal the freewheeling current direction. The fault category can be identified independently and also failure of power switches harmed by the functioning and reliability of CHB-MLI. This paper investigates the effects and performance of open and short switching faults of multilevel inverters. Output voltage characteristics of 5 level MLI are frequently determined from distinctive switch faults with modulation index value of 0.85 is used during simulation analysis. In the simulation experiment for the modulation index value of 0.85, one second open and short circuit faults are created for the place of faulty switch. Fault is identified automatically by means of artificial neural network (ANN) technique using sinusoidal pulse width modulation based on distorted total harmonic distortion (THD) and managed by its own. The **novelty** of the proposed work consists of a fast Fourier transform (FFT) and ANN to identify faulty switch. **Purpose.** The proposed architecture is to identify faulty switch during open and short failures, which has to be reduced THD and make the system in reliable operation. **Methods.** The proposed topology is to be design and evaluate using MATLAB/Simulink platform. **Results.** Using the FFT and ANN approaches, the normal and faulty conditions of the MLI are explored, and the faulty switch is detected based on voltage changing patterns in the output. **Practical value.** The proposed topology has been very supportive for implementing non-conventional energy sources based multilevel inverter, which is connected to large demand in grid. References 22, tables 2, figures 17.

**Key words:** artificial neural network, fast Fourier transform, multilevel inverter, sinusoidal pulse width modulation, total harmonic distortion.

**Вступ.** Каскадні багаторівневі інвертори H-bridge все частіше використовуються в таких пристроях, як розподільні системи, електричні тягові системи, системи прямого перетворення високої напруги та багато інших. Незважаючи на те, що багаторівневі інвертори містять велику кількість перемикачів, що управляють, виявлення несправності займає значний час. У конфігурації аварійного вимикача увімкнено діод для роботи в режими вільного ходу в умовах обриву несправності. При короткому замиканні аварійні стани виконуються запобіжником, який може визначити напрямок струму вільного ходу. Категорія несправності може бути визначена самостійно, а також відмова силових вимикачів, що порушує функціонування та надійність каскадних багаторівневих інверторів H-bridge. У цій статті досліджуються наслідки та характеристики обривів та коротких замикань багаторівневих інверторів. Характеристики вихідної напруги 5-рівневого інвертору часто визначаються характерними несправностями перемикача, при цьому при аналізі моделювання використовується значення індексу модуляції 0,85. В імітаційному експерименті значення індексу модуляції 0,85 в місці несправного перемикача створюються односекундні обриви і коротке замикання. Несправність ідентифікується автоматично за допомогою методу штучної нейронної мережі з використанням синусоїдальної широтно-імпульсної модуляції на основі спотвореного повного гармонійного спотворення та керується самостійно. **Новизна** запропонованої роботи полягає у застосуванні швидкого перетворення Фур'є та штучної нейронної мережі для ідентифікації несправного перемикача. **Мета.** Пропонована архітектура призначена для виявлення несправного комутатора при розмиканні та короткочасних відмовах, що має знизити повне гармонійне спотворення та забезпечити надійну роботу системи. **методи.** Запропонована топологія має бути спроектована та оцінена з використанням платформи MATLAB/Simulink. **Результати.** Використовуючи підходи швидкого перетворення Фур'є та штучної нейронної мережі, досліджуються нормальні та несправні стани багаторівневих інверторів, і несправний перемикач виявляється на основі моделей зміни напруги на виході. **Практична цінність.** Запропонована топологія дуже сприятлива для реалізації нетрадиційних джерел енергії на основі багаторівневого інвертора, пов'язаного з великим попитом у мережі. Бібл. 22, табл. 2, рис. 17.

**Ключові слова:** штучна нейронна мережа, швидке перетворення Фур'є, багаторівневий інвертор, широтно-імпульсна модуляція, повні гармонічні спотворення.

**1. Introduction.** Multilevel inverters (MLIs) have aroused huge attention in the examination of established manufacturing electric drive organizations in recent days, with the intention of reaching their power quality as well as demands. The key benefits of MLIs are the elimination of harmonic distortion in the output voltage waveform by increasing level capacity, and even the portability of battery packs or fuel including in intervals. Despite the fact that MLIs are an established technology that may be used in engineering applications, the failure of power electronic switches and fault analysis is a new research issue for researchers. It's used in engineering to check the condition of power switches in inverters. The number of levels in the inverter varies, as does the quantity of additional switching devices, increasing the risk of any one of the switches collapsing; hence, any such problem should be addressed at the outset so that the drive and motor processes are not accepted during abnormal situations. To improve system reliability, an effective problem diagnosis system must be implemented.

In [1] had investigated in both moderate and high-power applications of multilevel converters which play a significant role. MLIs come in three typical configurations: diode clamped, flying capacitor, and cascaded H-bridged. The modular design of cascaded H-bridged multilevel inverter (CHB-MLI) characteristics and performance are used to achieve medium voltage and high-performance characteristics. Short and open circuit faults are two types of failures which can occur in power switching devices in CHB-MLIs. Short circuit (SC) problems mostly damage, so protection from SC is required. Artificial neural network (ANN) approaches for SC protection by using high potency fuses and de-saturation method.

In [2] had analyzed open-circuit faults in power switches the device shutting down, and they can go undetected for a long time. This could cause secondary defects in the inverter or other drive components,

© E. Parimalasundar, R. Senthil Kumar, V.S. Chandrika, K. Suresh

culminating in the entire system being shut down and expensive repairs.

In [3] had investigated short-circuit faults in power electronic switches, on the other hand, are extremely damaging and necessitate special precautions to automatically shut down the entire drive. These types of failures must be identified and repaired in a microsecond in order to safeguard analogous semiconductor devices from damage in the converter leg. On the other perspective, extended open circuit fault behaviour of the power converters might cause the entire system. Expertise in fault behaviours, fault prediction, and fault diagnostics will be necessary to keep the MLI system functioning smoothly. The two aspects of power electronic device fault diagnosis are as follows: fault information acquisition, which entails gathering data whenever a failure occurs using a specific fault detection approach; and fault identification and characterization, which rely upon that specific of failure modes to recognize the category. The position of faults is identified by an algorithm which was developed in [4]. In [5] the open circuit fault can be caused by a number of factors, including a damaged inner wire, a transient short-circuits, or a gate driver failure. Over-voltage, over-current, safety component failure, and improper gating signal are some of the causes of SC failure. In [6] authors explained the recurrent neural network-based voltage stability for grid connected solar photovoltaic systems using static synchronous compensator with recurrent neural network. Authors in [7, 8] investigated a number of recent articles on problems such as the creation of inverted pulse width modulation (PWM) method in CHB-MLI systems. In [9] has analyzed fault analysis in inverter and also faults an inverter device is used continuously under abnormal settings, further issues will arise, resulting in severe consequences. Furthermore, the MLI is composed of several switching devices and the entire system is complex in structure, and there are numerous nonlinear impacts. As a result, MLIs need some novel diagnostic strategies which could not deal with nonlinear detection issues but also diagnose and locate faults easily. The device voltage and current of a multilayer inverter might vary based on the part and location of the faults. Some research concentrates on the device output current or voltage to assess fault form and position more quickly and easily, and then used the sample to expand a number of fault diagnosis techniques. Owing to the dangerous effects of SC faults on converter circuits, this type of fault must be detected as soon as possible. It is necessary to remember that certain circuit drivers are already in a position to detect defective switches. Hence considering the value of MV drives on the industry, robust detection mechanisms need to be discussed. In [10] had investigated electrical drives and devices require complex electrical converters to conform to high power requirements. MLI methods have also been tested as an approach to high and low voltage systems. Compared to traditional two-level inverters, MLIs produce major output voltage and low harmonic output current distortion.

The fundamental objectives of the proposed research effort is to develop a high-performance fault detection methodology for evaluating open and SC faults in MLI using enhanced signal processing and soft computing

techniques. The fast Fourier transform (FFT) technique and ANN approach are used to evaluate the spectrum properties of output voltage wave forms produced using both modeling and experimental investigations at various fault situations. By using FFT technique, extract salient features such as total harmonic distortion (THD) and harmonic contents of output voltage signal at different fault cases. The performance characteristics of the FFT-ANN model-based fault detection approach for MLIs can be compared to develop an effective fault diagnostic system. These concerns include the identification of switch faults and the monitoring of tolerances because parameters contribute to the reliability of the power converter systems. The validation of proposed model is implemented with the help of open and SC fault voltages and total harmonic distortion.

**2. Literature Review.** A fault-tolerant method for a CHB inverter was proposed in [11]. Additional versions provide the converter's trustworthy and efficient operation in the event of a failure. The recommended method utilises an additional cross-coupled cascaded H-bridged unit in addition to existing CHB components to preserve output voltage and ensure continuation of function in the event of an open/short-circuit fault.

In [12] was developed an innovative technique of fault diagnostics based on the minimum squares support vector machine using back propagation algorithm. Authors [13] established a digital circuit-based approach for identifying SC problems. The suggested approach detects two types of SC faults: hard switch fault and fault under load; it can be utilised through any switch, independent of its characteristics; and it does not employ artificial intelligence strategies and procedures when inverter function is in progress. Rough sets theory (RST) is used to create the digital diagnostic circuit, which optimizes and specifies a minimal set of variables required to identify problems. When the variables are subjected to RST, a sequence of diagnostic rules is generated. These criteria are implemented using simple logic operations, resulting in a digital diagnostics system.

In [14] had developed a fault diagnostic method for photovoltaic (PV) inverters that allows for various open-circuit fault analyses. In [15] recommended that a fuzzy-based fault detection technique be used to analyse a voltage source inverter supplied three-phase permanent magnet synchronous motor driving. The average current Park's vector approach, which uses phase current information, is used to calculate the fault symptom variables. A fuzzy logic approach is used to process fault symptom variables and recover faulty information from power switches. The suggested fault detection technique can identify and find not only two or more distinct open-circuit problems in switching devices, and moreover periodic failures in power switches, which may enhance the motor drive system's dependability. In a three-phase quasi-Z-source inverter, authors [16] proposed a method for detecting open-circuit failures. The proposed method is confined to Z-source inverters and is based on assessing the impact of shoot-through durations on state variables during switching periods. Defect site identification and open-circuit monitoring are the two steps of the proposed approach. After both steps of the open circuit fault

detection method have been completed, a redundant leg is activated and utilised in lieu of the failed limb. The recommended technique is validated by test results from a low-voltage q-ZSI device.

Authors [17] proposed a signal processing technique for detecting switch open-circuit faults and identifying the individual problematic switch, which will help with servicing and fault-tolerant functioning. The faulty phase and defective switching combination, consisting of the defective component and the switching on its diagonally, was identified using the stator phase currents statistical characteristics.

A fault diagnostic method comprised of multistate data processing through subsection variation analysis lock, and ANN which is created using feature extraction for the output currents of balanced and unbalanced stages. A novel generalized open-switch fault-diagnostic approach was proposed in [18]. In this detection method, defect prediction features are implemented as half-cycle mean bridge voltages for an N-level CHB-MLI, which are computed separately for positive and negative half cycles. Precedent half-cycle averages are utilised to anticipate these averages during open-circuit fault circumstances, which are then compared to observed values to determine the open-circuit fault. This fast detection approach may detect the faulty switch in cascaded inverters with many voltage levels by looking at one structural characteristic of the output voltage. This technique may successfully identify the faulty switch of the cascaded inverter using various level-shifted pulse width modulation methods, variable loading conditions, modulation indexes, and switching frequencies.

Authors [19] presented a novel fault-tolerant control technique for CHB-MLI to increase the greatest achievable voltage under faulty conditions. Instead of bypassing the damaged cell when a semiconductor breaks, this method uses it to generate voltage. Due to the lack of one level of defective cell voltage level, the voltage is decreased to half. In comparison to traditional fault-tolerant techniques, the maximum possible output voltage could be increased for the majority of problematic circumstances. In addition, the defective cell switching mechanism is changed to enhance the output voltage quality. A grid-connected single to three-phase multilevel converter with a fault-tolerant design was proposed in [20]. The induction motor drive can operate even if any of the power semiconductor switches have open circuit faults. A control mechanism on a single active front end converter was used to accomplish this. A separate control method is used to provide the power converter's on-grid fault tolerance capabilities. The control approach employed on a single grid-connected converter enhances the input power factor, resulting in a unity power factor at the source. The voltage control loop adjusts the DC-link voltage to get the command voltage.

The redundancy of the triangular carrier signals is a criterion for expanding sinusoidal pulse width modulation (SPWM) to numerous output voltage levels per phase-leg, according to [21]. The recommended control technique creates suitable modulation patterns for the CHB inverter by modifying a sinusoidal modulating pattern to fit within a single triangle carrier signal range. These frameworks

may be used on any level CHB inverter without any further control modifications.

To resolve the insulated gate bipolar transistor (IGBT) open-circuit failure problem of the propulsion inverter in a transmission line power supply system, subsequently, using the IGBT inverter open-circuit fault identification, a simulation model which is based on propulsion inverter structure is constructed, and different switching fault signal waveforms are evaluated. Secondly, the bus voltage magnitude data is poorly represented and turned into a fault signal using direct detection methodology.

The fault-tolerant five-level inverter technique described in [22] for open-end induction motor driving applications uses a single DC connection. One end of the drive is fed by a main inverter, while the other is fed by a supplemental inverter. The proposed approach, in compared to other current inverter systems, allows for five-level inverter operation with little interruption. Furthermore, the design is fault-tolerant in the case that the H-bridge switching devices and the extra two-level inverter fail.

Since these MLIs feature a large number of power semiconductors, the chance of failure is much higher. As a result, identifying potential faults and operating under faulty situations are critical. The identification of a failure might be complex in concept due to the large number of components. MLIs have interesting advantages due to their faulty structure, such as the ability to operate in medium, high voltage, and high-power applications, providing a better voltage waveform with low total harmonic distortion for electric machines applications, output filter elimination,  $dv/dt$  transient reduction during commutation, low electromagnetic interference emissions from over voltages, and reduced power loss.

### 3. Proposed method of fault diagnosis system in MLI.

Figure 1 illustrates literally the entire fault detection system set up for identifying defective power semiconductor switches in MLIs, which includes both MLI and fault diagnosis system. The characteristics of output voltage sequences were extracted using the FFT approach. Frequency domain analyses of the terminal voltage patterns are required to construct a significant application assessment method. The FFT approach was used to retrieve distinct attributes from the output voltage signal. Despite the fact that a skilled feature extractor should supply critical data facts more about ANN in the selected area, it was the highest degree of consistency reached within the adaptive intelligence network.

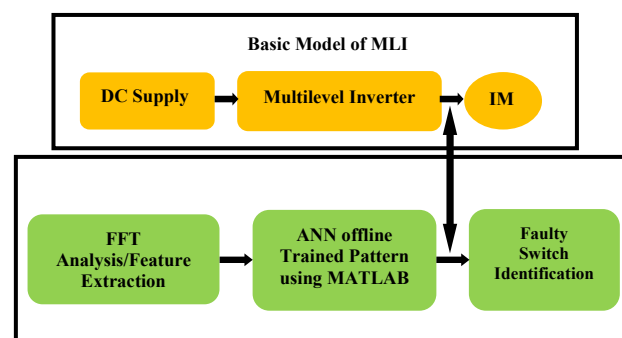


Fig. 1. Proposed fault diagnosis system of MLI



Figure 2 depicts the signal separation of output voltage in terms of harmonics and RMS voltage output. The FFT provides a frequency response representation for any periodic or non-periodic signal. Figure 3 depicts one of the 11<sup>th</sup> order sample harmonics, as well as THD and  $V_{rms}$  values, which are all utilized to extract characteristics from the output signal employing FFT analysis.

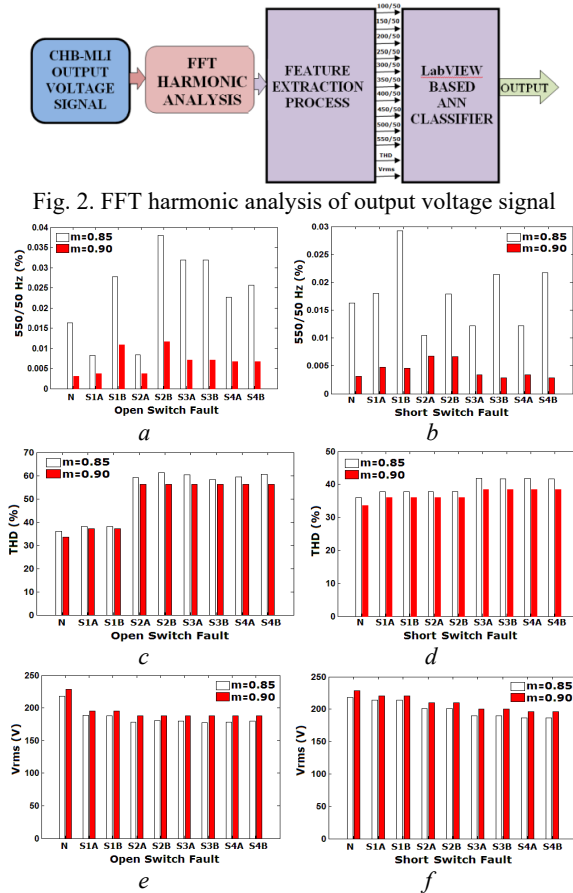


Fig. 2. FFT harmonic analysis of output voltage signal

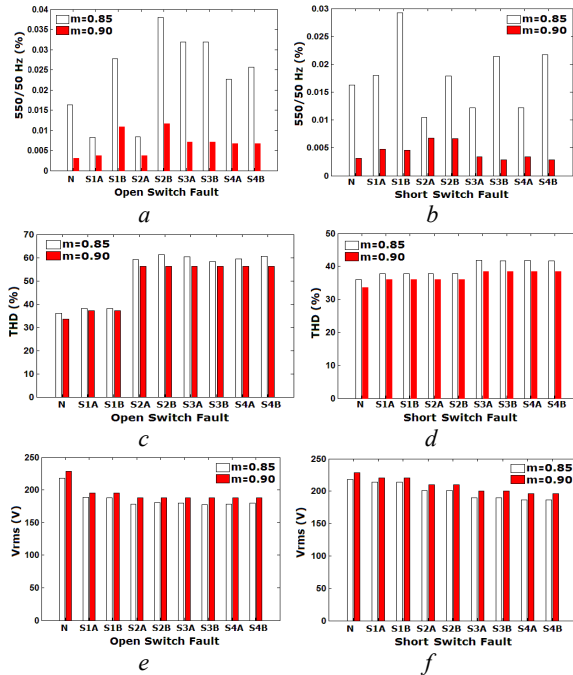


Fig. 3. Representation of FFT investigation during:

- 11<sup>th</sup> harmonic with open circuit fault;
- 11<sup>th</sup> harmonic with short circuit fault;
- THD analysis for open circuit fault;
- THD analysis for short circuit fault;
- $V_{rms}$  analysis for open circuit fault;
- $V_{rms}$  analysis for short circuit fault

The FFT provides frequency domain representation of any periodic or non-periodic signal. In general, the Fourier transform (FT) is a generalization of the Fourier series. Instead of sines and cosines, as in a Fourier series, the FT uses exponentials and complex numbers. For a signal or function  $f(t)$ , the FT is defined as:

$$F(\omega) = \int_{-\infty}^{\infty} f(t) \cdot e^{-j\omega t} dt. \quad (1)$$

The inverse FT is defined as:

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) \cdot e^{j\omega t} d\omega. \quad (2)$$

The expression below is used to calculate THD for an output voltage pattern as:

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}{V_1^2}}, \quad (3)$$

where  $V_n$  is the root means square (RMS) value of the voltage of the  $n^{\text{th}}$  harmonic;  $n = 1$  is the frequency of the signal. It determines the degree of distortion in a voltage output.

**A. Fault classification using ANN techniques.** In a multilayer feed forward network, Fig. 4 depicts the error back propagation. The back propagation technique is used to compute the necessary modifications once the network's weights are picked at random. The back propagation algorithm may be separated into four stages in general. The four steps of the back propagation algorithm are feed-forward processing, back propagation to the output layer, back propagation to the hidden layer, and weight changes. The algorithm is disrupted whenever the value of the error function has become reasonably low, i.e., when the error between the actual and planned output is less than a given number (convergence criteria). In this network, the deviation is back-propagated, and the weights and biases are essentially reconfigured using an approach to reduce the mean square error (MSE), which is the mean of all the errors for all sets of inputs and outputs, and is determined as:

$$MSE = \frac{1}{n} \sum_m^n (P_m - Q_m). \quad (4)$$

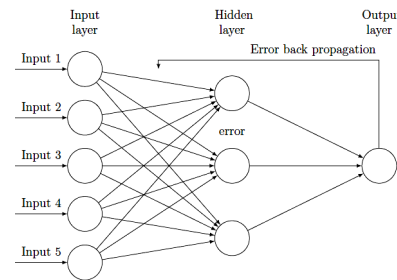


Fig. 4. Back propagation of error in multilayer feed forward network

In this case,  $P_m$  and  $Q_m$  are the desired and measured outputs for the  $m^{\text{th}}$  input set, where  $n$  is the total number of input sets. The failure detection of MLIs was automated using an ANN in this investigation. The ANN was used to solve the difficulty of detecting the faulty switch in a cascaded MLI. Due to its simple methodology and excellent predictive potential, the multilayer feed forward network with back propagation learning technique has been regarded one of the numerous ANN designs accessible in the literature.

Using the 9 output neurons, the fault is categorized as no fault, S1A to S4A fault, and S1B to S4B fault. The output layer neurons are set up to perform multiple binary training patterns in response to different degradation scenarios.

Network topology, size, and learning rate, number of training sets, convergence criterion, and number of iterations are all essential parameters that influence the neural network's convergence and learning time. The learning rate is known to damp out oscillations to some extent, during the training phase. Higher values of learning rate may result in fast convergence, but it may result in oscillation. The training time of the neural network will rise as the number of training sets and training cycle increases. For improved classification results, an appropriate neural network structure must be found. As a result, in order to arrive at an ideal topology,

the effectiveness of the neural network for varying parameters of the learning rate, training sets, convergence criterion, iterations, and number of neurons in the hidden layer must be examined in depth and assessed.

The majority of processing facilities in the hidden layer and the number of observations is two significant parameters that influence the neural network's functionality. The neural network fails to meet the convergence requirements when the number of hidden layer neurons is fewer than 10. The neural network takes longer to train and meet the convergence requirements when the quantity of hidden layer neurons rises over 24.

The current network achieves convergence criterion at 3800 iterations throughout the training phase. It shows that 3800 iterations are enough for the optimal neural network to be successfully trained. Then 150 more data points were employed for identification testing with modulation indices ranging from 0.8 to 0.95, which is as shown in Fig. 5.

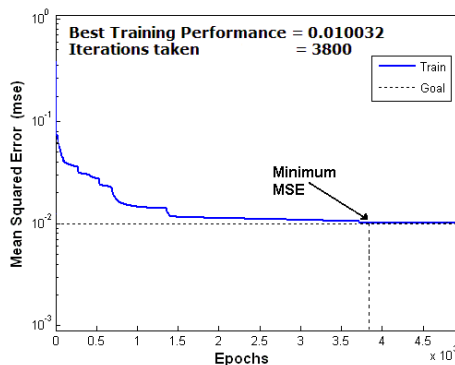


Fig. 5. Identification of best training performance of MSE

As the number of hidden layer neurons exceeds 18, the neural network takes more time to train and adhere to the convergence requirements. The network's mean square error was computed by keeping the step size at 0.1 with 18 hidden layer neurons in order to arrive at an optimal value for the number of epochs. The mean square error values derived from different amounts of hidden layer neurons are shown in Fig. 6 depicts the proposed fault diagnostic system's detection rates for various numbers of hidden layer neurons. As compared to other instances, the device performs better with 18 secret layer neurons. In this context, the overall detection performance for all fault conditions is 100 %, and the device can correctly find the fault in nearly any situation.

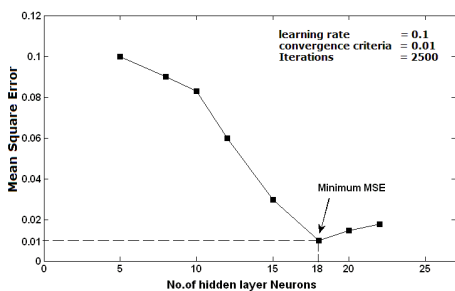


Fig. 6. Investigation of the ANN-MSE at various statistics of hidden layer neurons for 18

### B. Fault classification using ANN techniques.

Cascaded H-bridged inverter topology consists of a series of H-bridge inverter cells are interconnected to each cell

at each point with a different DC voltage configuration. Figure 7 shows that there is a traditional cascaded H-bridged inverter topology with three H-bridged cells attached to the three-phase inductive motor load at each point. The degree of waveforms in the output signal ranges may be calculated using  $2N+1$ , where  $N$  is typically the size of H-bridged cells in the network.

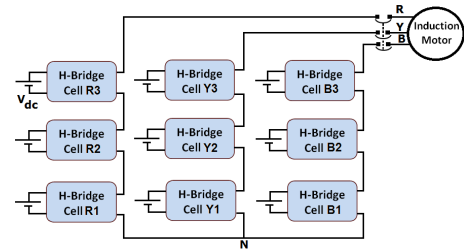


Fig. 7. Structure of traditional three phase cascaded H-bridged inverter topology comprising induction motor

However a three-phase MLI strategy is typically used across drive systems, a single-phase MLI may be used at this point, while a three-phase based fault detection system could be expanded.

Figure 8 shows the schematic single-stage, five-stage voltage output of the CHB-MLI used in existing positions correlated with induction motor load. Induction motor characteristics such as unbalanced stator currents and voltages, torque oscillations, efficiency and torque decreases, overheating, and excessive vibration are all affected if the MLI power semiconductor switches fail. Furthermore, some harmonic components of currents and voltages can be amplified by these motor problems. To achieve good performance, the defective switch must be identified and replaced as quickly as possible. Each IGBT switch is categorized as S1A, S1B, etc. by its cell position. The simulation experiments have been performed using the MATLAB/Simulink tool and Table 1 summarizes the parameters used for the simulation analysis.

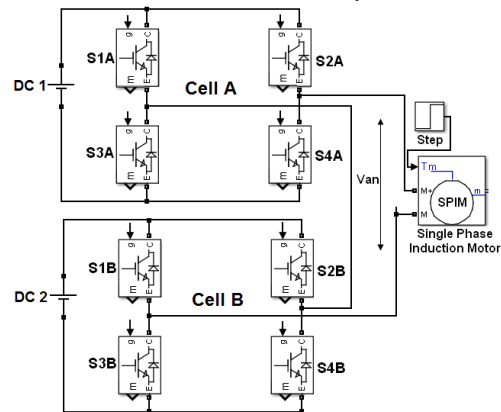


Fig. 8. Single-phase cascaded H-bridged 5-level MLI coupled to the drive system

Table 1

Simulation parameters of five level MLI	
Parameters	Values
DC input voltage	115 V
Number of H-bridges	2
No. of switches	4
Output levels	5
Modulation Index	0.85
Carrier frequency	3 kHz
Load	Single phase IM, 0.5 HP, 50 Hz, 230 V

**C. Fault classification using ANN techniques.** The SPWM switching technique is frequently utilised to create the requisite IGBT transition pulses. The pulse of the triangular carrier is the same as the reference sinusoidal signal when SPWM is resented. As illustrated in Fig. 9; the switching signals are processed using a sinusoidal and triangular signal with a modulation index of 0.85. The technique of SPWM addresses sinusoidal waveform creation by contrasting reference to carrier waves or filtering the pulse output waveform by altering the widths of triangular waveforms. The basic pulse generation circuit for the sine pulse width modulation technique is shown in Fig. 9. Low frequency reference sinusoidal waveforms are compared with high frequency triangular waves, often known as carrier waves. The switching phase is changed when the sine and carrier waves cross is shown in Fig. 10.

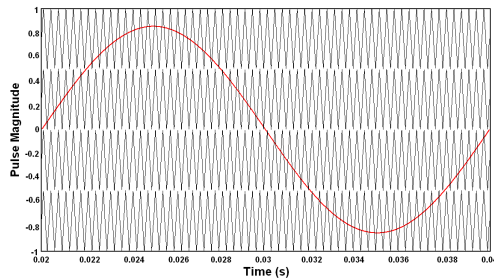


Fig. 9. The sinusoidal reference signal and the triangular carrier signal in PWM are used for modulation index of 0.85 carrier frequency of 3 kHz values

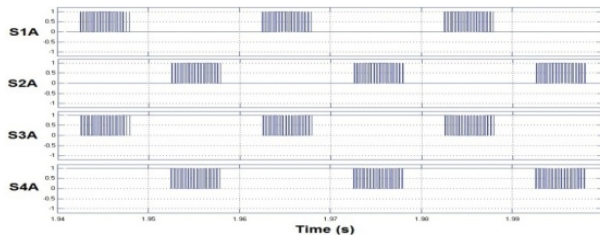


Fig. 10. SPWM based cell A switching pulses are generated by 3 kHz carrier frequency and 0.85 modulation index

Table 2 illustrates the switching patterns of five level cascaded MLI during healthy condition. SPWM based cell A switching pulses are generated by 3 kHz carrier frequency and 0.85 modulation index is shown in Fig. 4.

Table 2

Switching table of five level cascaded MLI								
Switching sequences								Voltage levels
Bridge – A				Bridge – B				
S1	S4	S2	S3	S1	S4	S2	S3	
1	1	0	0	1	1	0	0	+2V <sub>DC</sub>
1	1	0	0	0	0	0	0	+V <sub>DC</sub>
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	–V <sub>DC</sub>
0	0	1	1	0	0	1	1	–2V <sub>DC</sub>

Mode 1: Five level cascaded H-Bridge inverter switches S1 & S2 – A and S1 & S2 – B are turned on in this mode of operation.  $+2V_{DC}$  is the output voltage obtained across the load.

Mode 2: Five level cascaded H-Bridge inverter switches S1 & S2 – A is turned on in this mode of operation.  $+V_{DC}$  is the output voltage obtained across the load.

Mode 3: Five level cascaded H-Bridge inverter switches, all the bridge switches are zero, the output voltage obtained across the load is zero.

Mode 4: Five level cascaded H-Bridge inverter switches S3 & S4 – A is turned on in this mode of operation.  $+V_{DC}$  is the output voltage obtained across the load.

Mode 5: Five level cascaded H-Bridge inverter switches S3 & S4 – A and S3 & S4 – B are turned on in this mode of operation.  $+2V_{DC}$  is the output voltage obtained across the load. The same operation is shown in tabular form above in Table 2.

#### 4. Results and discussion.

**A. Open circuit fault analysis and discussion.** The primary open circuit failure occurs around 1 s with the bridged cell A switch in S1A to determine the voltage level output before and after the start of the open circuit failure of the MLI. Figure 11 reflects the typical output voltage, amplified view and output current at both the failure of such a single stage cascaded H-bridge inverter topology related to the inductive motor. Related voltages and pulses are sampled at 20 kHz, which is shown in Fig. 11.

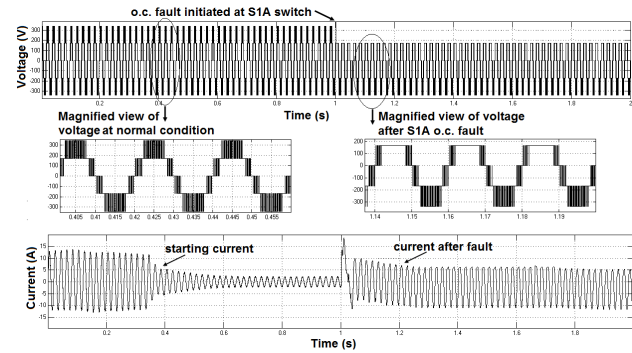


Fig. 11. Voltage and load current pattern of cascaded H-bridged inverter topology with inductive motor before and after S1A switch open circuit fault initialization

Figure 10 displays the typical output waveforms given by the normal and independent open-switch voltage fluctuations of cells A and B according to the basic requirements of the 0.85 modulation index. In the case of open switch fault waveforms, there is a fifty percent clipping at the voltage magnitude level in the positive or negative half of the time as opposed to no fault condition. Figure 11 illustrates the output voltage and current waveforms when an open circuit fault occurs in cell A's S2A switch. Visual examination of voltage and current waveforms reveals that the output voltage amplitude pattern varies significantly for each open circuit fault; however, classifying the sort of fault solely on the load current waveform is difficult. The equivalent load current waveform appears to follow a similar pattern following the onset of an open circuit fault in switches S1A and S2A, making it difficult to differentiate the problematic switch. Figure 12 shows the output voltage and load current waveforms with an induction motor load following an S2A open circuit fault. Figure 13 depicts the typical output voltage waveforms of cells A and B at 0.85 modulation index values under normal, open-switch fault circumstances, respectively. When comparing open switch fault voltage waveforms to no fault conditions, there is a fifty percent clipping in the voltage magnitude level in the positive or negative half cycle. When comparing the output voltage waveforms under open-

switch fault scenarios to the normal state, there is a significant variation in all output voltage patterns. These waveform images clearly depict the fluctuations at each problem instance, which can help to create a fault detection system that is more efficient.

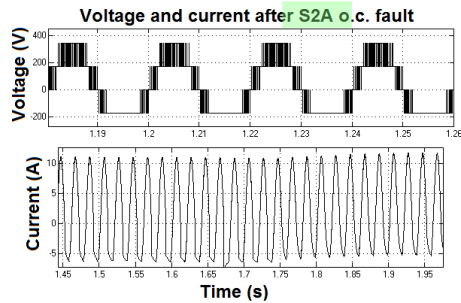


Fig. 12. Voltage and current after S2A open circuit fault

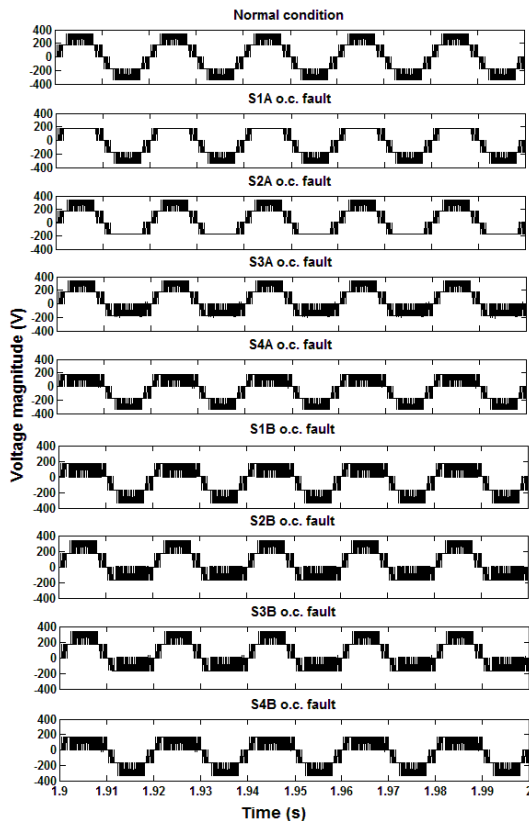


Fig. 13. Output voltage waveforms at normal condition and after open switch fault of Cell A and B

**B. Short circuit fault analysis and discussion.** The initial short-circuit fault is triggered by one second (1 s) of the H-bridge A S1A switch to consider the pre and post current and voltage series starting the short-circuit fault of the inverter topology. The output displays the normal output voltage and current waveform of the H-bridged multilevel cascaded single-phase inverter. The short circuit fault of S1A is generated at one second (1 s) and Fig. 14 shows the embellished current and voltage waveform and also shows the start of the fault. Figure 15 illustrates a magnified view of the output voltage and load current waveforms with an induction motor load following an S1B short circuit failure. Figure 16 shows the output voltage and load current waveforms with an induction motor load following an S1B short circuit fault. Figure 16 displays the standard output waveforms obtained under the normal and distinct short switch fault

conditions of cells A and B at the 0.85 modulation index value respectively. As a consequence, there is a small decrease in the output voltage and in the positive or negative half loop in the case of short switch fault waveform generation. As a result of a detailed inspection of the output voltage waveforms, it has been a significant change in all voltage output patterns in both the open-switch and short-switch voltage fluctuations as opposed to normal conditions. These waveform diagrams explicitly display the variations for each fault situation, which would help encourage the development of a successful fault detecting system.

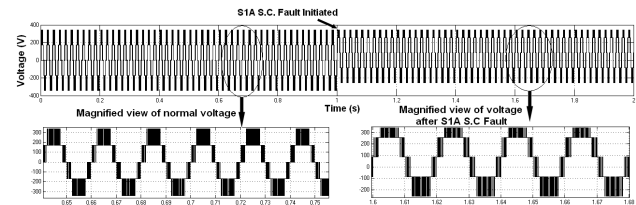


Fig. 14. Output voltage and load current waveform of MLI during short circuit condition

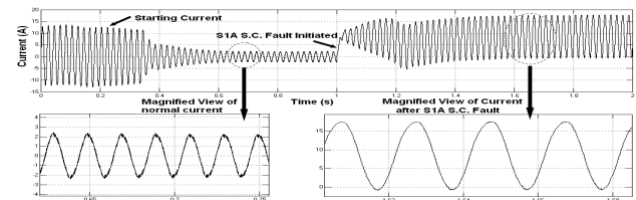


Fig. 15. Magnified view of fault analysis before and after the initiation of S1A short circuit fault with induction motor load  $m = 0.85$ . Fault initiated at 1 s

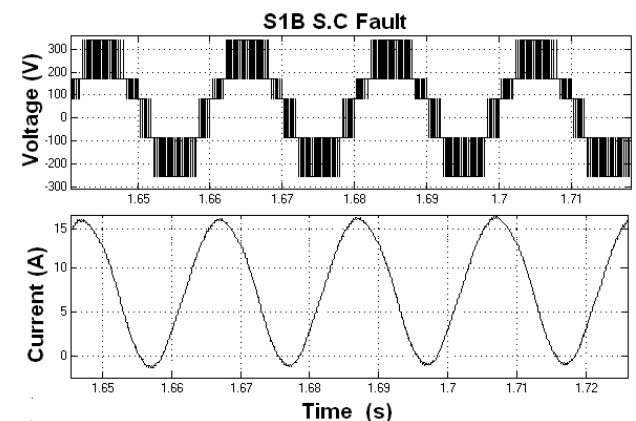


Fig. 16. Output current and voltage waveform of S1B SC fault with induction motor load for the modulation index of 0.85

Figure 15 illustrates visual examination of waveforms reveals that the output voltage pattern varies somewhat for each SC fault; however, classifying the nature of the fault solely on the load current is difficult. The load current pattern of a SC fault in S1A and S1B, for example, is identical, making it difficult to distinguish between the S1 switch faults in H-bridge A and H-bridge B. Furthermore, the type of the load and its changes affect the load current waveform. As a result, it's possible that a switch issue will be misdiagnosed. The output voltage waveform is a crucial parameter to create the fault diagnosis system since it is irrespective of load and has unique patterns for each switch problem. When a SC fault develops in cell B's S1B switch, Fig. 16 depicts the output voltage and current waveforms. Visual examination of voltage and current waveforms indicates



that the output voltage magnitude waveform for each SC fault varies greatly, however diagnosing the fault type purely based on the load current waveform is challenging. Following the commencement of a SC defect in switches S1B and S2B, the equivalent load current waveform seems to follow a similar pattern, making it difficult to differentiate the faulty switch.

Figure 17 depicts the typical output voltage waveforms of cells A and B at 0.85 modulation index values under normal, short-switch fault circumstances, respectively. When comparing short switch fault voltage waveforms to no fault conditions, there is a 50 % clipping in the voltage magnitude level in the positive or negative half cycle. When comparing the output voltage waveforms under short-switch fault scenarios to the normal state, there is a significant variation in all output voltage patterns. These waveform images clearly depict the fluctuations at each problem instance, which can help to create a fault detection system that is more efficient.

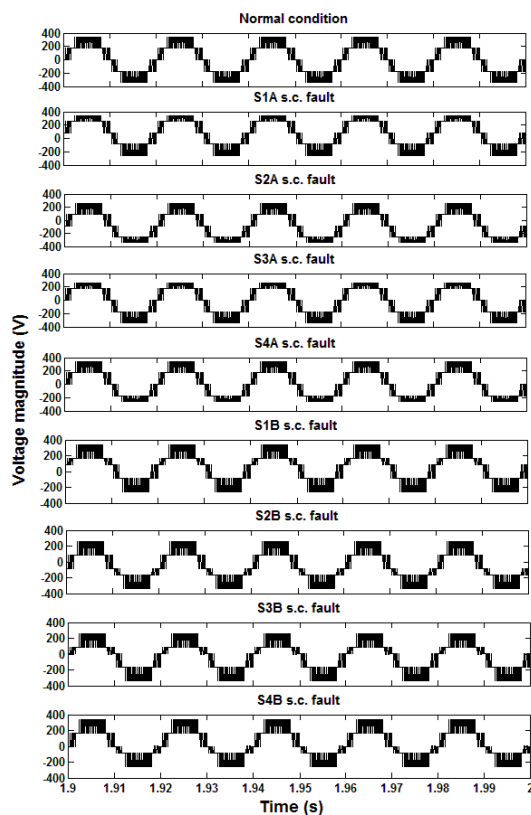


Fig. 17. Voltage output patterns in normal state as well as short circuit fault states of cells A and B

The key properties of the load voltage output waveform are explored utilising simulation under various open-switch and short-switch faulty conditions. Furthermore, major elements such as THD analysis using the FFT technique, as well as an assessment of the MSE at various numbers of hidden layer neurons, are defined to be fed to that back propagation trained ANN. In a cascaded MLI, this suggested fault detection approach could identify each individual fault switch. When compared to the load current pattern, the output voltage waveform at different fault circumstances exhibits distinct patterns, making it easier to discern the nature of the defect via visual observation. THD and harmonic/fundamental ratios up to 11<sup>th</sup> order harmonics retrieved from the FFT analysis give crucial information

regarding the malfunctioning switch of the MLI. For high power applications, the number of levels of MLIs is rising day by day; the suggested system may be tested for 7 level and 9 level inverter system.

**5. Conclusions.** This paper examines the malfunctioning transition fault diagnosis of a single-phase H-bridged cascaded 5-level inverter topology attached to the inductive motor. Specified output voltage waveform properties are explored through simulation research in various open-switch and short-switch fault conditions. This approach focuses on the similarity of the output voltage and indeed the modulated voltage signal, as well as on the effect of the modification of the multilevel inverters on the discrepancy. Digital filters may be created and implemented in the future for real-time applications while recording the output voltage signal to remove high-frequency noise. The suggested topology is restricted to a five-level multilevel inverter, but it may be expanded to seven, nine, eleven, and more levels. As the number of switches increases, so would the need for identification to locate a faulty switch. Also, the transients detected in the current signal during the open circuit or short circuit faults of the multilevel inverter may be studied and a diagnostic procedure created using this information for 7-level and 9-level inverters.

**Conflict of interest.** The authors declare that they have no conflicts of interest.

## REFERENCES

1. Jahan H.K., Panahandeh F., Abapour M., Tohidi S. Reconfigurable Multilevel Inverter With Fault-Tolerant Ability. *IEEE Transactions on Power Electronics*, 2018, vol. 33, no. 9, pp. 7880-7893. doi: <https://doi.org/10.1109/TPEL.2017.2773611>.
2. Haji-Esmaili M.M., Naseri M., Khoun-Jahan H., Abapour M. Fault-Tolerant and Reliable Structure for a Cascaded Quasi-Z-Source DC-DC Converter. *IEEE Transactions on Power Electronics*, 2017, vol. 32, no. 8, pp. 6455-6467. doi: <https://doi.org/10.1109/TPEL.2016.2621411>.
3. Jalhotra M., Gautam S.P., Kumar L., Gupta S., Chander A.H. Fault Tolerance and Energy Sharing Analysis of a Single Phase Multilevel Inverter Topology. *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 1209-1213. doi: <https://doi.org/10.1109/IECON.2018.8591853>.
4. Amini J., Moallem M. A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters. *IEEE Transactions on Industrial Electronics*, 2017, vol. 64, no. 3, pp. 1818-1826. doi: <https://doi.org/10.1109/TIE.2016.2624722>.
5. Babaei E., Laali S., Bayat Z. A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches. *IEEE Transactions on Industrial Electronics*, 2015, vol. 62, no. 2, pp. 922-929. doi: <https://doi.org/10.1109/TIE.2014.2336601>.
6. Praveen Kumar T., Ganapathy S., Manikandan M. Improvement of voltage stability for grid connected solar photovoltaic systems using static synchronous compensator with recurrent neural network. *Electrical Engineering & Electromechanics*, 2022, no. 2, pp. 69-77. doi: <https://doi.org/10.20998/2074-272X.2022.2.10>.
7. Suresh K., Parimalasundar E. A Modified Multi Level Inverter with Inverted SPWM Control. *IEEE Canadian Journal of Electrical and Computer Engineering*, 2022, vol. 45, no. 2, pp. 99-104. doi: <https://doi.org/10.1109/ICJECE.2022.3150367>.
8. Suresh K., Parimalasundar E. A novel dual-leg DC-DC converter for wide range DC-AC conversion. *Automatika*, 2022, vol. 63, no. 3, pp. 572-579. doi: <https://doi.org/10.1080/00051144.2022.2056809>.
9. Suresh K., Parimalasundar E. Design and Implementation of Universal Converter. *IEEE Canadian Journal of Electrical and*



Computer Engineering, 2022, vol. 45, no. 3, pp. 272-278. doi: <https://doi.org/10.1109/ICJECE.2022.3166240>.

10. Ezhilvannan P., Krishnan S. An Efficient Asymmetric Direct Current (DC) Source Configured Switched Capacitor Multi-level Inverter. *Journal Européen Des Systèmes Automatisés*, 2020, vol. 53, no. 6, pp. 853-859. doi: <https://doi.org/10.18280/jesa.530611>.

11. Mhiesan H., Wei Y., Siwakoti Y.P., Mantooth H.A. A Fault-Tolerant Hybrid Cascaded H-Bridge Multilevel Inverter. *IEEE Transactions on Power Electronics*, 2020, vol. 35, no. 12, pp. 12702-12715. doi: <https://doi.org/10.1109/TPEL.2020.2996097>.

12. Cheng Y., Dong W., Gao F., Xin G. Open-circuit fault diagnosis of traction inverter based on compressed sensing theory. *Chinese Journal of Electrical Engineering*, 2020, vol. 6, no. 1, pp. 52-60. doi: <https://doi.org/10.23919/CJEE.2020.000004>.

13. De Mello Oliveira A.B., Moreno R.L., Ribeiro E.R. Short-Circuit Fault Diagnosis Based on Rough Sets Theory for a Single-Phase Inverter. *IEEE Transactions on Power Electronics*, 2019, vol. 34, no. 5, pp. 4747-4764. doi: <https://doi.org/10.1109/TPEL.2018.2861564>.

14. Huang Z., Wang Z., Zhang H. Multiple Open-Circuit Fault Diagnosis Based on Multistate Data Processing and Subsection Fluctuation Analysis for Photovoltaic Inverter. *IEEE Transactions on Instrumentation and Measurement*, 2018, vol. 67, no. 3, pp. 516-526. doi: <https://doi.org/10.1109/TIM.2017.2785078>.

15. Yan H., Xu Y., Cai F., Zhang H., Zhao W., Gerada C. PWM-VSI Fault Diagnosis for a PMSM Drive Based on the Fuzzy Logic Approach. *IEEE Transactions on Power Electronics*, 2019, vol. 34, no. 1, pp. 759-768. doi: <https://doi.org/10.1109/TPEL.2018.2814615>.

16. Yaghoubi M., Moghani J.S., Noroozi N., Zolghadri M.R. IGBT Open-Circuit Fault Diagnosis in a Quasi-Z-Source Inverter. *IEEE Transactions on Industrial Electronics*, 2019, vol. 66, no. 4, pp. 2847-2856. doi: <https://doi.org/10.1109/TIE.2018.2847709>.

17. Yang S., Sun X., Ma M., Zhang X., Chang L. Fault Detection and Identification Scheme for Dual-Inverter Fed OEWM Drive. *IEEE Transactions on Industrial Electronics*, 2020, vol. 67, no. 7, pp. 6112-6123. doi: <https://doi.org/10.1109/TIE.2019.2922924>.

18. Anand A., Akhil Vinayak B., Raj N., Jagadanand G., George S. A Generalized Switch Fault Diagnosis for Cascaded H-Bridge Multilevel Inverters Using Mean Voltage Prediction. *IEEE Transactions on Industry Applications*, 2020, vol. 56, no. 2, pp. 1563-1574. doi: <https://doi.org/10.1109/TIA.2019.2959540>.

19. Ouni S., Narimani M., Zargari N.R., Cheng Z. A New Fault-Tolerant Control Method for Cascaded H-Bridge Multilevel

Inverter to Increase Maximum Output Voltage. *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2922-2927. doi: <https://doi.org/10.1109/ECCE.2019.8912282>.

20. Parimalasundar E., Kumar N.M.G., Geetha P., Suresh K. Performance investigation of modular multilevel inverter topologies for photovoltaic applications with minimal switches. *Electrical Engineering & Electromechanics*, 2022, vol. 6, pp. 28-34. doi: <https://doi.org/10.20998/2074-272X.2022.6.05>.

21. Odeh C.I., Lewicki A., Morawiec M. A Single-Carrier-Based Pulse-Width Modulation Template for Cascaded H-Bridge Multilevel Inverters. *IEEE Access*, 2021, vol. 9, pp. 42182-42191. doi: <https://doi.org/10.1109/ACCESS.2021.3065743>.

22. Ghosh Majumder M., Rakesh R., Gopakumar K., Umanand L., Al-Haddad K., Jarzyna W. A Fault-Tolerant Five-Level Inverter Topology with Reduced Component Count for OEIM Drives. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2021, vol. 9, no. 1, pp. 961-969. doi: <https://doi.org/10.1109/JESTPE.2020.2972056>.

Received 13.05.2022

Accepted 20.08.2022

Published 06.01.2023

Ezhilvannan Parimalasundar<sup>1</sup>, Associate Professor,  
Ramanathan Senthil Kumar<sup>2</sup>, Assistant Professor,  
Vanitha Selvaraj Chandrika<sup>3</sup>, Professor,  
Krishnan Suresh<sup>4</sup>, Associate Professor,  
<sup>1</sup>Department of Electrical & Electronics Engineering,  
Sree Vidyanikethan Engineering College,  
Tirupati, AP – 517102, India,  
e-mail: parimalasundar.e@vidyanikethan.edu (Corresponding Author);  
<sup>2</sup>Department of Electrical and Electronics Engineering,  
SRM Institute of Science and Technology,  
Chennai, TN – 603203, India,  
e-mail: rskrren@gmail.com  
<sup>3</sup>Department of Electrical and Electronics Engineering,  
KPR Institute of Engineering and Technology,  
Coimbatore, TN – 641407, India,  
e-mail: mailchandrika@gmail.com  
<sup>4</sup>Department of Electrical and Electronics Engineering,  
Christ (Deemed to be University), Bangalore, India,  
e-mail: sureshk340@gmail.com

#### How to cite this article:

Parimalasundar E., Senthil Kumar R., Chandrika V.S., Suresh K. Fault diagnosis in a five-level multilevel inverter using an artificial neural network approach. *Electrical Engineering & Electromechanics*, 2023, no. 1, pp. 31-39. doi: <https://doi.org/10.20998/2074-272X.2023.1.05>