Team NAN
RISC-V Processor

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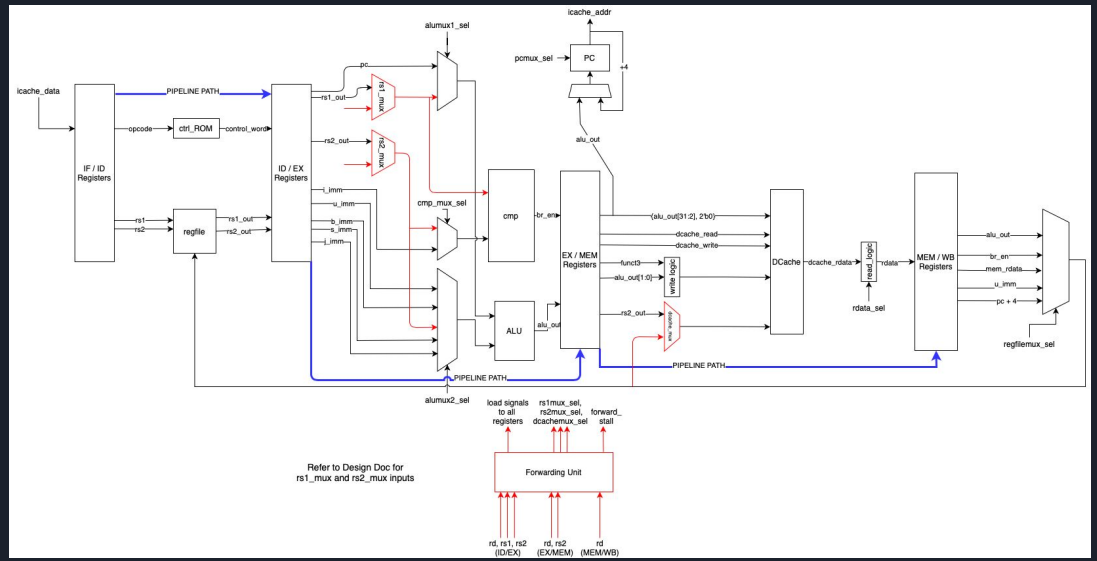
Overview & Advanced Features

There are 3 main improvements we made to the baseline RISC-V Processor...

- Perceptron Branch Prediction with 4-way Set Associative BTB
- Conversion from 8-Way Direct Mapped L1 Cache to 16-set Direct Mapped L1 Cache
- 8-way Set Associative L2 Cache



Perceptron Branch Prediction & 4-Way Set Associative BTB Cache

Description

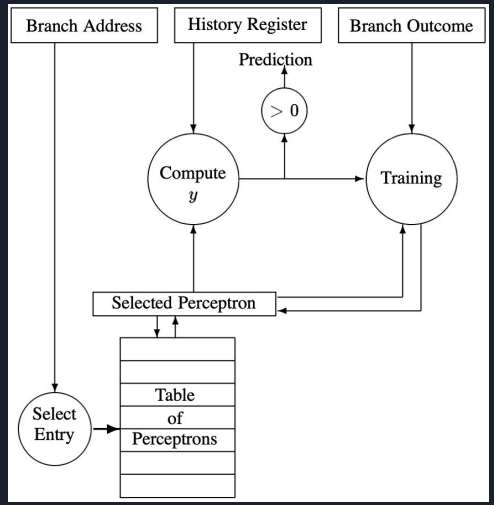
Global Branch History Length: 12

Table Size: 32 Perceptrons

Improvements

- Heavy usage of BTB with **84%** hit rate.
- Prediction accuracy above **60%** for conditional branching.
- Prediction accuracy above **69%** for unconditional branching.

	BTB %	Conditional Branch %	Unconditional Branch %
COMP 1	84.80%	71.87%	78.61%
COMP 2	93.51%	60.69%	69.28%
COMP 3	98.75%	75.60%	86.91%



Paper Referenced: https://www.cs.utexas.edu/~lin/papers/hpca01.pdf

Perceptron Branch Prediction with BTB

Performance Increase of **6.15%**

when compared to the baseline implementation.

	Baseline			Perceptron		
	COMP 1	**COMP 2**	**COMP 3**	**COMP 1**	**COMP 2**	**COMP 3**
F_max		104.94			101.10	
Power (*mW*)		460.74		519.97	504.12	480.8
Time (*ns*)	2,296,295	7,017,795	4,409,605	2,114,875	6,743,795	4,313,505
Total Score		3.27E-08			3.08E-08	

8-Way Set Associative L2 Cache (Adv. Feature) & 16-set Direct Mapped L1 Cache (Improvement)

Description

Data Line Size: 256 bits

Tag Size: 24 bits

LRU: 7 bits

Valid / Dirty: 1 Bit

Improvements

- Inclusive L2 cache has decreased complexity compared with exclusive.
- Drastically reduced memory hits due to high hit percentage

	L2 Cache Hit %
COMP 1	96.96%
COMP 2	98.90%
COMP 3	93.05%

8-Way Set Associative L2 Cache (Adv. Feature) & 16-set Direct Mapped L1 Cache (Improvement)

Performance Improvement of **3151.33%**

when compared to our baseline implementation.

	Baseline			L2 Cache + 16-Way L1		
	COMP 1	**COMP 2**	**COMP 3**	**COMP 1**	**COMP 2**	**COMP 3**
F_max	104.94			102.28		
Power (*mW*)	460.74			724.50	728.34	645.85
Time (*ns*)	2,296,295	7,017,795	4,409,605	695,385	1,830,825	1,132,355
Total Score	3.27E-08			1.01E-09		

Overall Performance Improvements

Performance Improvement of **3349.35%**

when compared to our baseline implementation.

	Baseline			Final Processor		
	COMP 1	**COMP 2**	**COMP 3**	**COMP 1**	**COMP 2**	**COMP 3**
F_max	104.94			89.75		
Power (*mW*)	460.74			776.83	779.01	692.86
Time (*ns*)	2,296,295	7,017,795	4,409,605	659,405	1,606,455	1,074,455
Total Score	3.27E-08			9.49E-10		

Potential Improvements for Design Choices

- Implement BRAM memory for faster accesses
- Implement tournament branch predictor for better branch prediction accuracies
- Change from 16-set direct mapped caches to 8-set 2-way set associative cache.
- START EARLIER

Thank you for a great semester!

TEAM NAN: Naveen, Anchit, Neo