

SWITCHED CAPACITOR STEP UP SINGLE PHASE 5 LEVEL INVERTER FOR PV APPLICATION

GUIDED BY
PROF. T G SANISH KUMAR

TEAM
ADHEEB SHIBU VATTASSERIL
ANOOP K C
BASTIN BABU C
CHARLES GEORGE

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INTRODUCTION

Recently, multilevel inverters (MLI) are getting more attention from researchers because of advantages like

- **Better waveform quality**
- **Lower EM noise**
- **Lower device stress**

MLIs are used to couple a DC source to an AC bus for applications like electric motor drivers, uninterrupted power supplies, and distributed generation systems.



OBJECTIVES

1

High power quality with minimum distortion factor.

2

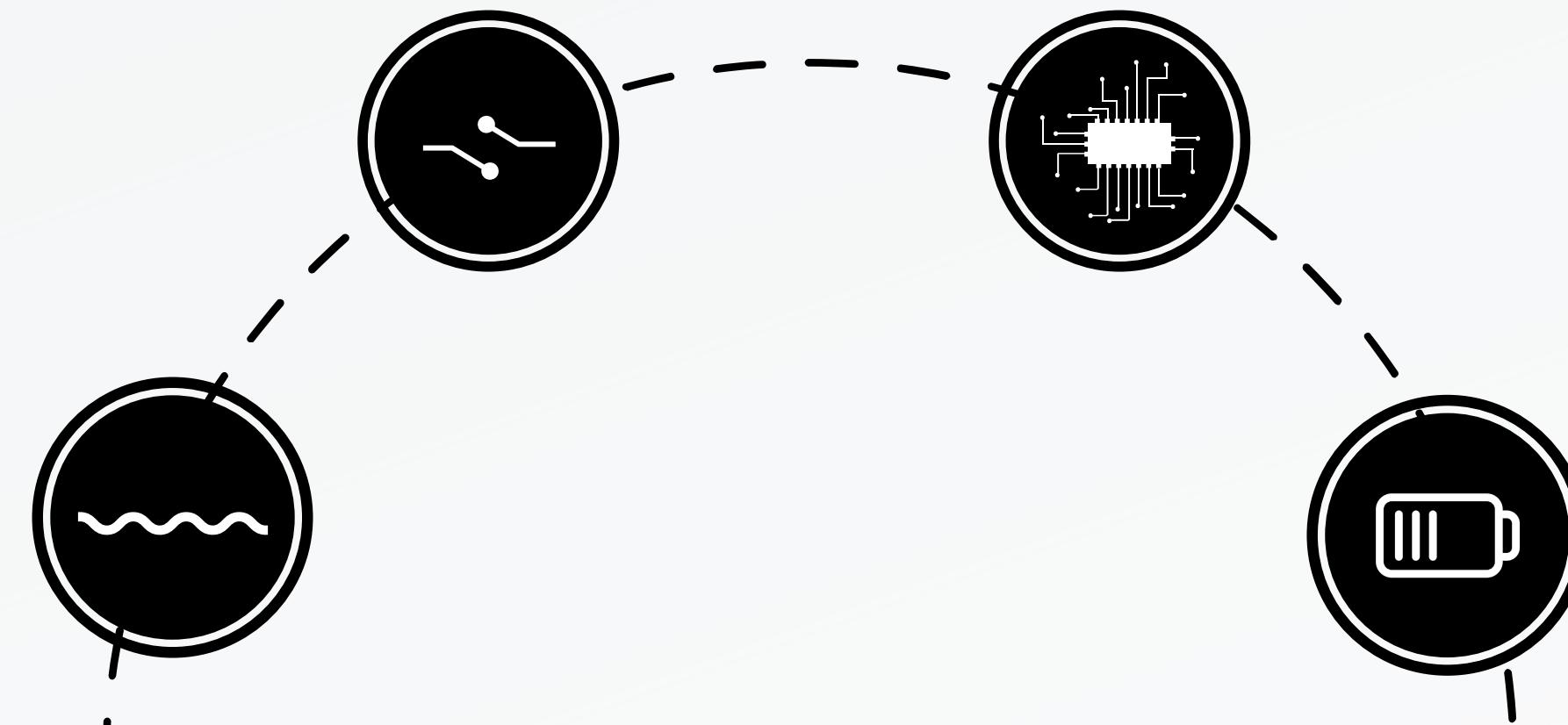
Minimal usage of semiconductor switches.

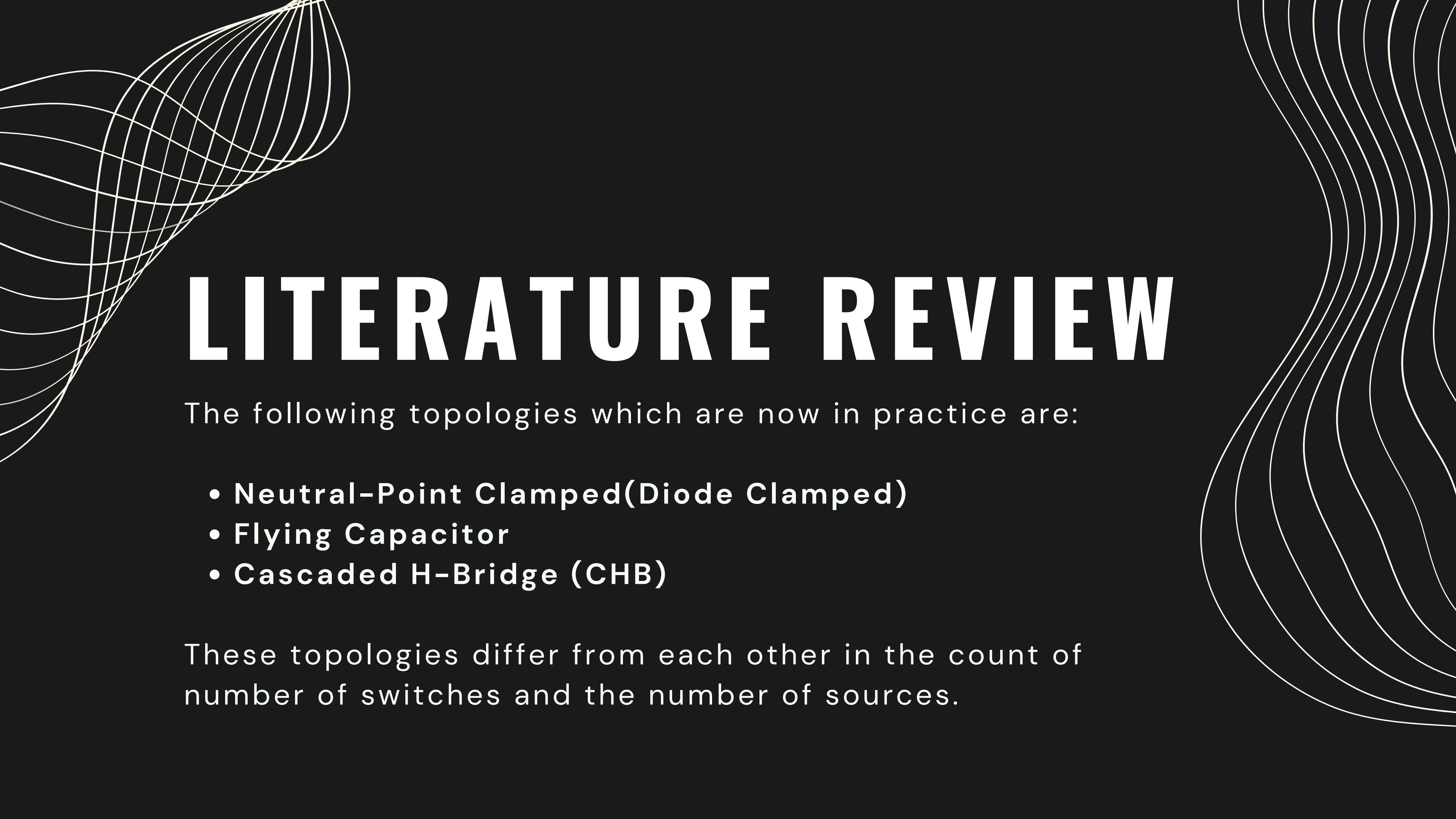
3

Eliminate complex control schemes.

4

To reduce DC link voltage.





LITERATURE REVIEW

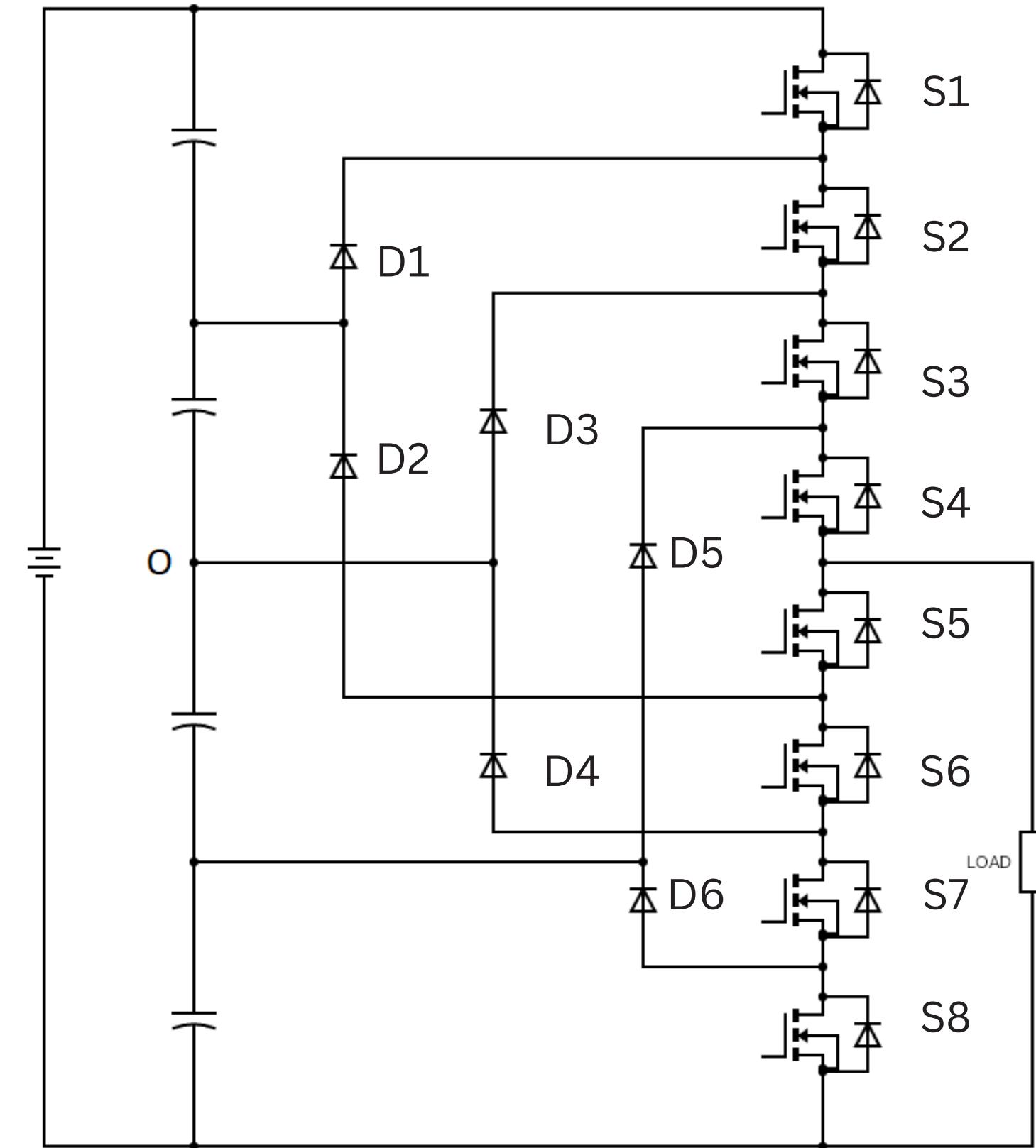
The following topologies which are now in practice are:

- Neutral-Point Clamped(Diode Clamped)
- Flying Capacitor
- Cascaded H-Bridge (CHB)

These topologies differ from each other in the count of number of switches and the number of sources.

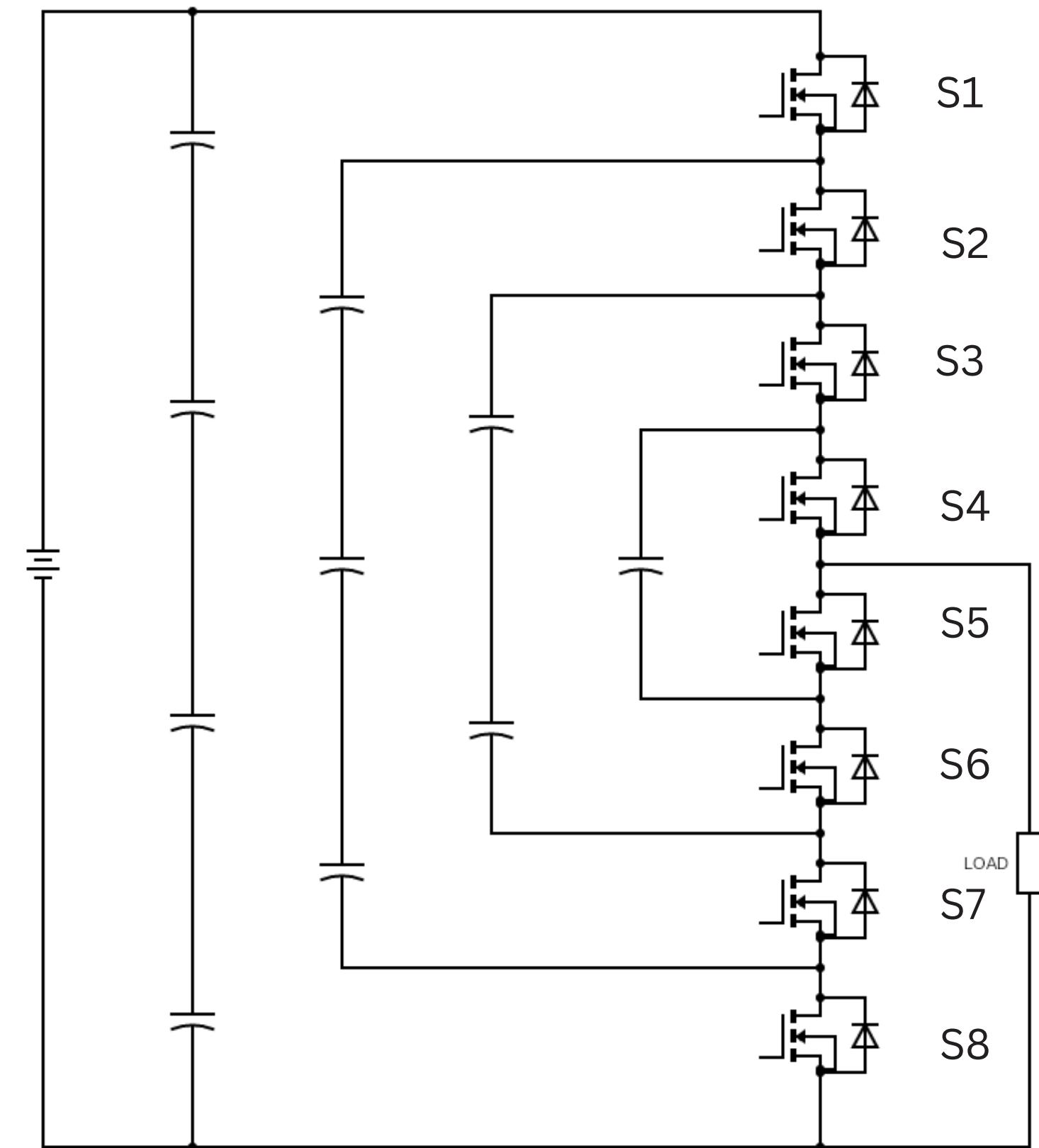
NEUTRAL-POINT CLAMPED

- Diode clamped structure is not modular (scalability is limited)
- Each voltage levels is obtained through one conducting path (zero redundancy)
- Blocking voltage across diodes are different. Extra diodes should be connected if identical diodes are using
- Complexity is high
- High switching loss as the no of switches is more.



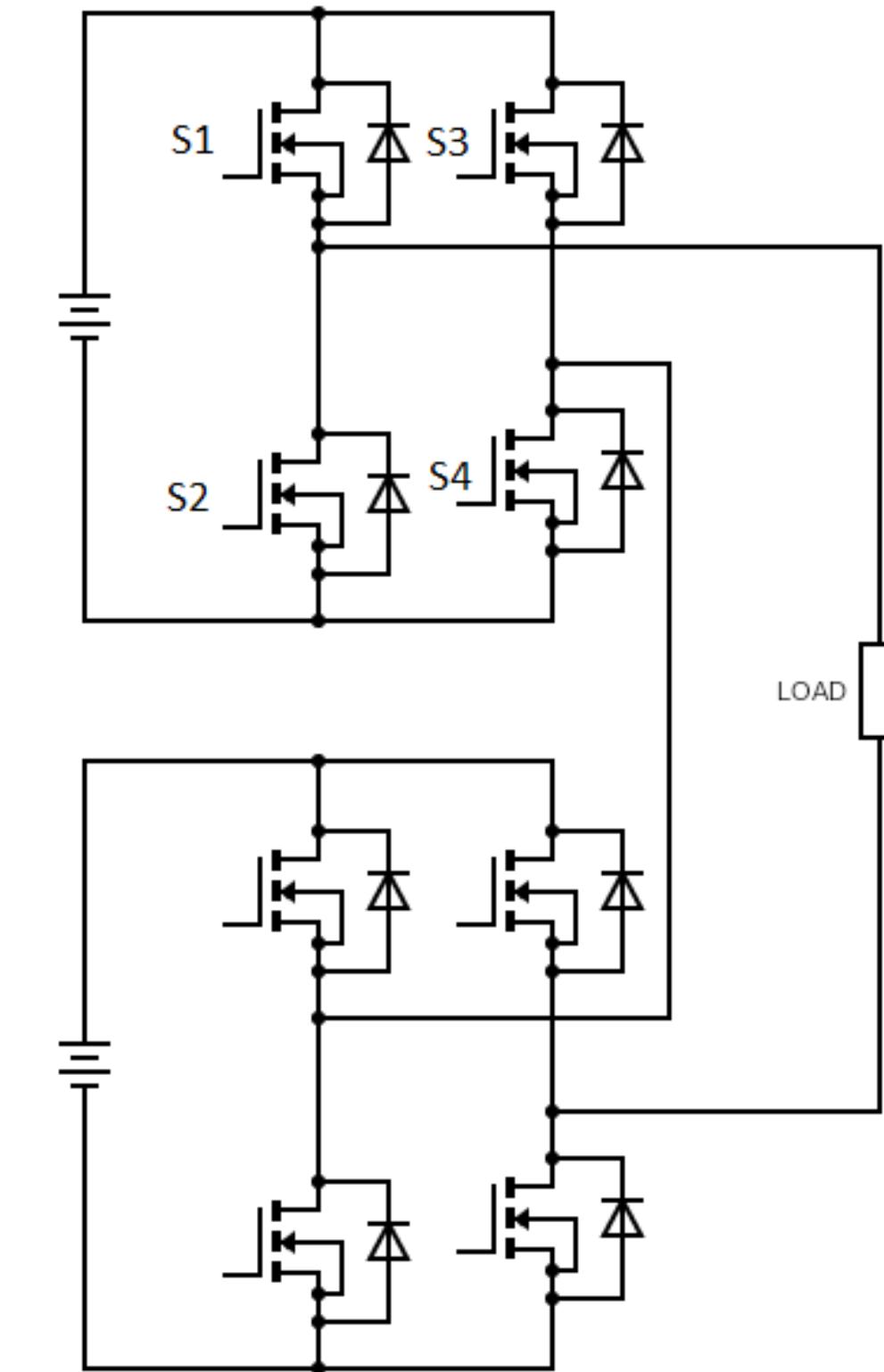
FLYING CAPACITOR

- Pre charging of flying capacitor is necessary.
- Very difficult to maintain the capacitors voltage balance.
- Large number of capacitors make the circuit bulky and comparatively expensive.
- Efficiency is lower in the real power transmission scenario



CASCADED H-BRIDGE

- Even the circuit looks simpler and less bulky the major disadvantage of this topology is the use of 2 isolated DC sources.



COMPARISON

Type	Neutral point Clamped	Flying capacitor	Cascaded H Bridge	Switched Capacitor
No. of Switches used	8	8	8	7
No. of Capacitors	4	10	0	3
No. of Diodes	12	0	0	1

ADVANTAGES OF SWITCHED CAPACITOR TOPOLOGY

- No. of required passive components and semiconductor switches are lower.
- It offers better scalability as additional voltage levels can be achieved by adding capacitor cells
- Single low input voltage source.
- The soft charging of capacitors in this circuit increases the reliability and life time of components in this circuit.

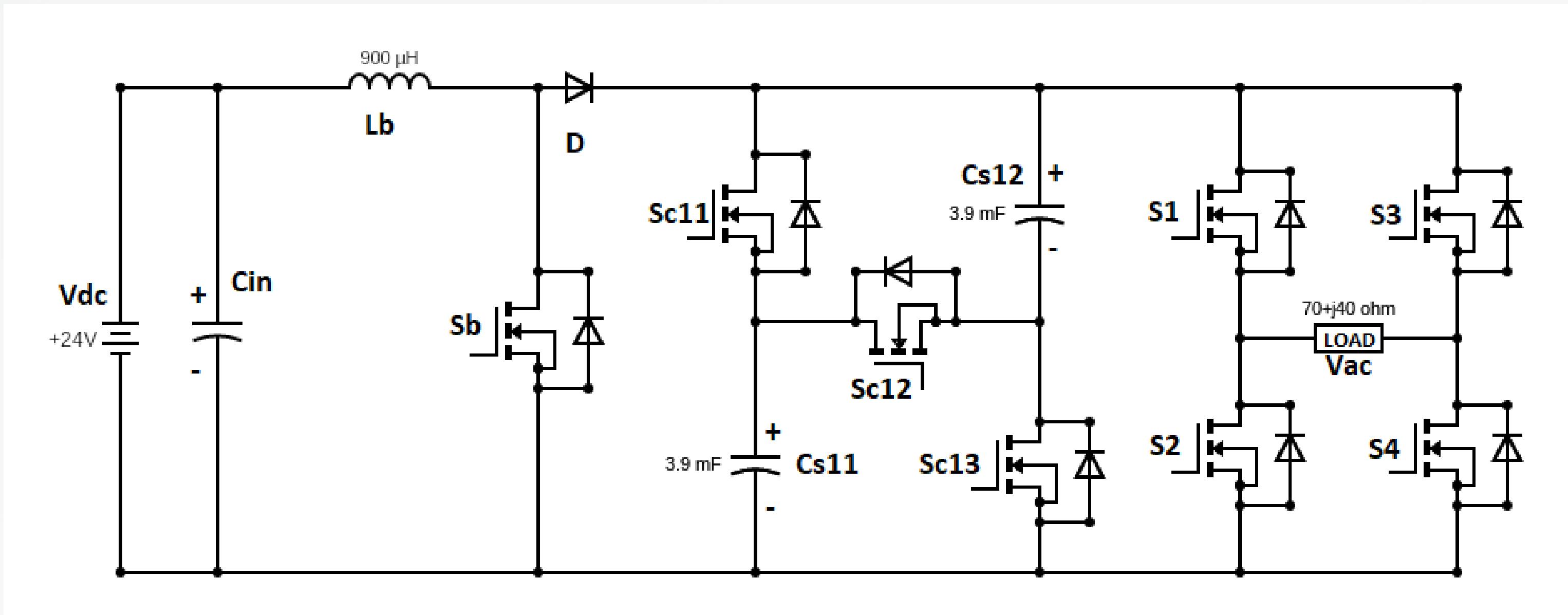
LITERATURE PAPERS

SL NO	Author	Title	Overview
1	Dargahi	A New Family of Modular Multilevel Converter Based on Modified Flying-Capacitor Multicell Converters	Got an overview on no. of semiconductor devices of flying capacitor topology
2	Akira Nabae	A New Neutral-Point-Clamped PWM Inverter	Got an overview on no. of semiconductor devices of Neutral-Point Clamped topology
3	Asha Gaikwad	Study of cascaded H-Bridge multilevel inverter	Got an overview on no. of semiconductor devices of cascaded H Bridge topology

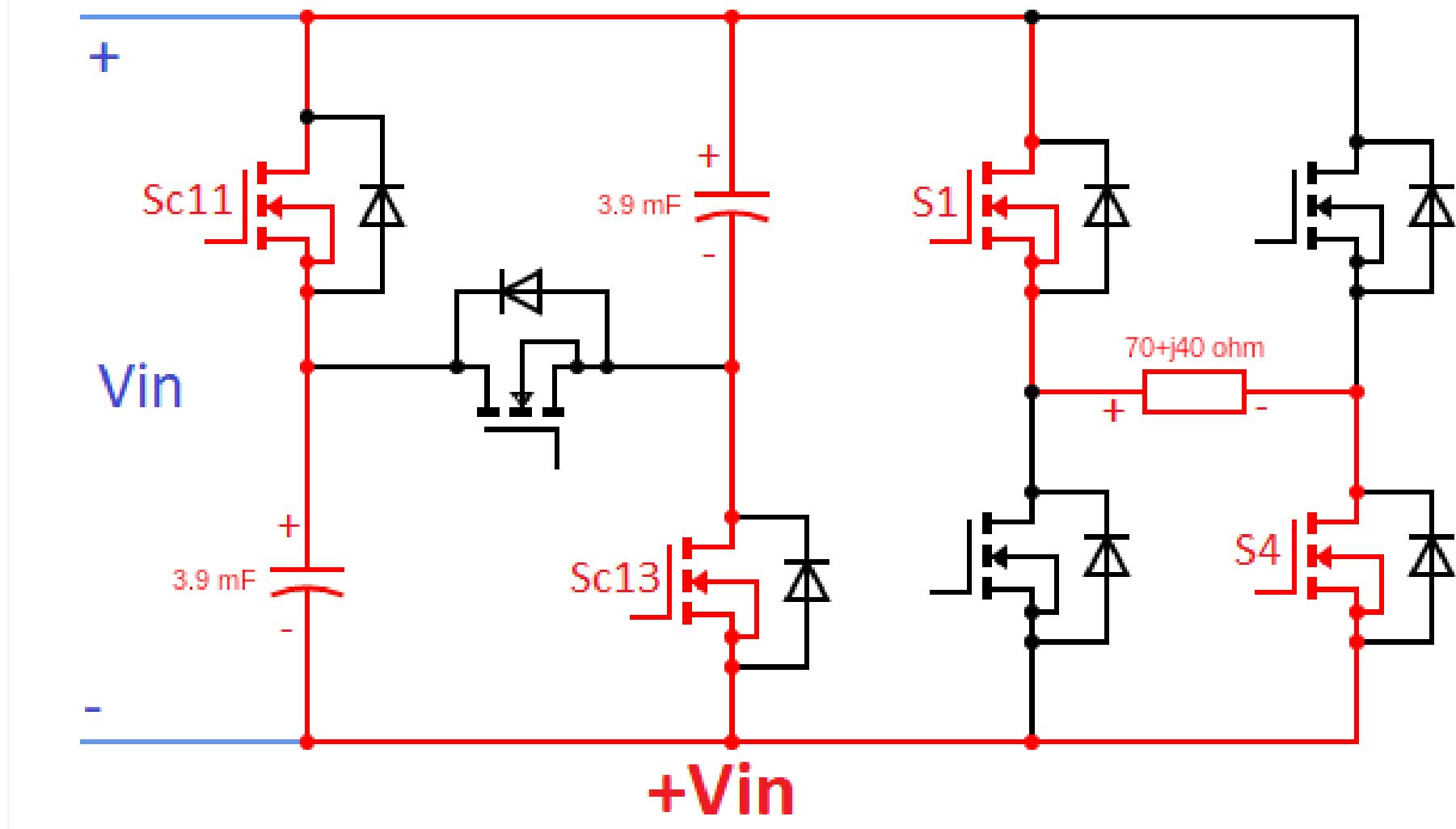
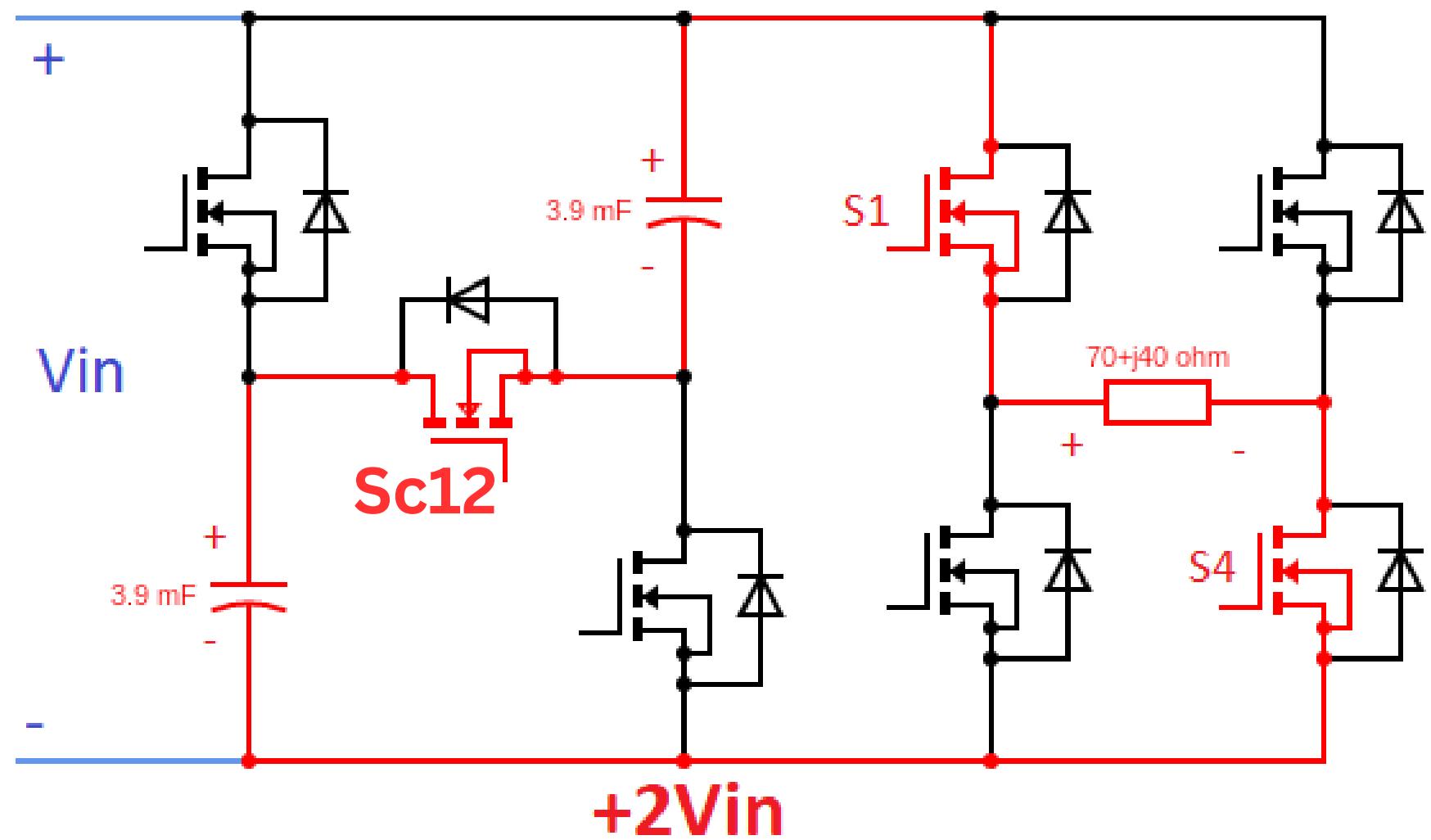
5 LEVEL INVERTER

- Consists of a boost, capacitor cell and an H bridge to obtain the inverter output. Which has levels $+2V_{in}$, $+V_{in}$, 0, $-V_{in}$, $-2V_{in}$

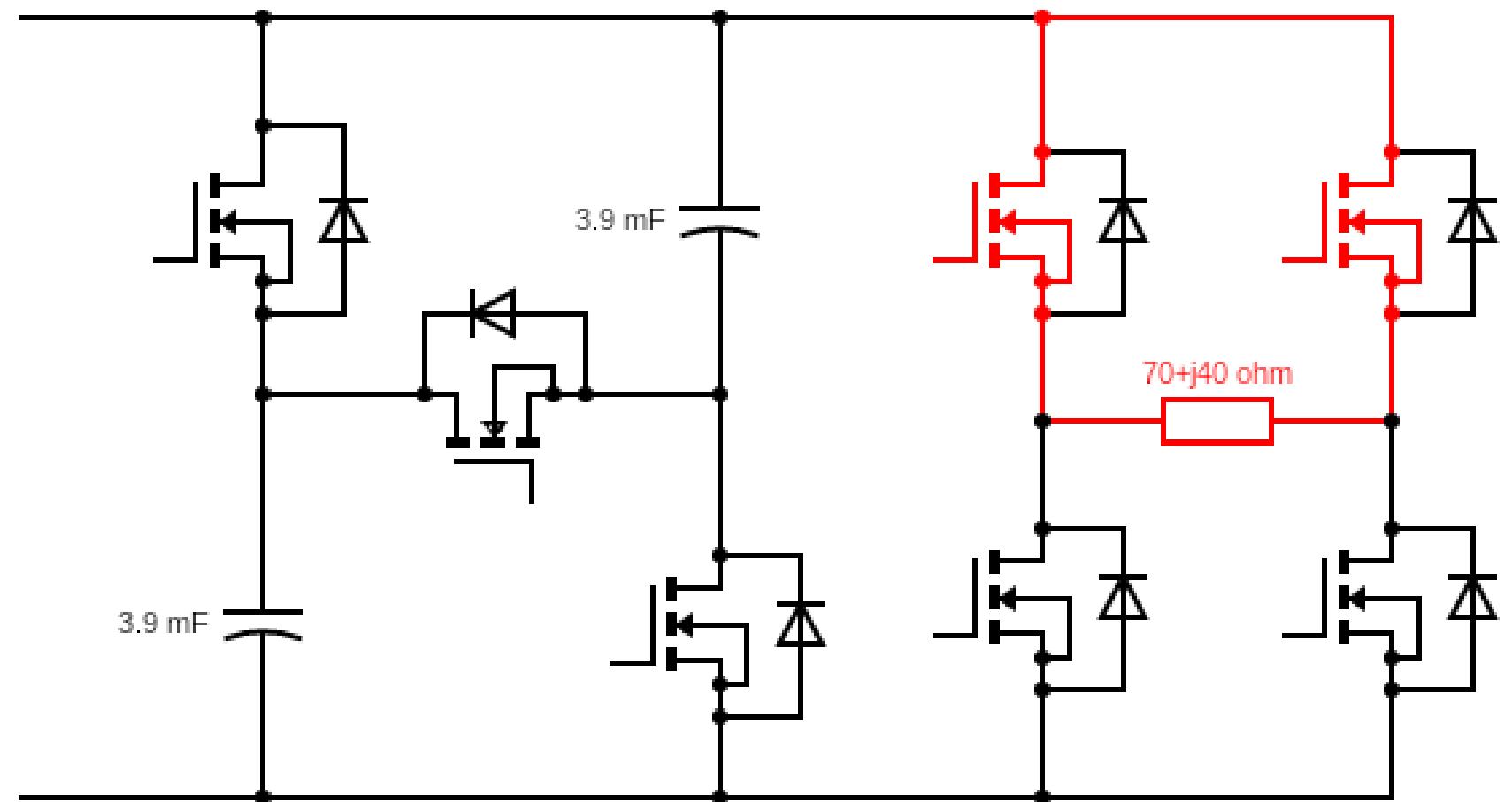
CIRCUIT SCHEMATIC DIAGRAM



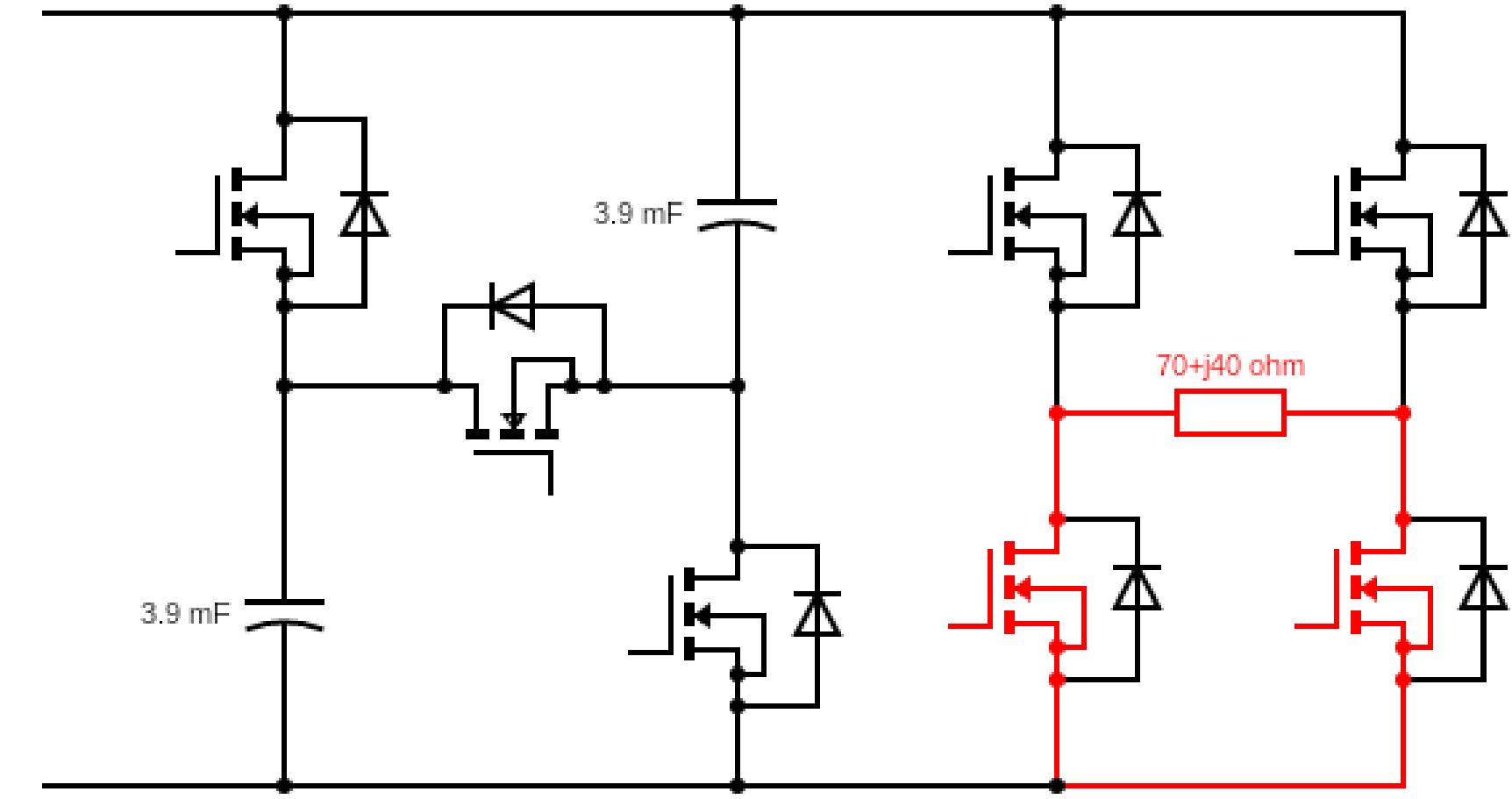
MODES OF OPERATION



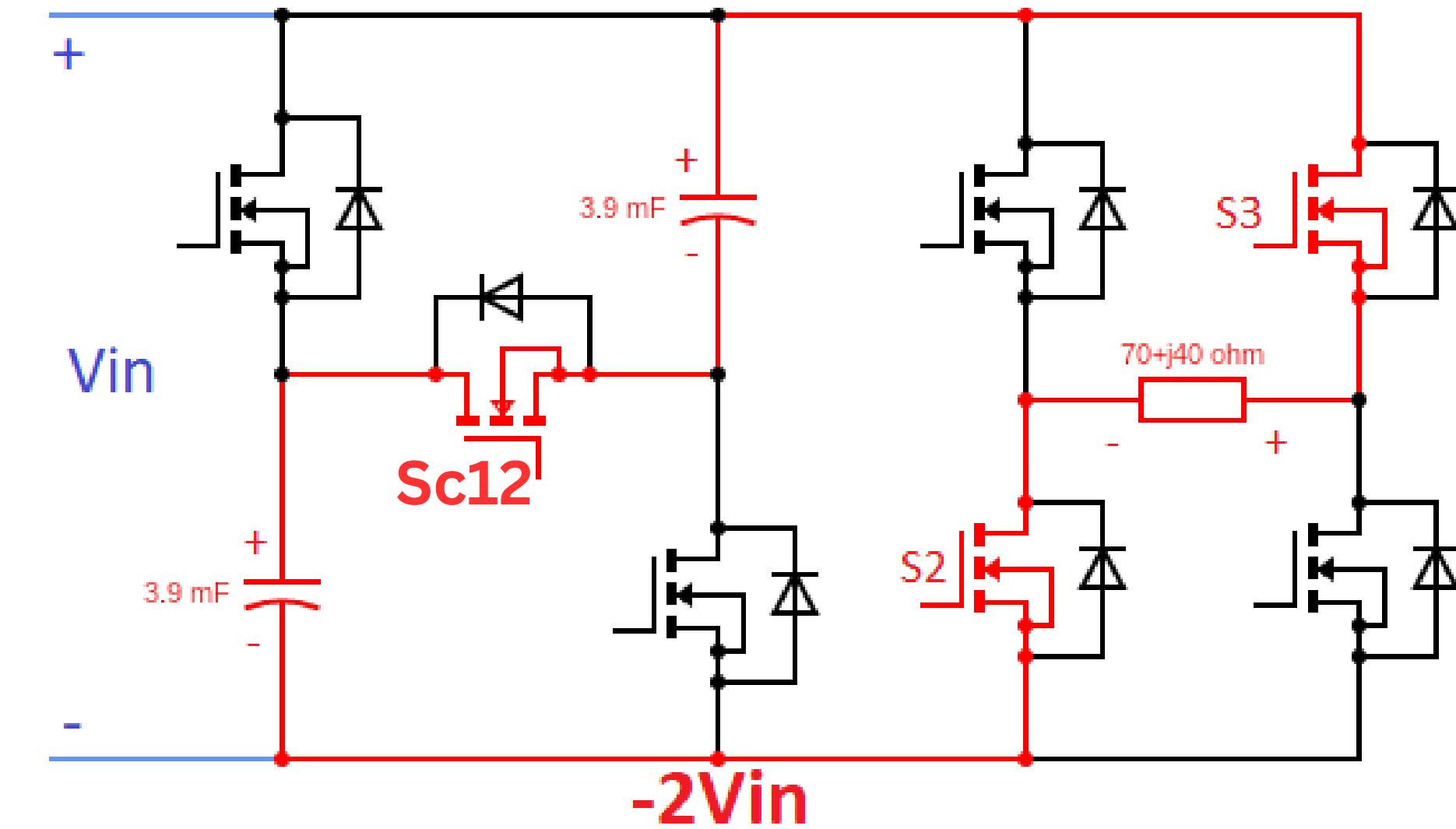
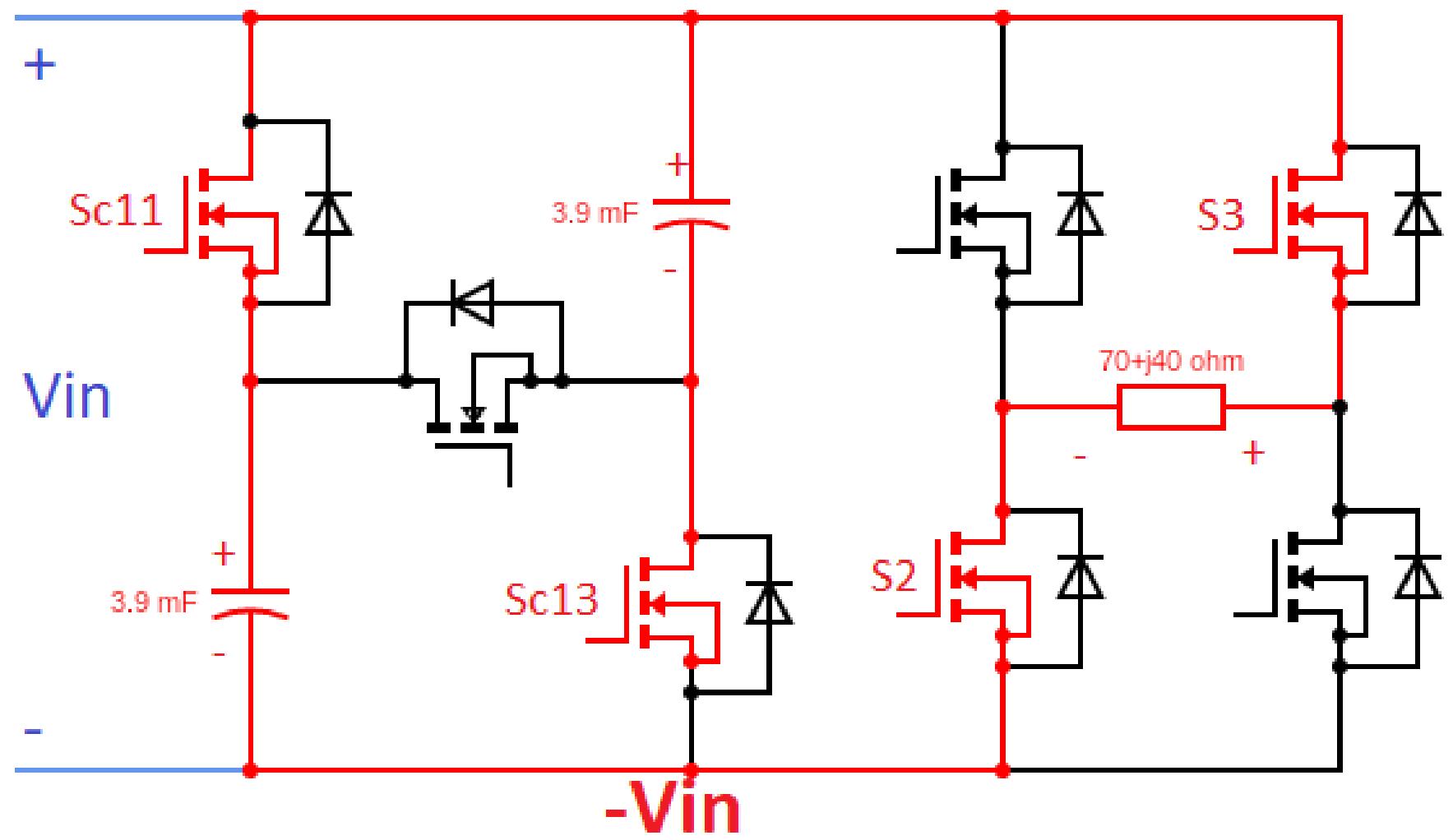
MODES OF OPERATION



0



MODES OF OPERATION



SWITCHING STATES

MODE	VOLTAGE STATE	SC11	SC12	SC13	S1	S2	S3	S4
1	0	ON/OFF	ON/OFF	ON/OFF	ON	OFF	ON	OFF
2	+VDC	ON	OFF	ON	ON	OFF	OFF	ON
3	+2VDC	OFF	ON	OFF	ON	OFF	OFF	ON
4	-VDC	ON	OFF	ON	OFF	ON	ON	OFF
5	-2VDC	OFF	ON	OFF	OFF	ON	ON	OFF

DESIGN

Peak of fundamental AC output,

$$\hat{v}_{ac} = MV_{PN} = \frac{2MV_{dc}}{1 - D_b} = 142V$$

Boost inductance,

$$L = \frac{V_{dc}(V_{op} - V_{dc})}{f_{sw} \times \Delta I \times V_{op}} = 0.9mH$$

Switching capacitance,

$$C_{sn2} \geq \frac{Q_N}{\Delta V_{in} \times V_{in}} = 3.9mF$$

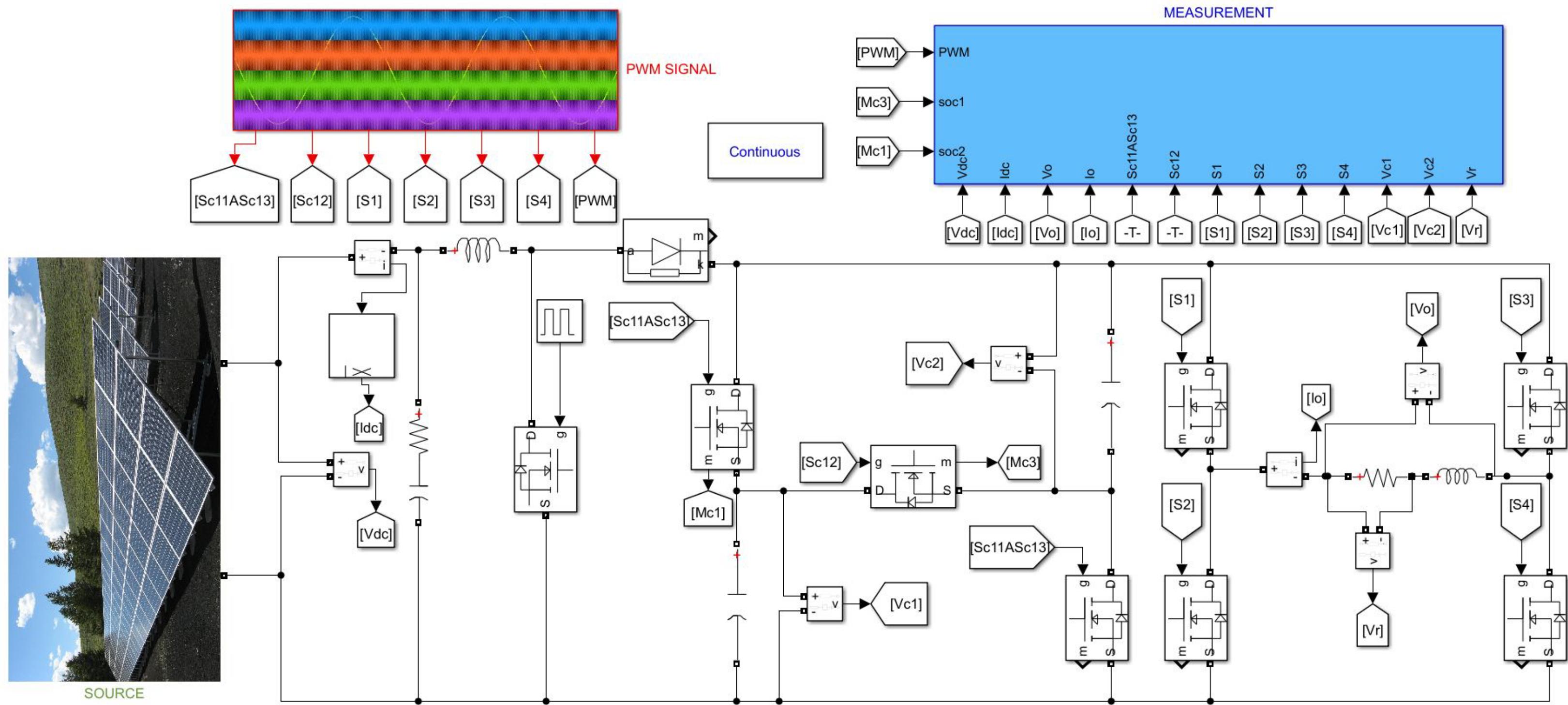
Specifications

Input Voltage (V_{dc})	24V
Output Voltage (V_{op})	72 V
Input Current (I_{dc})	4.2A
Output Current (I_{op})	1.2A
D_b	0.8
Modulation Index, M	0.95
Switching Frequency, f_{sw}	20KHz
Current Ripple, $\triangle I$	0.2A
Voltage Ripple, $\triangle V$	0.72V
Capacitor Discharge value	0.2C

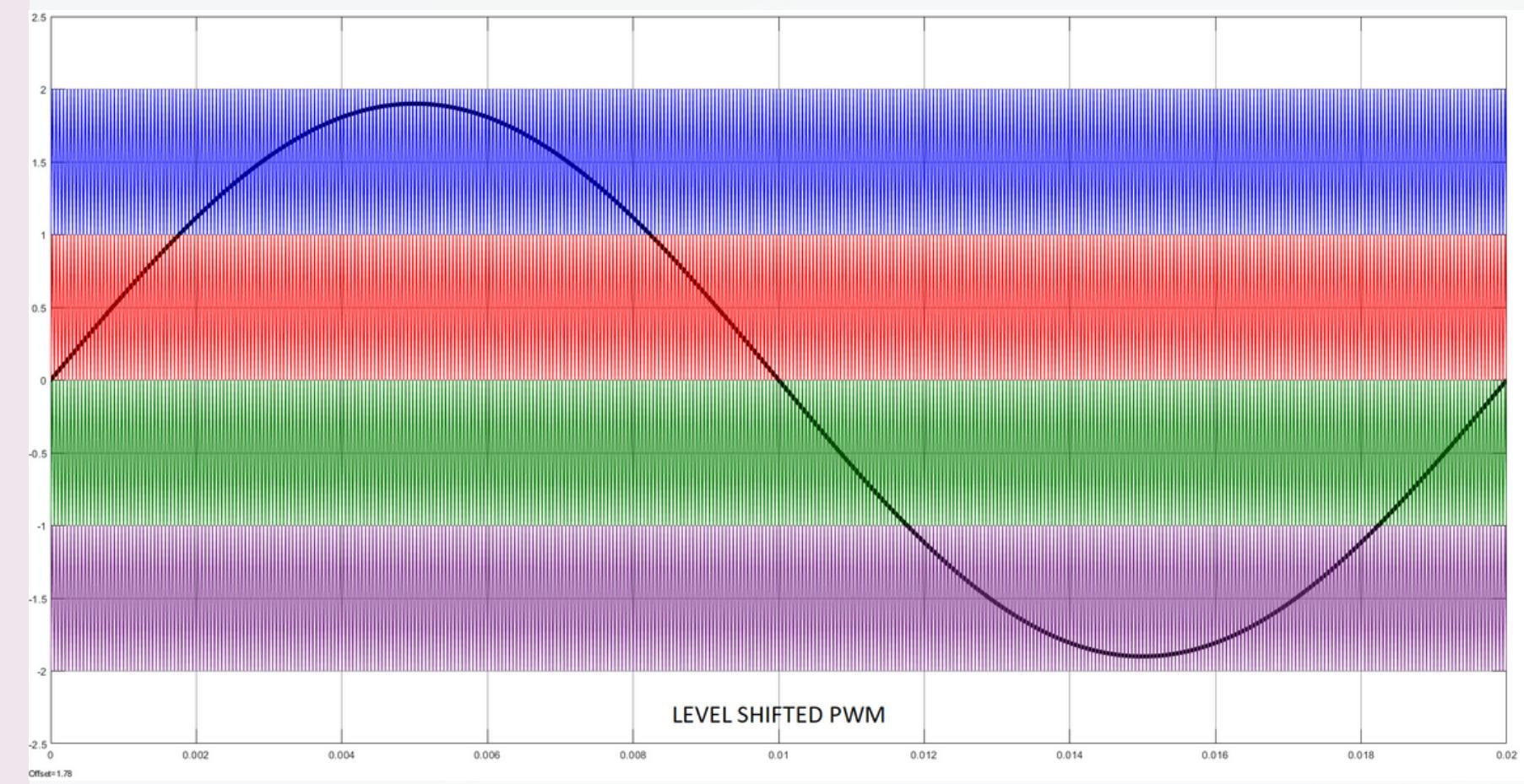
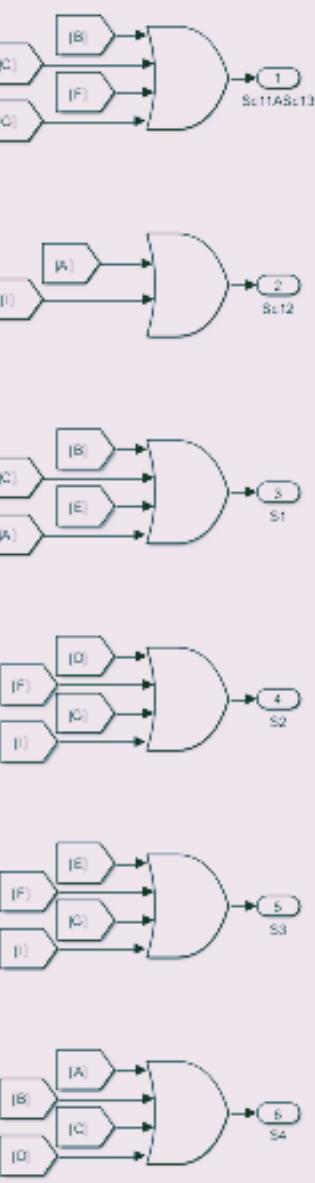
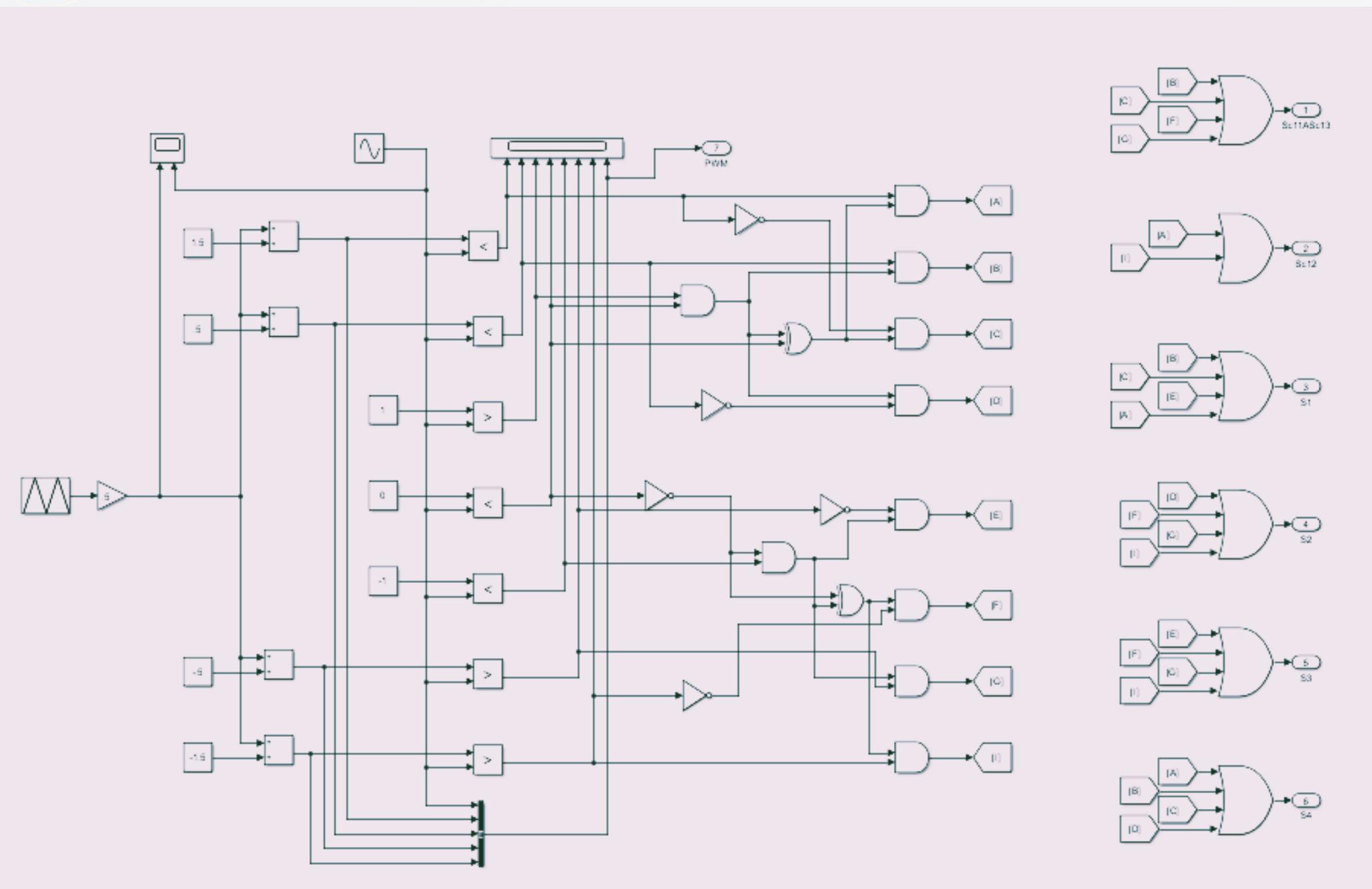
DESIGN SPECIFICATIONS

Parameters	Values
Input voltage (V_{dc})	24V
Boost circuit Output	72 V
Output voltage (v_{ac})(RMS)	100 V
Power rating (P_O)	100 W
Carrier frequency (f_s)	20kHz
Line frequency (f)	50 Hz
DC-link capacitor (C_1 & C_2)	4 mF, 150 V
Boost inductor (L_B)	0.9mH
Load Resistance	70 ohm

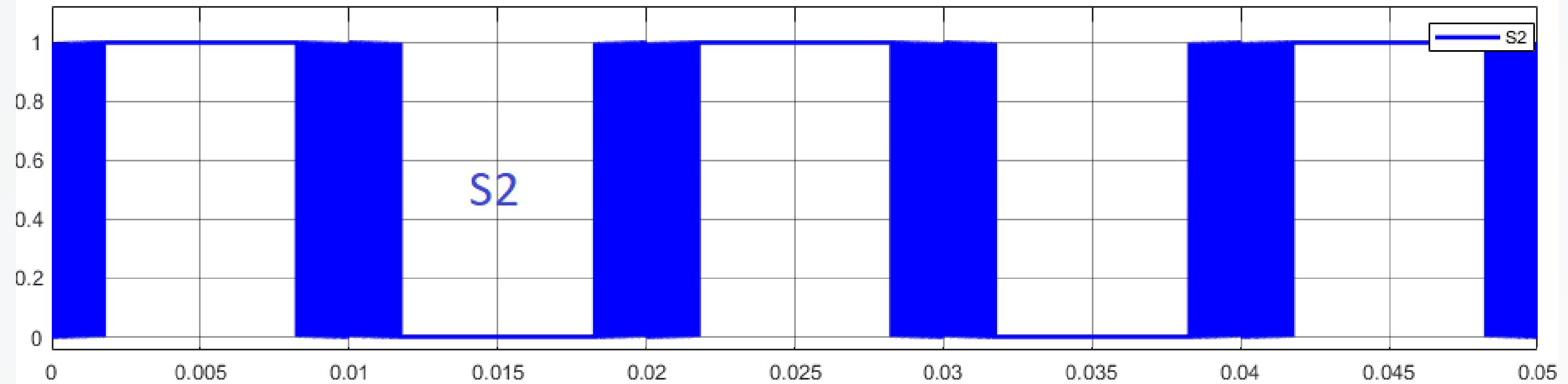
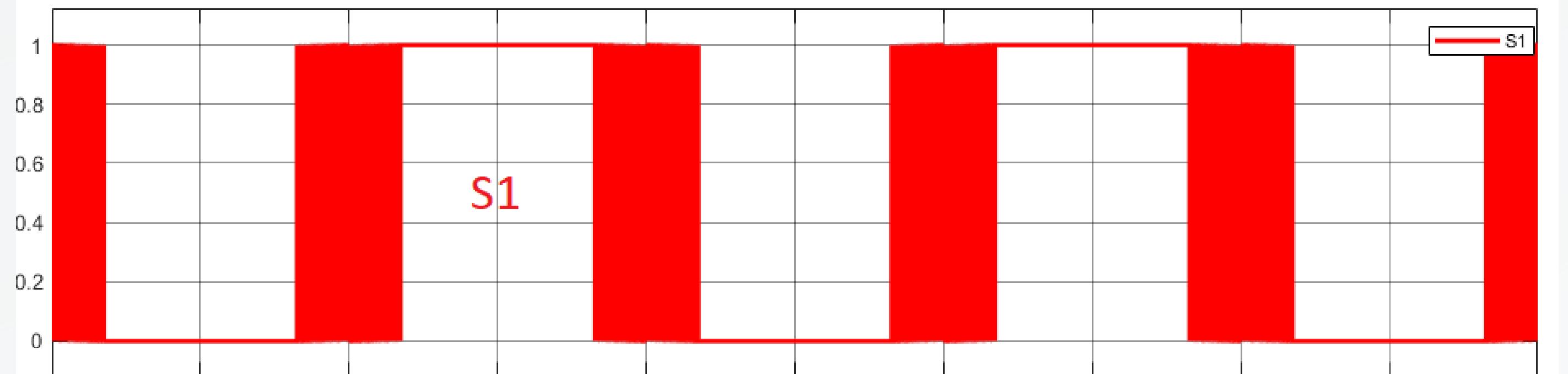
SIMULATION



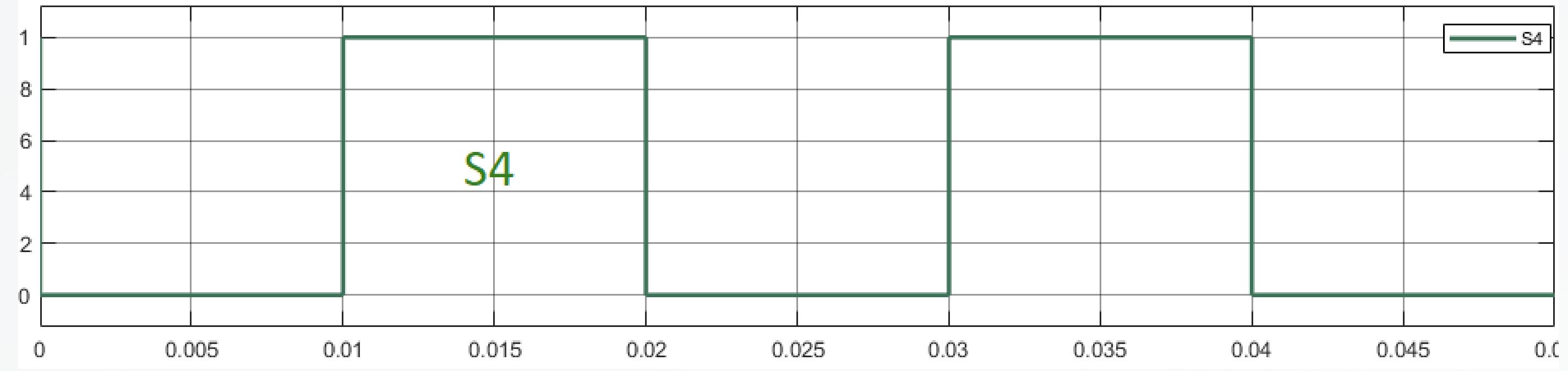
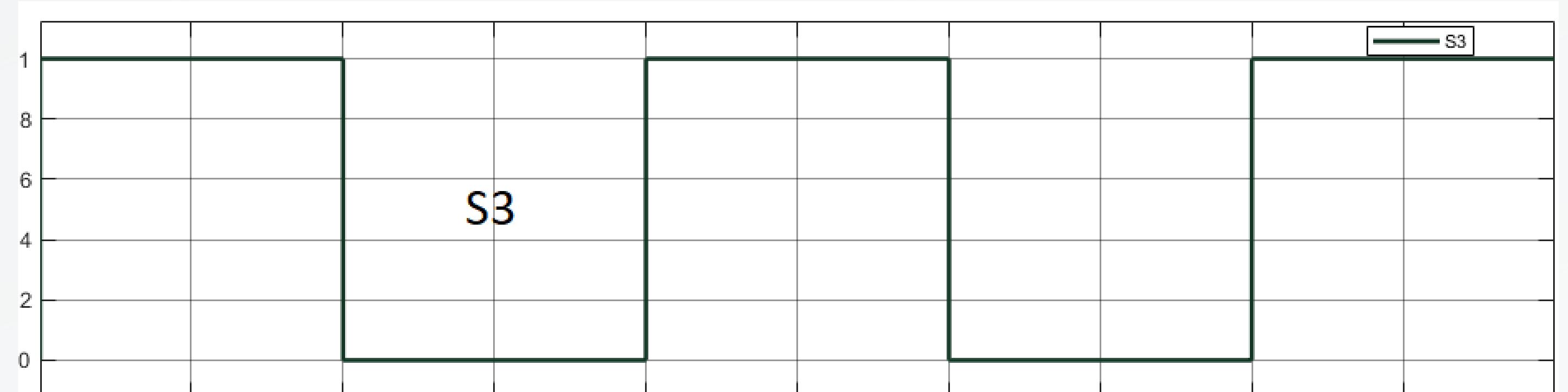
LEVEL SHIFTED PWM SIGNAL



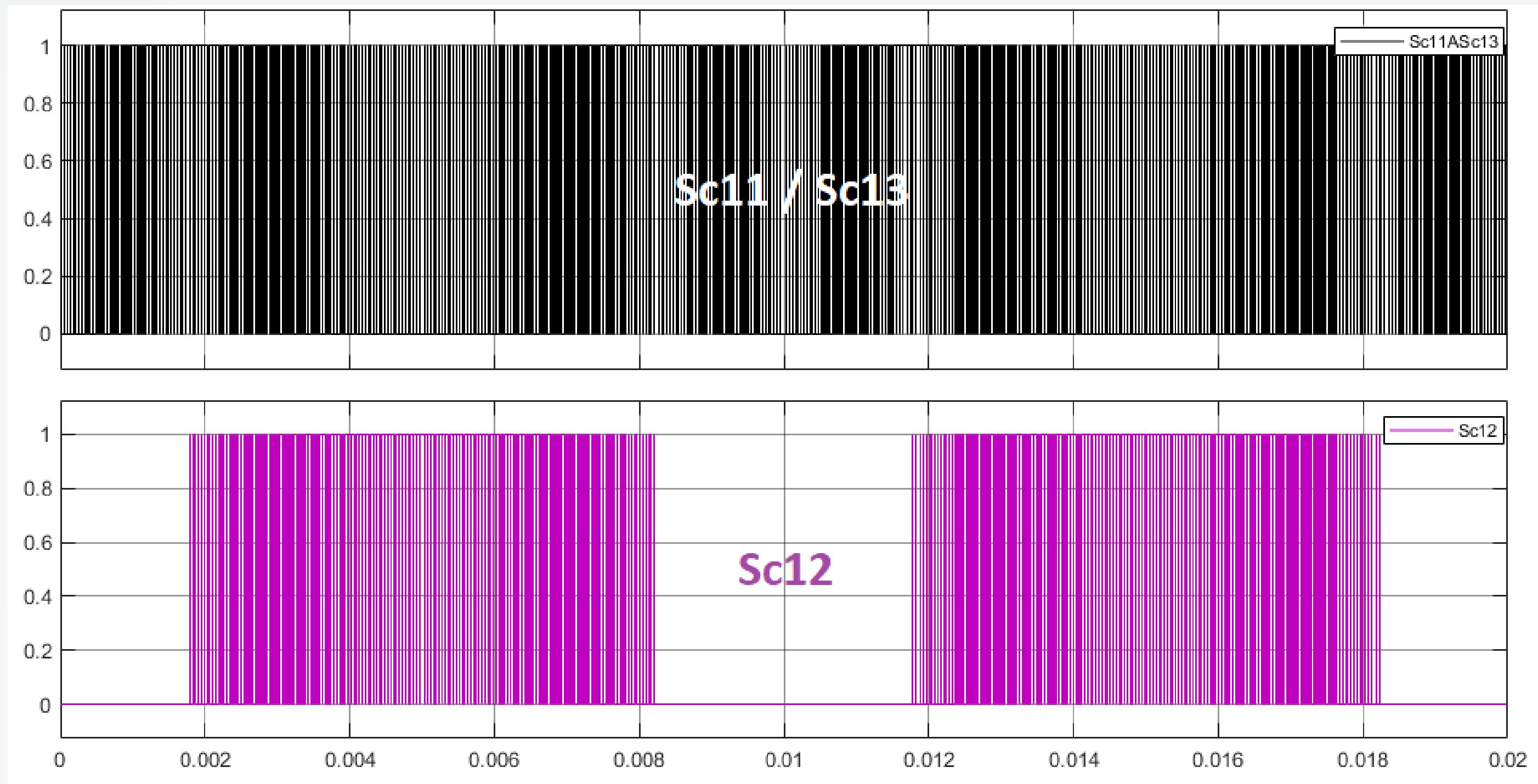
SWITCHING SIGNALS



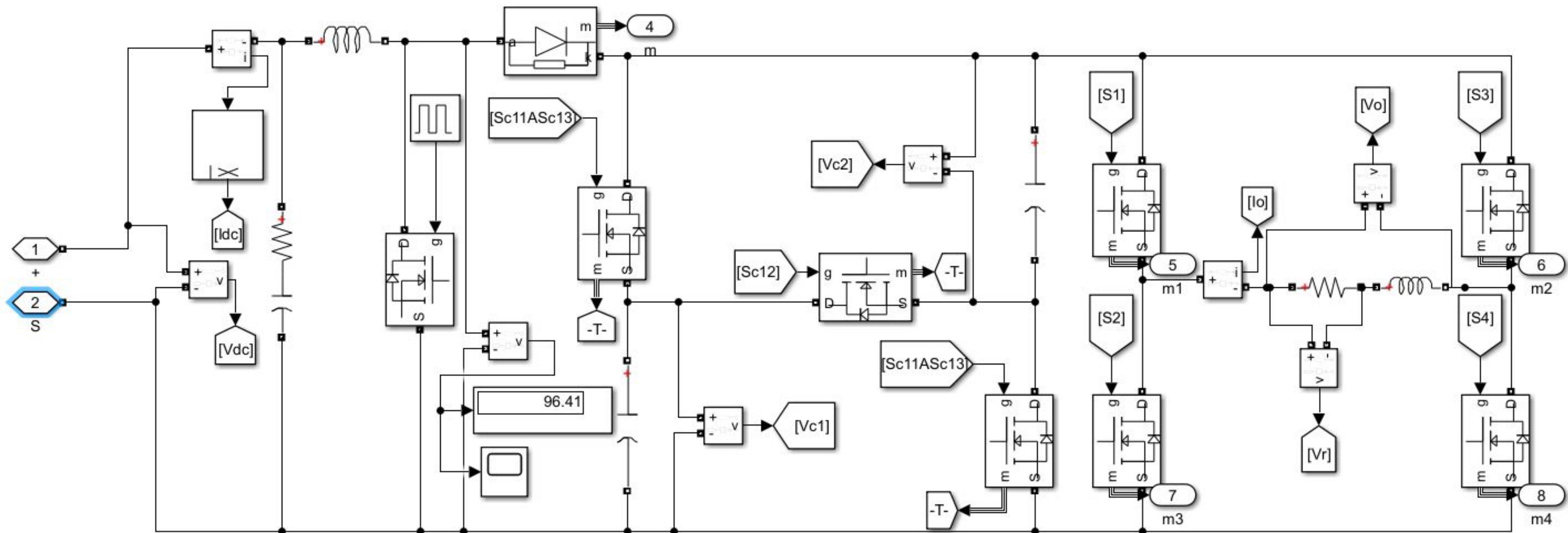
SWITCHING SIGNALS



SWITCHING SIGNALS

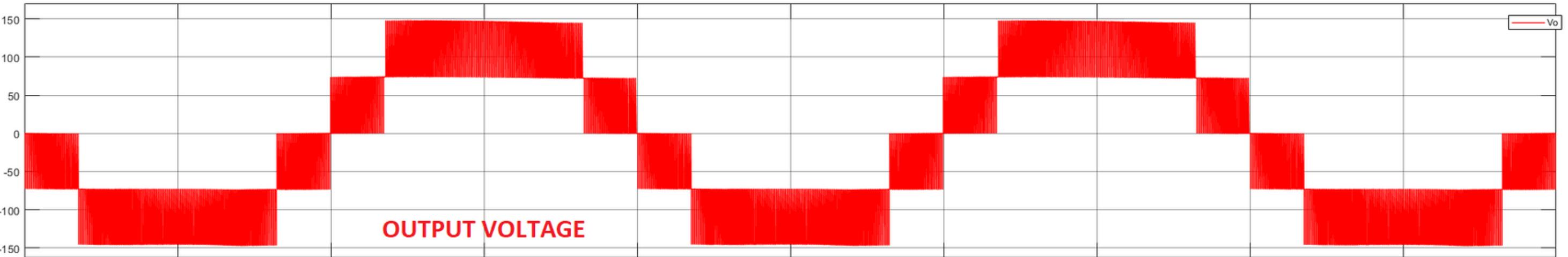


5 LEVEL INVERTER CIRCUIT

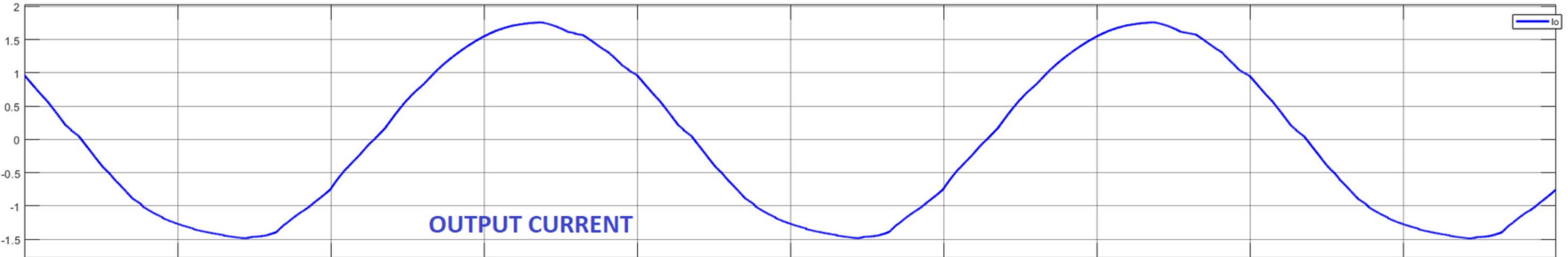


OUTPUT WAVEFORMS

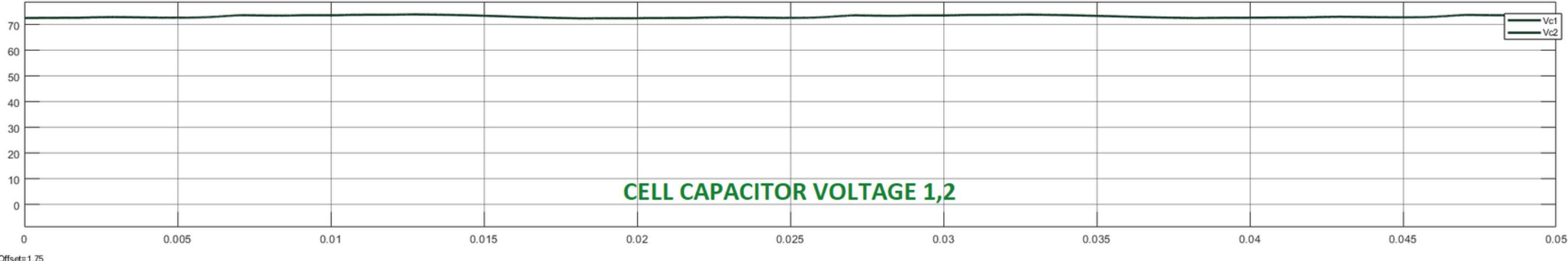
Output Voltage
 $V_o(\text{peak})= 142\text{V}$
 $V_o(\text{rms})= 99.93\text{V}$



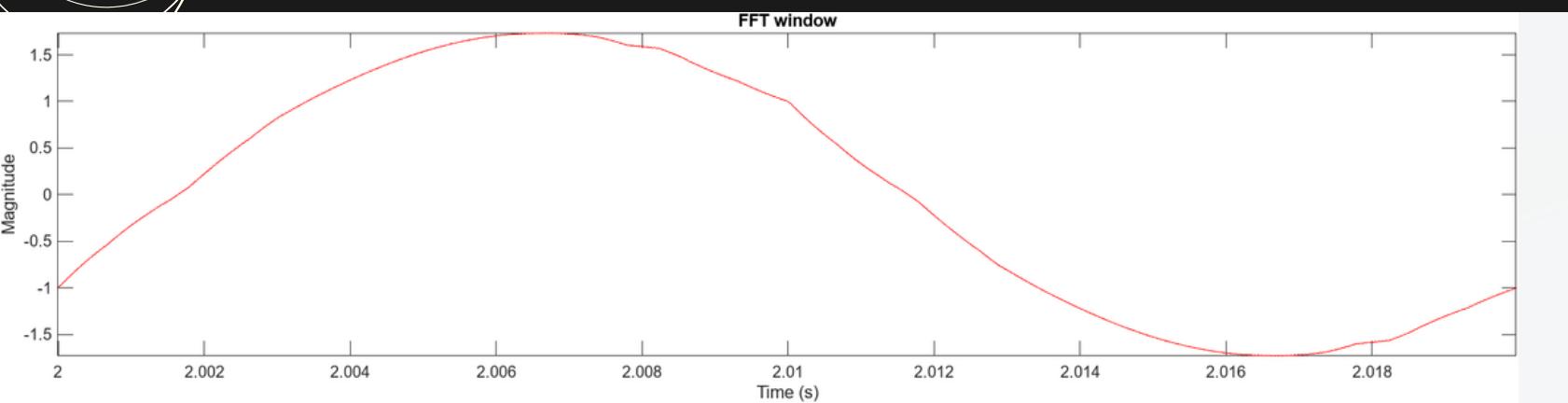
Output Current
 $V_o(\text{peak})= 1.51\text{A}$
 $V_o(\text{rms})= 1.146\text{A}$



Capacitor Cell Voltage
 $V_c= 72\text{V}$

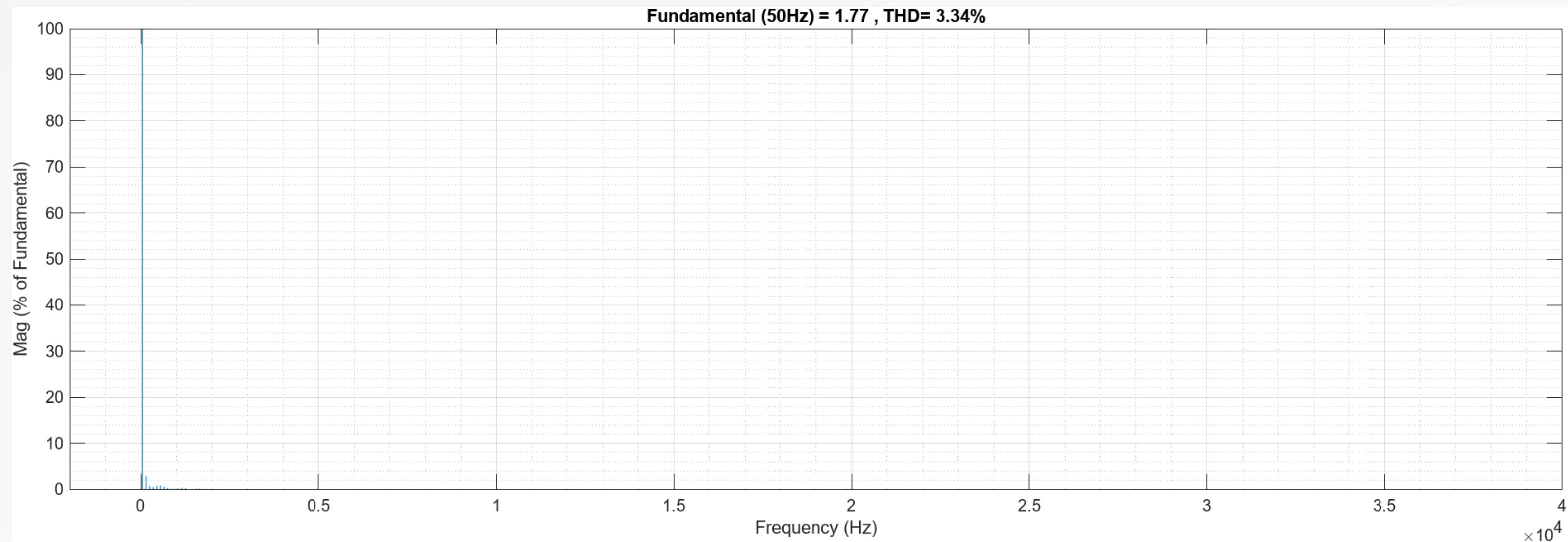


CURRENT FFT ANALYSIS

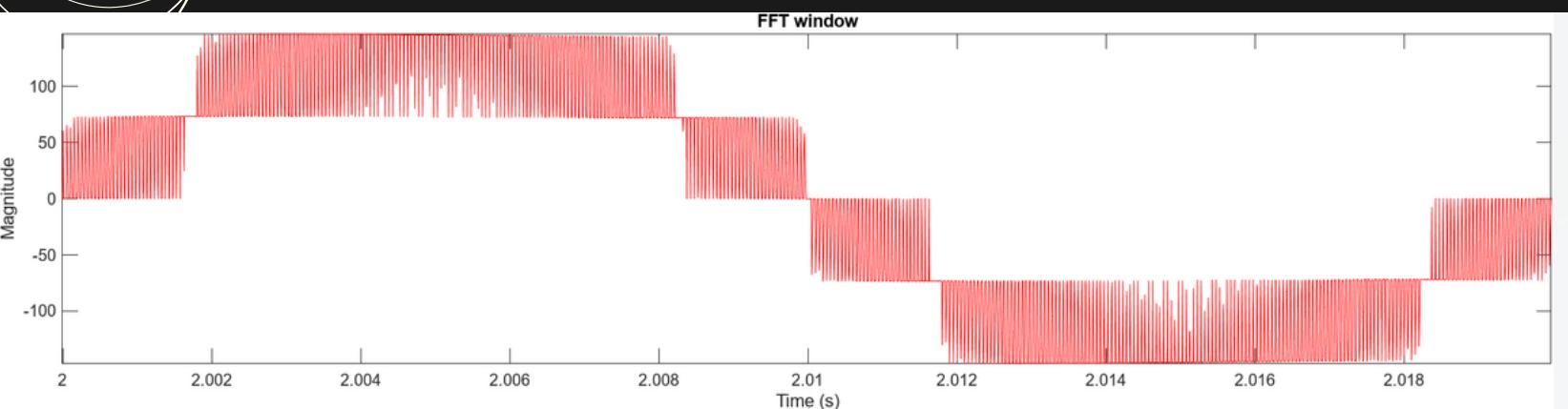


THD=3.34%

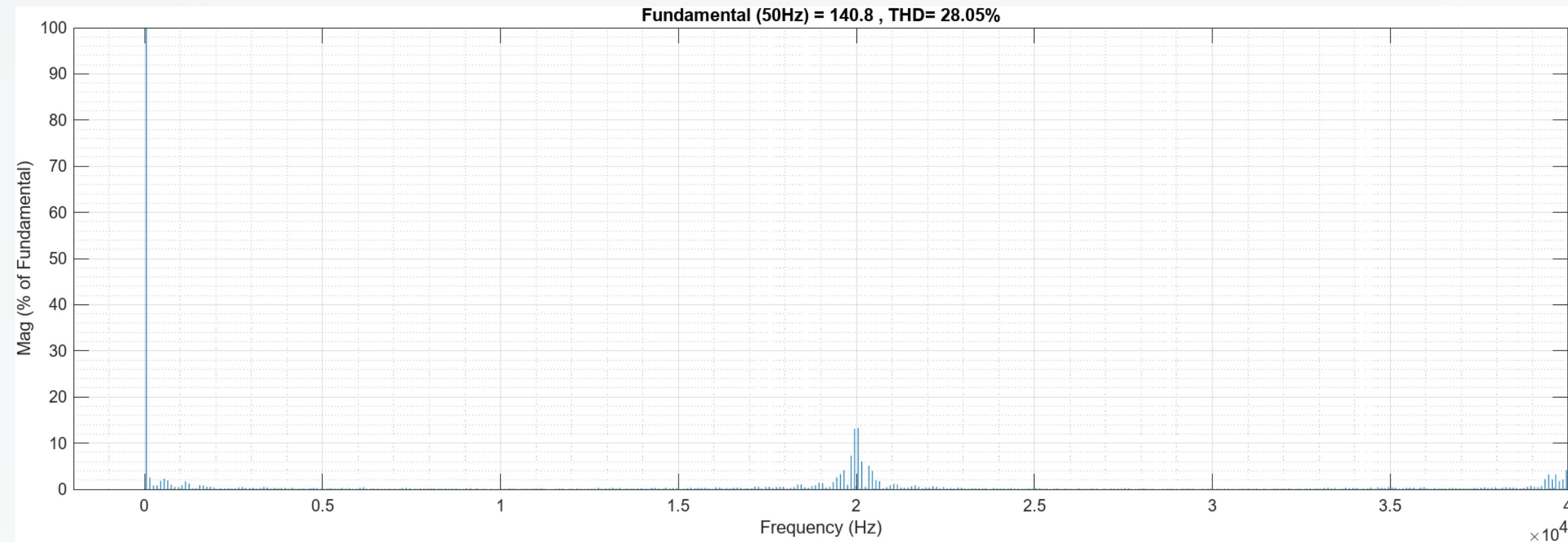
Fundamental (50Hz) = 1.77 , THD= 3.34%



VOLTAGE FFT ANALYSIS



THD=28.05%



SIMULATION OBSERVATIONS

Parameters	Values
Voltage (rms)	99.96 V
Current (rms)	1.164 A
Power Output	97.43 W
Power Input	106.4 W
Efficiency	92.43 %
Power Factor	0.8068
THD Voltage	28.01 %
THD Current	3.36 %

STEPS TO REALISE THE HARDWARE

Identifying different requirements for driving the inverter.

1

Selecting and designing suitable components for driving

2

Selecting the components required based on the values from CAE analysis.

3

Constructing pcb boards for signal circuit, gate driver circuit, inverter circuit.

4

Assembly and study of individual circuits and as whole.

5



HARDWARE

Realising the hardware part

1. Control Circuit.
2. Gate Power Circuit
3. Main Circuit.

COMPONENTS SELECTION

COMPONENTS	RATING	NOS
dsPIC30F2020		1
LM7815T		7
MUR460		10
IRF540		4
TLP250(F)		4
IRFP460C		8
CAPACITOR	$220\mu F$	14
CAPACITOR	$1000 \mu F$	9
CAPACITOR	$0.1 \mu F$	12
RESISTOR	1K Ohm	18
RESISTOR	270 Ohm	9
RESISTOR	720 Ohm	1
RESISTOR	560 Ohm	9

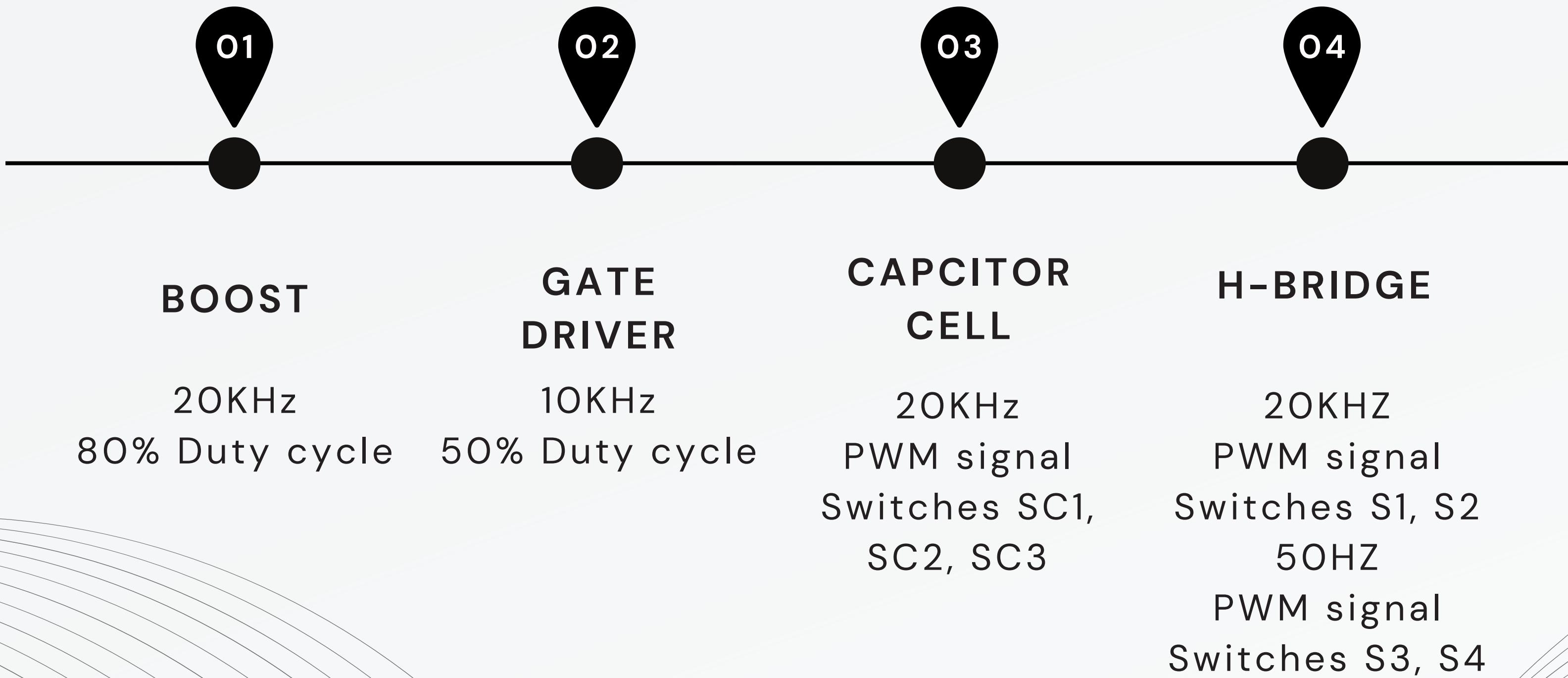
CONTROL CIRCUIT

Requirements:

- Sine PWM
- 4 Dedicated PWM modules.
- Supports 20 kHz switching frequency.
- Digital output



- Based on requirements we have selected microchip dsPIC30F series model **dsPIC30F2020**.
- It Have 4 dedicated PWM modules.
- Supports 20kHz stitching frequency.



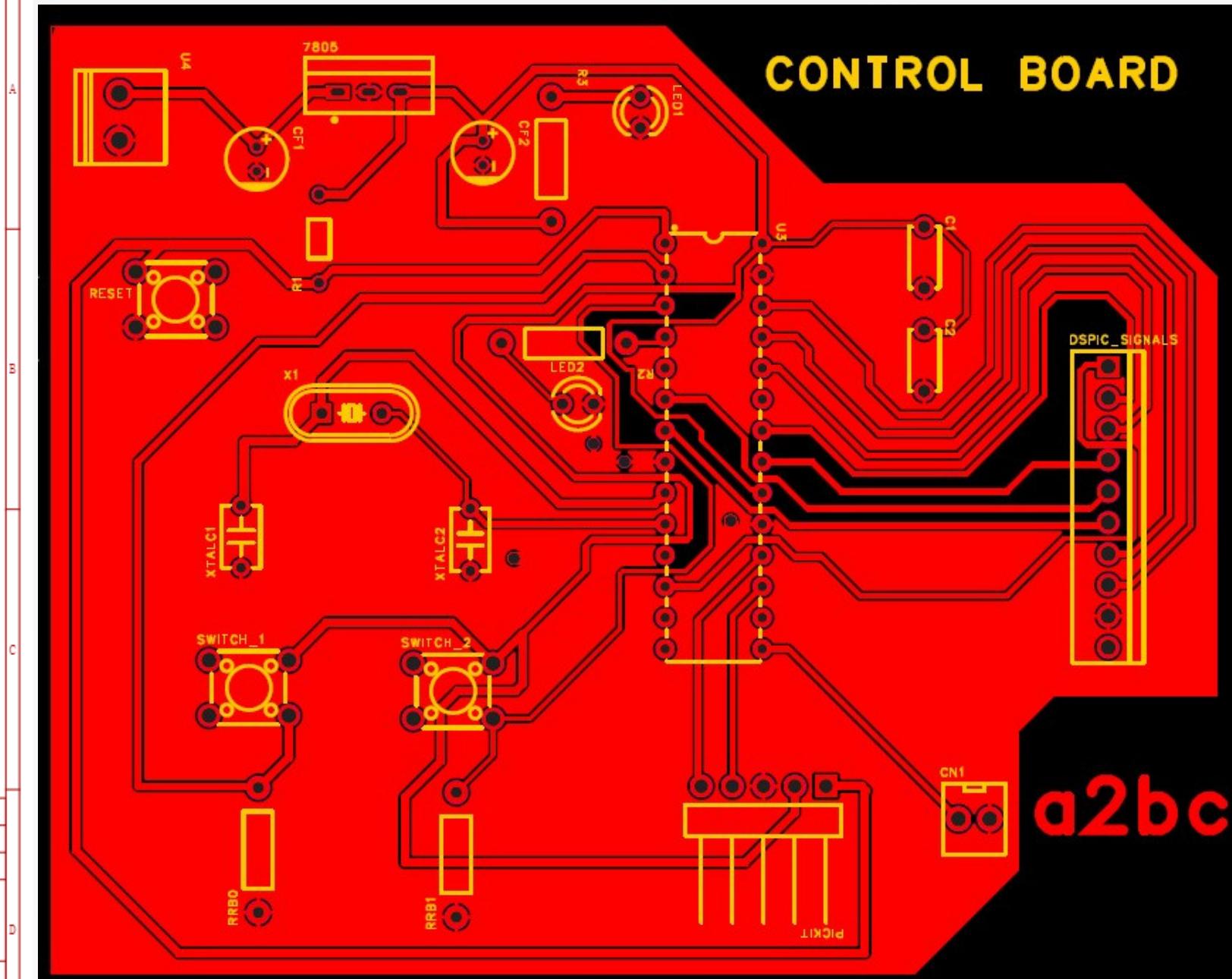
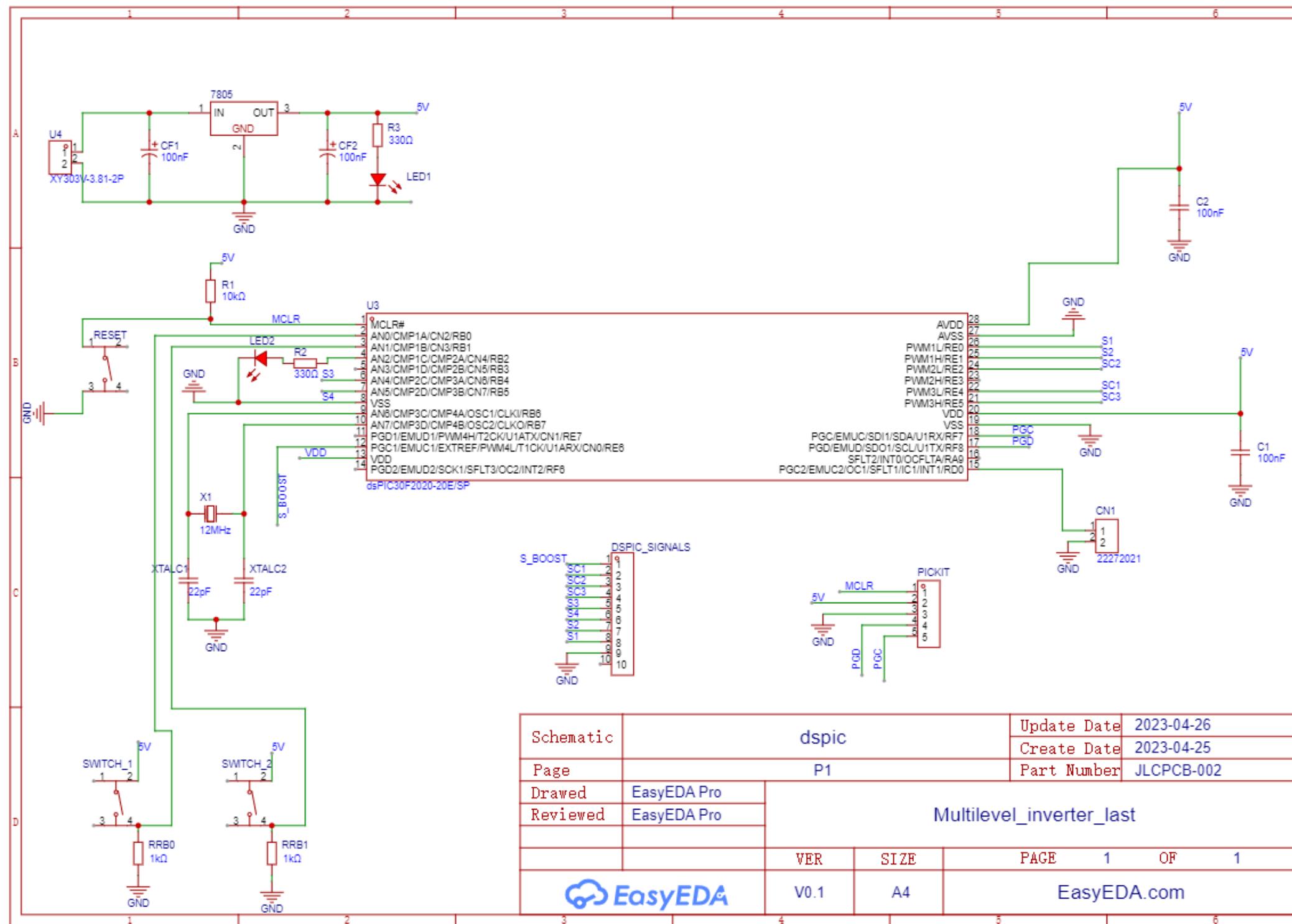
dsPIC30F2020

PIN DIAGRAM

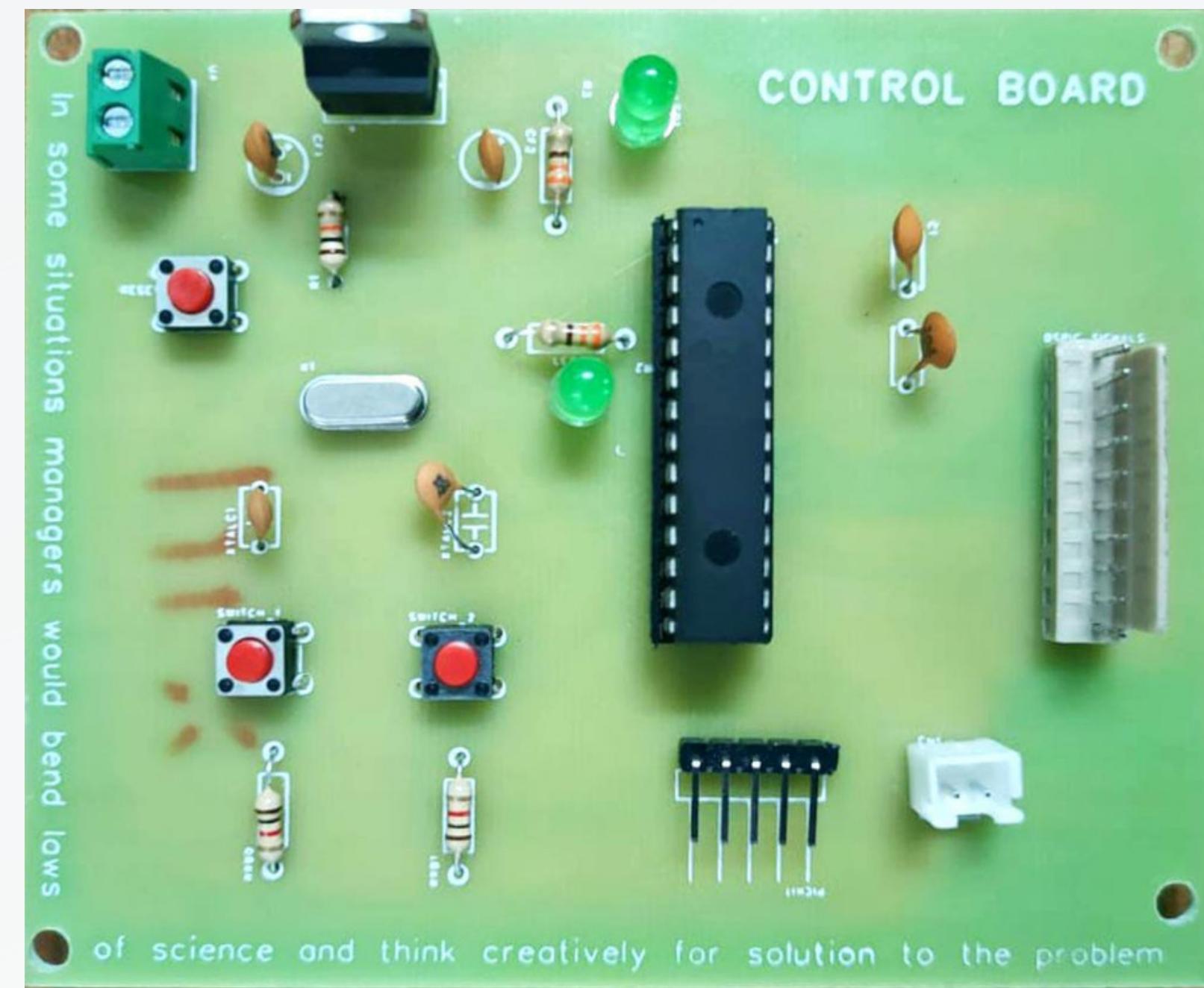
28-Pin SDIP and SOIC

MCLR	1	28	VDD
AN0/CMP1A/CN2/RB0	2	27	VSS
AN1/CMP1B/CN3/RB1	3	26	PWM1L/RE0
AN2/CMP1C/CMP2A/CN4/RB2	4	25	PWM1H/RE1
AN3/CMP1D/CMP2B/CN5/RB3	5	24	PWM2L/RE2
AN4/CMP2C/CMP3A/CN6/RB4	6	23	PWM2H/RE3
AN5/CMP2D/CMP3B/CN7/RB5	7	22	PWM3L/RE4
Vss	8	21	PWM3H/RE5
AN6/CMP3C/CMP4A/OSC1/CLKI/RB6	9	20	Vdd
AN7/CMP3D/CMP4B/OSC2/CLKO/RB7	10	19	Vss
PGD1/EMUD1/PWM4HT2CK/U1ATX/CN1/RE7	11	18	PGC/EMUC/SDI1/SDA/U1RX/RF7
PGC1/EMUC1/EXTREF/PWM4LT1CK/U1ARX/CND/RE6	12	17	PGD/EMUD/SDO1/SCL/U1TX/RF8
Vdd	13	16	SFLT2/INTD/OCFLTA/RA9
PGD2/EMUD2/SCK1/SFLT3/OC2/INT2/RF6	14	15	PGC2/EMUC2/OC1/SFLT1/IC1/INT1/RD0

SCHEMATIC DIAGRAM & PCB LAYOUT

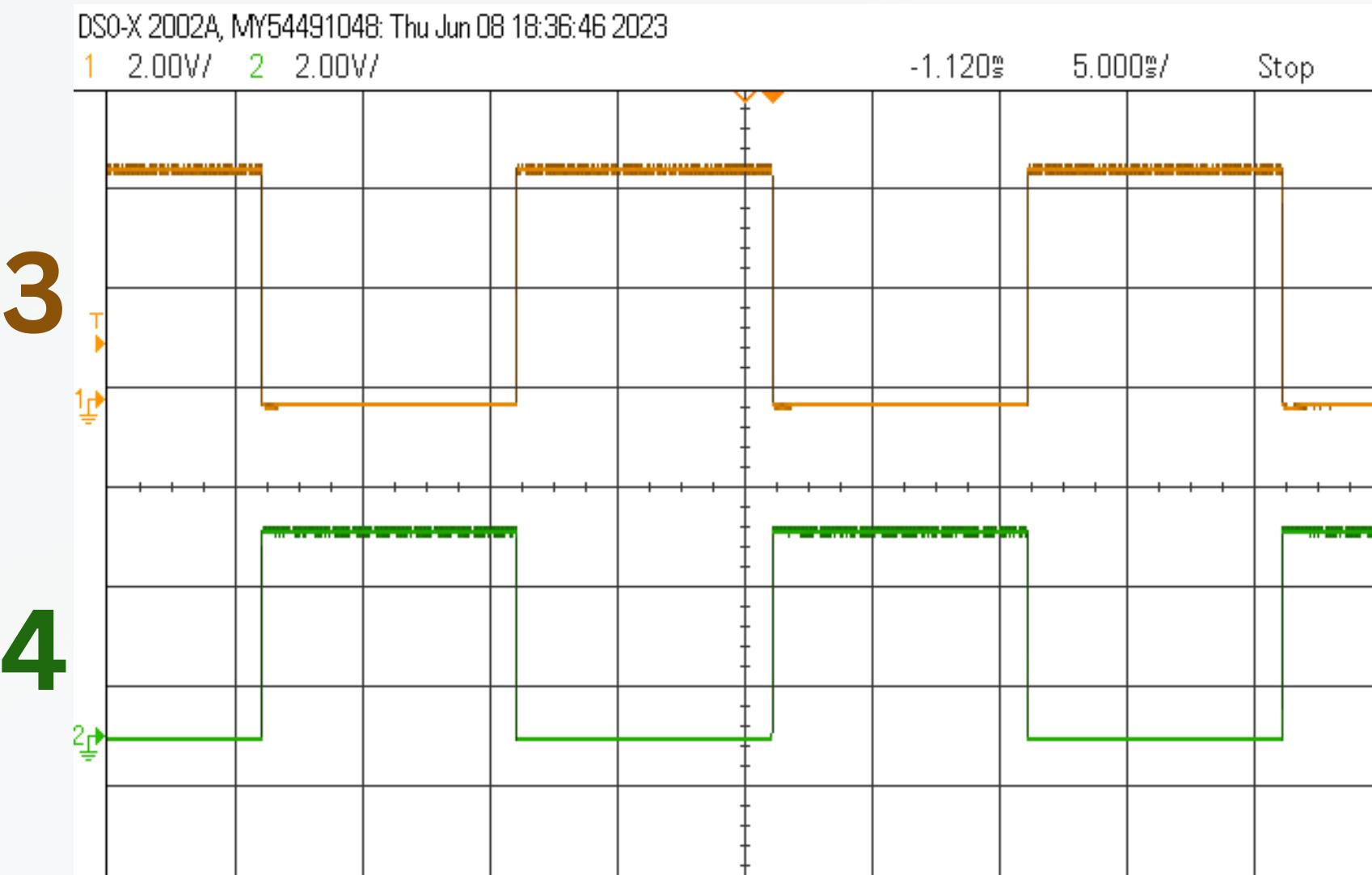
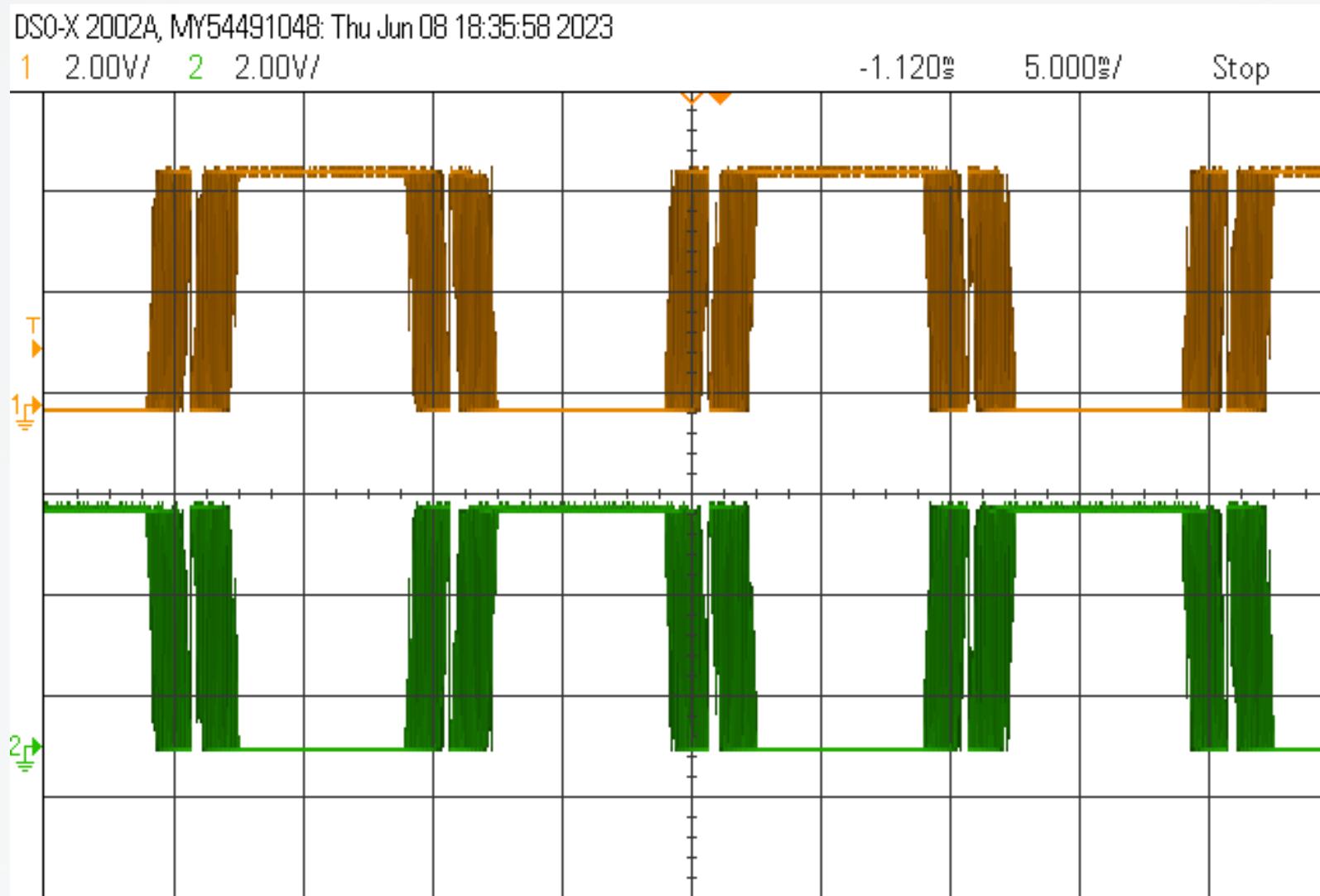


DSPIC CIRCUIT BOARD



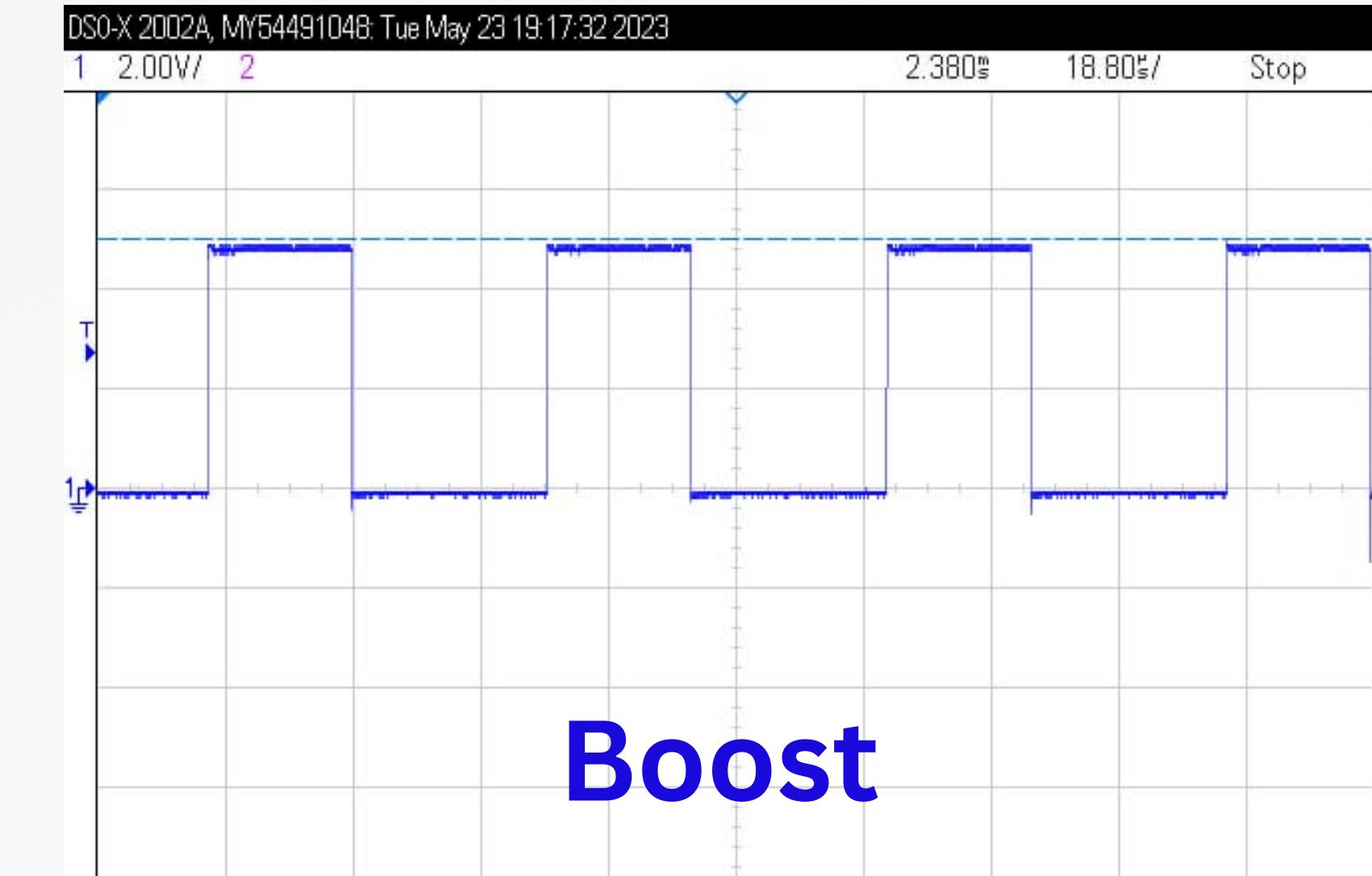
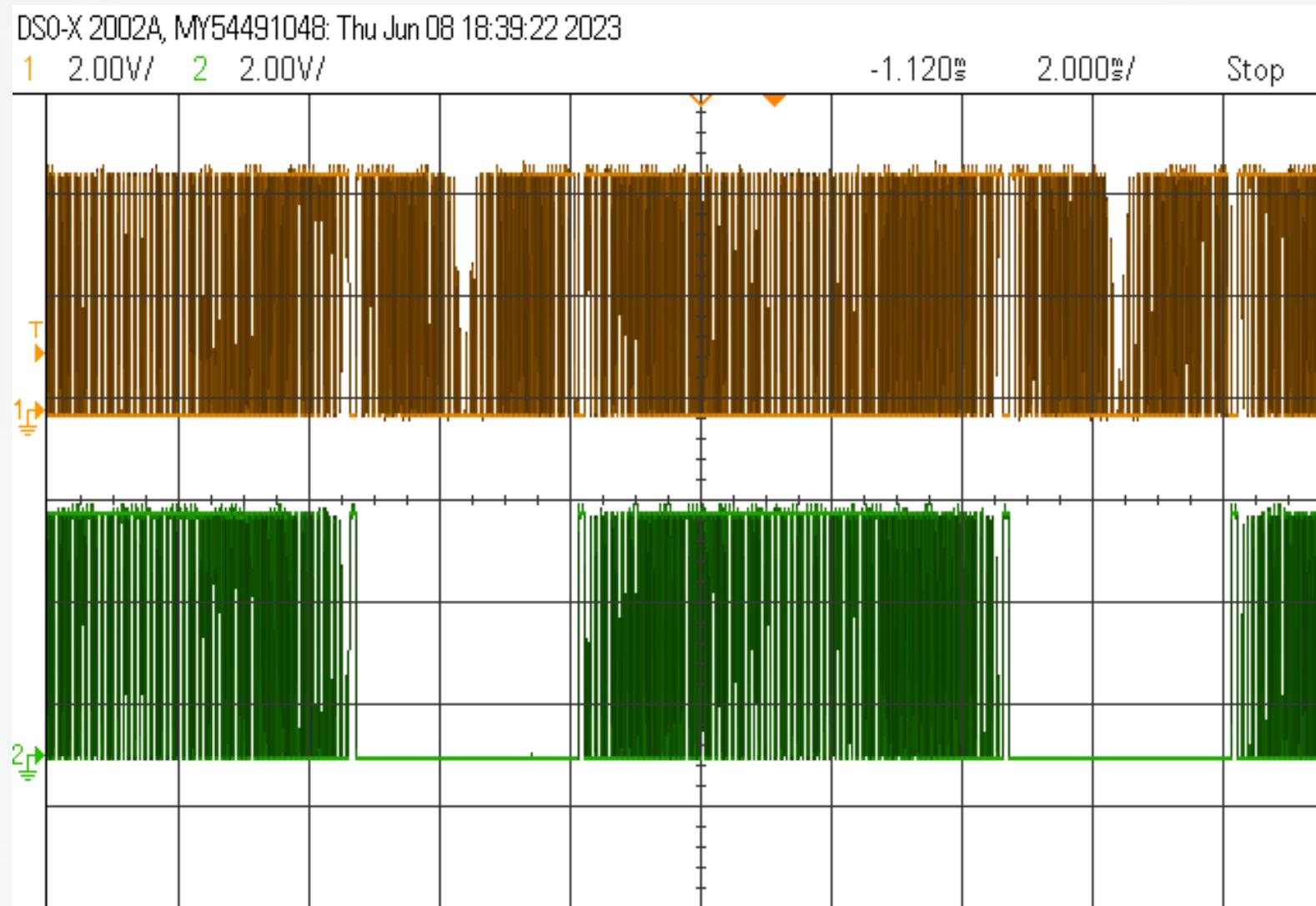
SWITCHING SIGNALS

H-BRIDGE



SWITCHING SIGNALS CAPACITOR CELL & BOOST

Sc1
Sc3
Sc2



GATE POWER

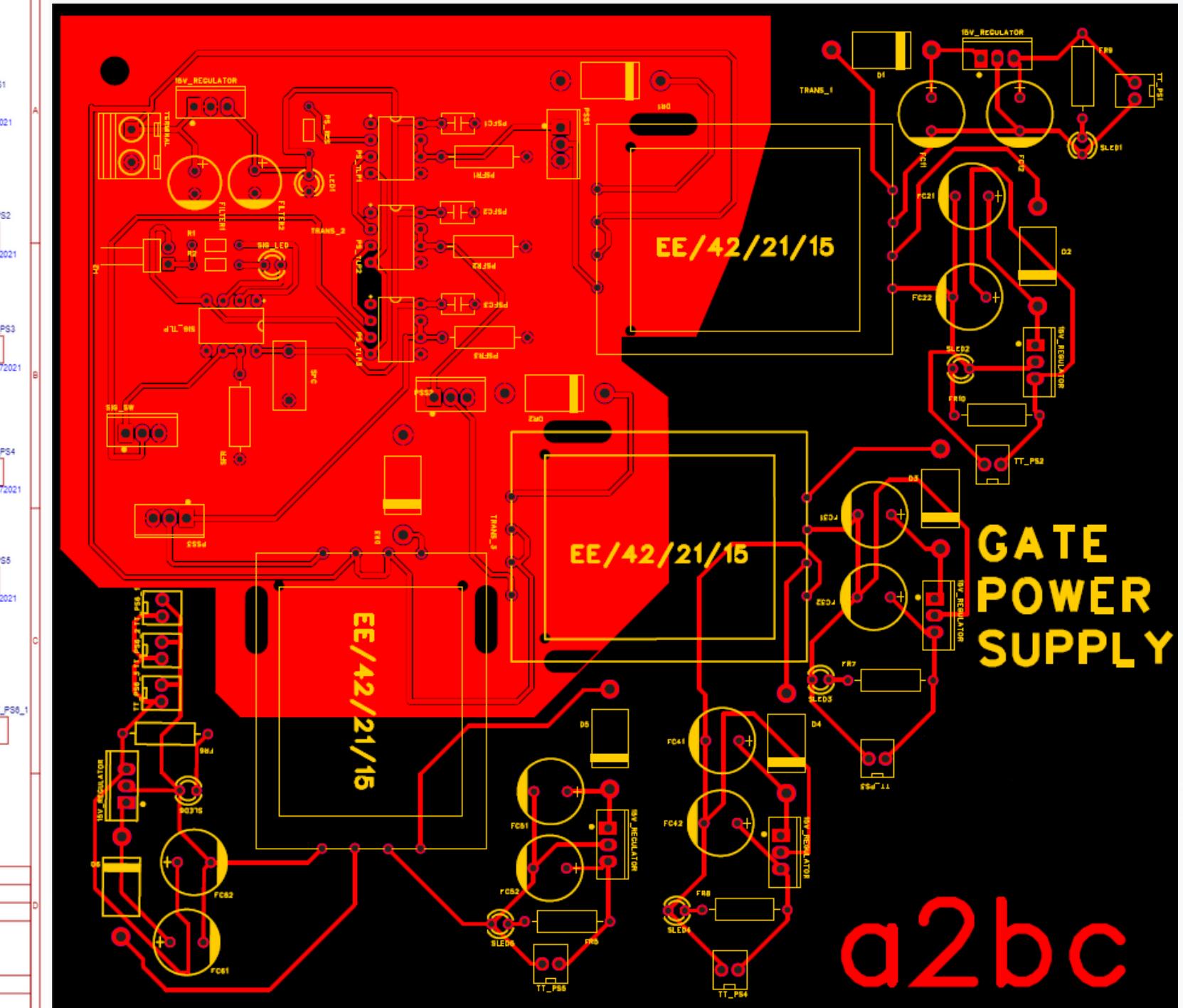
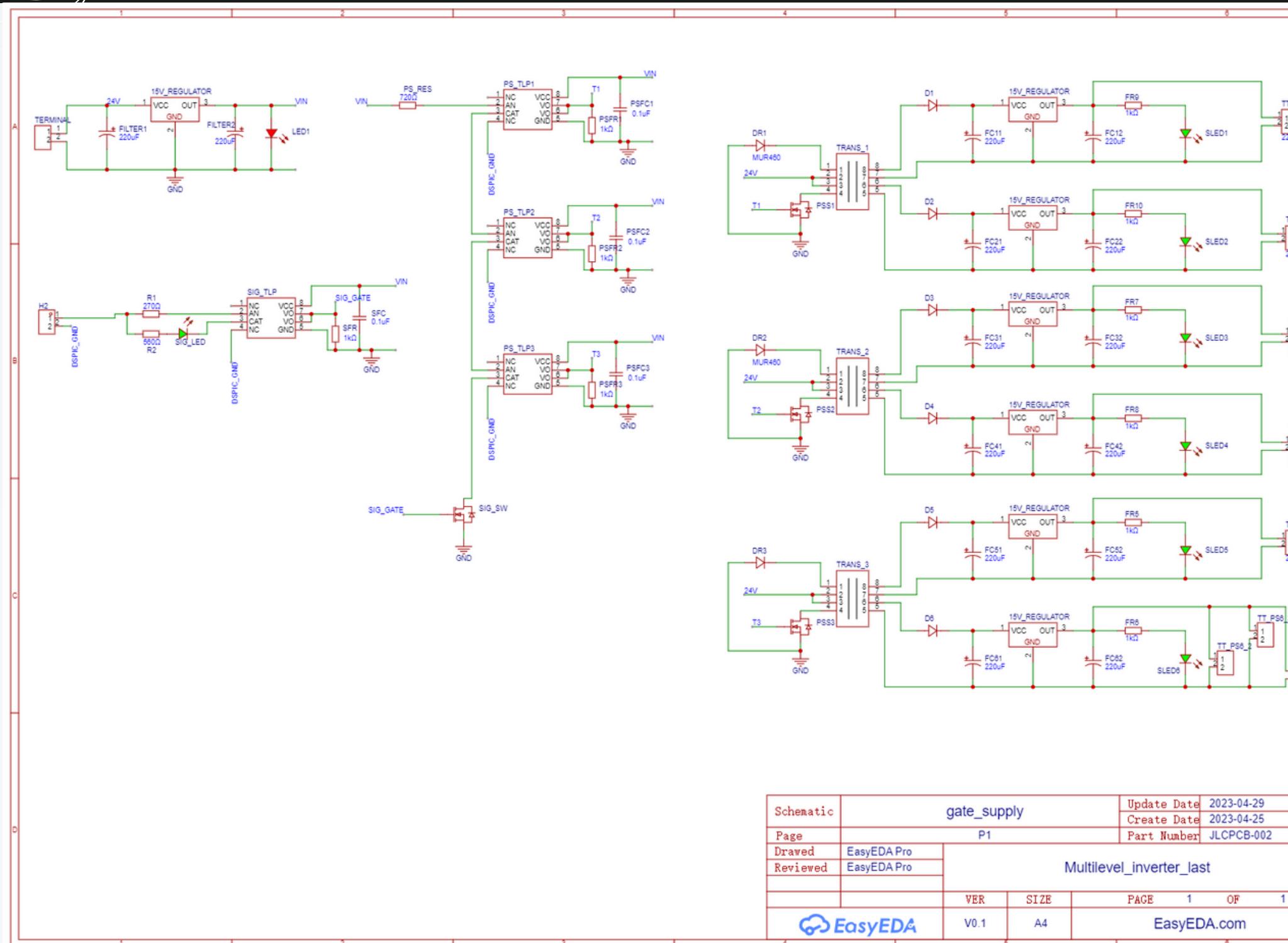
Need of Gate Power circuit??

- The non sharing of common ground of all switches.
- The requirement of 6 independent 15 volt sources to power up all the gate driver IC's(TLP250).
- Idea of bringing about all sources of supply from one single unit.
- Used forward converter isolator mode.
- Designed 3 transformers such that a single transformer has two secondary windings with each output as 15 volts.

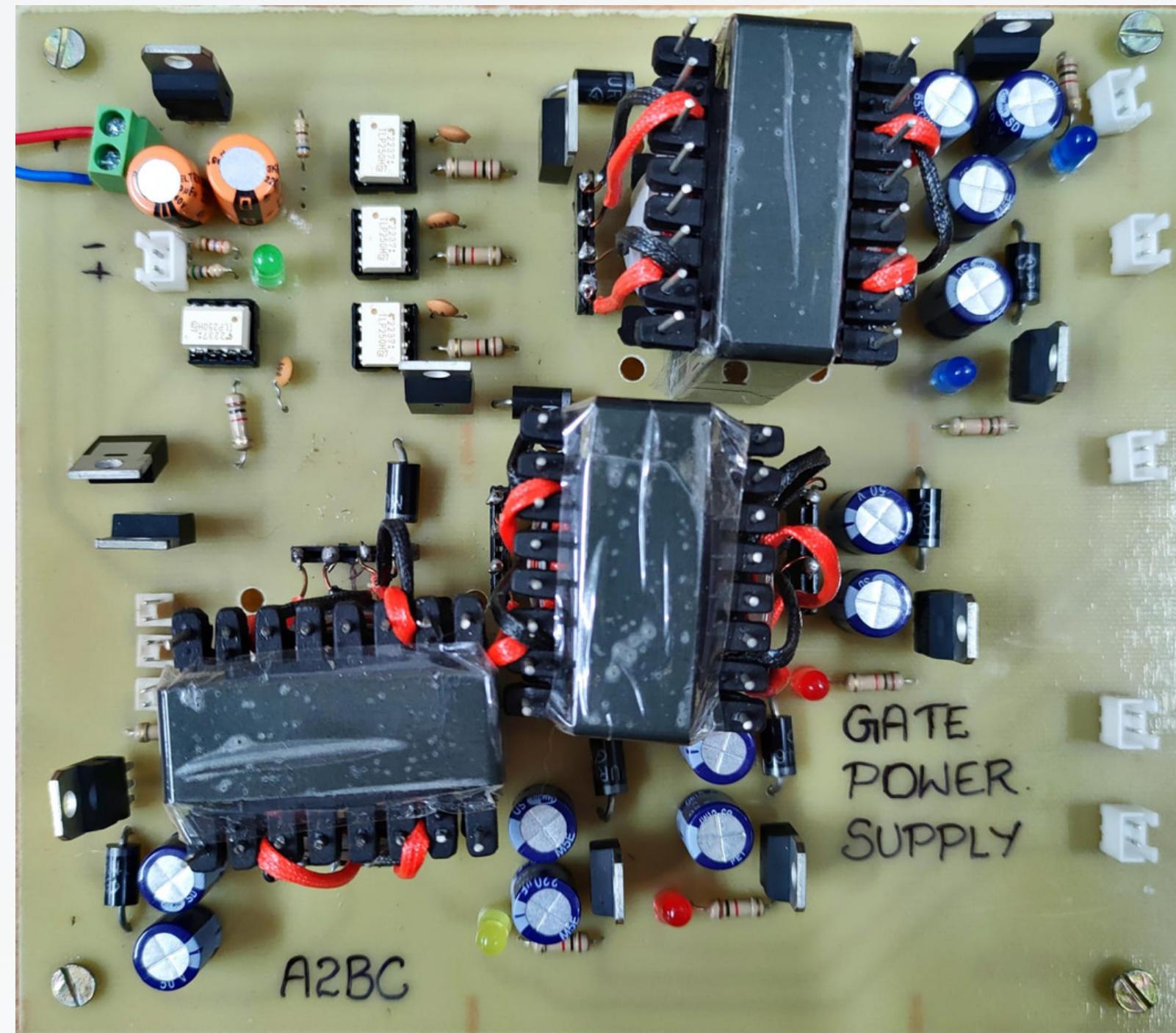


Transformer Specifications		
Core		EE42/21/15
No.of turns	Primary	33
	Secondary	28
Input Voltage		24V
Output Voltage		20V

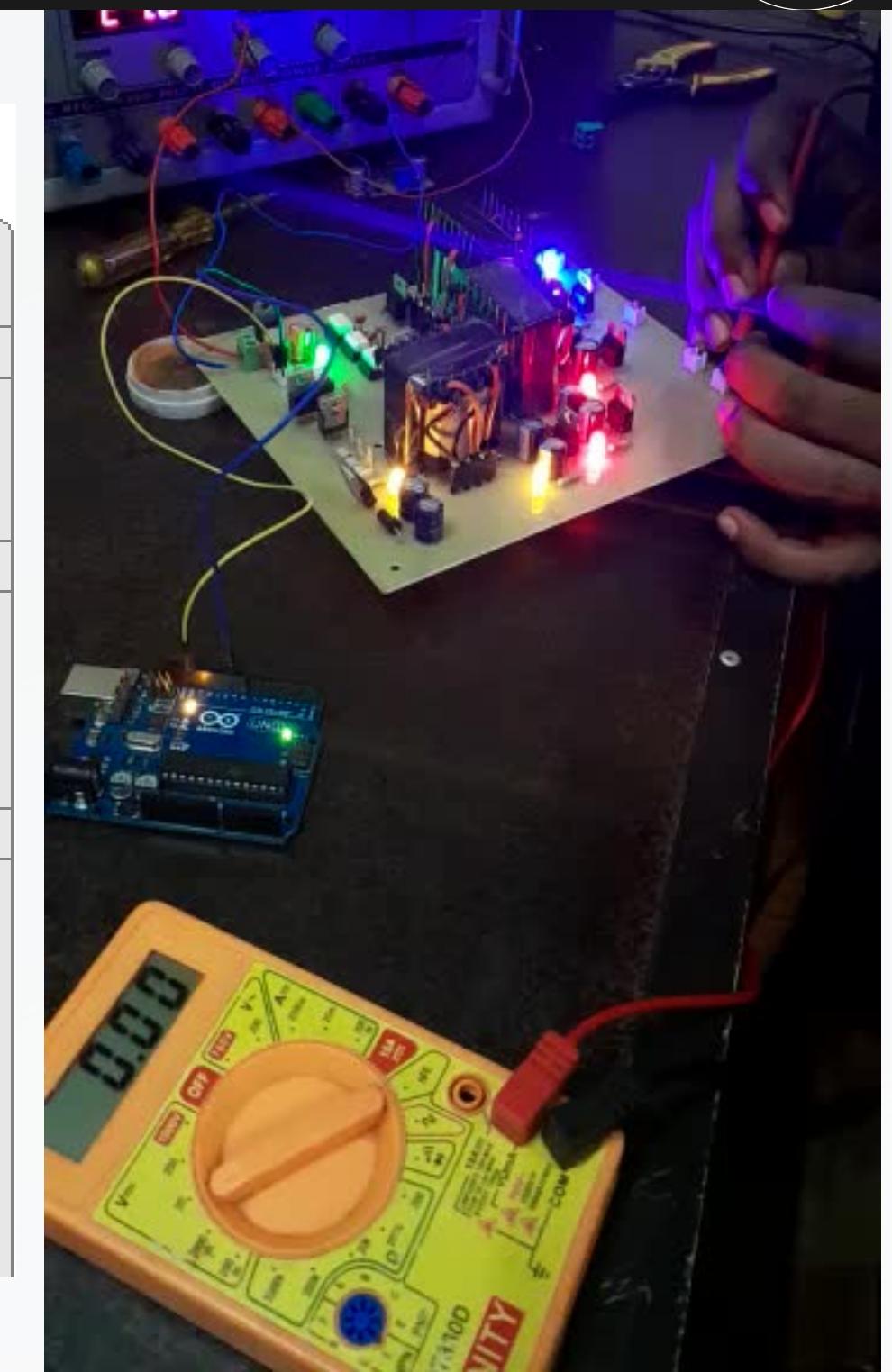
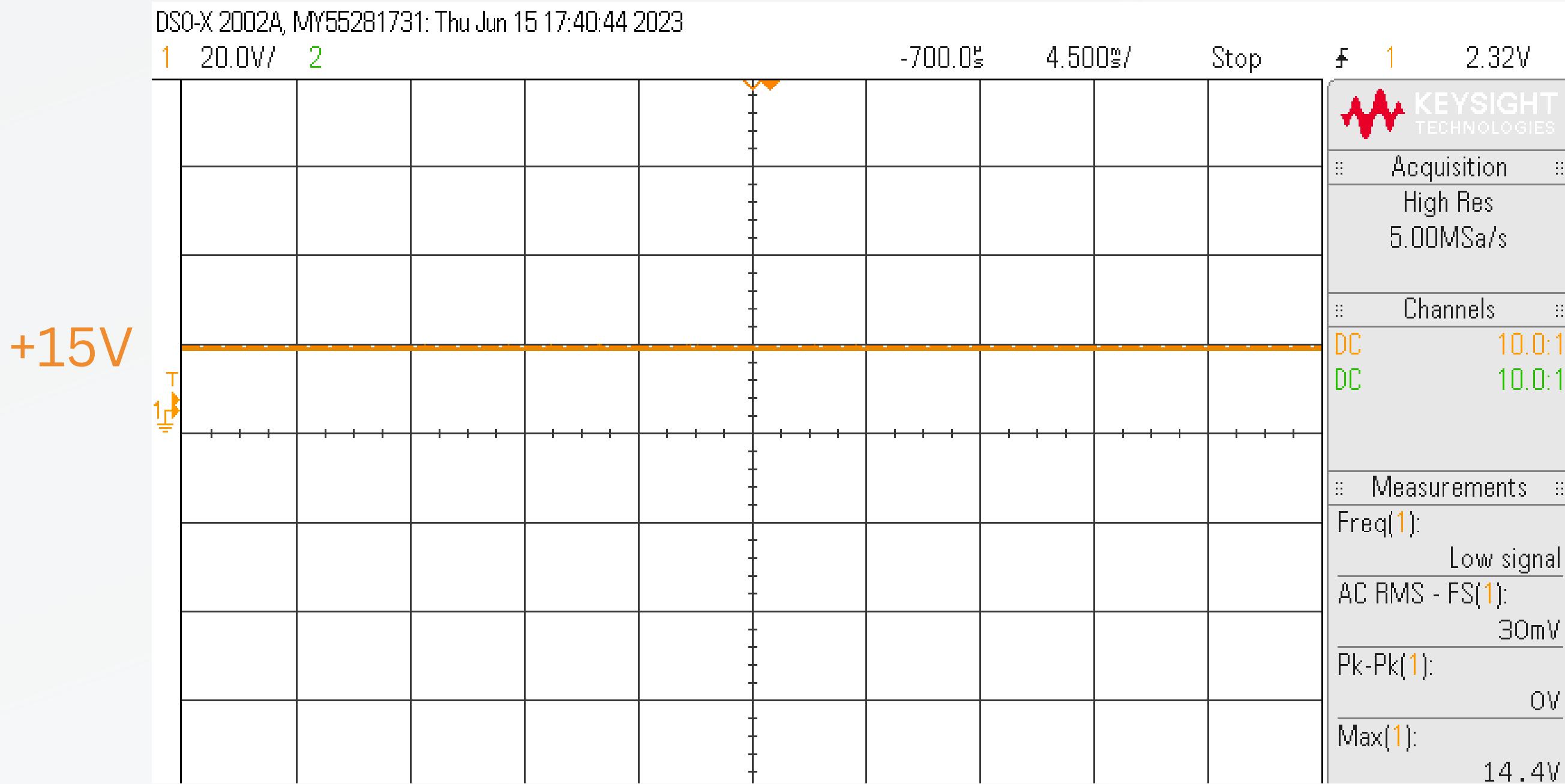
Schematic Diagram & PCB Layout



GATE POWER CIRCUIT BOARD



GATE POWER CIRCUIT OUTPUT



MAIN CIRCUIT

- Boost converter
- Switched capacitor cell structure
- H-Bridge inverter

MAJOR COMPONENTS



IRFP460

- $V_{DSS} = 500V$
- $V_{GS} = 2-4V$
- $I_S = 20A$

• MUR460

- Peak RRV : 600V
- Permissible peak current: upto 70 A

SWITCHING CAPACITOR



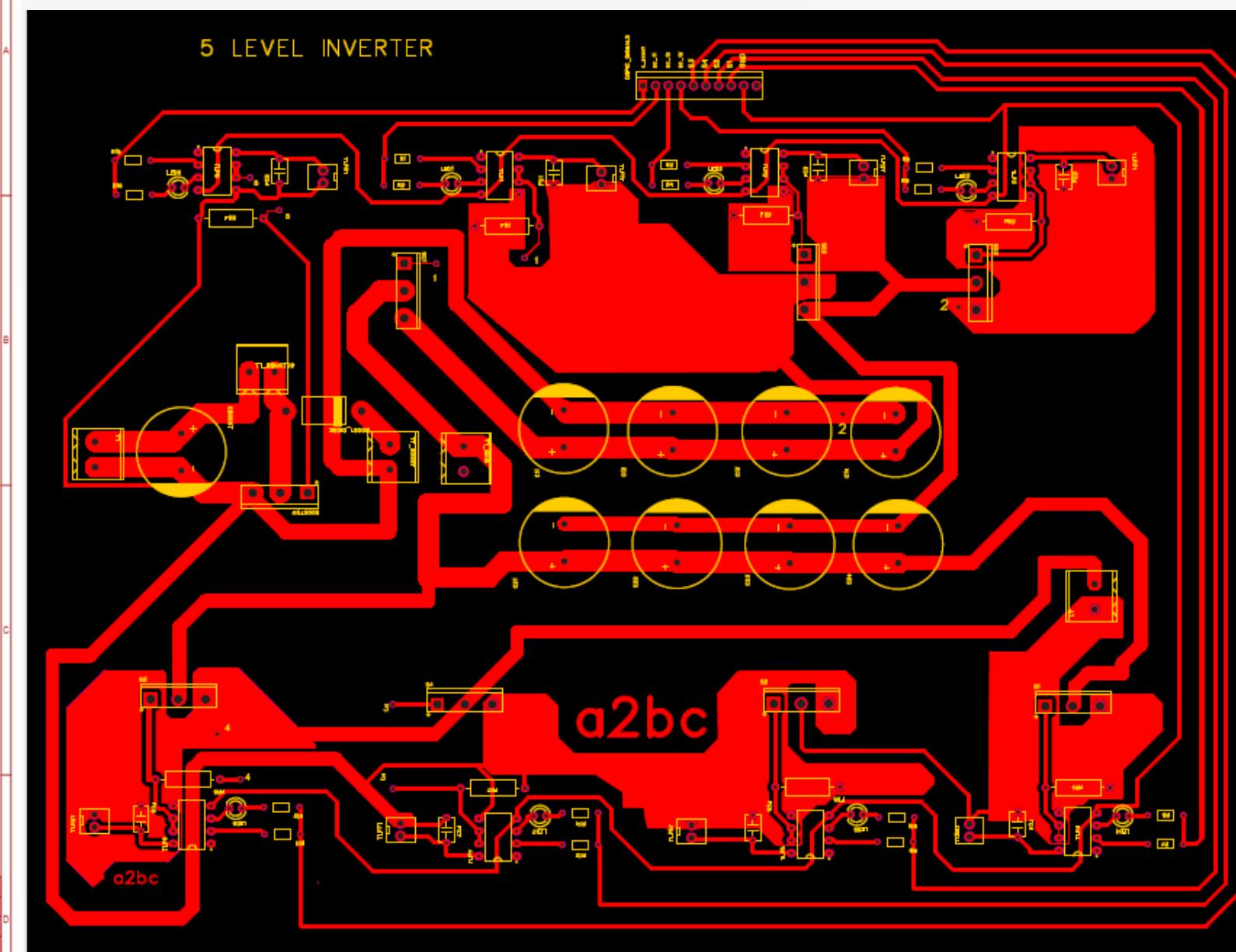
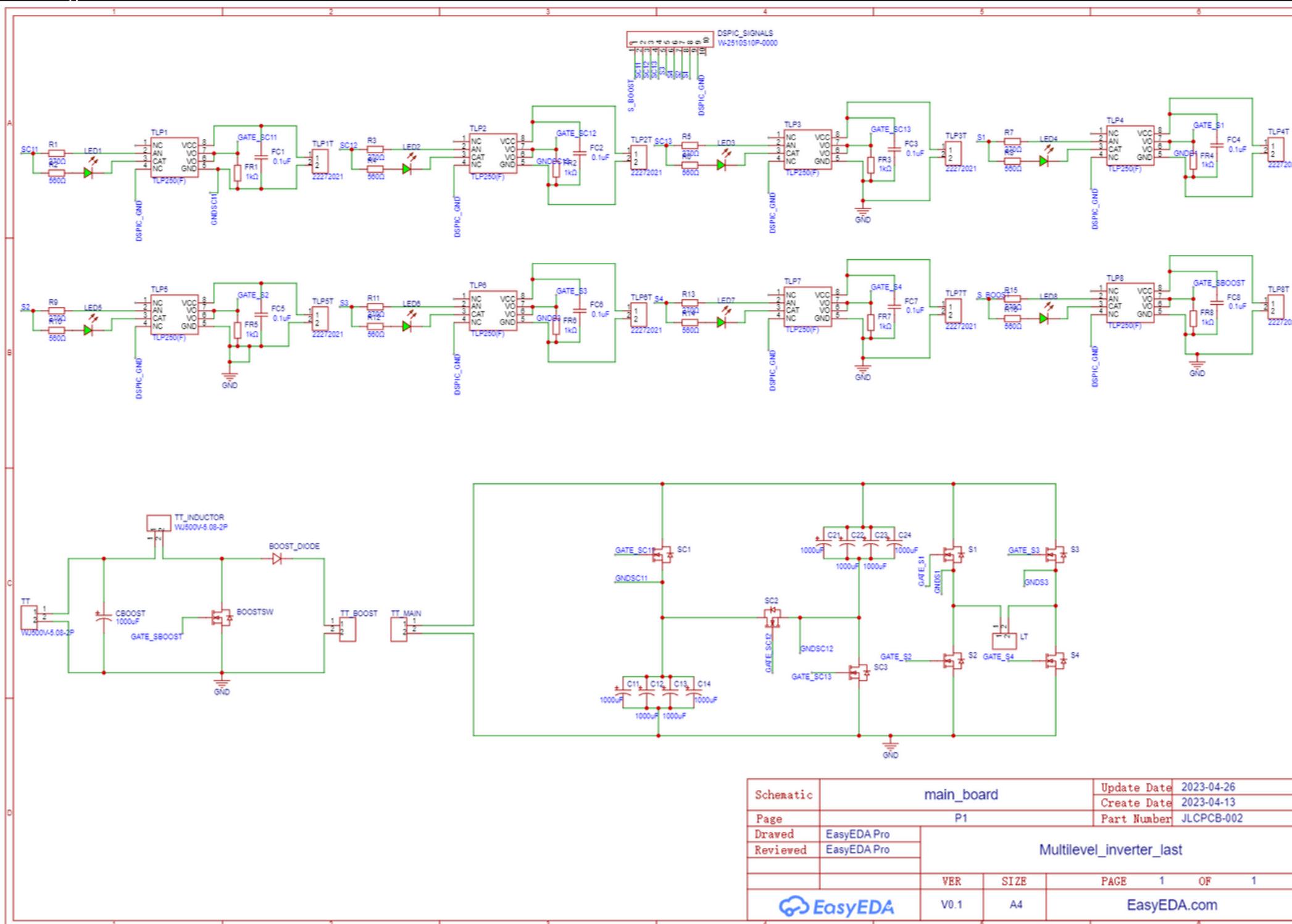
- Required Capacitance: 3.9mH
- Capacitor : 1000 μF 100 V
- 4 capacitors in parallel

BOOST INDUCTOR

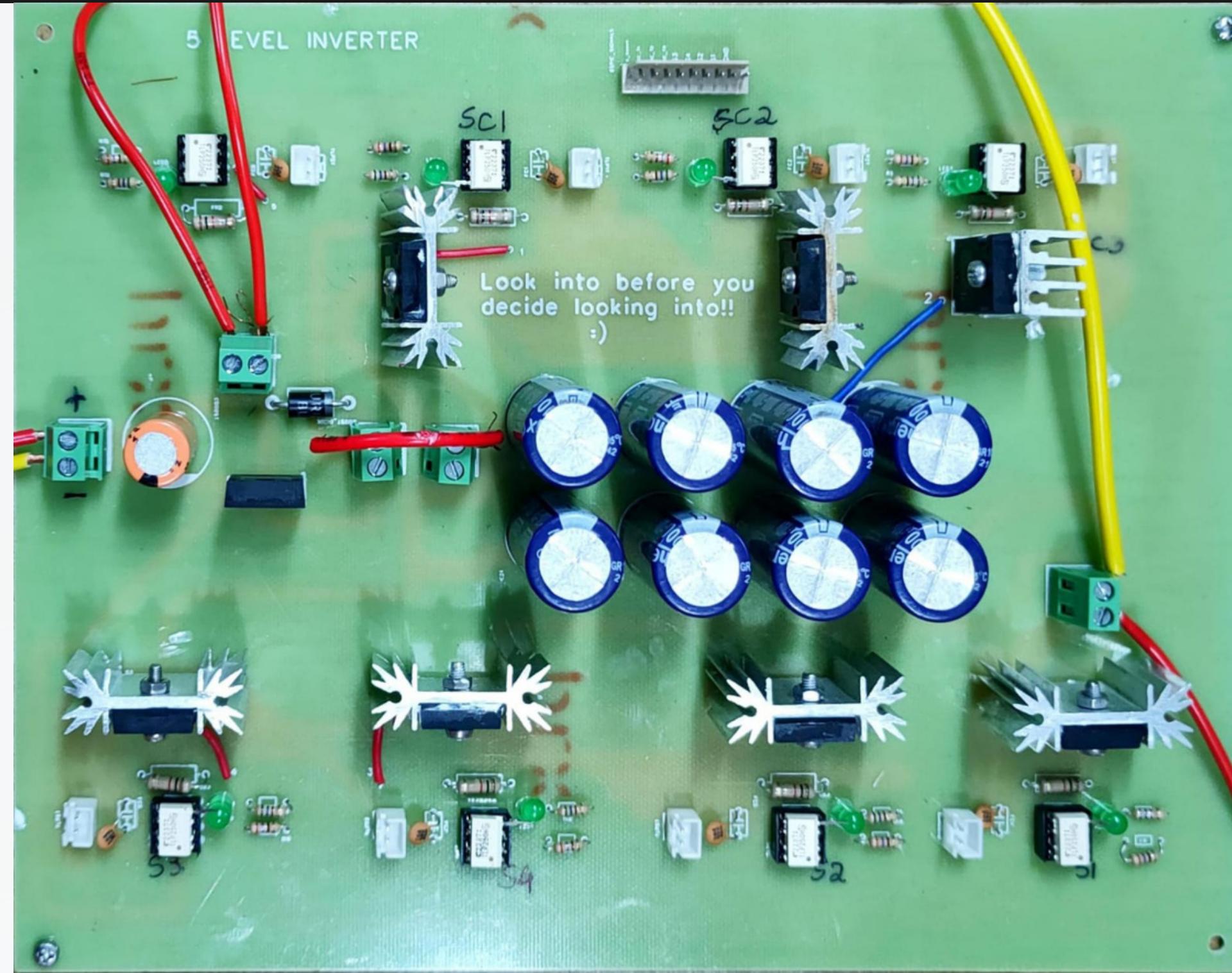


- Required Inductance $> 0.9mH$
- Core: EE65/32/26
- Conductor size: 16 SWG
- No, of Turns: 124

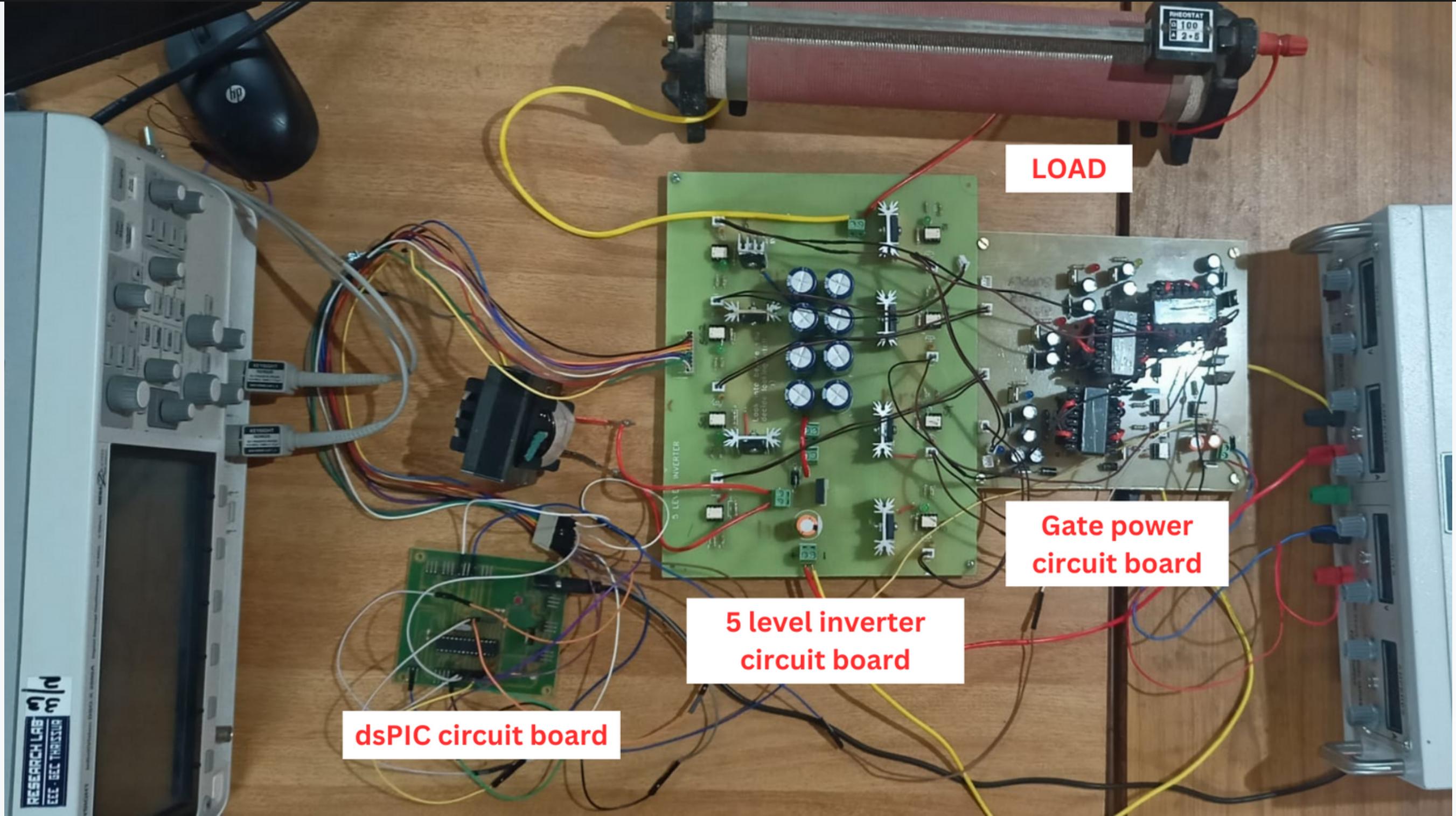
SCHEMATIC DIAGRAM & PCB LAYOUT



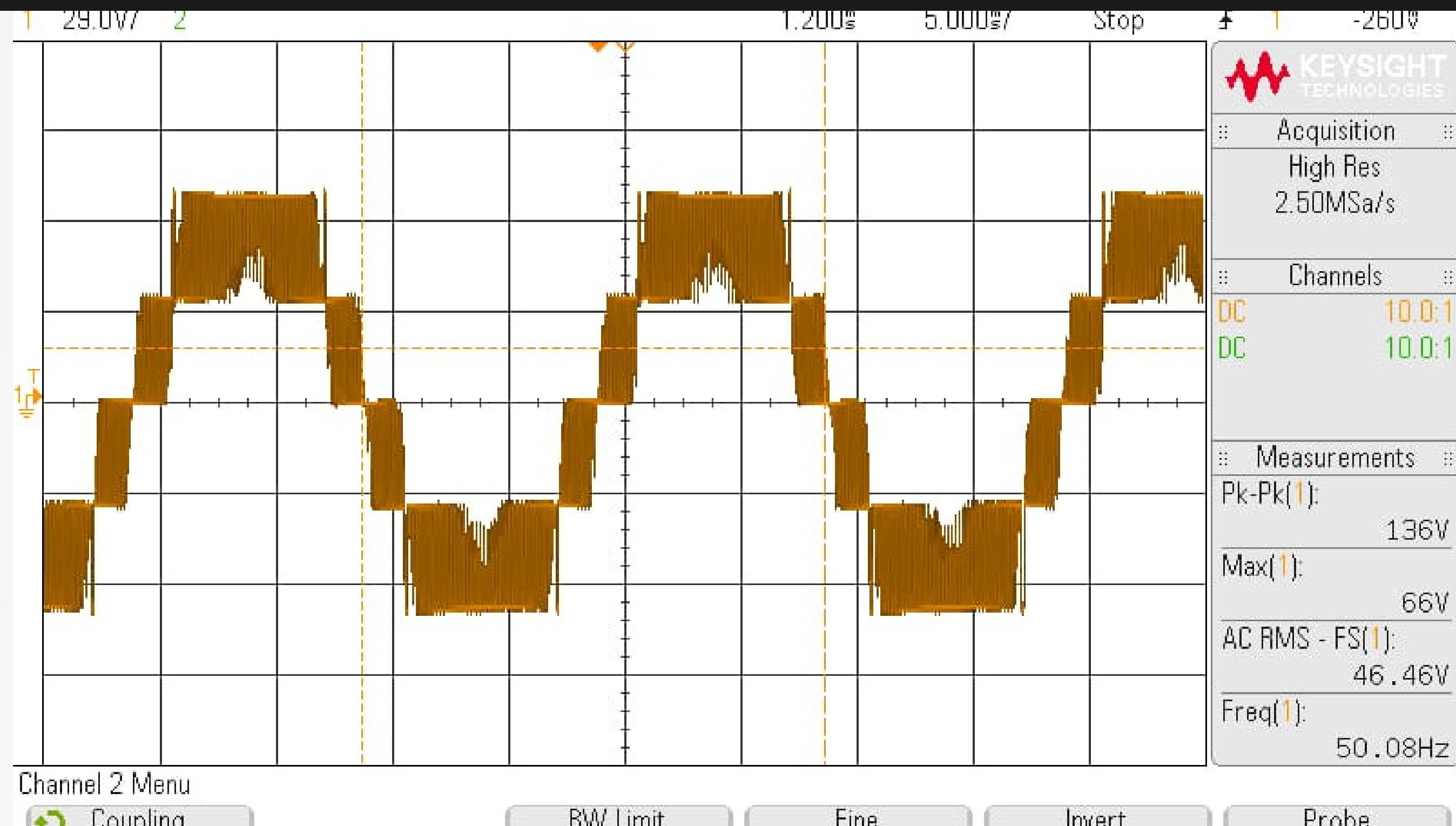
MAIN CIRCUIT BOARD



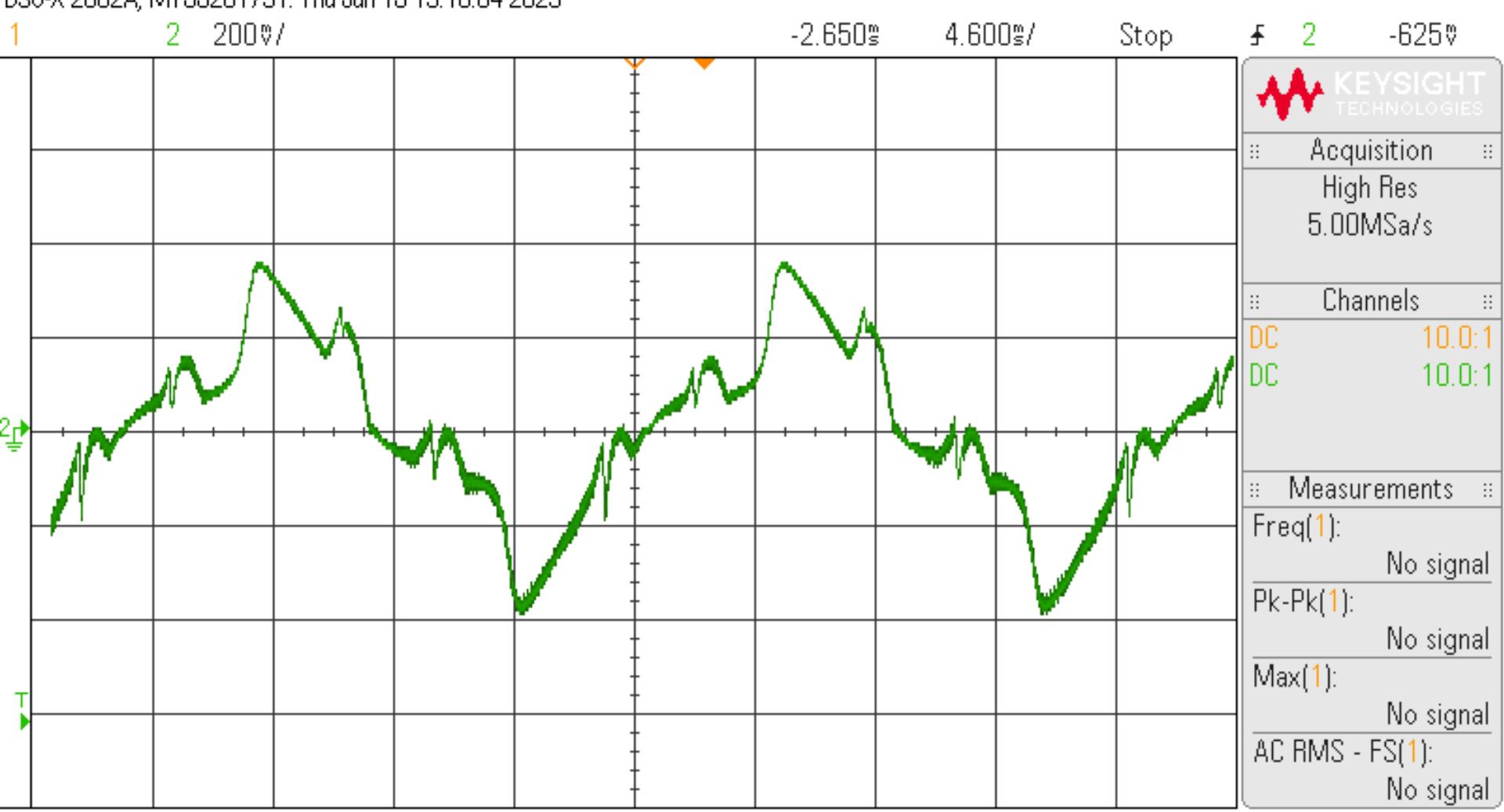
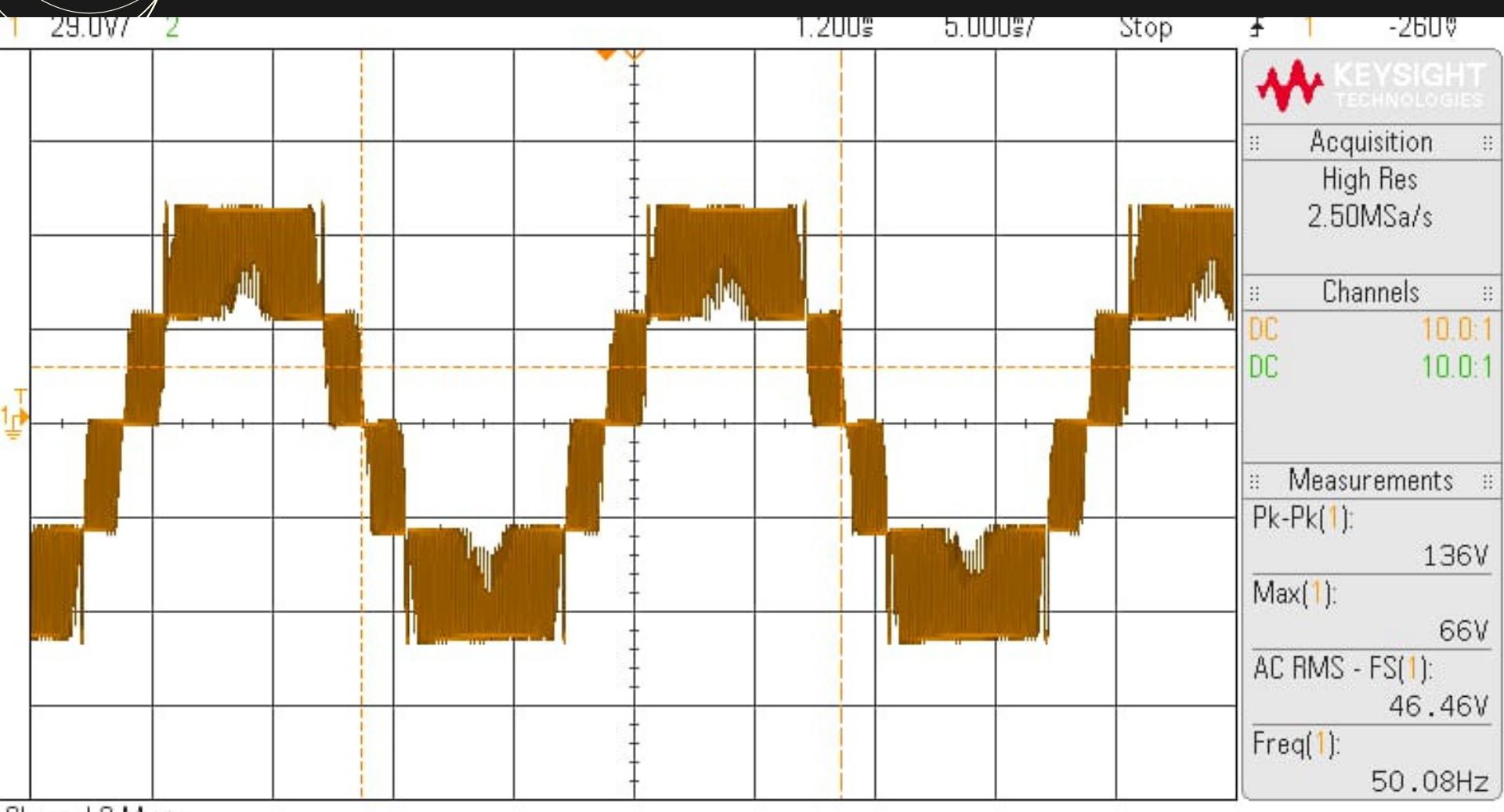
SYSTEM SETUP



VOLTAGE WAVEFORM WITH R LOAD

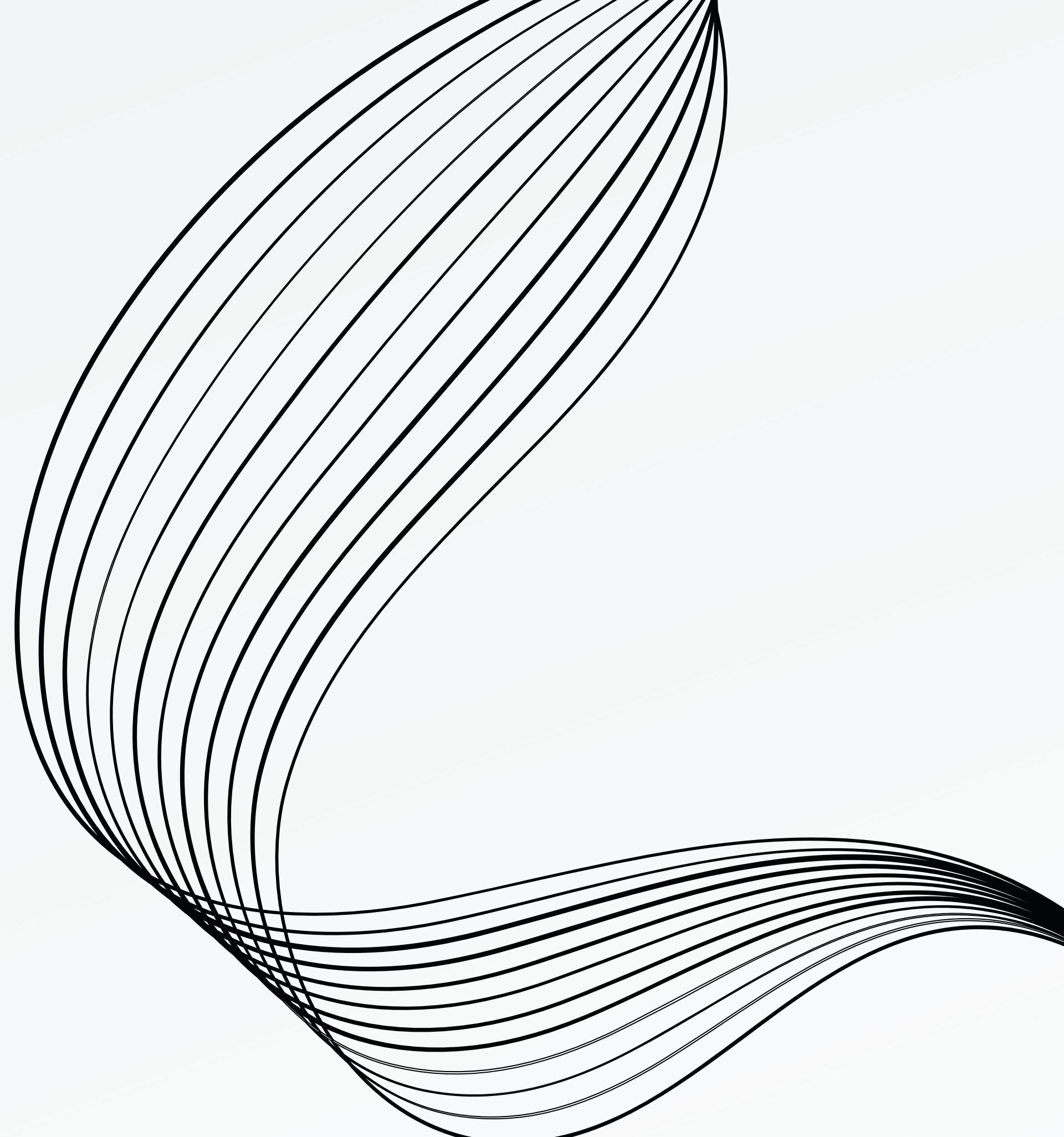


VOLTAGE AND CURRENT WAVEFORM WITH RL LOAD



HARDWARE PARAMETERS

Parameters	Values
Input Voltage	24V
Input Current	2.8A
Output Voltage (rms)	46V
Output Current (rms)	1.26A
Output Frequency	49.84Hz



FUTURE SCOPE

- In this topology of multilevel inverters Increasing the no. of levels is easy just by adding identical switched capacitor structure.
- Compatible for large power applications.
- Integration with the grid system

CONCLUSION

- Literature survey of the existing multilevel inverter topology was carried out.
- Based on the survey,it is identified that switched capacitor topology with front-end boost stage will give a better performance
- The simulation and modelling of the inverter based on 5-level switched capacitor was done
- Hardware implementation was done to verify the same and got satisfactory results
- Documentation of the findings and results were prepared.

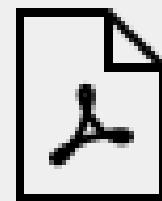
REFERENCES



M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li and F. Blaabjerg, "Switched Capacitor Integrated $(2n + 1)$ -Level Step-Up Single-Phase Inverter," in IEEE Transactions on Power Electronics, vol. 35, no. 8, pp. 8248-8260, Aug. 2020, doi: 10.1109/TPEL.2019.2963344.



Dargahi, V., Sadigh, A. K., Abarzadeh, M., Eskandari, S., & Corzine, K. A. (2015). A New Family of Modular Multilevel Converter Based on Modified Flying-Capacitor Multicell Converters. *IEEE Transactions on Power Electronics*, 30(1), 138–147. doi:10.1109/tpel.2014.2304964



Nabae, A., Takahashi, I., & Akagi, H. (1981). A New Neutral-Point-Clamped PWM Inverter. *IEEE Transactions on Industry Applications*, IA-17(5), 518–523. doi:10.1109/tia.1981.4503992

QUERIES

A2BC

