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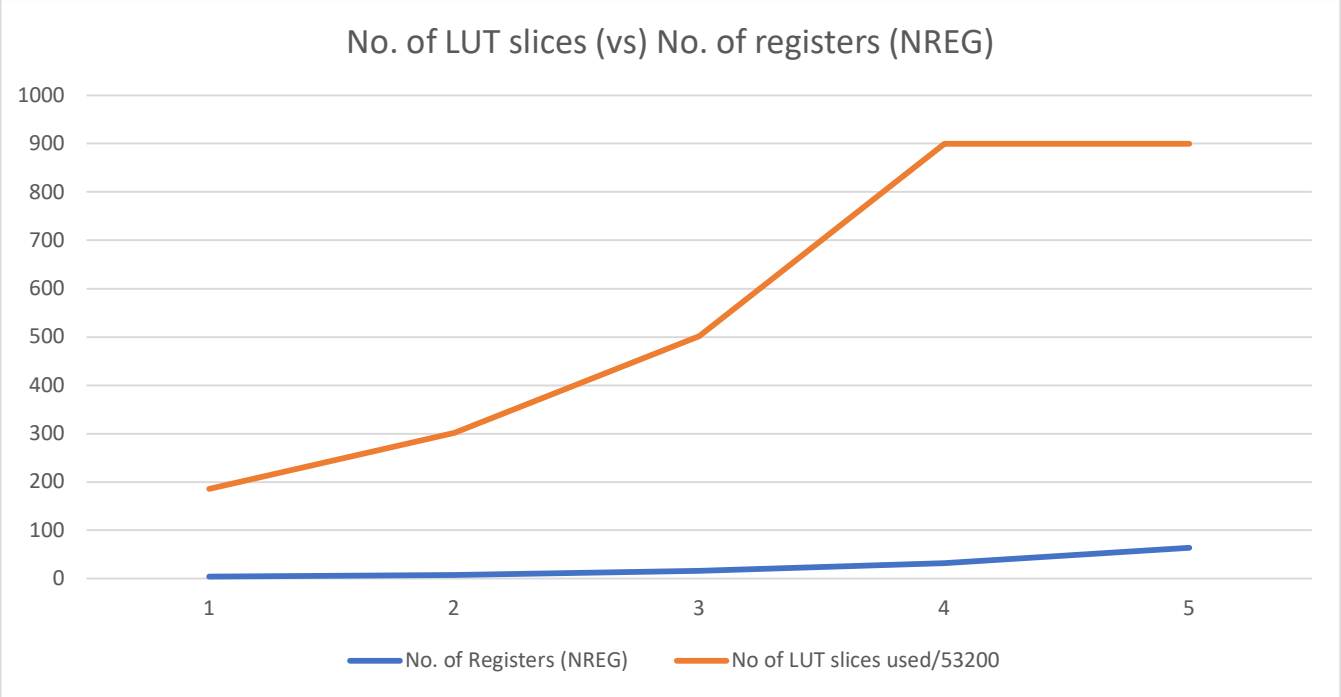
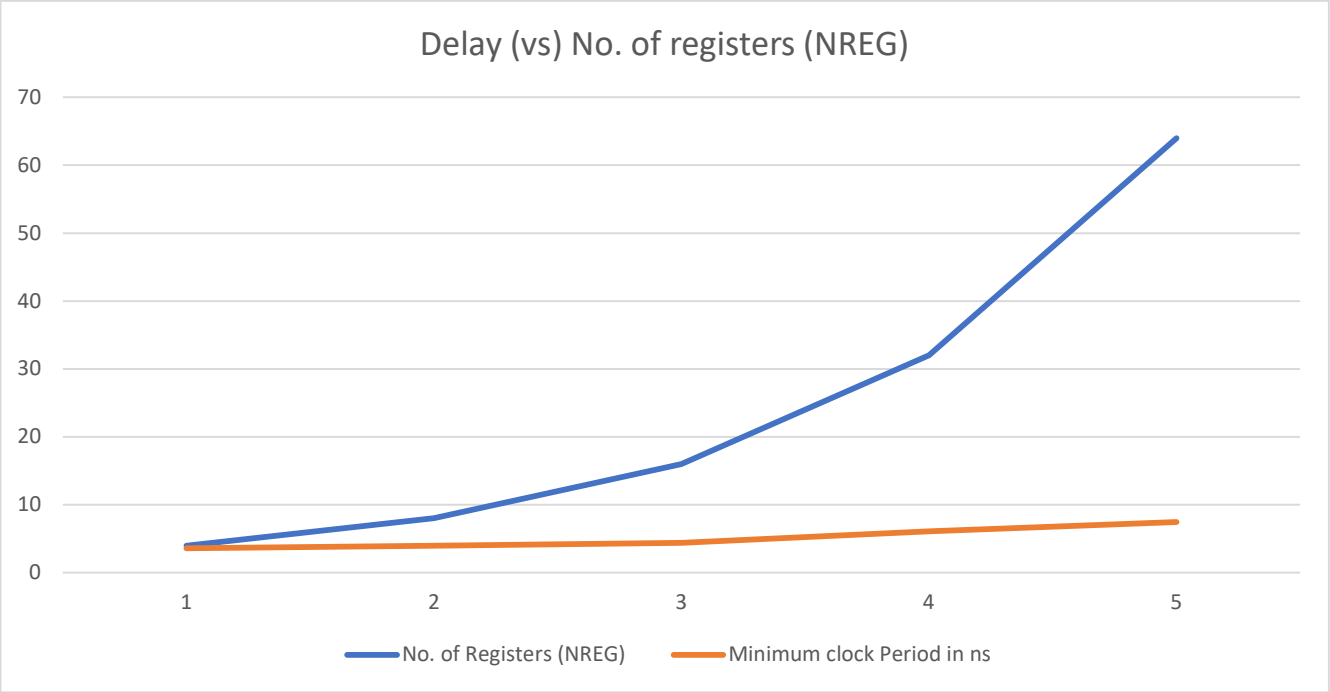
CS221 ASSIGNMENT

TASK 1

1. Plot the graph, area in LUT slices (vs) No. of registers (NREG) as well as delay (vs) No.of registers (NREG) for the register file module for NREG = 16, 32, 64. Set DSIZE (bit-width of each register) =32.

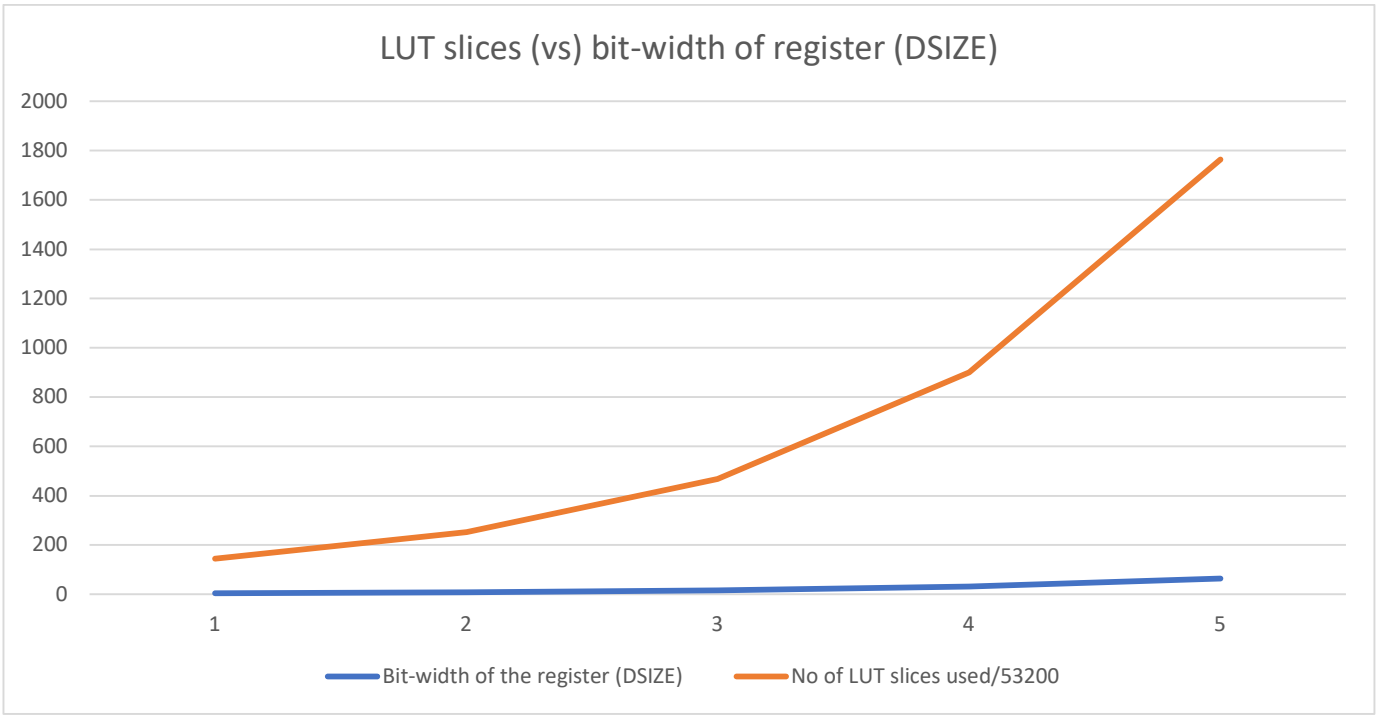
No. of Registers (NREG)	Bit-width of the register (DSIZE)	No of register slices used	No of LUT slices used	Minimum clock Period in ns
4	32	128/106400	186/53200	3.602
8	32	256/106400	302/53200	4.003
16	32	512/106400	502/53200	4.402
32	32	1024/106400	900/53200	6.11
64	32	1024/106400	900/53200	7.47

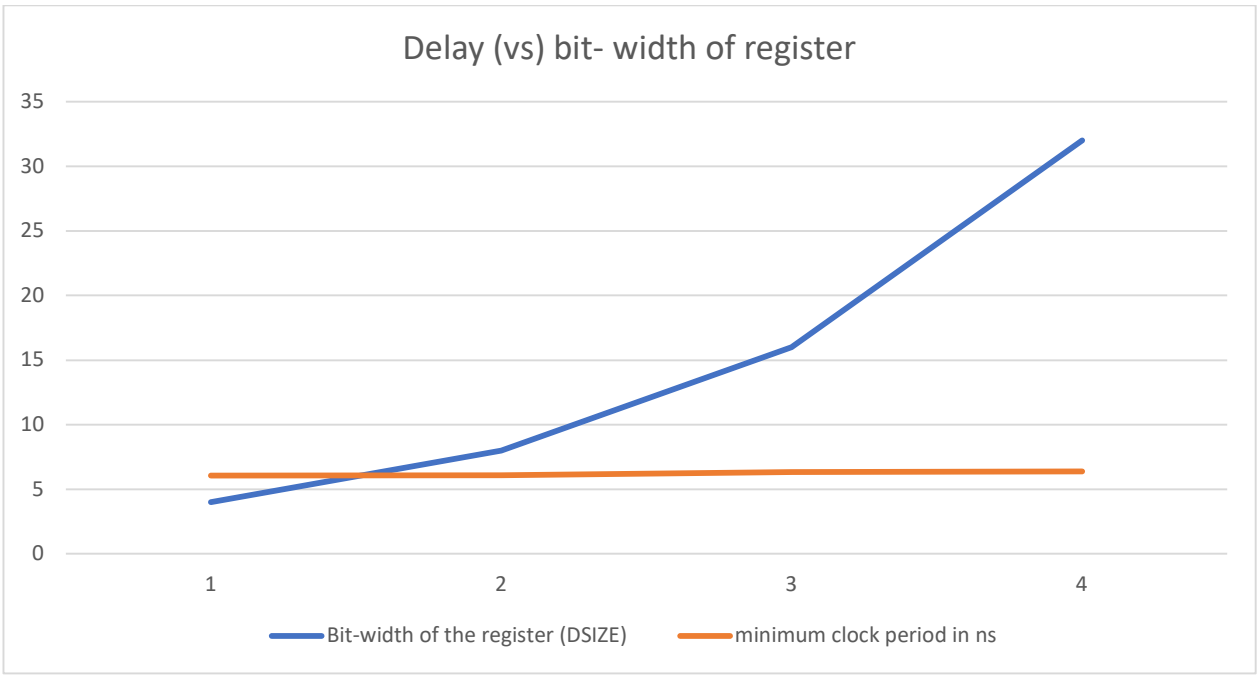




2) Plot the graph, area in LUT slices (vs) bit-width of register (DSIZE) as well as delay (vs) bit-width of register (DSIZE) for the register file module for DSIZE = 16, 32, 64. Set NREG (number of registers) =32.

Bit-width of the register (DSIZE)	**No. of registers (NREG)**	**No of register slices used**	**No of LUT slices used**	**minimum clock period in ns**
4	32	128/106400	144/53200	6.07
8	32	256/106400	252/53200	6.097
16	32	512/106400	468/53200	6.339
32	32	1024/106400	900/53200	6.38
64	32	2048/106400	1764/53200	(Some error was occuring) *


LUT slices (vs) bit-width of register (DSIZE)
2000
1800
1600
1400
1200
1000
800
600
400
200
0
1
2
3
4
5
Bit-width of the register (DSIZE)
No of LUT slices used/53200


Delay (vs) bit- width of register
35
30
25
20
15
10
5
0
1
2
3
4
Bit-width of the register (DSIZE)
minimum clock period in ns

TASK 2

You need to set the input bit-width to 8, 16 and 32 (one by one) and find out the number of slices used. You need to plot area (vs) bit-width as well as delay (vs) bit-widthfor the ALU module. In FPGA you cannot find area directly so instead of area you can take number of slices, which would be considered proportional to the area.

Bit-width of the register (DSIZE)	**No. of registers (NREG)**	**No of LUT slices used/53200**	**minimum clock period in ns**
8	32	8	8.438
16	32	16	8.416
32	32	32	11.037