Nine-Level Active Neutral Point Clamped Inverter for EV Charging Station Applications

A

Thesis

Submitted in partial fulfillment of the requirements for the Degree of

MASTER OF TECHNOLOGY

by

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June 2024

Declaration

This is to certify that the thesis entitled "**Nine-Level Active Neutral Point Clamped Inverter for EV Charging Station Applications**", submitted by me to the Indian Institute of Technology Guwahati, for the award of the degree of M.Tech, is a bonafide work carried out by me under the supervision of **Dr. Ravindranath Adda**. The content of this thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree. I have made every effort to uphold academic integrity and honesty throughout this research. Proper citations and acknowledgments have been provided whenever external information, statements, or results have been utilized

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Supervisor: **Dr. Ravindranath Adda**

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Abstract

This report presents a standalone single-phase nine-level active neutral point clamped inverter topology. The proposed topology significantly reduces voltage stress on switches and has added benefit of modularity required for system-level studies in various applications that use ANPCI as the main power conversion stage. Here an LC filter is used to reduce switching harmonics and improve quality of output waveform. The study implements DSP based algorithm for the DC-link capacitor and flying capacitors. The system uses a synchronous reference frame (SRF)-based dq closed-loop control strategy to maintain output quality even under load change. The open-loop and closed-loop of the converter is analyzed in detail, and the simulation results demonstrate its effectiveness. Moreover, the capacitor voltage balancing technique proves effective in maintaining capacitor voltages, reducing capacitor leakage currents and enhancing the system's overall performance. The hardware prototype of single-leg ANPCI has been developed and tested. Additionally, the proposed nine-level ANPCI is simulated with non-linear load and the results obtained are satisfactory.

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Chapter 1

Introduction

One of the prominent drivers behind implementation of renewable energy sources (RES) is the increasing concern for environmental sustainability and the need to reduce greenhouse gas emissions. Traditional thermal power generation, which heavily relies on fossil fuels, is a major contributor to air pollution and climate change. RES, on the other hand, offer a clean and sustainable alternative. Solar, Wind, Biomass, and other RES are a pollution-free ways to supply green energy to a variety of loads. Among all the RES, solar energy is one of the top choice among renewable sources because of its abundance. Solar energy is the fastest-growing RES in the world. In 2022, solar PV accounted for 10% of global electricity generation, up from 9% in 2021. Solar PV is one of the largest contributor of RES globally, and it is expected to continue to grow rapidly in the coming years. Its applications can be seen in transportation sector, electric vehicles (EVs) and solar power sector. [1]

EVs are becoming increasingly popular in transportation sector as a substitute for petroleum based vehicles. However, EVs can be expensive to purchase and have dependence on fossil fuel based power generation system. Solar energy can be used to address both of these challenges. Solar panels can be installed in the charging stations. EVs characteristics are built using solar modules in such a way that when power is not needed by the EV, it will be supplied back to the grid. Additionally, EVs and solar power can work together to provide a more robust and sustainable energy system. Solar energy can be utilized to power buildings and other infrastructure by being produced and stored in batteries, which lessens reliance on the conventional power grid. Solar

energy can help to reduce our reliance on fossil fuels, which are a finite resource and a major source of greenhouse gas emissions. [2]

The need for solar energy has grown in significance in the context of electric vehicles since it offers a clean, affordable, and sustainable source of energy for their operation. Combining solar power and electric vehicles can result in a more robust and sustainable energy system, reducing our dependence on fossil fuels

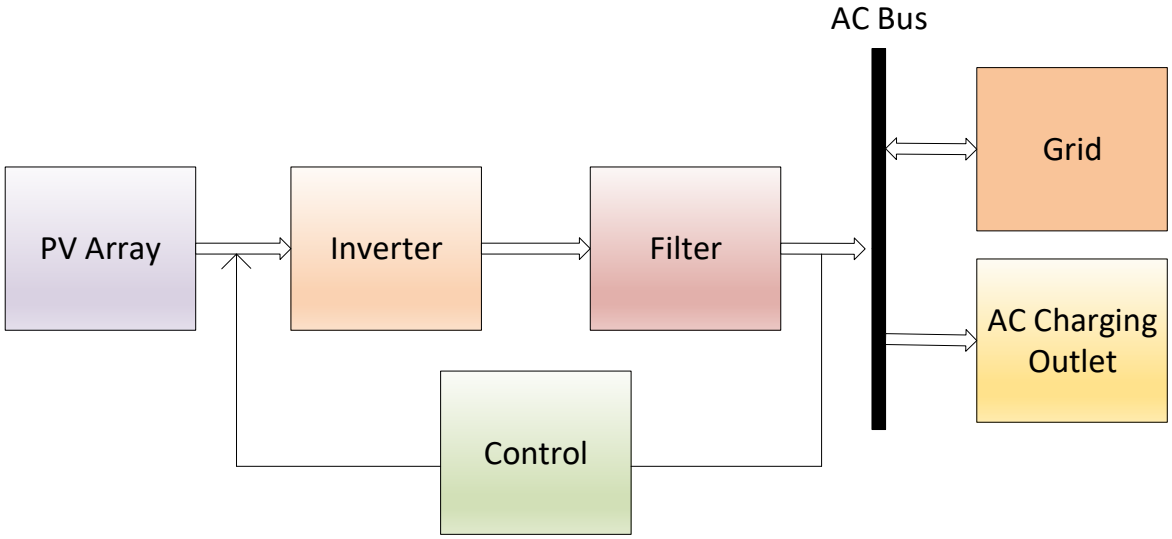

Figure 1.1: General block diagram for inverter based system

But due to deployment of more EVs on the road, charging of the vehicle will be problematic if electric grid power is used which generally takes power from conventional energy sources. When more number of EVs are connected to the grid, it will unavoidably bring a huge impact to its function and control Moreover, charging the EVs using the electric grid powered by conventional energy sources gives no benefits. Thus an PV connected inverter can be used as a viable option in the charging stations [3]. EVs stores power in terms of DC which can be charged from multiple ports available in the charging stations and for this multiple number of choppers and inverters are present in the charging stations. These choppers will helps in controlling the DC output voltage given to the battery and inverter will supply the DC voltage to chopper through the PV connected to the input of the inverter [4]. Here power generated by the PV will be either supplied to the charging stations or if there is an excess of the power it will be given to the grid for other applications.

Inverter-based systems are becoming increasingly popular as a way to generate and integrate renewable energy sources into the grid. These systems typically consist of a source which can be dc source as well as pv array, an inverter, a controller and a load. Control is also a critical aspect of inverter systems. It allows the inverter to regulate the output voltage and current to ensure that the loads are powered with a robust, reliant, better quality waveform. This is important in PV systems, where the input voltage from the PV array can vary depending on the solar irradiation available. [5]

Inverters are power electronic system that convert direct current (DC) power to alternating current (AC) power. AC power is used in homes and businesses in different components such as heater, fans etc.

These are the types of inverters:

1. **Single-phase inverters:** Single-phase inverters are used to convert DC power to single-phase AC power. Single-phase AC is used in homes and commercial applications. Single-phase is used in low power applications and cost effective. Single-phase inverters are essential components of photovoltaic (PV) systems, uninterruptible power supplies (UPS), variable frequency drives (VFDs) etc.

2. **Three-phase inverters:** Three-phase inverters convert DC power to three-phase AC power. Three-phase inverters are much more beneficial for high power applications generally used for industrial applications. Three-phase inverters are used in a wide variety of applications, including motor control centers (MCCs), PV power plants, variable frequency drives (VFDs) etc. [6]

3. **Multi-Level Inverters:** Multi-Level inverters are more complex compared to two-level inverters. These inverters have many levels such as $\pm V_{DC}$, $\pm\frac{V_{DC}}{2}$, $\pm\frac{V_{DC}}{4}$ etc. making them having many advantages as low harmonic distortion, better quality output waveform, reducing voltage stress on power devices. [7]

1.1 Organisation of Thesis

This thesis presents a standalone single-phase nine-level active neutral point clamped inverter topology under linear and non-linear loads.

The thesis contains the DSP based implementation of single-phase five-level ANPCI with hardware prototype in chapter 3 and DSP based implementation of single-phase nine-level ANPCI with linear and non-linear loads explained in chapter 4.

Chapter 2

Literature Review, Motivation, and Problem Formulation

2.1 Literature Review

Traditional two-level inverters are simplest and most widely used inverters switching between two levels $+V_{dc}$ and $-V_{dc}$ [8]. The problem arises when the requirement is for high power applications. Two-level inverters cannot be implemented for higher power applications due to their limitation on switches which can only handle upto certain voltages. A multilevel inverter (MLI) synthesizes a desired AC voltage waveform from several DC voltage sources unlike traditional two-level inverter shown in Fig. 2.1 which only produces a voltage waveform that switches between two levels: positive and negative DC voltage. MLIs also exhibit some interesting advantages compared to

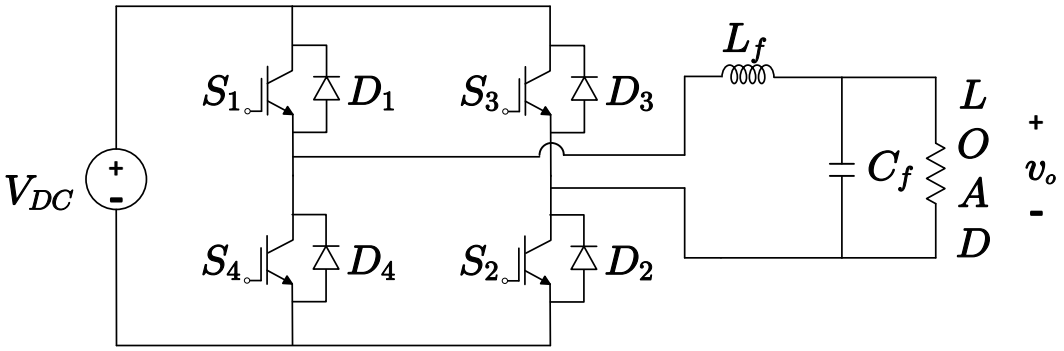

Figure 2.1: Two level inverter

two-level VSIs, e.g., better output waveforms with low harmonic distortion, reduced stress across the power electronic devices, and fault-tolerant [9]. MLIs produce a more

sinusoidal waveform than two-level inverters, which reduces harmonic distortion in the output voltage and MLIs divide the DC voltage into multiple levels, which reduces the voltage stress on the individual switching devices. Many MLIs have been most recognised due to their different advantages. Neutral point clamped MLI (NPCMLI), Diode-clamped MLI (DCMLI), Flying capacitor MLI (FCMLI), and Cascaded H-bridge MLI (CHBMLI) are the widely recognised topologies [10].

The new neutral point clamped multilevel-inverters (MLIs) are first proposed in 1981 for high power applications shown in Fig 2.2. NPC MLIs work by dividing the DC voltage input into multiple levels thus producing a more sinusoidal waveform than other types of multilevel inverters. NPC MLIs has lower harmonic distortion compared to other MLIs because of the simpler switching scheme of NPC MLIs [11].

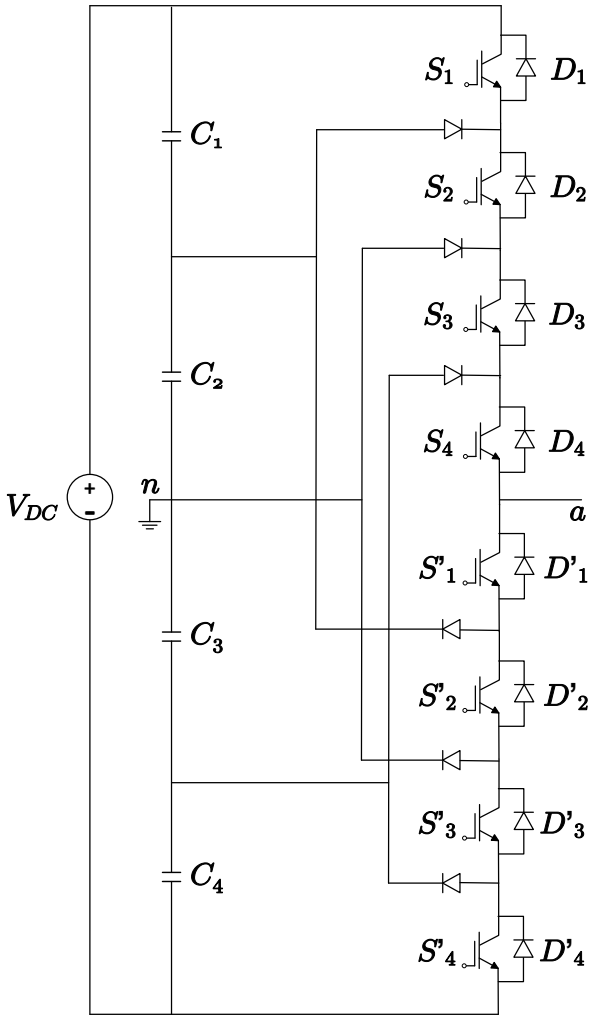

Figure 2.2: Three level NPC inverter

Flying Capacitor (FC) MLIs operates by connecting and disconnecting the flying capaictor to the output which helps in to produce high-quality waveform and uses flying capacitor to store energy which reduces the need for switching losses [12]. Flying Capacitor (FC) require a higher number of capacitors to achieve multi-level voltage, and as the number of levels increases, the number of capacitors also increases as shown in Fig. 2.3. While having these advantages, FCMLI suffers from disadvantages also which is the presence of unbalanced capacitor voltages and increased voltage stress on switches.

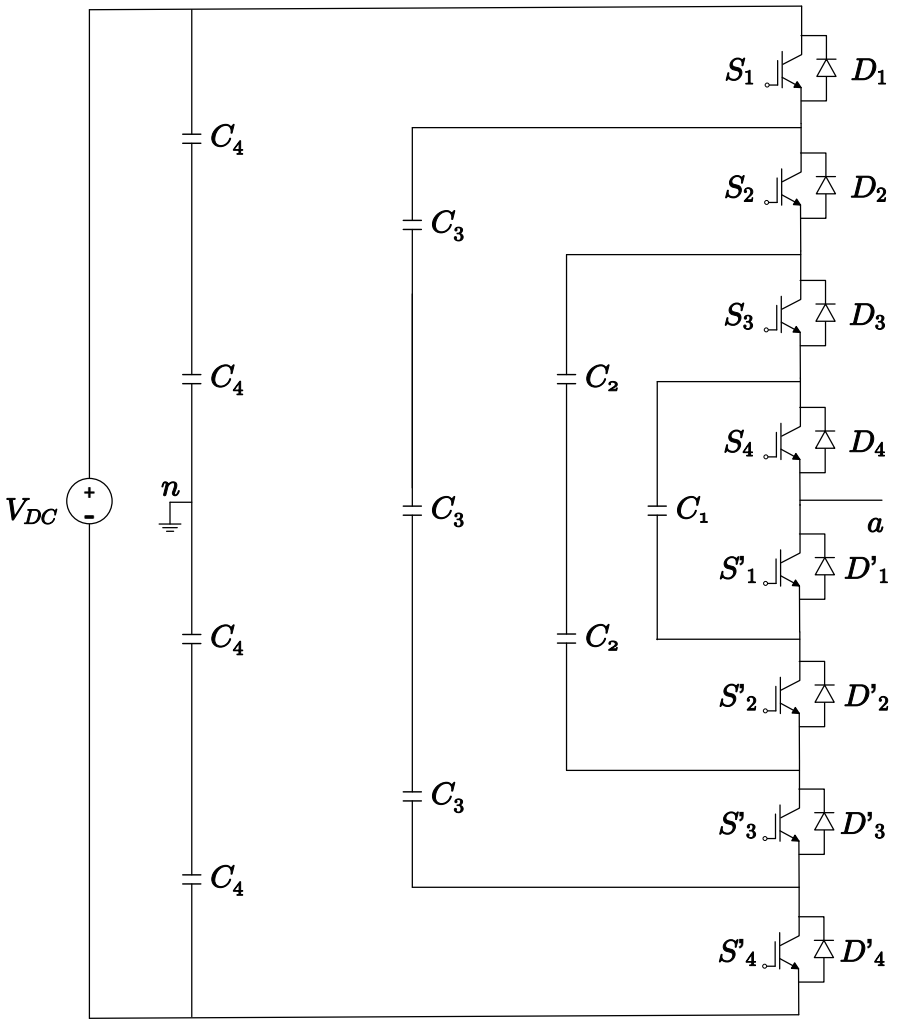

Figure 2.3: Flying Capacitor MLI

Neutral point clamped (NPC) MLIs uses clamping diodes to clamp the neutral potential. This allows the inverter to generate a high-quality output waveform with low

harmonic distortion. Some of the disadvantages are the uneven distribution of switching losses among these devices and higher voltage stress on semiconductor switches.

The Active Neutral point clamped MLIs is introduced due to some disadvantages of NPC MLIs. The unequal loss distribution among the power electronic devices is one major disadvantage of the NPC MLIs. This unequal loss distribution yields an unequal junction temperature distribution among the semiconductors. Thus, the losses in the most stressed device limit the switching frequency and the maximum phase current of the entire converter [13]. A further ANPCI model is proposed with eight switches which reduces losses [14].

The Active Neutral point clamped (ANPCI) has been analysed and compared over three level diode neutral-point-clamped inverter (DNPCI) and found out to be the better in performance and having lower switching losses [15].

A method suggested for FC voltage balancing for Active neutral-point clamped inverter with five levels. It overcomes the problems associated with flying capacitor MLIs and maintains the unbalanced flying capacitor (FC) voltages at the required level. In order to balance the flying capacitors (FC) and dc-link capacitors in the inverter, a modified switching scheme is required [16].

2.2 Motivation and Problem Formulation

Due to numerous advantages over Neutral point clamped and Flying Capacitor MLIs and growing popularity, ANPCI presents itself as a viable and effective alternative. Active Neutral Point Clamped MLI uses half the voltage rating for their power components when compared to NPC and FC MLI, resulting in lower conduction losses. Also, ANPC MLI have lower voltage stress on the power electronic switches, resulting in smaller switching losses. The redundancy in the switching states in the ANPC MLI enables the regulation of the voltage across its DC-link capacitors and Flying Capacitor (FC) to their respective nominal levels. Additionally, the voltage stress and losses are distributed equally among the switches, which is another reason why ANPCI is increasingly popular in industrial applications.

Single-phase nine-level ANPCI is introduced in order to increase output voltage levels. It offers enhanced (THD) reduction and utilizes a higher input voltage compared to the five-level inverter, which only employed half of the input voltage. A DSP based implementation for the single-phase nine-level Active Neutral Point Clamped (ANPC) inverter is being proposed. Moreover, single-phase nine-level ANPCI has been tested with non-linear loads.

Chapter 3

A DSP Based Implementation of Single-Phase Five-Level Active Neutral Point-Clamped Inverter (ANPCI)

Single-phase Active Neutral Point Clamped Inverter (ANPCI) is a type of multilevel inverter which is used in single-phase applications to convert the direct current (DC) to alternating current (AC). Considering the growing in popularity and renewable energy systems, photovoltaic (PV) systems are considered to be one of the best sources for the ANPCI.

Active Neutral Point Clamped Inverter (ANPCI) is a circuit which utilizes power electronic devices such as IGBTs, MOSFETs etc. for its operation. It has various advantages over two-level inverter making it popular these days including, better output waveform quality, lower harmonic distortion and higher efficiency.

Some major features and characteristics of single phase ANPCI are given as:

- **Multilevel Output Voltage:** ANPCI utilizes multiple voltage levels which enables it to produce a multilevel output voltage. This approach reduces harmonic distortion and produces better output waveform.
- **Neutral Point Clamping:** ANPCI clamps the neutral point to generate a higher voltage output with less voltage stress on the power electronics. This clamping mechanism aids in decreasing voltage stress on power electronic switches, enhancing their reliability and lowering losses.

- **Improved Reliability:** ANPC inverters offer more flexibility in controlling the output waveform than other multilevel inverters. This is because ANPC inverters have more control over the neutral point potential. This is useful for applications where it is necessary to generate a custom output waveform or to compensate for disturbances in the input voltage.
- **Higher Efficiency:** ANPC inverters are typically more efficient than other multilevel inverters, such as diode-clamped multilevel inverters (DCMIs) and cascaded H-bridge multilevel inverters (CHBMIs). This is because ANPC inverters use active switching devices to clamp the neutral point potential, which reduces conduction losses.

ANPC inverters are a versatile and powerful type of inverter with a wide range of applications. They are a good choice for applications where high efficiency, low harmonic distortion, improved flexibility, wider operating range, and increased reliability are important. [17]

3.1 Circuit Diagram and Operation

Fig. 3.1 shows that the circuit diagram of single-phase single-leg ANPCI which consists of eight switches with anti parallel diodes, two DC-link capacitors C_1 and C_2 and one flying capacitor FC_1.

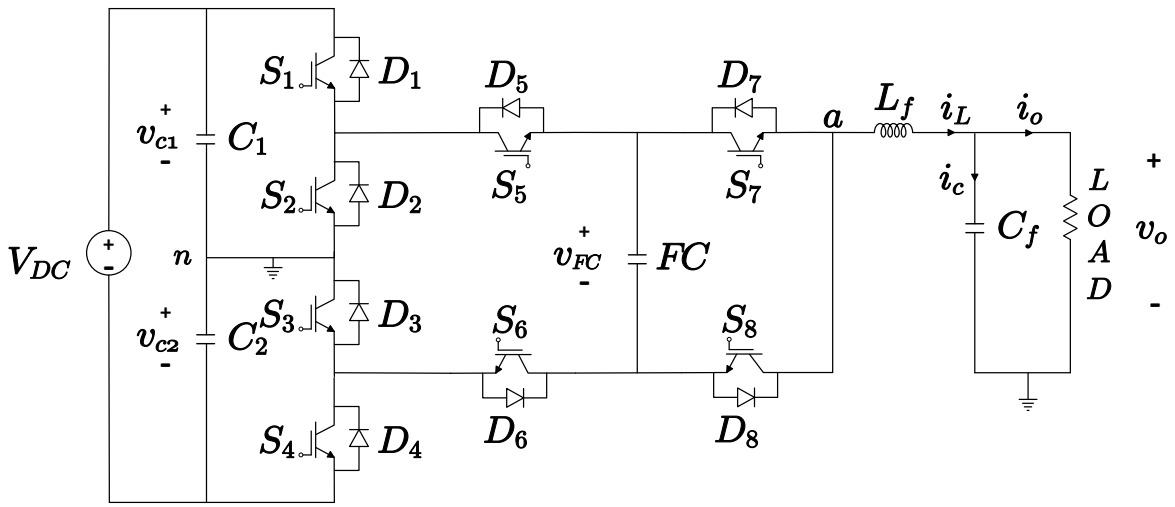

Figure 3.1: Circuit Diagram of Single-phase five-level ANPCI

The single-leg ANPCI generates five-level of voltages: $+\frac{V_{DC}}{2}$, $+\frac{V_{DC}}{4}$, 0, $-\frac{V_{DC}}{4}$, $-\frac{V_{DC}}{2}$. The voltage V_{an} can be any one of the above voltages. LC filter is implemented to filter out unwanted frequencies to produce a sinusoidal waveform at the output. The voltage across the DC-link capacitors is kept at 50% of V_{DC} and the average voltage across flying capacitor is kept 25% of V_{DC}. Table 3.1 shows eight possible ANPCI switching

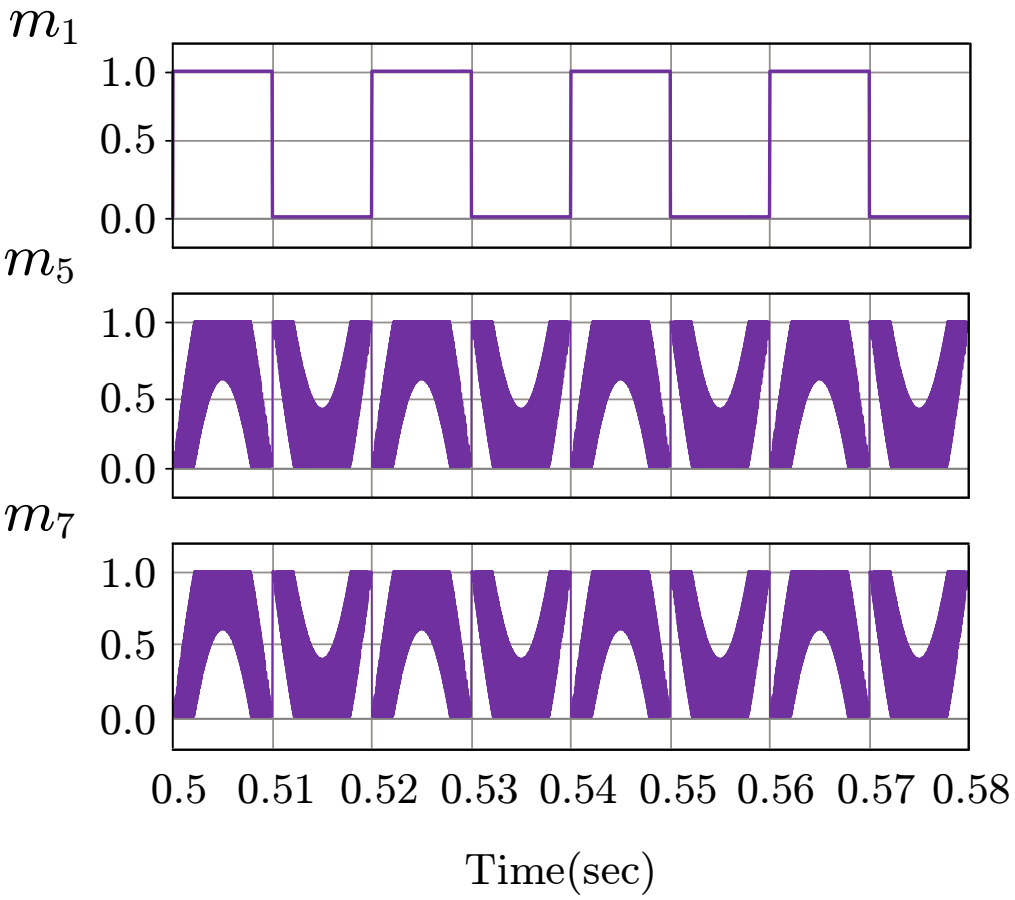

Figure 3.2: Modulating signals for generating switching signals

states and their voltage levels. Single-leg ANPCI has only three independent switching signals S_1, S_1, S_7 despite having eight switches. The rest of the switching signals can be obtained from these independent switching signals, for ex. S_2=S_4=S_1', S_3=S_1, S_6=S_5' and S_8=S_7'. The arrows signifies the charging and discharging of capacitor depending upon the inductor current i_L whether it is increasing or decreasing. [18]

3.2 Switching Technique

Phase Disposition (PD), Phase Opposition Disposition, and Alternative Phase Opposition Disposition are well-known pulse width modulation (PWM) techniques used for generating switching signals in Neutral-Point-Clamped (NPC) Multilevel Inverters (MLI). These techniques can also be adapted for generating switching signals in Active Neutral point clamped inverter (ANPCI). In this work and an adaptation of PDS-PWM technique is used for DSP-based implementation due to its ability to produce the lowest Total Harmonic Distortion (THD) in the output voltage for single-phase ANPCIs. Generation of switching signals has been explained in the Table 3.1. The modulating

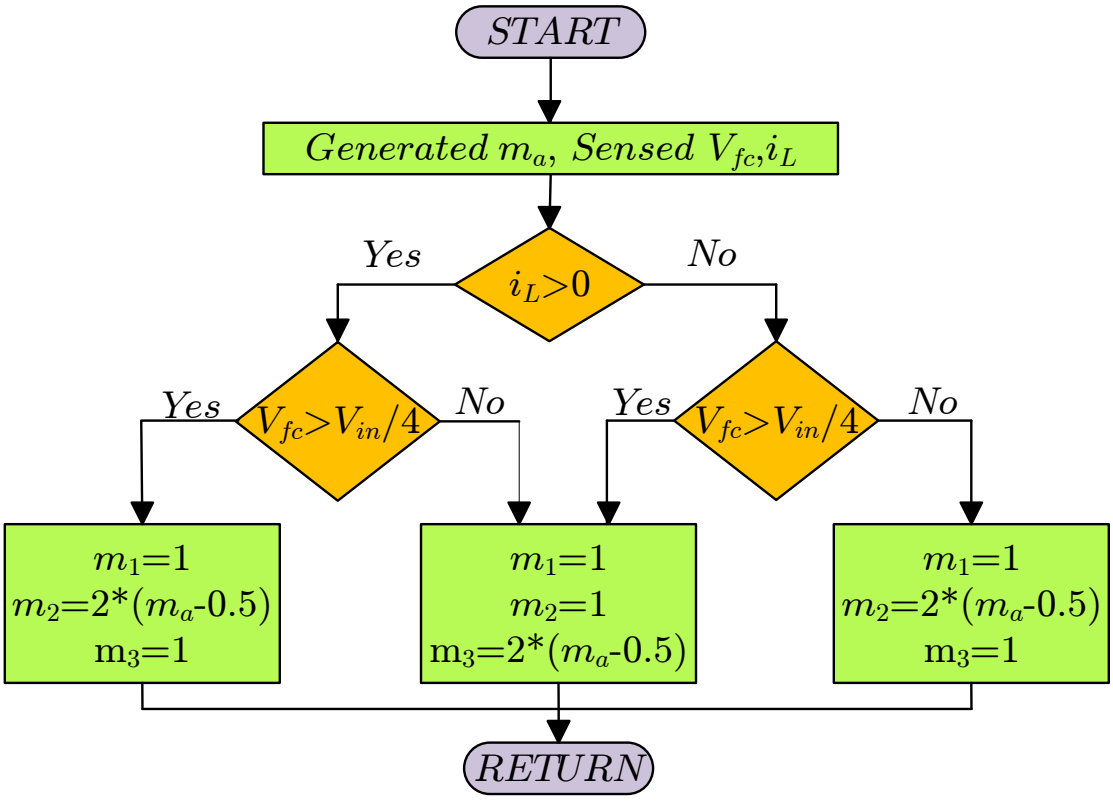

Figure 3.3: Flow chart explaining generation of switching signals

signals generated from the algorithm shown in Fig. 3.2. These signals are essential for generating the switching signals of the single-leg ANPCI.

3.3 Capacitor Voltage Balancing

The capacitor voltage balancing algorithm is implemented to ensure the balancing of the flying capacitors (FC) voltage and the neutral-point potential (NPP) in the grid connected Active Neutral Point Clamped inverter (ANPCI) with the LC filter. The purpose of this balancing is to maintain equal voltages across the DC-link capacitors, C_1 and C_2, and achieve the desired multilevel voltage output.

Table 3.1: Switching States of five-level ANPCI

Sr.No	v_{an}	Switching States			$i_L > 0$			$i_L < 0$		
		S_1	S_5	S_7	v_{c1}	v_{c2}	v_{fc}	v_{c1}	v_{c2}	v_{fc}
I	$\frac{+V_{dc}}{2}$	1	1	1	↓	↑	-	↓	↓	-
II	$\frac{+V_{dc}}{4}$	1	1	0	↓	↑	↑	↑	↓	↓
		1	0	1	-	-	↓	-	-	↑
III	0	1	0	0	-	-	-	-	-	-
		0	1	1	-	-	-	-	-	-
IV	$\frac{-V_{dc}}{4}$	0	1	0	-	-	↑	-	-	↓
		0	0	1	↓	↑	↓	↑	↓	↑
V	$\frac{-V_{dc}}{2}$	0	0	0	↓	↑	-	↑	↓	-

To obtain desired multilevel output voltage, voltage across DC-link capacitors need to be kept at $+\frac{V_{DC}}{2}$ and the voltage across flying capacitor is to be maintained at $+\frac{V_{DC}}{4}$. The charging and discharging status of the DC-link capacitors C_1 and C_2, and the flying capacitor (FC) for all switching states are provided in Table including redundant states.

FC charging/discharging control is explained in the following cases: From Table 3.1 , when the voltage level is $+\frac{V_{DC}}{4}$ and $i_L > 0$; if $V_{FC} > \frac{V_{DC}}{4}$, then ($S_1$, S_5, S_7) = (1 0 1), otherwise (S_1, S_5, S_7) = (1 1 0). When the voltage level is $+\frac{V_{DC}}{4}$ and $i_L < 0$; if $V_{FC} > \frac{V_{DC}}{4}$, then ($S_1$, S_5, S_7) = (1 1 0), otherwise (S_1, S_5, S_7) = (1 0 1). when the voltage level is -$\frac{V_{DC}}{4}$ and $i_L > 0$; if $V_{FC} > \frac{V_{DC}}{4}$, then ($S_1$, S_5, S_7) = (0 0 1), otherwise (S_1, S_5, S_7) = (0 1 0). When the voltage level is -$\frac{V_{DC}}{4}$ and $i_L < 0$; if $V_{FC} > \frac{V_{DC}}{4}$, then ($S_1$, S_5, S_7) = (0 1 0), otherwise (S_1, S_5, S_7) = (0 0 1). Similarly for other voltage levels, same procedure will be followed.

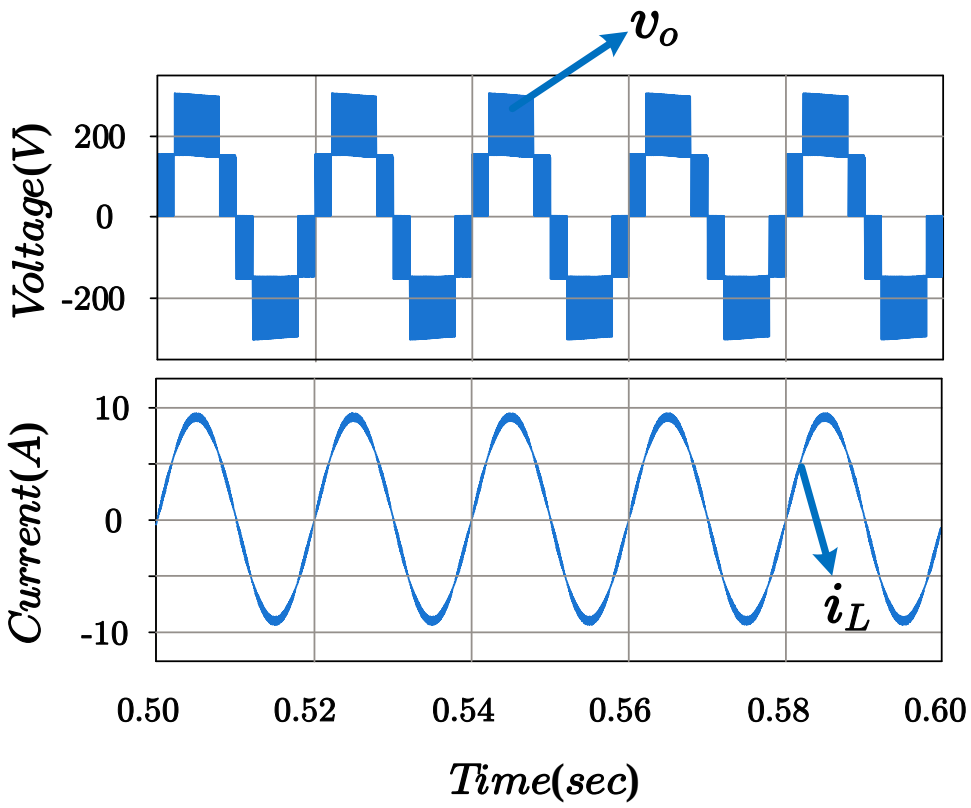

Figure 3.4: Five-level inverter voltage (v_o) and inductor current (i_L)

3.4 Design of LC filter

An LC filter is a passive network that utilizes an inductor (L) and a capacitor (C) to eliminate undesired frequencies from an output waveform. Inductors and capacitors exhibit opposing reactance properties, meaning they hinder the flow of alternating current (AC) in distinct ways. By strategically combining an inductor and a capacitor in a circuit, a specific range of frequencies can be either blocked or allowed to pass.

The selection of cutoff frequency is the key in the design of LC filter [19]. In order to make the waveform of the output voltage close to the sine wave and to avoid resonance problem, the resonant frequency of the LC filter must be chosen less than the carrier frequency of PWM control strategy, and should also be far greater than its fundamental frequency. Generally, the cutoff frequency obeys the eq. 3.1,

$$10f_1 < f_c < \frac{f_s}{10} \tag{3.1}$$

where f_1 is the fundamental frequency, f_c is the cutoff frequency of LC filter and f_s is the carrier frequency of the PWM control strategy.

The parameters for the LC filter are inductor and capacitor which follows the eq 3.2,

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.2}$$

The fundamental frequency for AC systems are generally considered to be 50 Hz and here the carrier frequency is taken as 10 kHz. To follow eq. 3.1 , the cutoff frequency is chosen as 1000 Hz.

According to the calculation, the value of inductor found out to be 2 mH and the value of capacitor is 12.66 μ F.

3.5 Closed-loop SRF-dq Control of ANPCI

The block diagram of the closed-loop controller shown in Fig.3.5 uses a second-order generalized integrator to generate a set of orthogonal signals $\begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^T$ and $\begin{bmatrix} v_\alpha & v_\beta \end{bmatrix}^T$ from the sensed inductor current i_L and output voltage v_o. These $\alpha\beta$ domain signals are then converted to dq-domain using the park transformation given by

$$T_{\alpha\beta\rightarrow dq} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix} \tag{3.3}$$

The SRF-dq controller block takes the dq-domain quantities $\begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^T$ and $\begin{bmatrix} v_\alpha & v_\beta \end{bmatrix}^T$ and the reference voltage $\begin{bmatrix} V_d^* & V_q^* \end{bmatrix}^T$ as inputs. The synchronous reference frame (SRF)-dq controller has a cascaded control structure with an inner current controller and an outer voltage controller. Both d-axis and q-axis currents and voltages are regulated using PI controllers. To design these PI controllers, the ANPCI circuit diagram can be modeled as

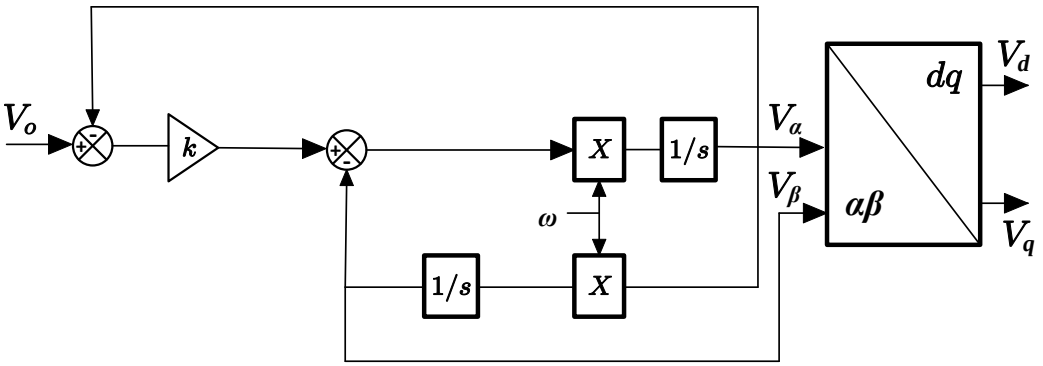

Figure 3.5: Single-phase $\alpha\beta$ to dq conversion

$$\frac{dv_o}{dt} = \left(\frac{i_L}{C_f}\right) - \left(\frac{v_o}{R_L C_f}\right) \tag{3.4}$$

$$\frac{di_L}{dt} = \frac{(v_{an} - v_o - i_L r_L)}{L_f} \tag{3.5}$$

where R_L is the load resistance and r_L is the equivalent series resistance of L_f which is then transformed to dq-domain using the transformation given in [20]. The mathematical model of ANPCI in dq-domain is given by

$$\frac{d}{dt}\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_L C_f} & \omega \\ -\omega & -\frac{1}{R_L C_f} \end{bmatrix} . \begin{bmatrix} v_d \\ v_q \end{bmatrix} + \frac{1}{C_f}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{3.6}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L_f} & \omega \\ -\omega & -\frac{r_L}{L_f} \end{bmatrix} . \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} v_{and} - v_d \\ v_{anq} - v_q \end{bmatrix} \tag{3.7}$$

The time domain model is transformed into frequency domain, which is given by the transfer functions

$$\frac{v_d(s)}{i_d(s) + \omega C_f v_q(s)} = \frac{R_L}{1 + sR_L C_f} \tag{3.8}$$

$$\frac{v_q(s)}{i_q(s) - \omega C_f v_d(s)} = \frac{R_L}{1 + sR_L C_f} \tag{3.9}$$

$$\frac{i_d(s)}{v_{and}(s) - v_d + \omega L_f i_q(s)} = \frac{1}{sL_f + r_L} \tag{3.10}$$

$$\frac{i_q(s)}{v_{anq}(s) - v_q - \omega L_f i_d(s)} = \frac{1}{sL_f + r_L} \tag{3.11}$$

These transfer functions are used to determine the PI controller parameters. The outer voltage controller generates the dq-domain reference currents, $\begin{bmatrix} I_d^* & I_q^* \end{bmatrix}^T$ which are given as inputs to the inner current controller. The current controller block generates the modulation signal $\begin{bmatrix} m_d & m_q \end{bmatrix}^T$ in SRF, which will then be transformed back into stationary reference frame and used to generate gate signals for ANPCI.

Fig. 3.6 illustrates the process of generating an orthogonal system (OSG), which produces two output signals, namely V_α and V_β, with a phase difference of 90 degrees. The V_α component possesses the same phase and magnitude as the fundamental frequency of the input signal V_g. These signals are subsequently fed into the Park transformation module, denoted as $\alpha\beta\rightarrow$dq, in order to derive V_d and V_q.

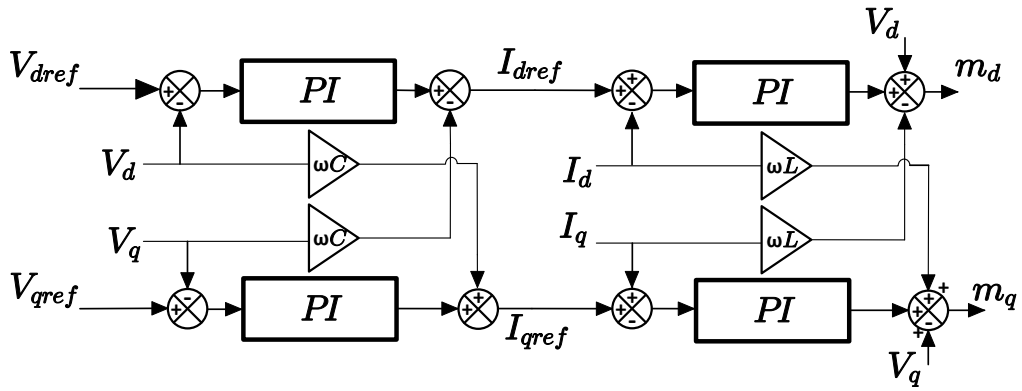

Figure 3.6: SRF-dq control loops

If it being assumed that the input signal is a pure sinusoid represented as $V_g = V_m \sin\theta_g$, and the Second-Order Generalized Integrator (SOGI) generates a pair of signals with the same amplitude as the input signal but with a 90°phase difference, eq. 3.1 can be restated as follows:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3.12}$$

The control structure of a single-phase grid-connected system is illustrated in Fig.

3.6. This requires the utilization of Park transformation (dq $\rightarrow \alpha\beta$) or inverse Park transformation ($\alpha\beta \rightarrow$ dq), which are essential components of the control process.

To regulate the output voltage of a grid-connected ANPCI (Active Neutral Point Clamped Inverter), an SRF (Synchronous Reference Frame) dq control approach is employed. The SRF-dq controller adopts a cascaded control structure consisting of an inner current controller and an outer voltage controller.

In cases where the resonance frequency of the filter is higher than the grid frequency, the grid current is primarily determined by the summation of the filter inductors. As a result, the inverter output current becomes equivalent to the grid output current. In the SRF-dq controller, PI (Proportional-Integral) controllers are employed to regulate the currents and voltages in both the d-axis and q-axis.

The measured signals are i_L and V_o. These signals first transformed into stationary $\alpha\beta$ reference frame signals as shown in Fig. 3.6 and further transformed into dq reference frame signals. The controller generates modulation signals (m_d and m_q) which serve as the input to the switching scheme block giving the gate signals for the respective switches in the ANPCI.

3.6 Simulation Results

The simulations performed to evaluate the performance and efficiency of the LC filter and capacitor voltage balancing technique in refining the output quality and stability of the ANPCI system. All simulations for this study were conducted using PSCAD software.

Table 3.2: Simulation parameters for 5L-ANPCI

Parameters	Values
DC Voltage (V_{DC})	600 V
Load voltage (rms)	230V
Output Power	2 kW
Filter inductance (L_f)	5mH
Fundamental Frequency	50 Hz
Switching Frqeuency	10 kHz
DC-link Capacitors (C_1 and C_2)	2.2 mF
Flying Capacitor (FC_1)	100 μ F

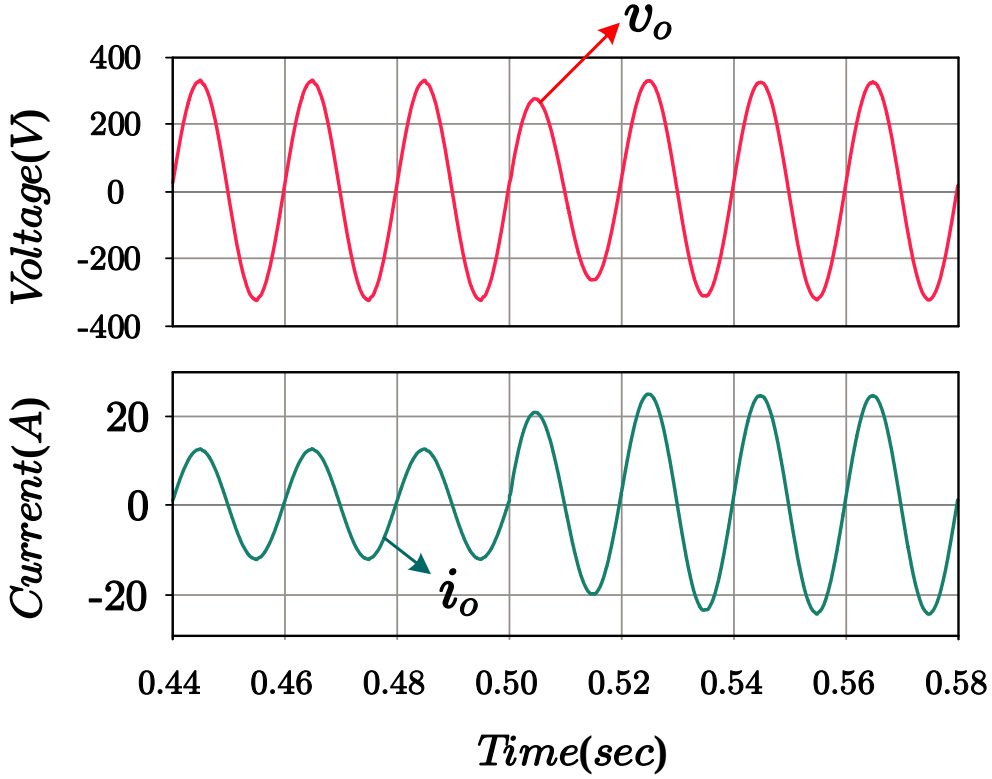

Figure 3.7: Simulation results showing Load voltage (v_o) and current (v_o)

Table 3.2 shows parameters and their respective values. To evaluate the stability of the controller specifically designed for the given model, a load change was abruptly applied at 0.5 seconds.

The circuit's response to this disturbance was characterized by a settling time of 0.2

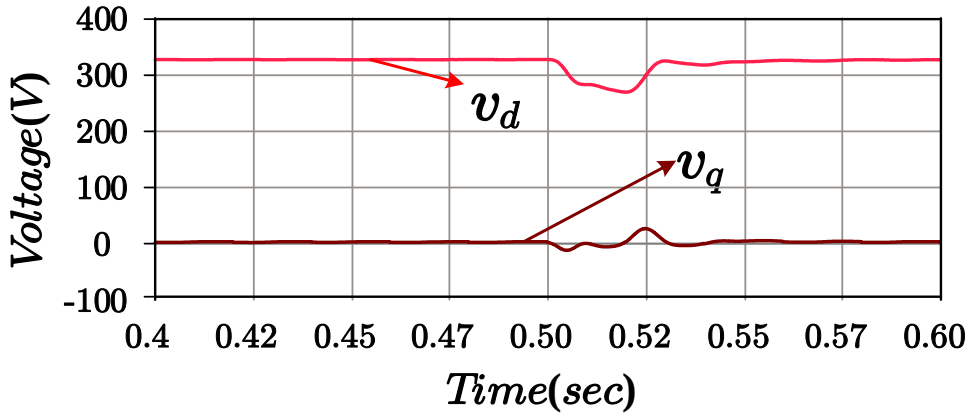

Figure 3.8: Simulation results showing dq components of Load voltage (v_d & v_q)

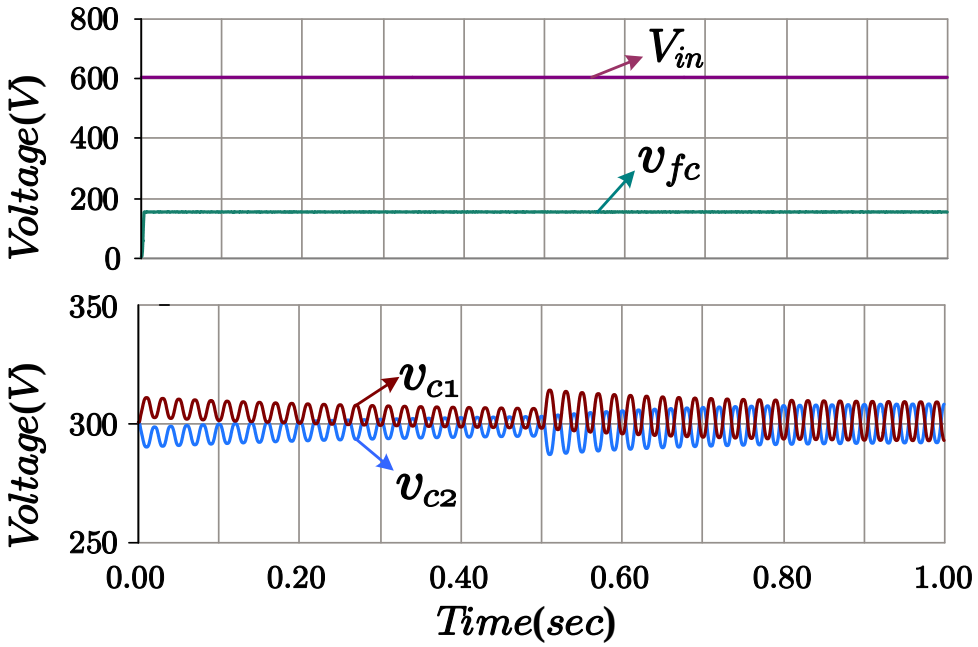

Figure 3.9: Voltage across flying capacitor (v_{fc}) and DC-link capacitors (v_{c1} & v_{c2})

seconds, indicating the controller's ability to effectively regulate the system's output despite the sudden change in load conditions. The corresponding wave-forms captured from the circuit's operation provide visual confirmation of the controller's effectiveness in maintaining system stability.

The performance of a standalone ANPCI employing SRF-dq control and an LC filter is demonstrated through the presentation of its output voltage and current wave-forms in the Fig. 3.7 for load variations at 0.5 sec. The corresponding dq voltage components are also presented in the Fig. 3.8 for a more comprehensive understanding of the system's behavior.

Fig. 3.9 a) shows the input voltage and voltage across flying capacitor which is $\frac{V_{in}}{4}$ and Fig. 3.9 b) show the voltage across the two DC-link capacitors which is half of the input supply voltage.

3.7 Hardware Results

A physical model of a single-phase single-leg Active Neutral Point Clamped Inverter (ANPCI) has been constructed and integrated to function as an independent inverter. This hardware prototype represents a tangible realization of the ANPCI design concept, enabling its performance to be evaluated in real-world conditions.

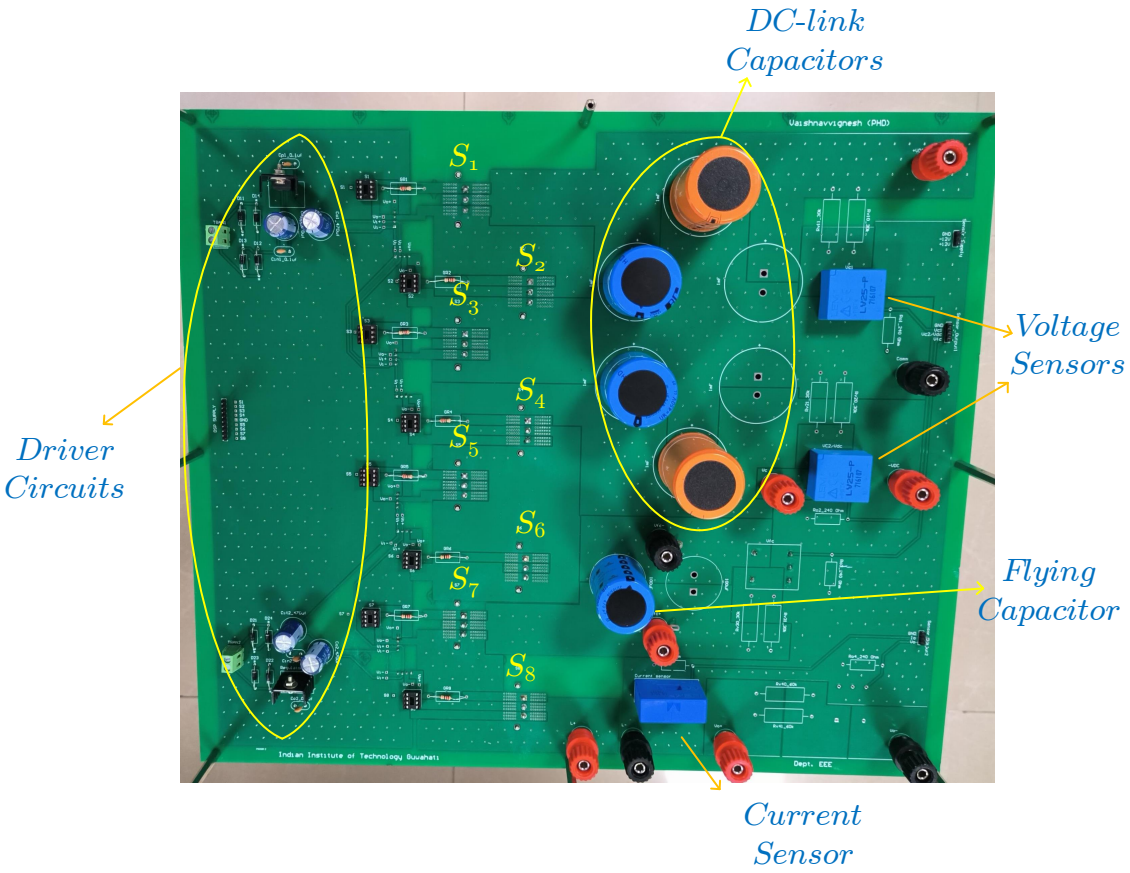

Figure 3.10: Hardware prototype for single-phase five-level ANPCI

The single-phase single-leg configuration simplifies the implementation while still capturing the essential operating principles of the ANPCI topology.

Table 3.3: Parameters for Hardware experiment

Parameters	Values
DC Voltage (V_{DC})	180 V
Load voltage (peak-to-peak)	81 V
Filter Inductance (L_f)	1.5mH
Fundamental Frequency	50 Hz
Switching Frqeuency	10 kHz
DC-link Capacitors (C_1 and C_2)	1 mF
Flying Capacitors (FC_1)	100 μ F

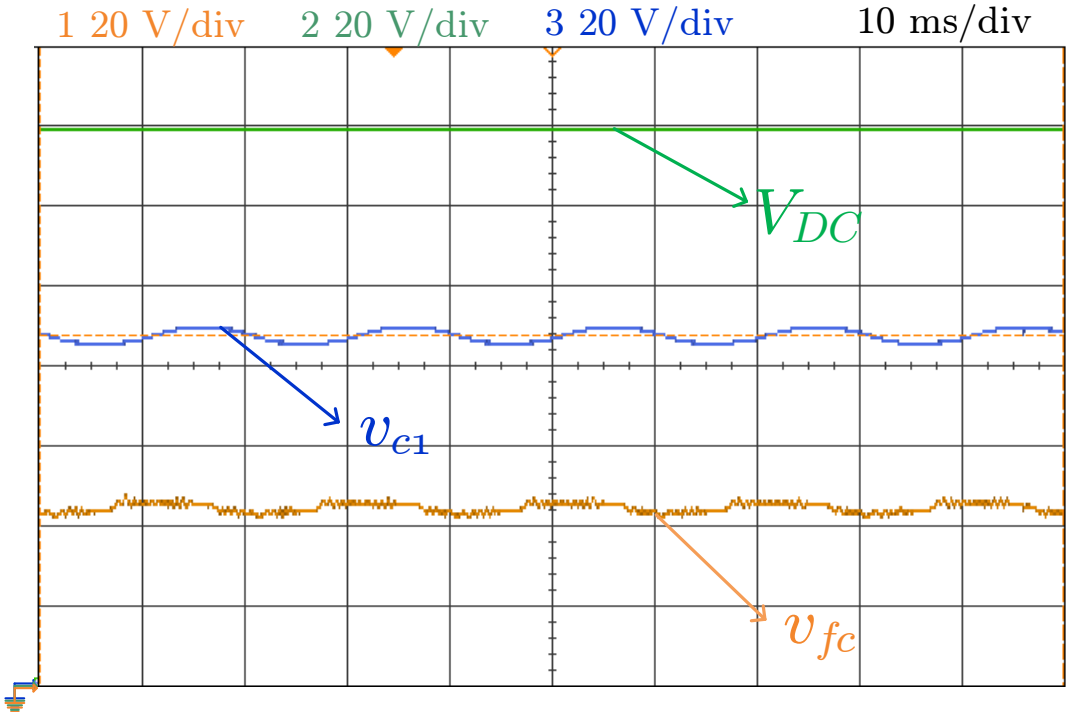

Figure 3.11: Hardware results showing DC-link capacitor voltage (V_{c1}), DC voltage (V_{DC}) and flying capacitor voltage (V_{fc})

The experimental set-up of five-level ANPCI is built with the parameters given in Table 3.3 to verify the capacitor voltage balancing algorithm mentioned in section 3.3. Fig. 3.10 shows the experimental setup of five-level ANPCI. Texas instruments TMS320F28335 digital signal controller is used to generate and implement the switching signals and the capacitor voltage balancing algorithm. The capacitor voltages are

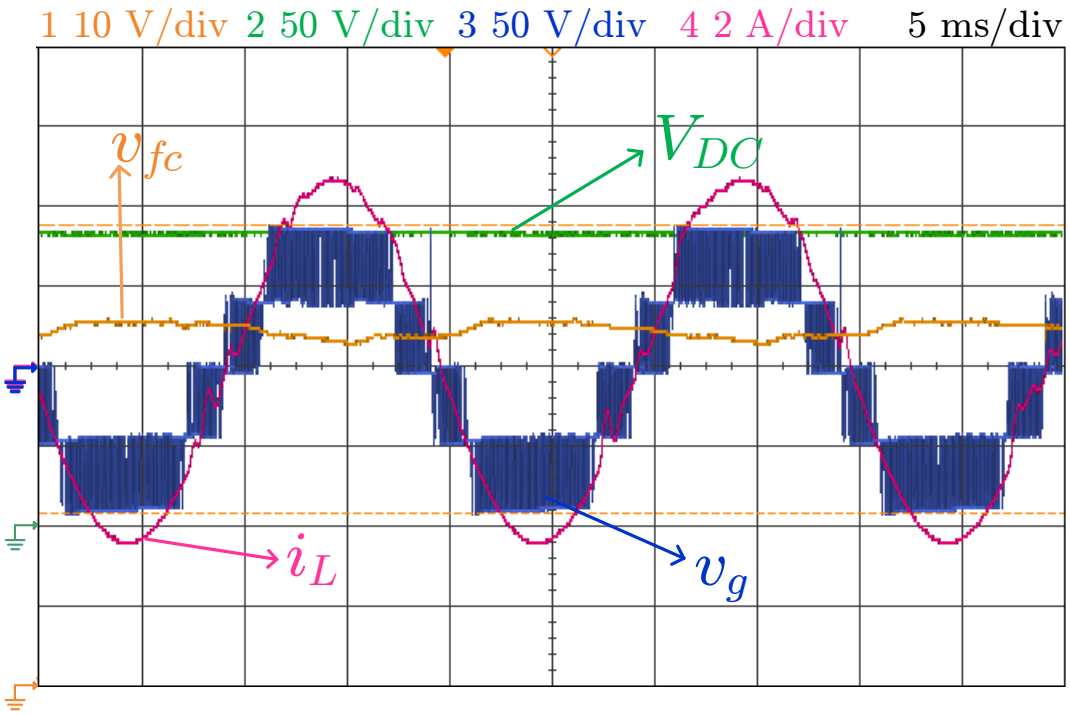

Figure 3.12: Steady state results showing DC voltage (V_{DC}), flying capacitor voltage (V_{fc}), five-level ANPCI output voltage (V_g) and inductor current (I_L)

measured using the LEM voltage sensor LV-25P and the inductor current is measured using the LEM current sensor LA-55P.

Fig. 3.11 shows the steady state waveforms of DC voltage V_{DC}, flying capacitor voltage V_{fc} and DC-link capacitor voltage V_{c1}. As seen from the figure the DC-link capacitor voltage V_{c1} are maintained at almost half of the DC voltage having value of 86.3 V with peak-to-peak ripple of 1.5 V according to the capacitor voltage balancing algorithm. Also the flying capacitor voltage are almost maintained at quarter of DC voltage = 44.55 V with peak-to-peak ripple of 0.8 V.

Fig. 3.12 shows the five distinct voltage levels generated by the ANPCI inverter achieved with a modulation index of 0.9 and a peak-to-peak value of 180 V. Also, inductor current I_L is being shown having peak value of 4.6 A .

Fig. 3.13 shows the output voltage of five-level ANPCI V_o having peak value of 162 V. and the flying capacitor voltage V_{fc} with the value of 44.7 V with peak-to-peak ripple of 0.8 V. THD calculated for the output voltage of five-level ANPCI is 6.3%.

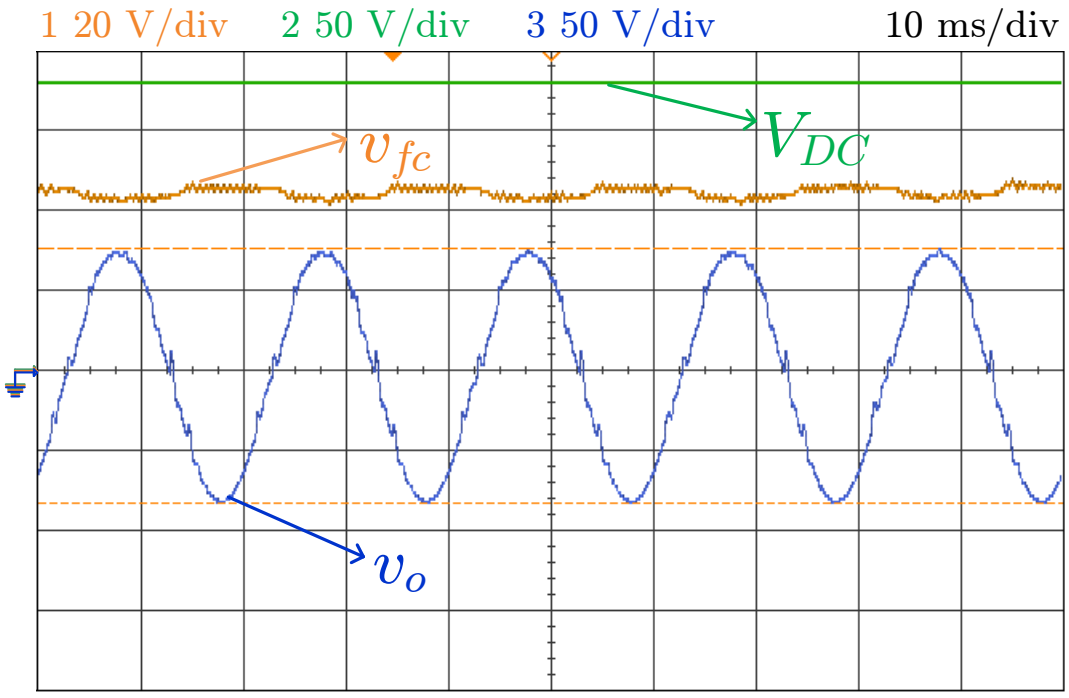

Figure 3.13: Experiment results showing five-level ANPCI load voltage (V_o), DC voltage (V_{DC}) and flying Capacitor voltage (V_{fc})

3.8 Conclusion

Experimental results serve as a crucial bridge between the simulations and the practical hardware. In this case, the DSP-based capacitor voltage balancing algorithm, designed and tested through simulation, has successfully implemented to the physical hardware prototype of the five-level ANPCI. The hardware results obtained serve as a compelling demonstration, verifying that the algorithm's effectiveness translates from the simulations to the actual operation of the hardware. Also the model developed is modular in nature and can be implemented as N-level ANPCI.

Chapter 4

A DSP based implementation of Single-Phase Nine-Level Active Neutral Point-Clamped Inverter (ANPCI)

A Single-phase two-leg Active neutral point clamped inverter is the upgraded version of single leg which utilizes its whole input voltage.

4.1 Circuit Diagram and Operation

Fig. 4.1 shows the circuit diagram of single-phase two-leg ANPCI which consists of two single-leg ANPCI connected together. It consists of sixteen switches with anti parallel diodes, two DC-link capacitors C_1 and C_2 and two flying capacitors FC_1 and FC_2.

Compared to single-leg ANPCI, two-leg ANPCI generated nine-level of voltages: $+V_{DC}$, $+\frac{3V_{DC}}{4}$, $+\frac{V_{DC}}{2}$, $+\frac{V_{DC}}{4}$, 0, $-\frac{V_{DC}}{4}$, $-\frac{V_{DC}}{2}$, $-\frac{3V_{DC}}{4}$ and $-V_{DC}$. Voltage across the flying capacitors is kept as 25% of V_{DC} and the average voltage across the DC-link capacitors is kept as 50% of V_{DC}.

Table 4.1 shows thirty-two possible ANPCI switching states and their voltage levels. Two-leg ANPCI has only six independent switching signals S_{a1}, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7} despite having sixteen switches. The rest of the switching signals can be obtained from these independent switching signals, for ex. S_{a2}=S_{a4}=$S_{a1'}$, S_{a6}=$S_{a5'}$, S_{a8}=$S_{a7'}$, similarly S_{b2}=S_{b4}=$S_{b1'}$, S_{b6}=$S_{b5'}$ and S_{b8}=$S_{b7'}$. There are redundant switching states

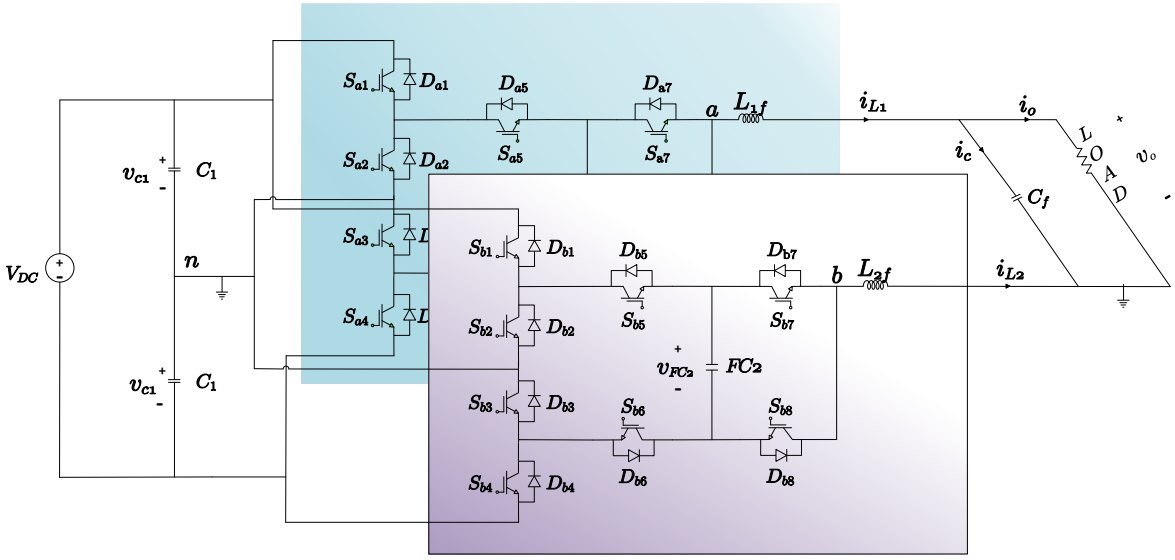

Figure 4.1: Circuit Diagram of Nine-level ANPCI

for the voltage levels $+\frac{3V_{DC}}{4}$, $+\frac{V_{DC}}{2}$, $+\frac{V_{DC}}{4}$, $-\frac{V_{DC}}{4}$, $-\frac{V_{DC}}{2}$ and $-\frac{3V_{DC}}{4}$ The arrows signifies the charging and discharging of capacitor depending upon the inductor current i_L.

4.2 Switching Scheme and capacitor voltage balancing

The switching scheme for two-leg ANPCI is an enhanced version of the single-leg ANPCI scheme. For the first leg, the switching signals are identical to those used in the single-leg configuration. However, for the second leg, the switching signals are generated by inverting the modulating signal, taking into account that current will flow through one leg and enter through the second leg. To obtain desired multilevel output voltage, voltage across DC-link capacitors is kept as $\frac{V_{DC}}{2}$ and voltage across flying capacitors is to be maintained as $\frac{V_{DC}}{4}$.

From Table 4.1, when the voltage level is $+\frac{3V_{DC}}{4}$ and $i_L > 0$; if $V_{FC1} > \frac{V_{DC}}{4}$, then ($S_{a1}$, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 0 1 0 0 0), otherwise (S_{a1}, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 1 0 0 0 0) and if $V_{FC2} > \frac{V_{DC}}{4}$, then ($S_{a1}$, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 1 1 0 1 0), otherwise (S_{a1}, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 1 1 0 0 1). When the voltage level is $+\frac{3V_{DC}}{4}$ and $i_L < 0$; if $V_{FC1} > \frac{V_{DC}}{4}$, then ($S_{a1}$, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 1 0 0 0 0), otherwise (S_{a1}, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 0 1 0 0 0) and if $V_{FC2} > \frac{V_{DC}}{4}$, then

(S_{a1}, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 1 1 1 0 1), otherwise (S_{a1}, S_{a5}, S_{a7}, S_{b1}, S_{b5} and S_{b7}) = (1 1 1 0 1 0).

For $m_a > 0.75$, the switching signal generation is being discussed in the Table 4.1.

Table 4.1: Switching States of nine-level ANPCI

v_{an}	Switching States						$i_o > 0$				$i_o < 0$			
	S_{a1}	S_{a5}	S_{a7}	S_{b1}	S_{b5}	S_{b7}	v_{c1}	v_{c2}	v_{fc1}	v_{fc2}	v_{c1}	v_{c2}	v_{fc1}	v_{fc2}
$+V_{dc}$	1	1	1	0	0	0	↓	↓			↑	↑		
$\frac{+3V_{dc}}{4}$	1	1	1	0	1	0	↓			↓	↑			↑
	1	0	1	0	0	0		↓	↓			↑	↑	
	1	1	0	0	0	0	↓	↓	↑		↑	↑	↓	
	1	1	1	0	0	1	↓	↓		↑	↑	↑		↓
$\frac{+V_{dc}}{2}$	1	1	1	1	0	0	↓				↑			
	0	1	1	0	0	1		↓				↑		
	1	0	1	0	1	0			↓	↓			↑	↑
$\frac{+V_{dc}}{4}$	1	1	0	0	1	1	↓		↑		↑		↓	
	0	1	0	0	0	0		↓	↑		↑	↓		
	1	1	1	1	0	1	↓			↑	↑			↓
	0	1	1	0	0	1		↓		↑		↑		↓
	1	0	1	1	0	0			↓				↑	
	0	1	1	0	1	0				↓				↑
0	0	1	1	1	0	1	-	-	-	-				
	1	0	0	0	1	1					-	-	-	-
	1	0	1	1	0	1			↓	↑			↑	↓
	0	1	0	1	1	0			↑	↓			↓	↑
$\frac{-V_{dc}}{4}$	0	1	1	1	1	0	↑			↓	↓			↑
	0	0	0	0	1	0		↑		↓		↓		↑
	1	0	1	1	1	1	↑		↓		↓		↑	
	0	0	1	0	1	1		↑	↓			↓	↑	
	1	0	0	1	0	1				↑				↓
	0	1	0	0	1	1			↑				↓	
$\frac{-V_{dc}}{2}$	1	0	0	1	1	1	↑				↓			
	0	0	0	0	1	1		↑				↓		
	0	1	0	1	0	1			↑	↑			↓	↓
$\frac{-3V_{dc}}{4}$	0	1	0	1	1	1	↑		↑		↓		↓	
	0	0	0	1	0	1		↑		↑		↓		↓
	0	0	0	1	1	0	↑	↑		↓	↓	↓		↑
	0	0	1	1	1	1	↑	↑	↓		↓	↓	↑	
$-V_{dc}$	0	0	0	1	1	1	↑	↑			↓	↓		

4.3 Simulation Results

The simulation results showed that SRF-dq control was effective in regulating the output voltage and current of the ANPCI. The settling time, overshoot, and steady-state error of the output voltage were all within acceptable limits. The LC filter effectively suppressed harmonic distortion in the output voltage. The total harmonic distortion (THD) found out to be 5%, which is considered as a good level of performance. The nine level ANPCI is shown in the Fig. 4.2 taking 550 V as the supply voltage. The inductor current is also shown in same Fig. 4.2.

Table 4.2: Simulation parameters for 9L-ANPCI

Parameters	Values
DC Voltage (V_{DC})	550 V
Load voltage (rms)	290V
Filter Inducatance (L_f)	2mH
Fundamental Frequency	50 Hz
Switching Frqeuency	10 kHz
DC-link Capacitors (C_1 and C_2)	1 mF
Flying Capacitors (FC_1 and FC_2)	100 μ F

To assess the controller's ability to maintain system stability under transient conditions, a load change was abruptly introduced at 0.5 seconds. The resulting disturbances in the output voltage and current were effectively mitigated, and the system regained its steady-state operating point within a finite time frame as shown in Fig. 4.3.

This demonstrates the controller's robustness and effectiveness in regulating the system's behavior despite sudden changes in load demand. The capacitor balancing algorithm shown in the section 4.2 is matched with the simulated results shown in Fig. 4.4 where V_{c1} and V_{c1} has the value of $\frac{V_{dc}}{2}$. And the flying capacitors has the value of $\frac{V_{dc}}{4}$ shown in same Fig. 4.4.

The inner current control loop, responsible for regulating the instantaneous current flowing through the load, derives its reference value from the outer voltage loop con-

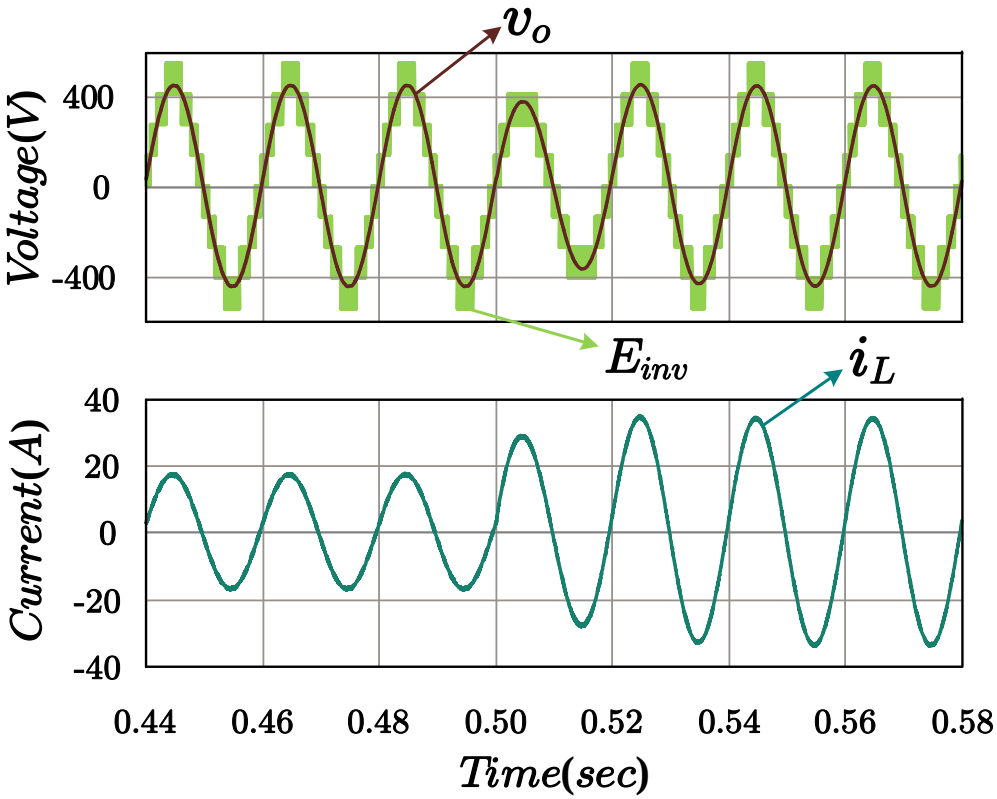

Figure 4.2: Simulation results of 9-L ANPCI output voltage (E_{inv}) and inductor current (i_L)

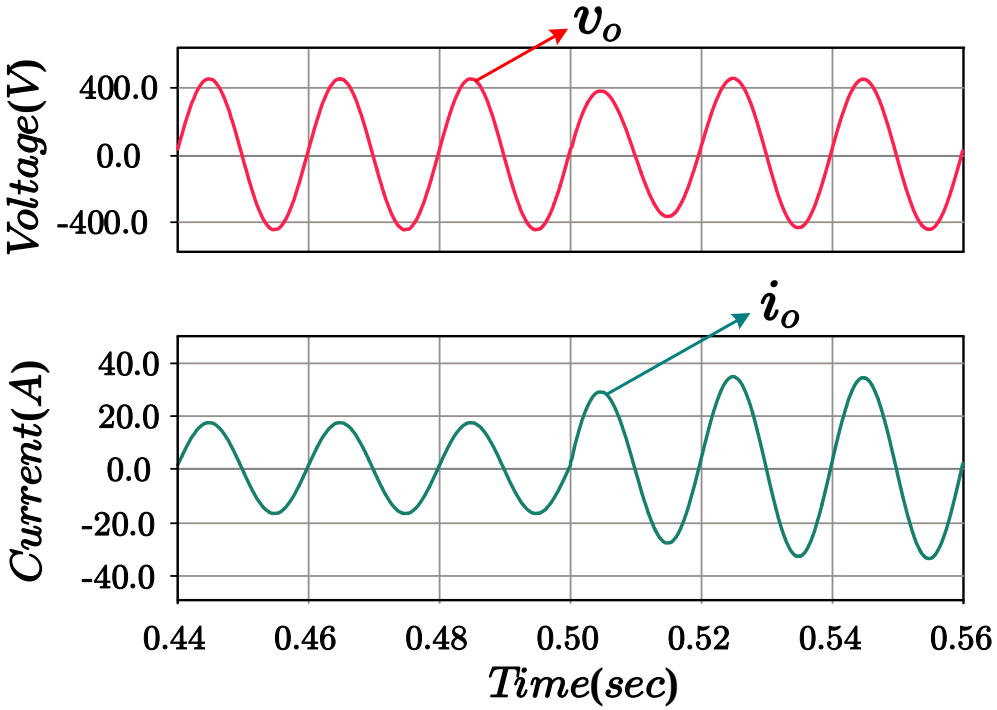

Figure 4.3: Simulation results shows load voltage (v_o) and current (i_o)

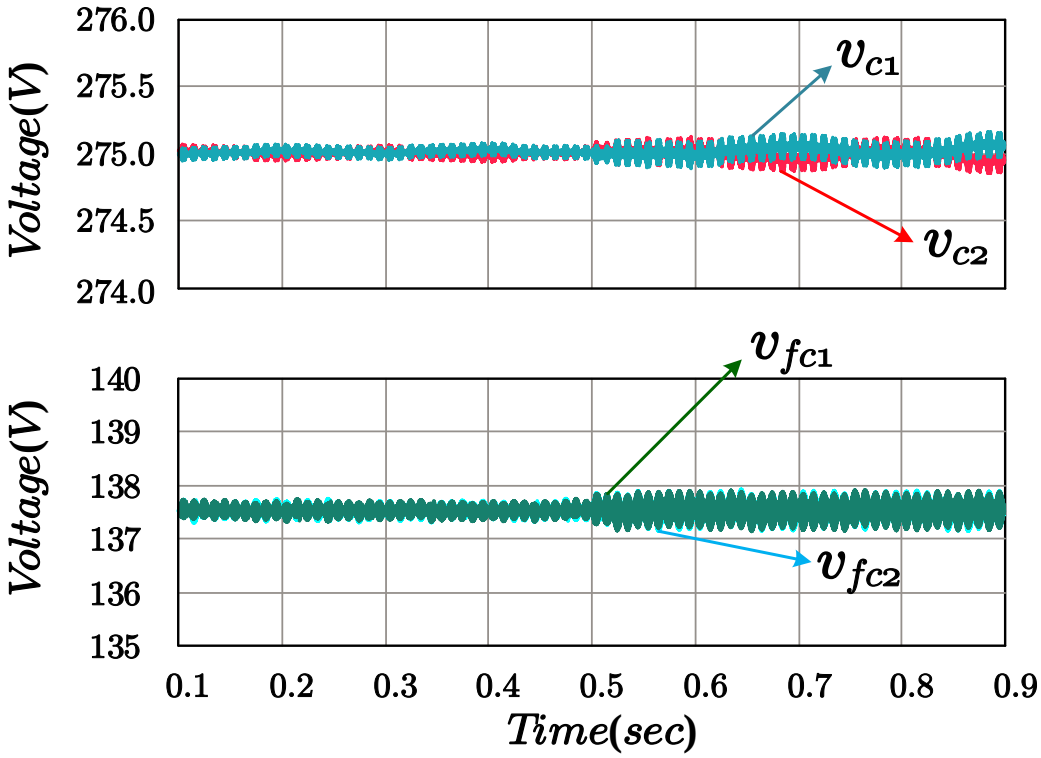

Figure 4.4: Voltage across DC-link (v_{c1} & v_{c2}) and flying capacitors (v_{fc1} & v_{fc2})

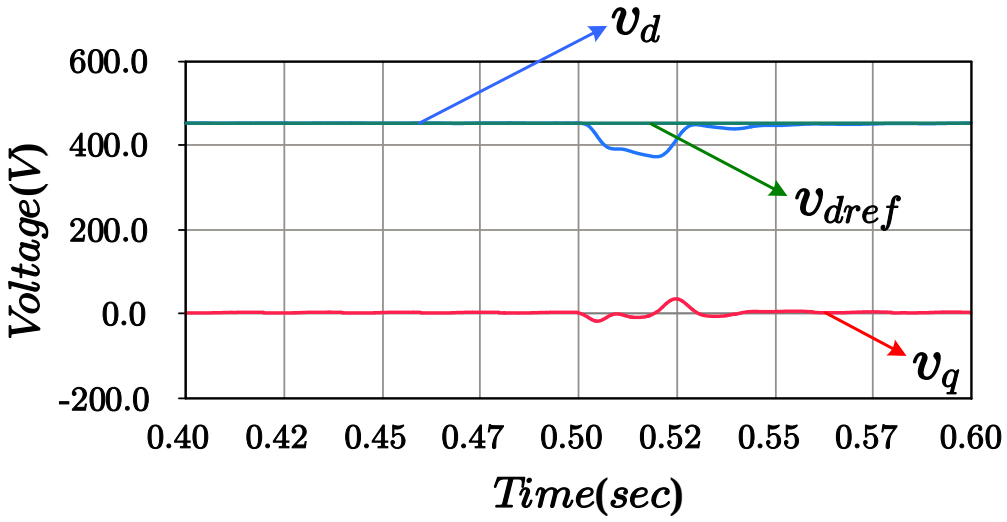

Figure 4.5: Simulation results shows dq components of load voltage (v_d & v_q)

troller. This outer loop controller, tasked with maintaining the desired output voltage, utilizes the dq parameters of the load voltage, which represent the active and reactive power components, in conjunction with its reference value.

This combined information provides the inner loop with the necessary guidance to effectively control the current and achieve the desired voltage regulation. After 0.05

sec, The load voltage rapidly regains its steady-state value, restoring system stability within a short time frame is being shown in the Fig. 4.5.

The THD value obtained for nine-level ANPCI which is around 0.66% for 26.4 Ω and when the load is changed to 13.2 Ω at 0.5 sec is reduced to around 0.33%.

4.4 Non linear load

A Single-phase two-leg Active neutral-point clamped inverter has been connected to a non-linear load which introduces many challenges due to the way it draws current. Some of those points has been discussed and been remedied accordingly.

4.4.1 Circuit Diagram

Fig. 4.6 shows the circuit diagram of single-phase ANPCI with a non-linear load. A non-linear load is a diode bridge rectifier load consists of four diodes and a resistor at the end.

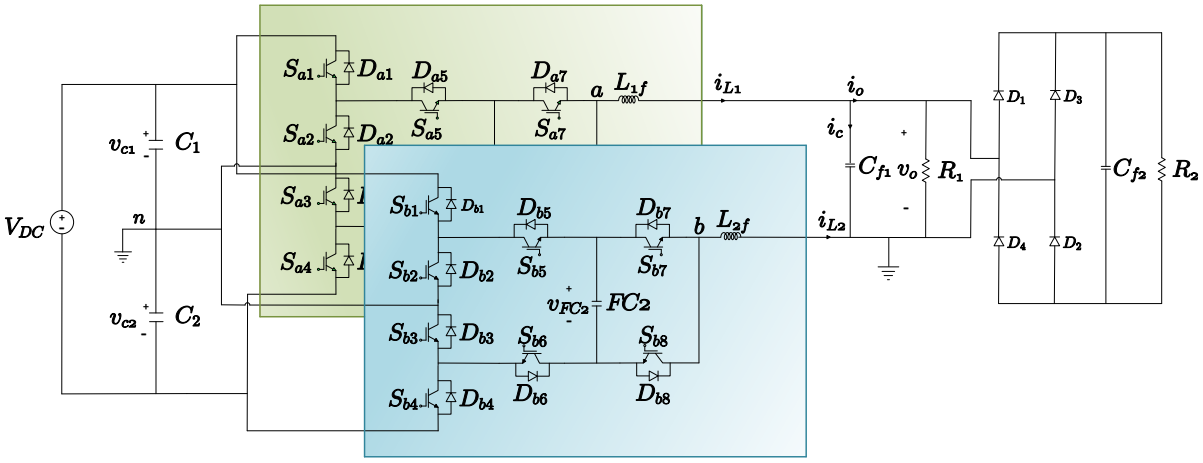

Figure 4.6: Single-phase two-leg ANPCI with Non-linear load

4.4.2 Operation of a non-linear load

A non-linear load is that type of load which doesn't draw current in a smooth, proportional way when connected to AC power source [21]. Unlike a linear load, which

draws current consistently as the voltage increases and decreases, a non-linear load draws current in pulses or bursts and the wave-forms tends to be more spiky in nature.

The main concern with introducing non-linear load to an inverter is that the wave-form exhibits sharp peaks and dips and primary reason for this is they generate additional higher order frequencies on top of fundamental frequency. Due to generation of higher order harmonics, the total harmonic distortion (THD) increases and overall efficiency reduces.

The non-linear load's pulsed current draw disrupts the inductor's attempt to maintain a smooth flow. This disruption, caused by the inductor's initial resistance and gradual current build-up, translates to voltage spikes and uneven current flow, manifesting as spikes in the inductor current waveform.

4.4.3 Simulation Results

The simulation results showed that SRF-dq control was effective in regulating the output voltage for non-linear load also. All simulations for this study were conducted using PSCAD software. Table 4.3 shows parameters and the values of the parameters which are being used in simulation.

Table 4.3: Simulation parameters for 9L-ANPCI with non-linear load

Parameters	Values
DC Voltage (V_{DC})	450 V
Load voltage (rms)	230V
Filter Inductance (L_f)	2mH
Fundamental Frequency	50 Hz
Switching Frqeuency	10 kHz
DC-link Capacitors (C_1 and C_2)	1 mF
Flying Capacitors (FC_1 and FC_2)	100 μ F

The circuit's response to this disturbance was characterized by a settling time of 0.2 seconds, indicating the controller's ability to effectively regulate the system's output despite the sudden change in load conditions. The corresponding wave-forms captured

from the circuit's operation provide visual confirmation of the controller's effectiveness in maintaining system stability.

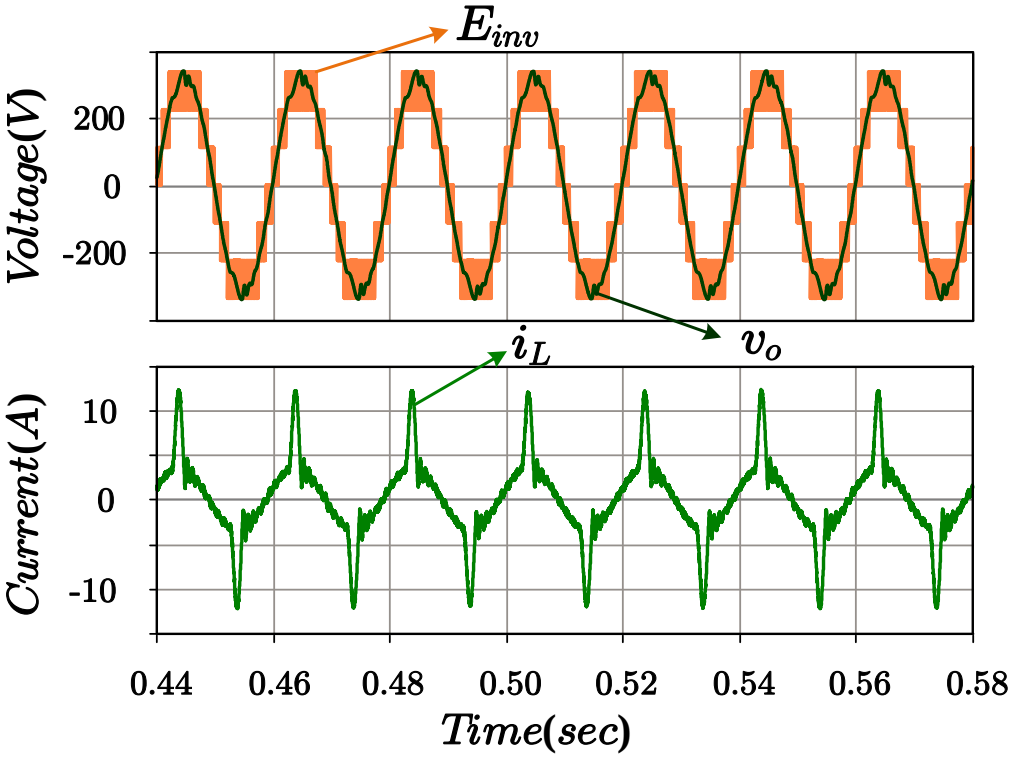

Figure 4.7: Simulation results of 9-L ANPCI output voltage (E_{inv}) and inductor current (i_L)

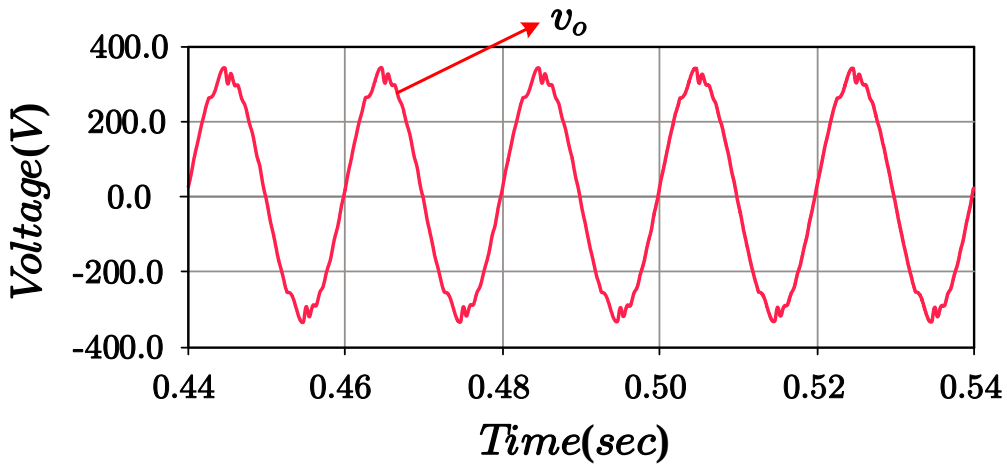

Figure 4.8: Simulation results shows nine-level ANCPI load voltage (v_o)

The nine-level inverter output voltage taking 450 V as the supply voltage shown in Fig. 4.7. In the same Fig 4.7 inductor current has also been shown. The spikes observed in the inductor current are due to effects of non-linear load.

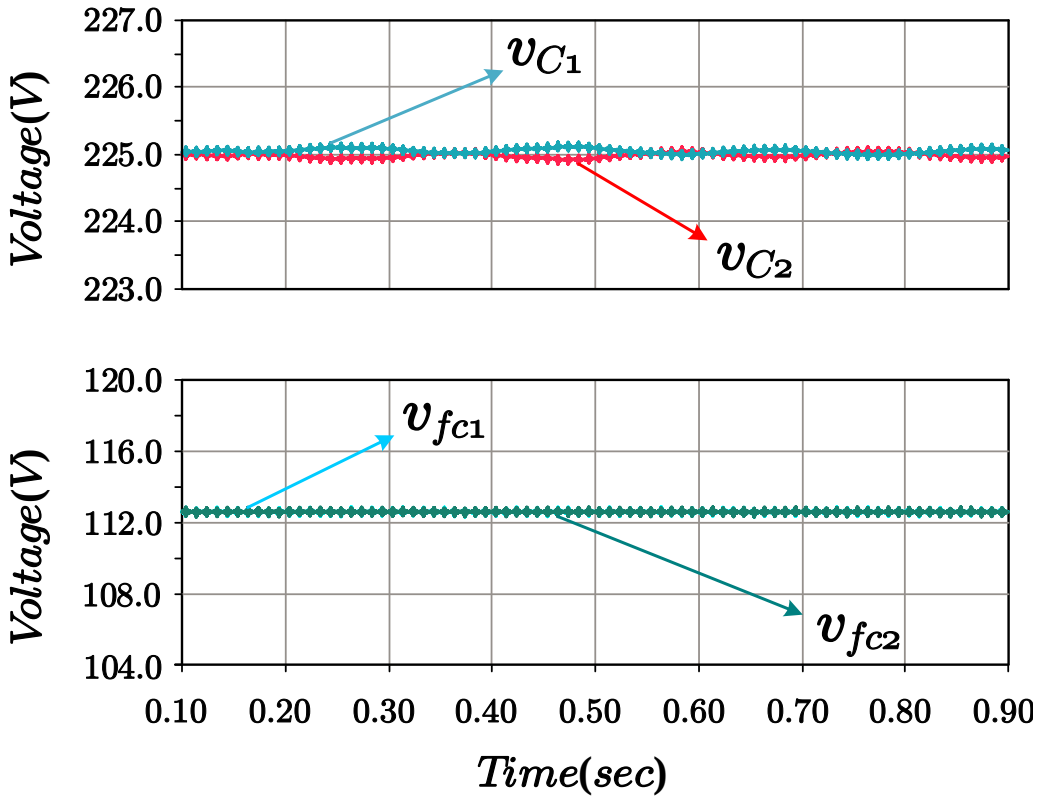

Figure 4.9: Voltage across DC-link (v_{c1} & v_{c2}) and flying capacitors (v_{fc1} & v_{fc2})

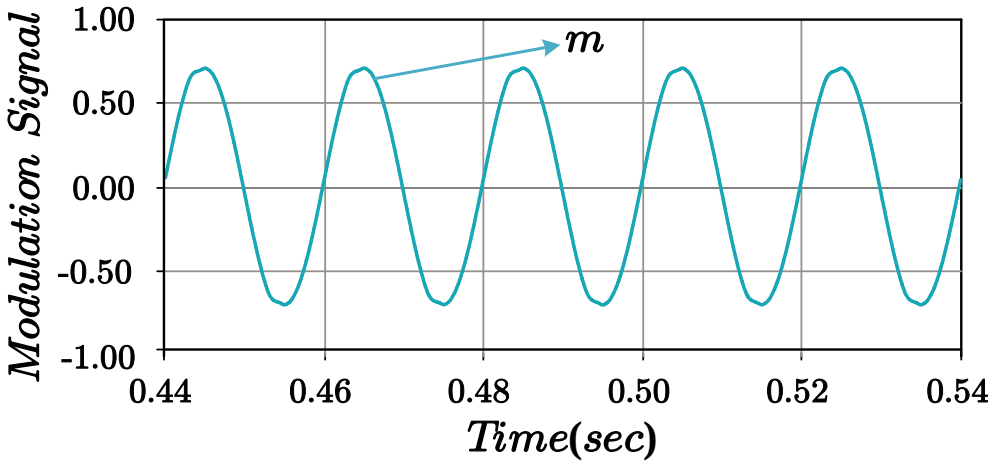

Figure 4.10: Simulation results showing modulating signal

The resulting disturbances in the output voltage and current were effectively mitigated, and the system regained its steady-state operating point within a finite time frame as shown in Fig. 4.8.

The capacitor voltage balance algorithm shown in section 4.2 is also being matched when nine-level ANPCI connected to a non-linear load with the simulation results and

being shown in Fig. 4.9. The values of V_{C1} and V_{C2} has the value of 225 V which is $\frac{V_{dc}}{2}$ and flying capacitors has the value of 112.5 V which is $\frac{V_{dc}}{4}$.

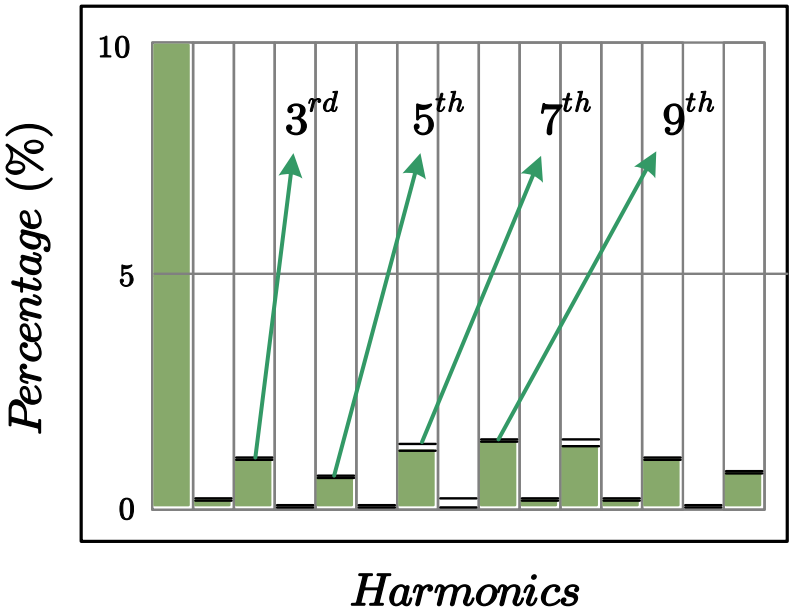

Figure 4.11: Simulation results shows harmonic contents of load voltage of 9-L ANCPI with non-linear load

Fig. 4.10 shows the modulating signal which is being obtained to generated switching pulses. Its value is 0.72 according to the chosen value of reference.

THD calculated for the nine-level ANCPI connected to a non-linear load (rectifier load) is approximately 2.9% and the harmonic components are shown in Fig. 4.11. The 3^{rd} harmonic content is 0.65 %, 5^{th} harmonic content is 0.3%, 7^{th} harmonic content is 0.94% and 9^{th} harmonic content is 1.13% respectively.

4.5 Conclusion

In conclusion, nine-level ANPCI paired with the SRF-dq control is able to maintain satisfactory results even with non-linear loads. This combination achieves highly satisfactory results, obtaining THD which is close to 3% well within the limits of IEEE 519 standards. Additionally, the capacitor balancing algorithm is able to maintain the flying capacitor voltages within the desired limits under non-linear load operation.

Chapter 5

Work Done and Future Scope

Work Done includes the following:

- The development of DSP based control scheme for five-level ANPCI.
- Successful implementation of developed controller in hardware prototype.
- Extension of developed controller for nine-level ANPCI.
- Simulation based testing of nine-level ANPCI with the developed controller under linear and non-linear loads.

Future scope includes the following:

- The proposed scheme, encompassing DSP implementation and grid connection, will be rigorously evaluated through comprehensive testing of the hardware prototype.
- The hardware prototype will incorporate MPPT to facilitate a thorough investigation of its performance under varying conditions.
- The proposed control scheme will be extended to accommodate non-linear loads while incorporating practical considerations to ensure real-world applicability.

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