**PCB Manufacturing Constraints**

- Size 54.1 x 75.2 mm, 6 Layer
- 0.15 mm Track Width
- 0.15 mm Copper Clearance
- 0.38 mm Edge Clearance
- 0.35 mm Toolsize / non plated Hole
- 0.20 | 0.35 mm Plated Hole | Annular Ring Dia
- 2.54 mm milling radius
- Solder Paste Pads are optimized for a 70 - 110 um Stencil

**Assembly (v2.4)**

- 2 Variations, recorder / emulator are self-contained and optional
- with Rec & Emu => 353 parts, 53 unique
- with Emu => X parts, X unique
- Mech-15 contains assembly notes / Pick and Place
- marking origin of part: cross (+) on assembly notes layer
- marking pad 1 of ICs: chamfered edge and circle (assembly notes) and filled triangle (silk)
- marking cathode of diodes: "C" or chamfered edge (assembly notes) and filled triangle (silk)
- Mech-2 contains Top Part Designators
- smallest part 0402
- smallest pitch 0.35 mm, XSON8
- only top layer populated

**Manual Assembly**

- Mech-13 contains info about non-reflow parts ( 8 items)

**BOM-Additions****P1**

BeagleBoneGreen

**P2**

P\_HDR\_2x11\_254mm\_LongPinSocket

**P3**

P\_HDR\_2x11\_254mm\_LongPinSocket

**P4**

P\_HDR\_2x12\_254mm\_Header

**P5**

P\_HDR\_2x12\_254mm\_Header

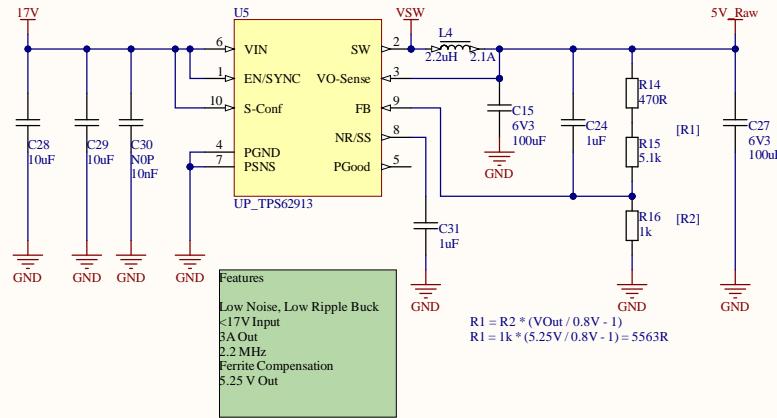
**BOM PMEG1001-Alternative**

SMMSD701T1G IR = 1.4 nA  
PMEG1001ELRX IR = 2.1 nA  
RB168MM-40TR IR = 8.0 nA

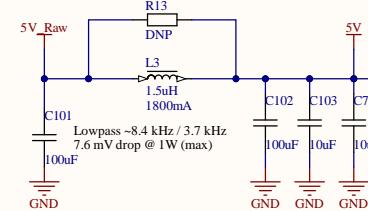
Title	Shepherd - Overview	
Size	Number	Revision
A4		
Date: 3/03/2025	Sheet of shepherd_v2.PriPcb	Drawn By: Ingmar
File: C:\Users\...\overview.SchDoc		

### LowNoise-BuckConverter

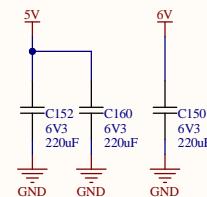
MAX 17V



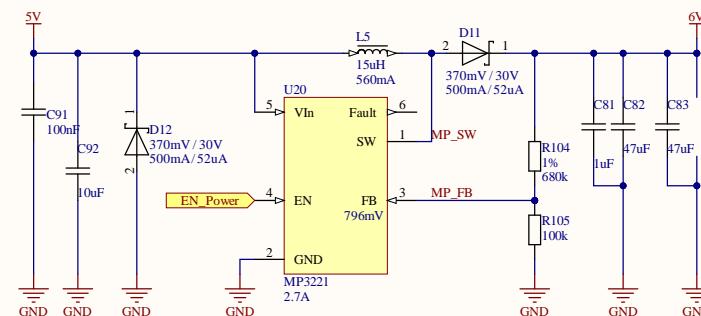
### LC-LowPass (Optional)



### Optional Caps / Backside

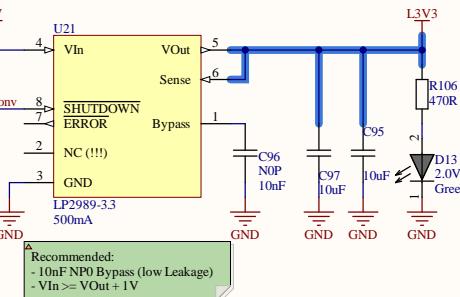
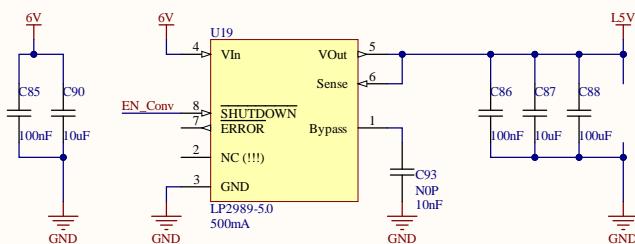
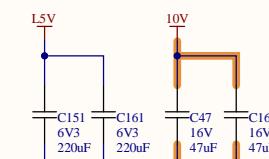
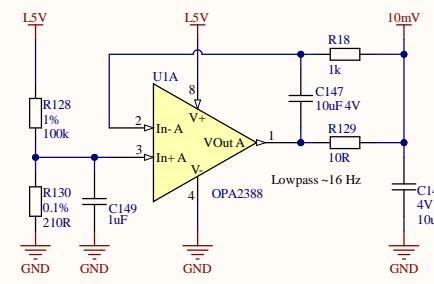
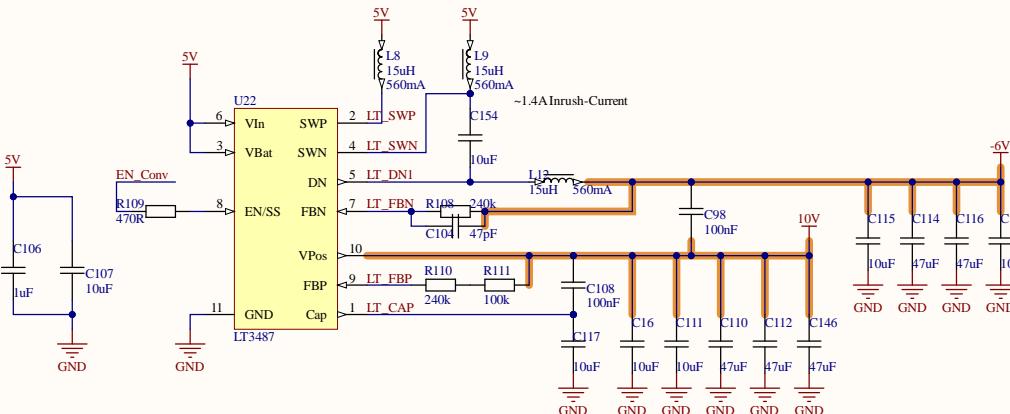


### BoostConverter



Title Shepherd - Input Voltage Converters  
NES Lab / TU Dresden

Size	Number	Revision
A4		
Date: 3/03/2025	Sheet of shepherd_v2.PriPcb	Drawn By: Ingmar
File: C:\Users\...\Power-input.SchDoc		

**LowNoise LDOs****Optional Caps / Backside****Reference-Offset****Boost & Inverter**

R1=(Vp-1.23V)/25uA  
R1=350.8 kOhm (10V)  
340kOhm > 9.73V @ 1%

R2=-Vn/25uA  
R2=240 kOhm (-6V)

Regulator drives at least 50mA on both Outputs

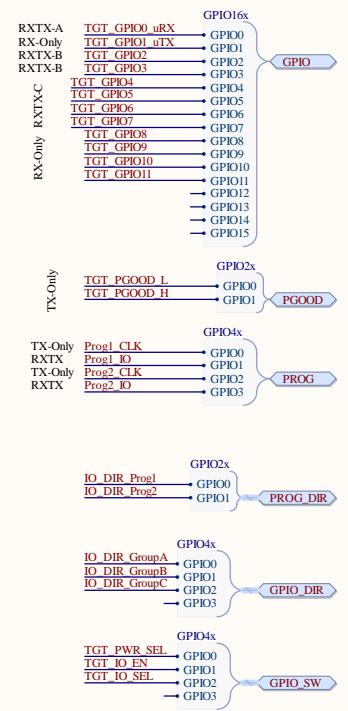
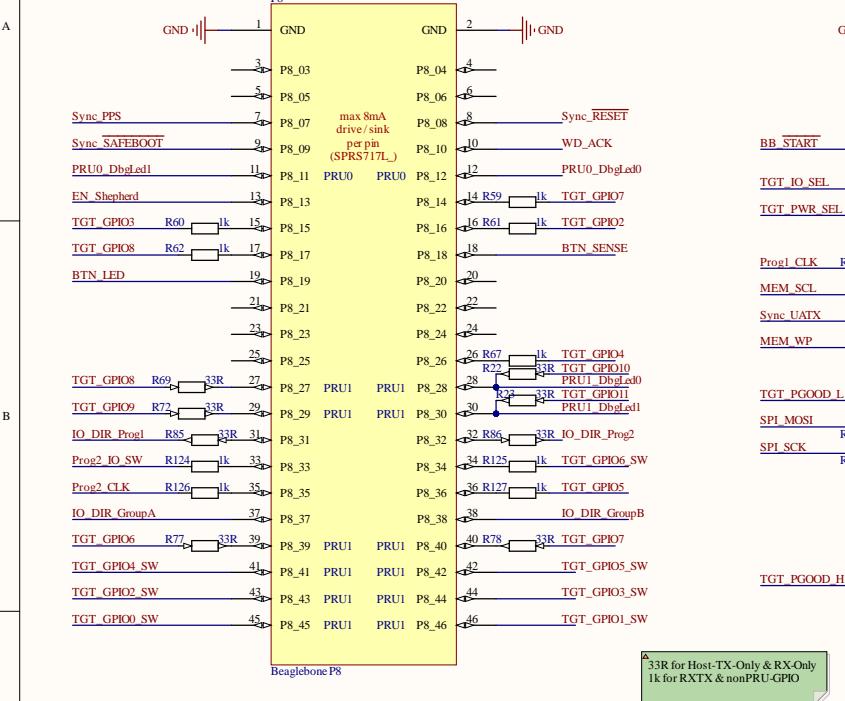
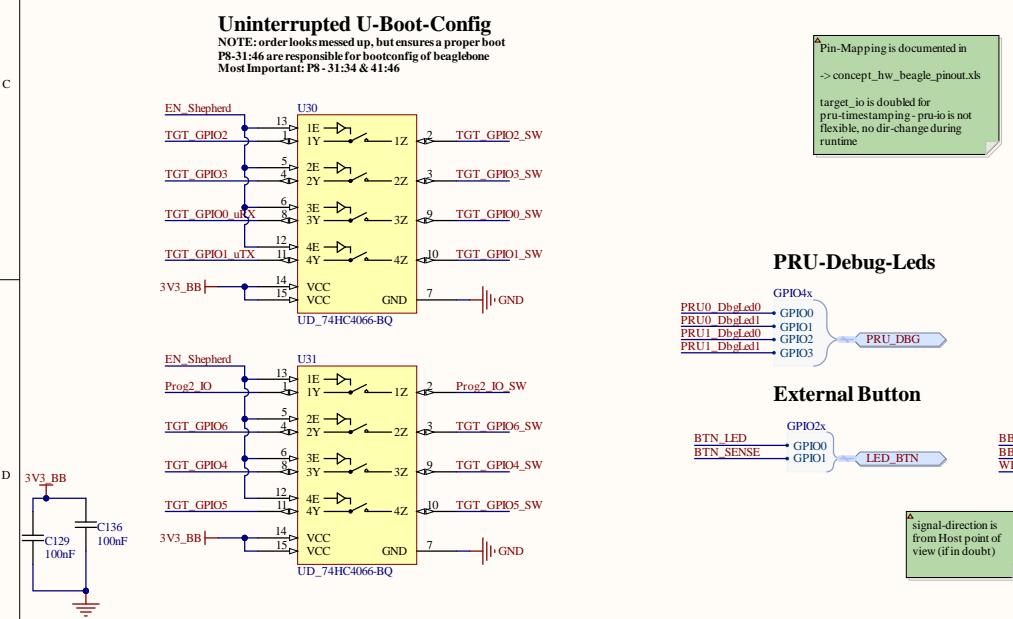
**Consumption:**  
- Disabled < 2 mA  
- Enabled 67 mA @ 5.1 V (Emu & Rec)  
- BB 390 mA during boot, 170 to 240 mA later

Shepherd ON 272 mW (Emu only)  
18mW @ 3V 144mW @ 5V  
36mW @ 6V 37mW @ 16V

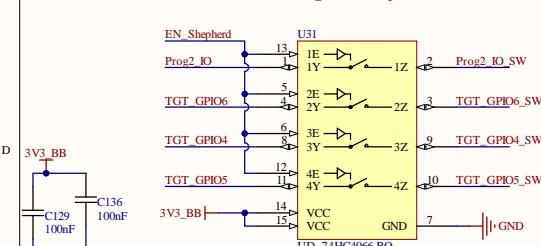
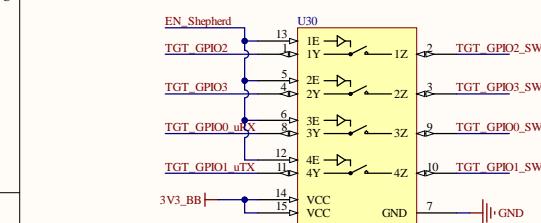
Shepherd ON 401 mW (Emu & Rec)  
18mW @ 3V 198mW @ 5V  
36mW @ 6V 101mW @ 16V

Shepherd MAX 1121mW (both targets drain 50mA)  
20mW @ 3V 795mW @ 5V  
36mW @ 6V 101mW @ 16V

**Main Voltages:**  
A5V/LSV -> 5.000 V Should be Spot On  
L3V3 -> 3.300 V Should be Spot On  
6V -> 5.38 V [5.29; 5.47] V with 1% Res  
10V -> 9.73 V [9.56; 9.90] V with 1% Res  
-6V -> -6 V, [5.94; 6.06] V with 1% Res

**Target****Beaglebone Pinheader P8****Beaglebone Pinheader P9****Uninterrupted U-Boot-Config**

NOTE: order looks messed up, but ensures a proper boot  
P8\_31:46 are responsible for bootconfig of beaglebone  
Most Important: P8\_31:34 & 41:46

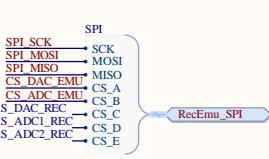


NOTE: needs PWR during U-Boot-phase to boot properly  
NOTE: the IC-internal 50 Ohm replace possible 33R

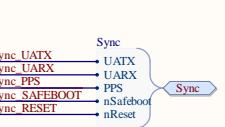
1      2      3      4      5      6

**PRU-Debug-Leds****External Button****Sys\_Watchdog**

signal-direction is from Host point of view (if in doubt)

**Calibration\_Storage****Emulator & Recorder****Emulator & Recorder**

EN\_Shepherd → EN\_Shepherd, EN\_Emulator → EN\_Emulator

**Sync-Adapter**

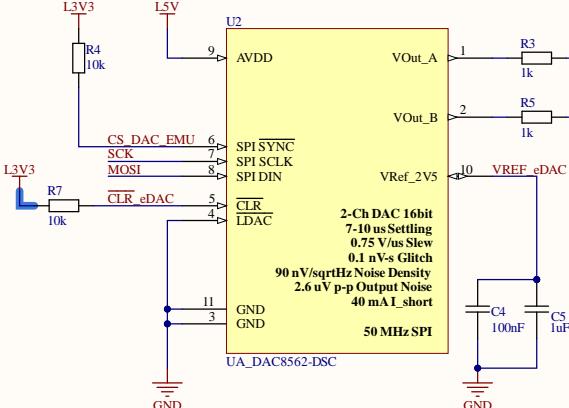
Title: Shepherd - Host Interface  
NES Lab / TU Dresden

Size	Number	Revision
A4		
Date:	3/03/2025	Sheet of shepherd_v2.PjPcb
File:	C:\Users\...\Host-Interface.SchDoc	Drawn By: Ingmar

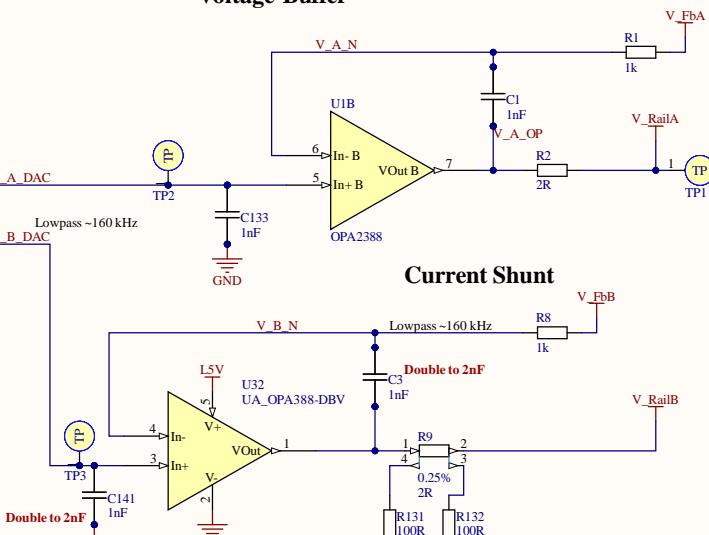
1      2      3      4      5      6

1 2 3 4 5 6

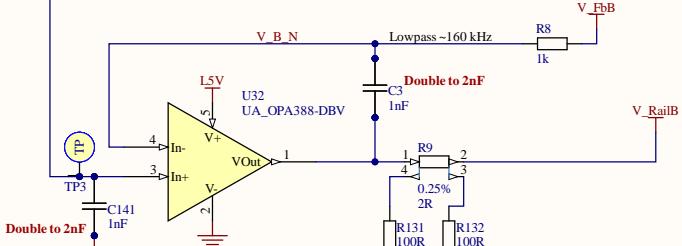
### precision DAC



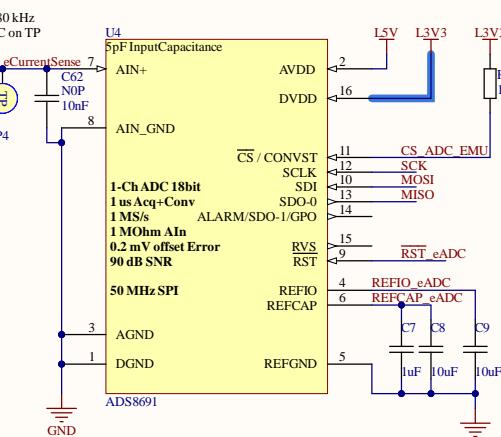
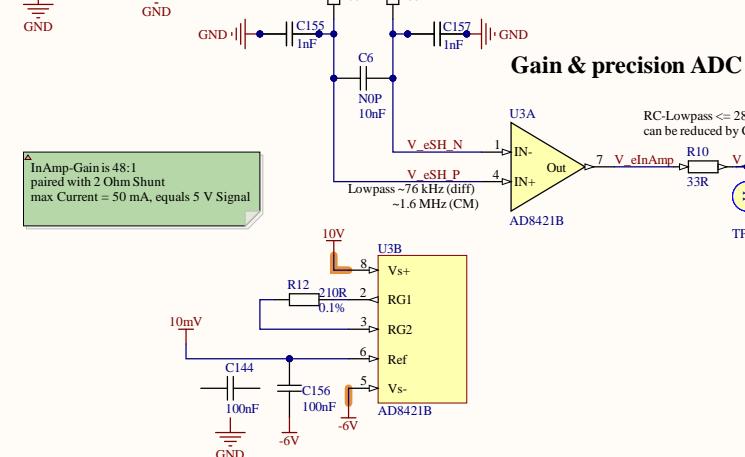
### Voltage-Buffer



### Current Shunt



### Gain & precision ADC



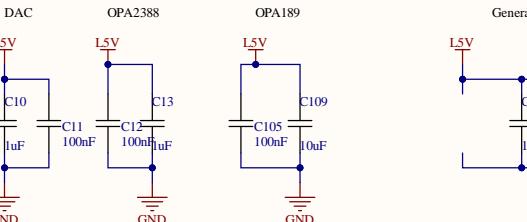
### Interchangeable Version with 500 kS & 100 kS

Title Shepherd -Emulator Frontend NES Lab / TU Dresden		
Size A3	Number	Revision
Date: 3/03/2025		Sheet of shepherd_v2.PnjPcb
File: C:\Users\...\Emulator.SchDoc		Drawn By: Ingmar

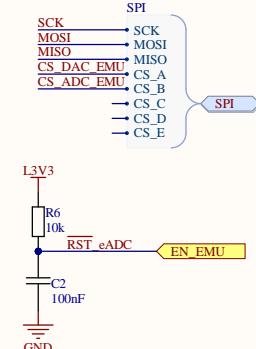
1 2 3 4 5 6

# for Performance-Analysis see Recorder-Schematic  
# Signal-Propagation-Delay  
# Noise-Estimate  
# Signal Ranges

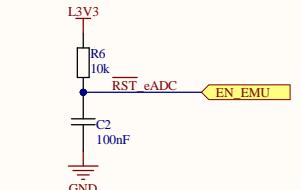
InAmp-Gain is 48:1 paired with 2 Ohm Shunt  
max Current = 50 mA, equals 5 V Signal



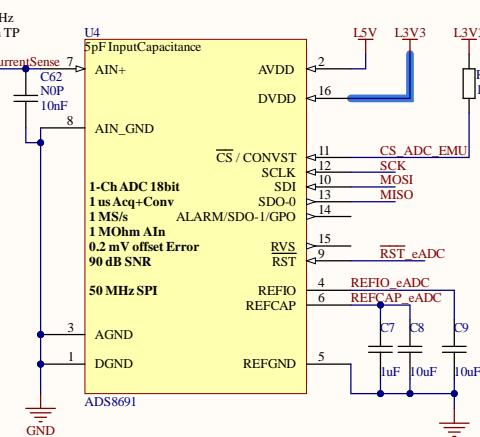
A



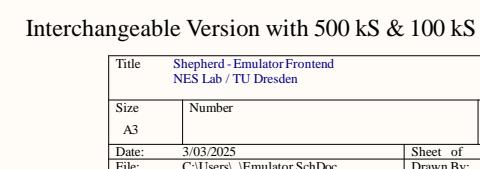
B



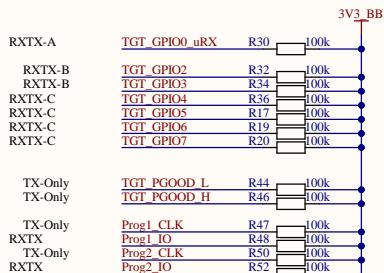
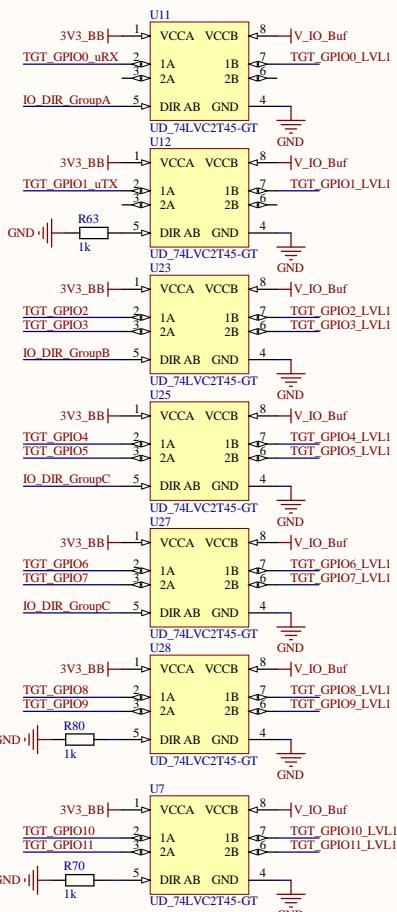
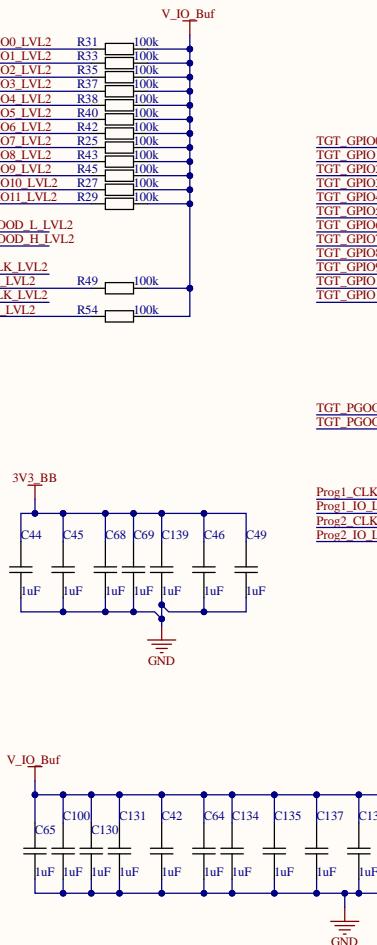
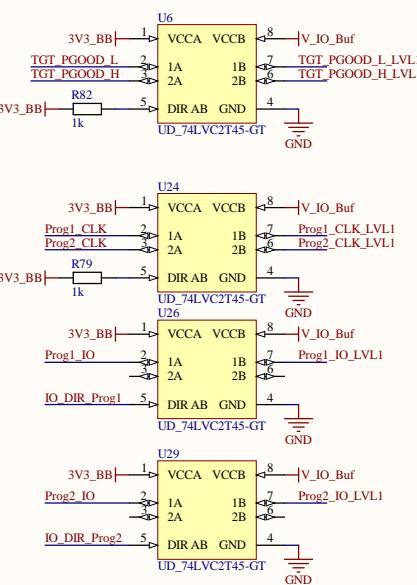
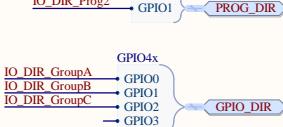
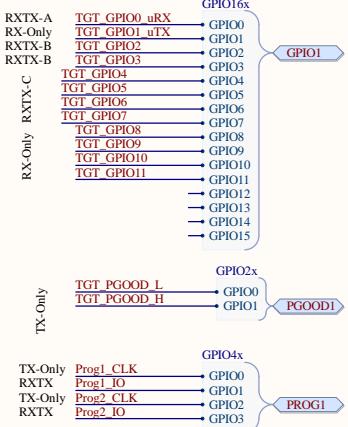
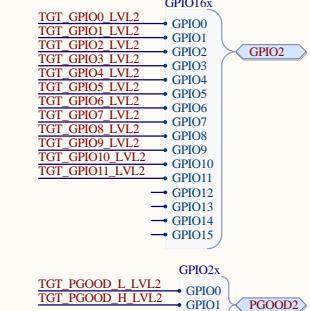
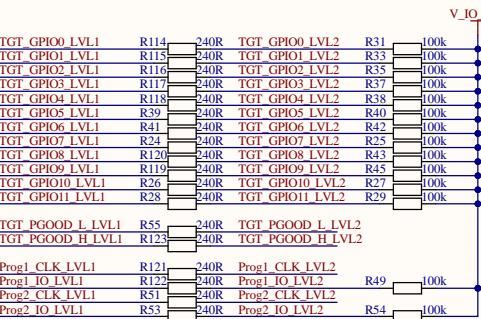
C



D



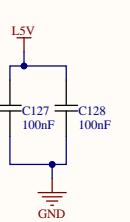
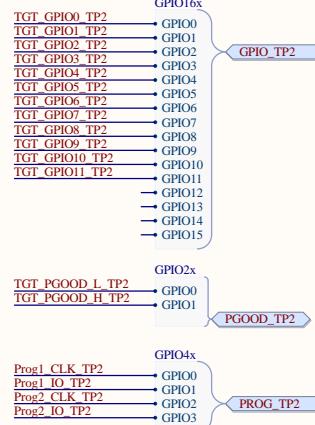
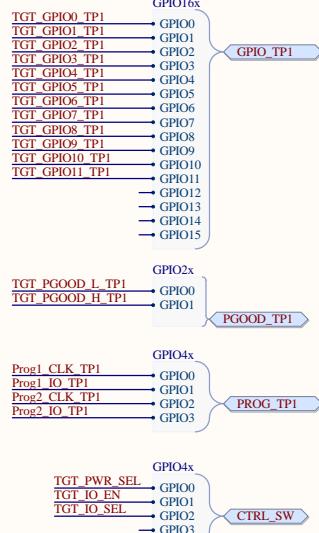
5 6

**SideA - Pull Ups****Level Translators****SideB - Shunts & Pull Ups**

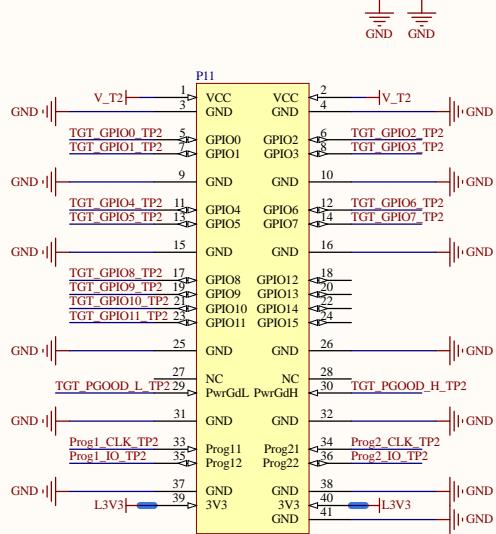
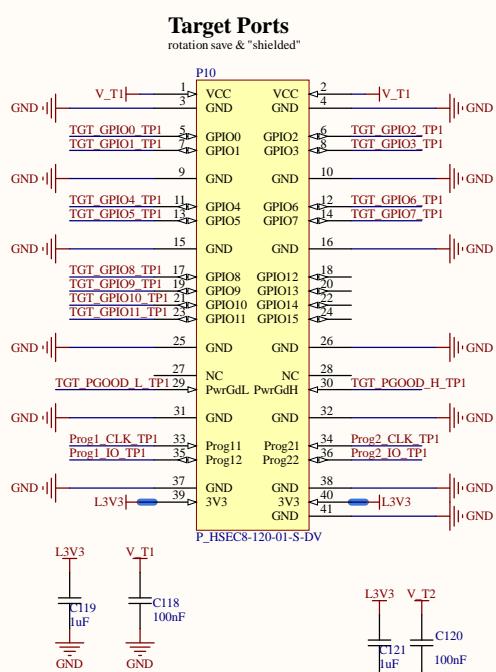
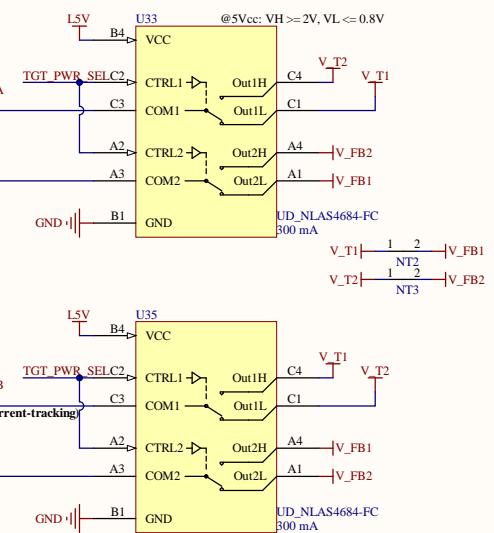
Title Shepherd - Level Translators  
Nes Lab / TU Dresden

Size	Number	Revision
A3		
Date:	3/03/2025	Sheet of shepherd_v2.PnjPcb

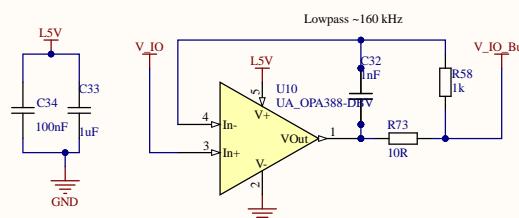
File: C:\Users...\LevelTranslators.SchDoc Drawn By: Ingmar



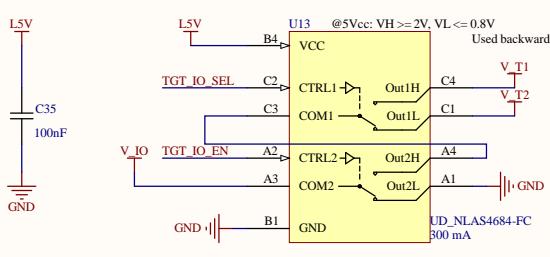
## Power Switches



## IO-Voltage - Buffer



## IO-Voltage - Reverse Routing Switch



**D**

**Programming-Hints:**

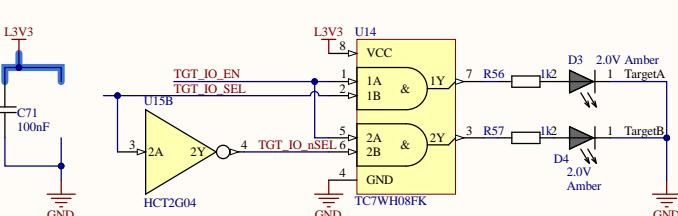
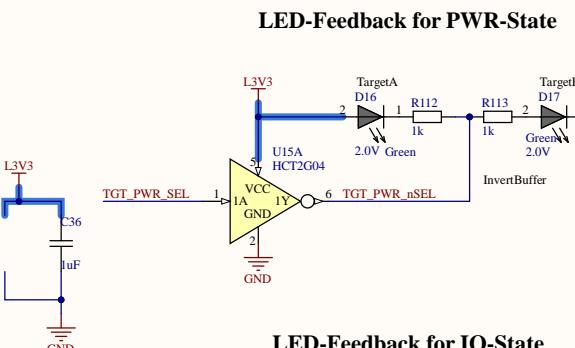
- Equalize DACs before switching
- unused GPIO should be switched to Input (target and bbone)
- level translators can be switched to other target for low leakage

**Leakage Analysis (max per Pin):**

NLAS4684	1-2 nA
NXS0101	1 uA
LSF010x	1-5 uA

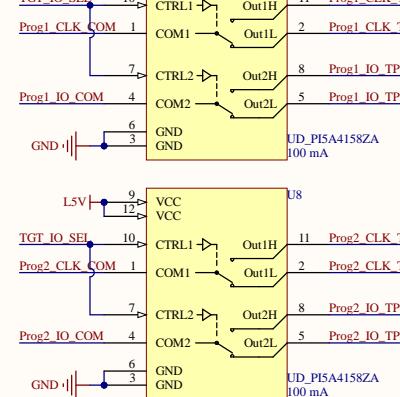
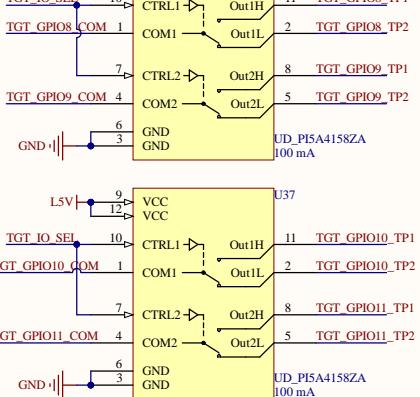
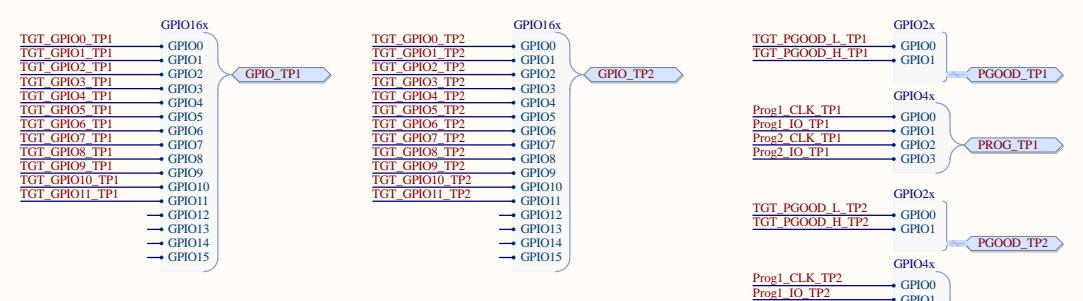
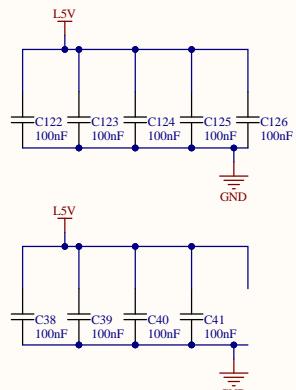
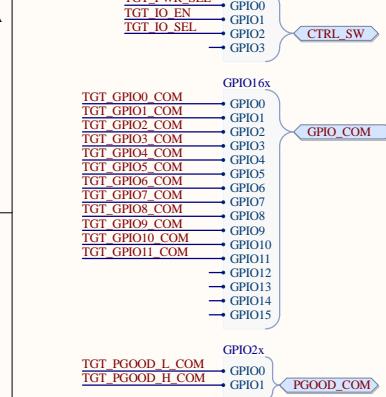
**Max Current:**

Target Switches 300mA  
3V3(unmonitored) 250mA  
V\_Target -> OPA#388 VoltageBuffers source 30-60mA, current measurement up to 50mA

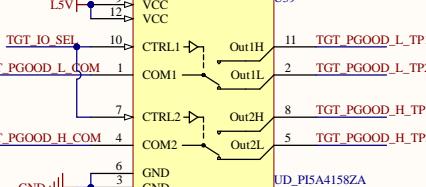


Title Shepherd - Target Interface NBS Lab / TU Dresden		
Size A3	Number	Revision
Date: 3/03/2025	Sheet of shepherd_v2.PriPcb	
File: C:\Users...\Targets.SchDoc	Drawn By: Ingmar	

## Signal Switches



SEL Tar1 Tar2  
 0 VA VB  
 1 VB VA  
 only VB has current-tracking  
 -> so SEL=1 enables tracking of Target 1  
 0 enables tracking of Target 2



Title Shepherd - Signal Routing NES Lab / TU Dresden		
Size A3	Number	Revision
Date: 3/03/2025	Sheet of shepherd_v2.PriPcb	
File: C:\Users\...\SignalRouting.SchDoc	Drawn By: Ingmar	

