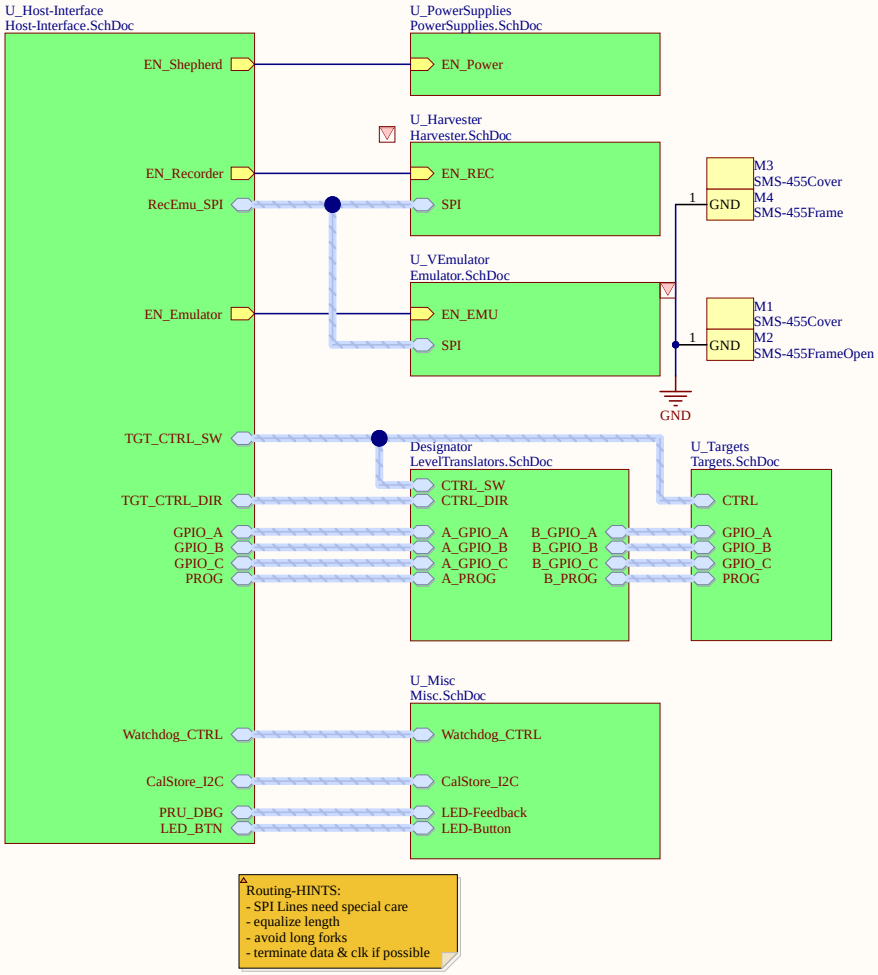
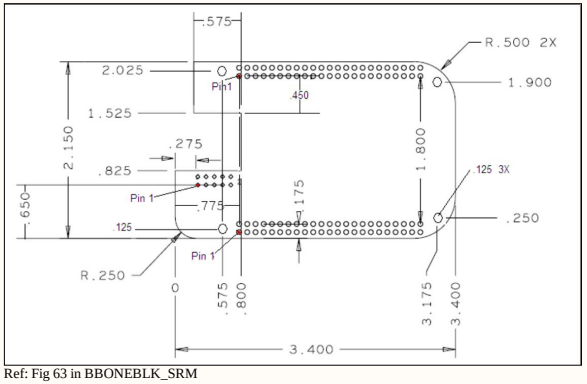




Ref: Fig 63 in BBONEBLK_SRM

PCB Manufacturing Constraints

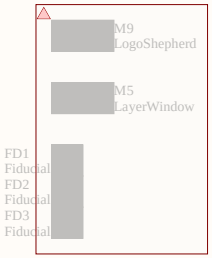
- Size 54.1 x 75.2 mm, 6 Layer
- 0.15 mm Track Width
- 0.15 mm Copper Clearance
- 0.38 mm Edge Clearance
- 0.35 mm Toolsize / non plated Hole
- 0.25 mm Plated Hole (End-)Size
- 0.125 mm Annular Ring
- 2.54 mm milling radius
- Solder Paste Pads are optimized for a 70 - 110 um Stencil

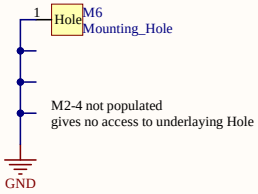
Assembly (v2.4)

- 2 Variations, recorder / emulator are self-contained and optional
- with Rec & Emu -> 353 parts, 53 unique
- with Emu -> X parts, X unique
- Mech-15 contains assembly notes / Pick and Place
- marking origin of part: cross (+) on assembly notes layer
- marking pad 1 of ICs: chamfered edge and circle (assembly notes) and filled triangle (silk)
- marking cathode of diodes: "C" or chamfered edge (assembly notes) and filled triangle (silk)
- Mech-2 contains Top Part Designators
- smallest part 0402
- smallest pitch 0.35 mm, XSON8
- only top layer populated

Manual Assembly
- Mech-13 contains info about non-reflow parts (8 items)

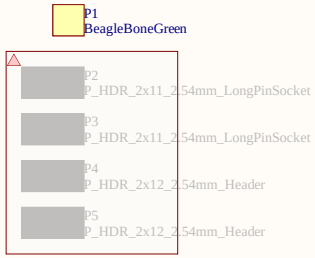
Misc





M2-4 not populated
gives no access to underlaying Hole

BOM-Additions



BOM PMEG1001-Alternative

SMMSD701T1G IR = 1.4 nA
PMEG10010ELRX IR = 2.1 nA
RB168MM-40TR IR = 8.0 nA

External-BOM

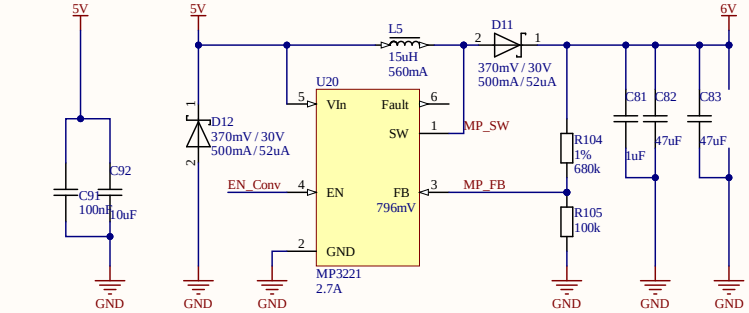
USB-Stick 256 GB
Ethernet Cables
POE-Adapter
uSD-Card (for flashing)

Calibration Resistors
1k-0603-0.05% 667-ERA-3ARW102V
100R-0603-0.05% 754-RG1608N-101-W-T1

Pinheader Connection BBone Variants
2x23 Header -> 77313-802-46LF 1.3 €
2x23 LongPinSocket
Samtec SSQ-123-23-G-D or 03-G-D 6 € (Default in BOM)
Major League SSHQ-123-D-10-G-LF 3 €
2x11 LongPinSocket & 2x12 Header
Samtec SSQ-111-03-G-D 3 €
Amphenol 10129381-924003BLF 0.4 €

Title	Shepherd - Overview NES Lab / TU Dresden		
Size A4	Number		Revision
Date:	9.17.2023	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\overview.SchDoc	Drawn By:	Ingmar

BoostConverter

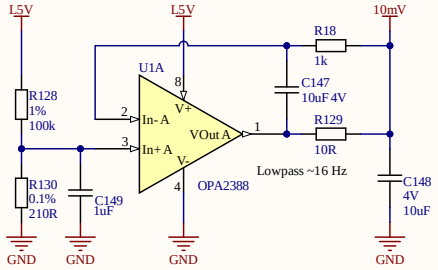


Vout 6.2088 V, 1% range is [6.102; 6.318] V

I_out [36; 166] mA
dV_out <= 9.2 - 42 uV (min/max load) Output-Ripple

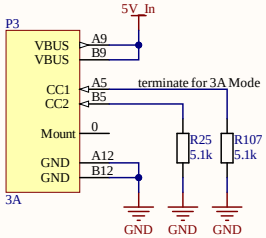
L_Opt = 20 uH

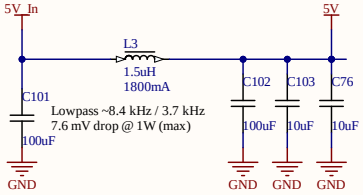
Reference-Offset



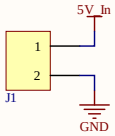
Lowpass ~1.6 Hz

External Power Input

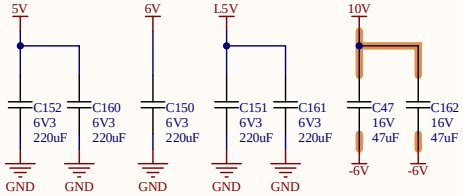




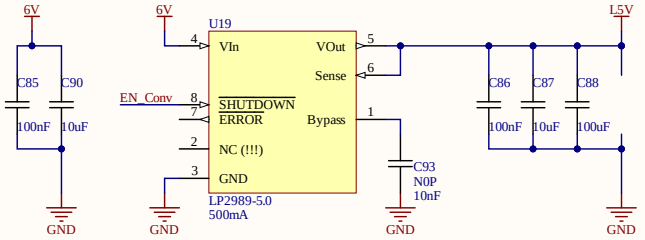
MAX 5V

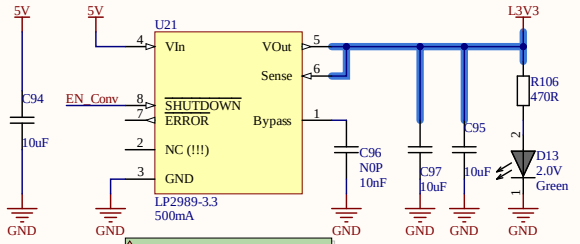


Optional Caps / Backside



LowNoise LDOs





Recommended:
- 10nF NP0 Bypass (low Leakage)
- VIn >= VOut + 1V

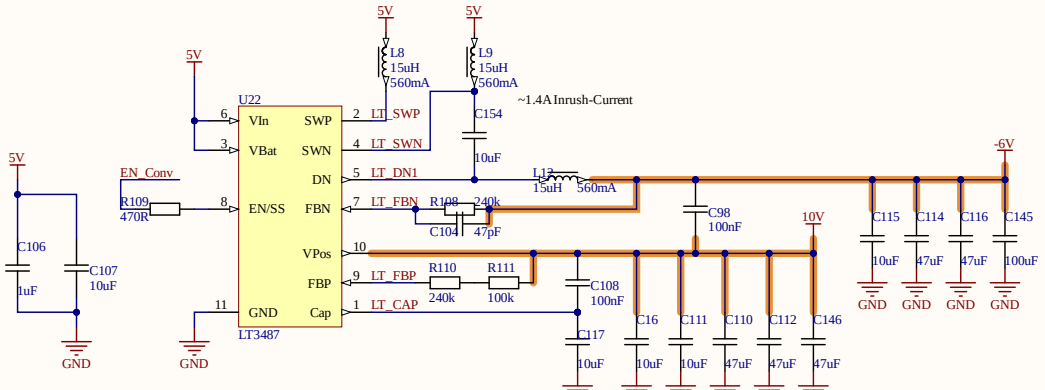
Consumption:
- Disabled < 2 mA
- Enabled 67 mA @ 5.1 V (Emu & Rec)
- BB 390 mA during boot, 170 to 240 mA later

Shepherd ON	272 mW (Emu only)	
	18mW @ 3V	144mW @ 5V
	36mW @ 6V	37mW @ 16V
Shepherd ON	401 mW (Emu & Rec)	
	18mW @ 3V	198mW @ 5V
	36mW @ 6V	101mW @ 16V
Shepherd MAX	1121mW (both targets drain 50mA)	
	20mW @ 3V	795mW @ 5V
	36mW @ 6V	101mW @ 16V

Main Voltages:

A5V/L5V	-> 5.000 V	Should be Spot On
L3V3	-> 3.300 V	Should be Spot On
6V	-> 5.38 V	[5.29; 5.47] V with 1% Res
10V	-> 9.73 V	[9.56; 9.90] V with 1% Res
-6V	-> -6 V,	[5.94; 6.06] V with 1% Res

Boost & Inverter



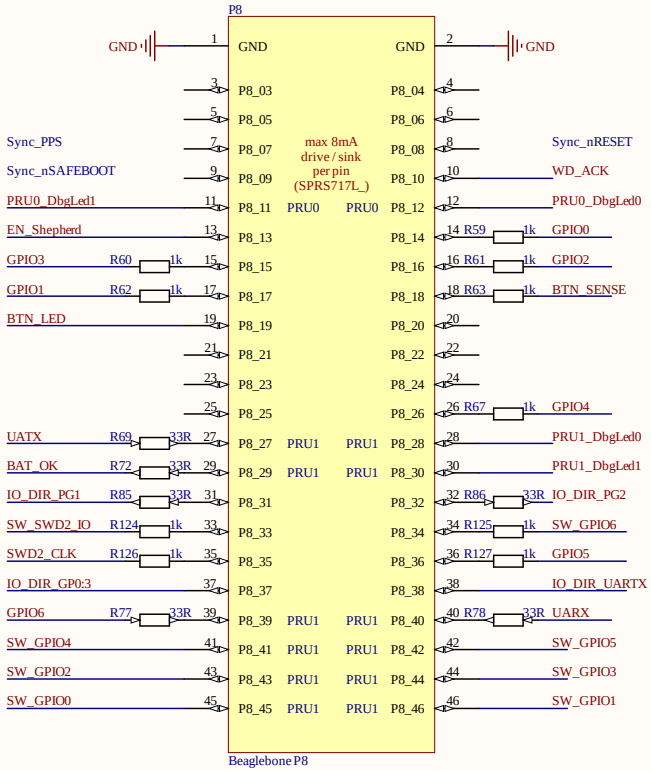
R1=(Vp-1.23V)/25uA
R1=350.8 kOhm (10V)
340kOhm -> 9.73V @1%

R2=-Vn/25uA
R2=240 kOhm (-6V)

Regulator drives at least 50mA on both Outputs

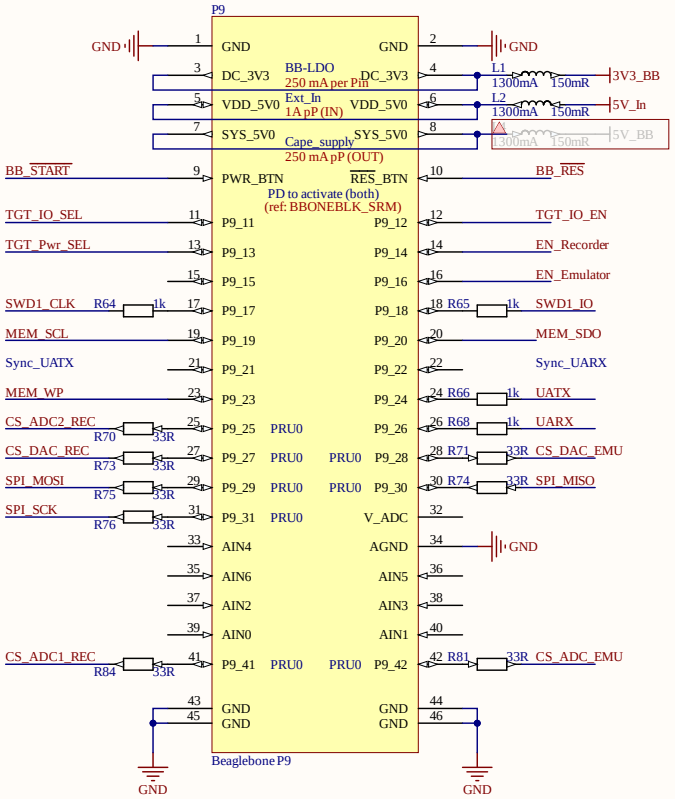
Title	Shepherd - Power Supplies NES Lab / TU Dresden		
Size	Number		Revision
A4			
Date:	9.17.2023	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\PowerSupplies.SchDoc	Drawn By:	Ingmar

Beaglebone Pinheader P8

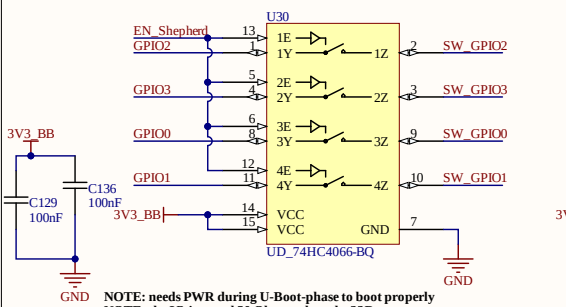


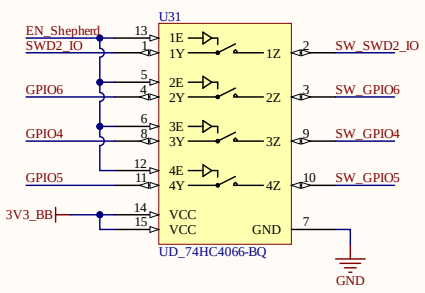
NOTE: order looks messed up, but ensures a proper boot
P8-31:46 are responsible for bootconfig of beaglebone
Most Important: P8 - 31:34 & 41:46

Beaglebone Pinheader P9



Uninterrupted U-Boot-Config





NOTE: needs PWR during U-Boot-phase to boot properly
NOTE: the IC-internal 50 Ohm replace the 33R

Pin-Mapping is documented in

-> concept_hw_beagle_pinout.xls

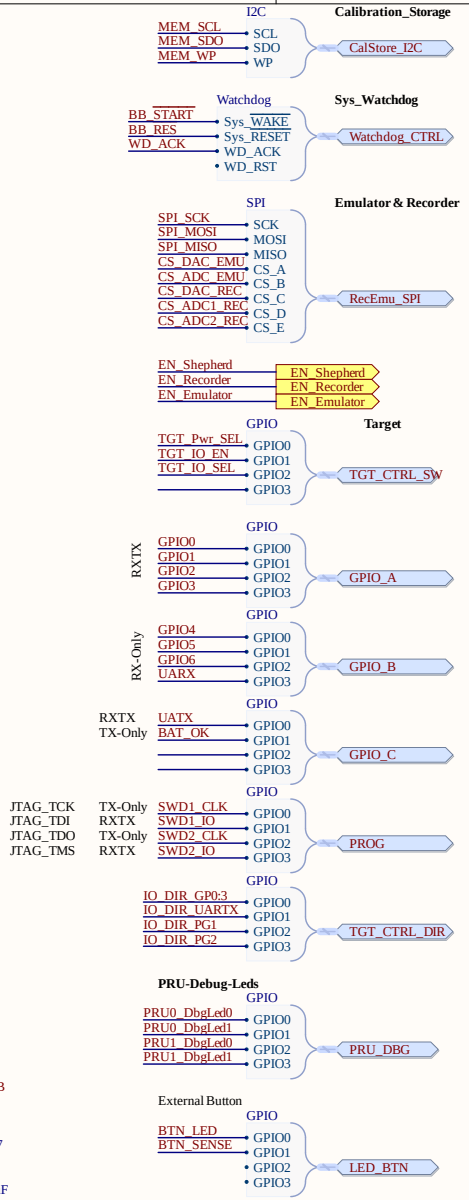
target_io is doubled for pru-timestamping - pru-io is not flexible, no dir-change during runtime

Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V
PWR_BTN	3.74V
nRES_BTN	0.15V

nSTART: BB_PCB has nothing discrete except switch to GND

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & switch to GND



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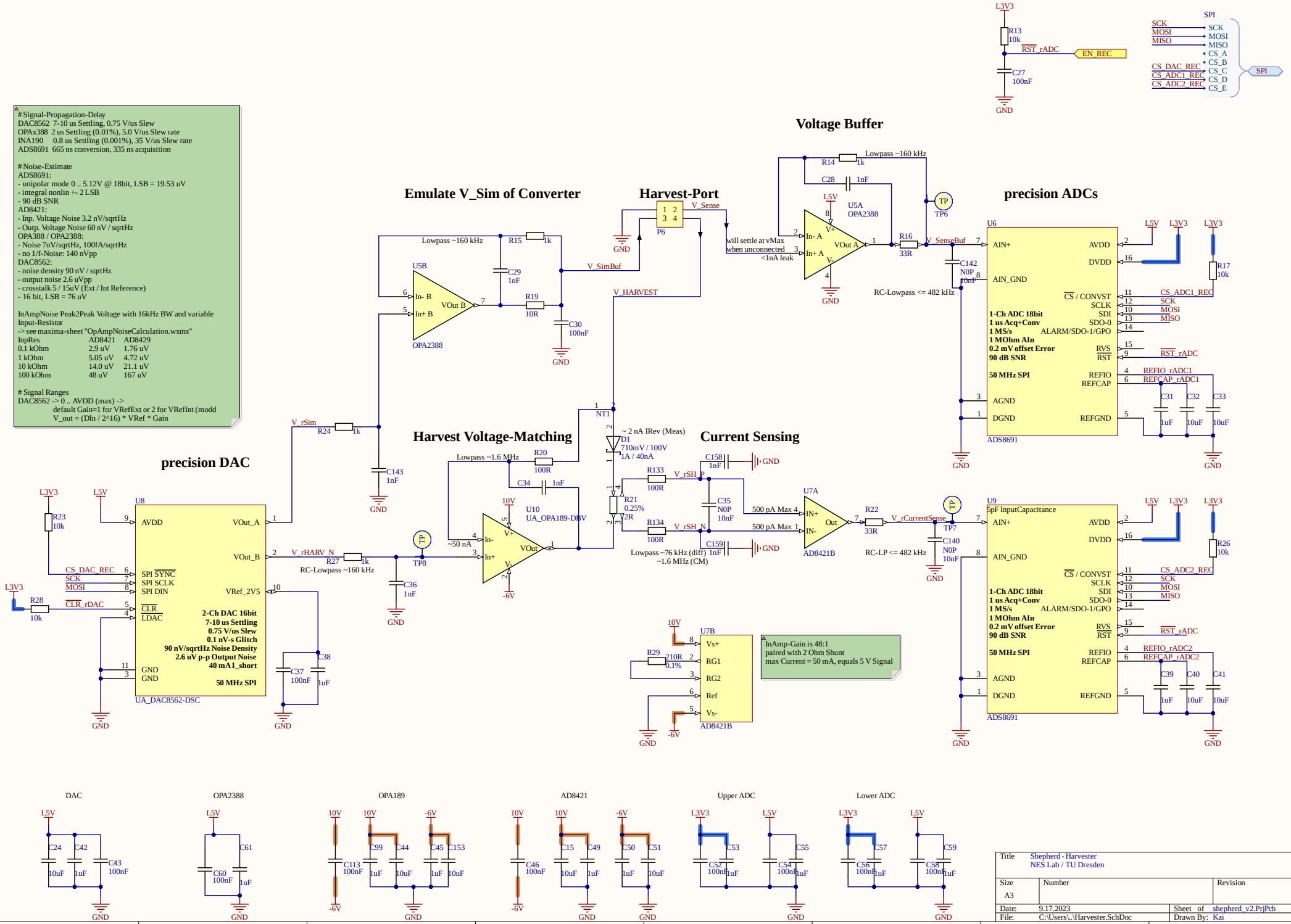
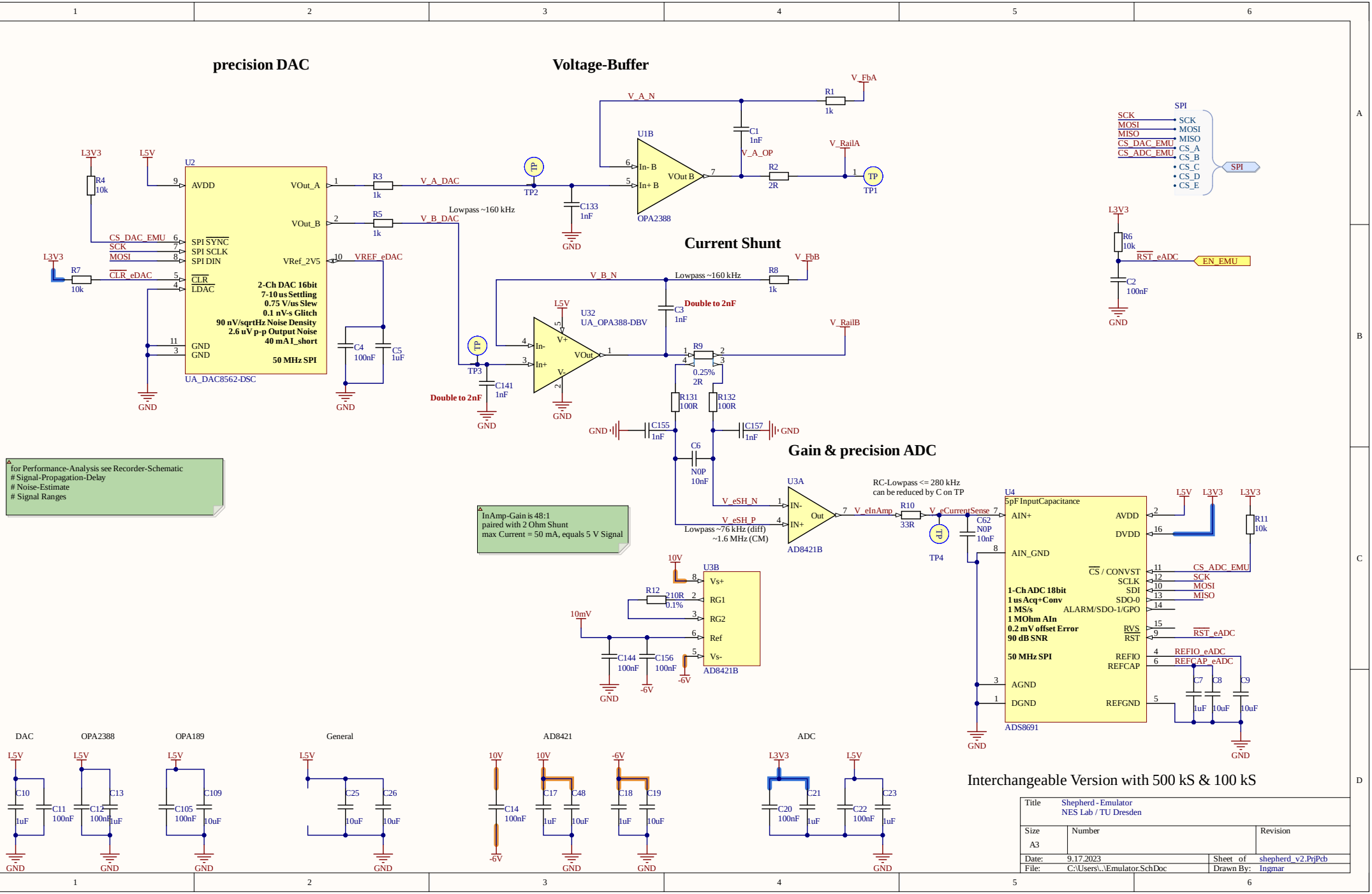
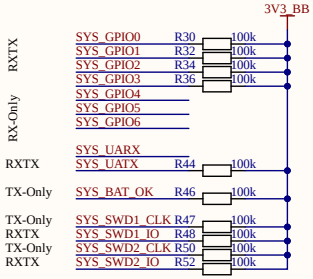
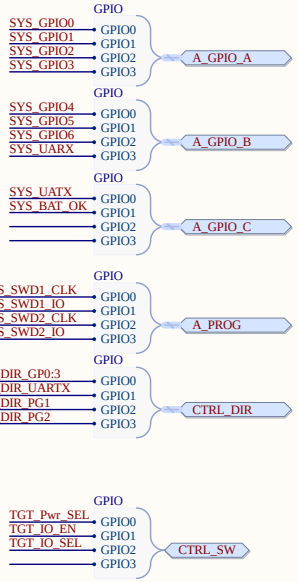
File: C:\Users\..\Host-Interface.SchDoc		Drawn By: Ingmar


Signal-Propagation-Delay
DAC8562 7-10 us Settling, 0.75 V/us Slew
OPAx388 2 us Settling (0.01%), 5.0 V/us Slew rate
INA190 0.8 us Settling (0.001%), 35 V/us Slew rate
ADS8691 665 ns conversion, 335 ns acquisition
Noise-Estimate
ADS8691:
- unipolar mode 0 .. 5.12V @ 18bit, LSB = 19.53 uV
- integral nonlin +- 2 LSB
- 90 dB SNR
AD8421:
- Inp. Voltage Noise 3.2 nV/sqrtHz
- Outp. Voltage Noise 60 nV / sqrtHz
OPA388 / OPA2388:
- Noise 7nV/sqrtHz, 100fA/sqrtHz
- no 1/f-Noise: 140 nVpp
DAC8562:
- noise density 90 nV / sqrtHz
- output noise 2.6 uVpp
- crosstalk 5 / 15uV (Ext / Int Reference)
- 16 bit, LSB = 76 uV
InAmpNoise Peak2Peak Voltage with 16kHz BW and variable Input-Resistor
-> see maxima-sheet "OpAmpNoiseCalculation.wxmx"
InpRes AD8421 AD8429
0.1 kOhm 2.9 uV 1.76 uV
1 kOhm 5.05 uV 4.72 uV
10 kOhm 14.0 uV 21.1 uV
100 kOhm 48 uV 167 uV
Signal Ranges
DAC8562 -> 0 .. AVDD (max) -> default Gain=1 for VRefExt or 2 for VRefInt (modd V_out = (Dln / 2^16) * VRef * Gain
Voltage Buffer
Emulate V_Sim of Converter
Harvest-Port
precision ADCs
precision DAC
Harvest Voltage-Matching
Current Sensing
L3V3
R13 10k
RST_rADC
EN_REC
C27 100nF
GND
SPI
SCK
MOSI
MISO
CS_A
CS_B
CS_C
CS_D
CS_E
CS_DAC_REC
CS_ADC1_REC
CS_ADC2_REC
R14 1k
Lowpass ~160 kHz
C28 1nF
L5V
U5A OPA2388
will settle at vMax when unconnected <1nA leak
TP6
R16 33R
V_SenseBuf
C142 N0P 10nF
RC-Lowpass <= 482 kHz
U6
AIN+
AIN_GND
AVDD
DVDD
CS / CONVST
SCLK
SDI
SDO-0
ALARM/SDO-1/GPO
RVS
RST
REFIO
REFCAP
REFGND
AGND
DGND
1-Ch ADC 18bit
1 us Acq+Conv
1 MS/s
1 MOhm AIn
0.2 mV offset Error
90 dB SNR
50 MHz SPI
ADS8691
R17 10k
REFIO_rADC1
REFCAP_rADC1
C31 1uF
C32 10uF
C33 10uF
U5B OPA2388
R15 1k
C29 1nF
R19 10R
C30 100nF
V_SimBuf
V_HARVEST
P6
V_Sense
V_rSim
R24 1k
C143 1nF
NT1
~ 2 nA IRev (Meas)
D1 710mV / 100V 1A / 40nA
R20 100R
C34 1nF
R21 0.25% 2R
R133 100R
R134 100R
V_rSH_P
V_rSH_N
C35 N0P 10nF
C158 1nF
C159 1nF
500 pA Max 4
500 pA Max 1
U7A AD8421B
R22 33R
V_rCurrentSense
TP7
C140 N0P 10nF
RC-LP <= 482 kHz
U9
5pF InputCapacitance
R26 10k
REFIO_rADC2
REFCAP_rADC2
C39 1uF
C40 10uF
C41 10uF
U8
SPI SYNC
SPI SCLK
SPI DIN
CLR
LDAC
VOut_A
VOut_B
VRef_2V5
2-Ch DAC 16bit
7-10 us Settling
0.75 V/us Slew
0.1 nV-s Glitch
90 nV/sqrtHz Noise Density
2.6 uV p-p Output Noise
40 mA I_short
50 MHz SPI
UA_DAC8562-DSC
R23 10k
R28 10k
CS_DAC_REC
SCK
MOSI
CLR_rDAC
V_rHARV_N
R27 1k
RC-Lowpass ~160 kHz
TP8
C36 1nF
C37 100nF
C38 1uF
Lowpass ~1.6 MHz
R20 100R
C34 1nF
U10 UA_OPA189-DBV
~50 nA
Lowpass ~76 kHz (diff) 1nF
~1.6 MHz (CM)
U7B AD8421B
R29 210R 0.1%
InAmp-Gain is 48:1
paired with 2 Ohm Shunt
max Current = 50 mA, equals 5 V Signal
DAC
OPA2388
OPA189
AD8421
Upper ADC
Lower ADC
C24 10uF
C42 1uF
C43 100nF
C60 100nF
C61 1uF
C113 100nF
C99 1uF
C44 10uF
C45 1uF
C153 10uF
C46 100nF
C15 10uF
C49 1uF
C50 1uF
C51 10uF
C52 100nF
C53 1uF
C54 100nF
C55 1uF
C56 100nF
C57 1uF
C58 100nF
C59 1uF
Title Shepherd - Harvester
NES Lab / TU Dresden
Size A3
Number
Revision
Date: 9.17.2023
Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Harvester.SchDoc
Drawn By: Kai

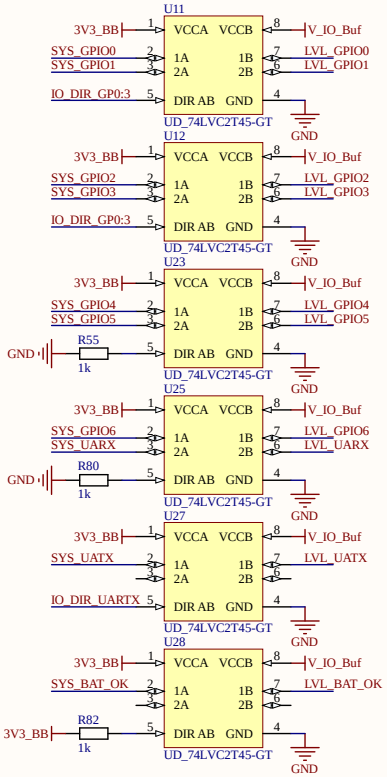

precision DAC
Voltage-Buffer
Current Shunt
Gain & precision ADC
U2
UA_DAC8562-DSC
AVDD
VOut_A
VOut_B
VRef_2V5
SPI SYNC
SPI SCLK
SPI DIN
CLR
LDAC
GND
2-Ch DAC 16bit
7-10 us Settling
0.75 V/us Slew
0.1 nV-s Glitch
90 nV/sqrtHz Noise Density
2.6 uV p-p Output Noise
40 mA I_short
50 MHz SPI
U1B
OPA2388
U32
UA_OPA388-DBV
U3A
U3B
AD8421B
U4
ADS8691
5pF InputCapacitance
AIN+
AIN_GND
AGND
DGND
DVDD
REFIO
REFCAP
REFGND
CS / CONVST
SCLK
SDI
SDO-0
ALARM/SDO-1/GPO
RVS
RST
1-Ch ADC 18bit
1 us Acq+Conv
1 MS/s
1 MOhm AIn
0.2 mV offset Error
90 dB SNR
50 MHz SPI
V_A_DAC
V_B_DAC
V_A_N
V_B_N
V_A_OP
V_FbA
V_FbB
V_RailA
V_RailB
V_eInAmp
V_eCurrentSense
V_eSH_N
V_eSH_P
Lowpass ~160 kHz
Lowpass ~76 kHz (diff)
~1.6 MHz (CM)
RC-Lowpass <= 280 kHz
can be reduced by C on TP
Double to 2nF
0.25%
SPI
SCK
MOSI
MISO
CS_DAC_EMU
CS_ADC_EMU
CS_A
CS_B
CS_C
CS_D
CS_E
RST_eADC
EN_EMU
REFIO_eADC
REFCAP_eADC
VREF_eDAC
CLR_eDAC
for Performance-Analysis see Recorder-Schematic
Signal-Propagation-Delay
Noise-Estimate
Signal Ranges
InAmp-Gain is 48:1
paired with 2 Ohm Shunt
max Current = 50 mA, equals 5 V Signal
DAC
OPA2388
OPA189
General
AD8421
ADC
Interchangeable Version with 500 kS & 100 kS
Title
Shepherd - Emulator
NES Lab / TU Dresden
Size
A3
Number
Revision
Date: 9.17.2023
Sheet of
shepherd_v2.PrjPcb
File: C:\Users\..\Emulator.SchDoc
Drawn By: Ingmar

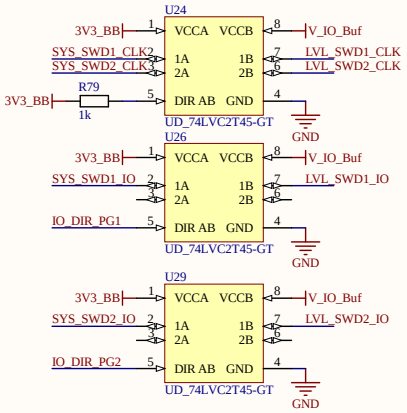
SideA - Pull Ups



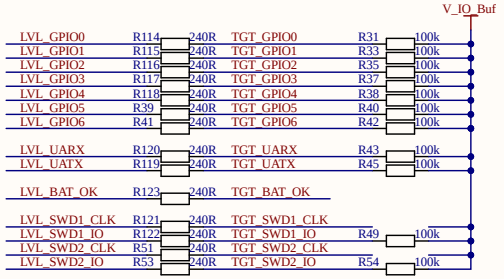


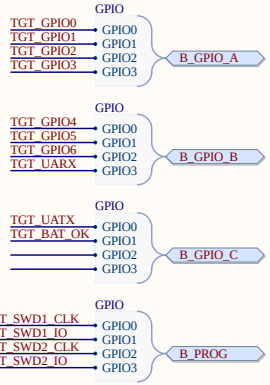
Level Translators

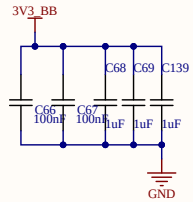


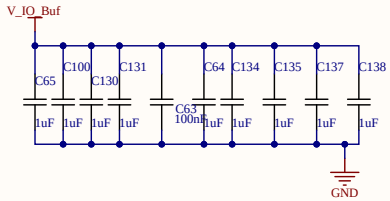


SideB - Pull Ups

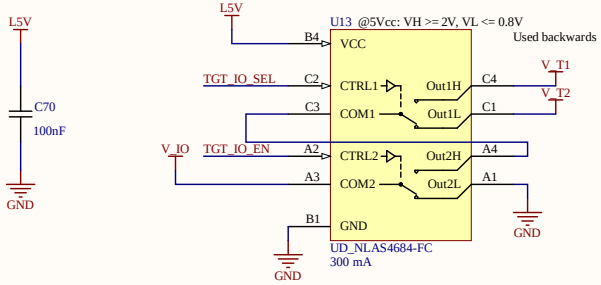




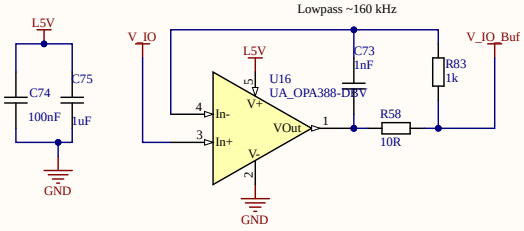




IO-Voltage - Reverse Routing Switch



IO-Voltage - Buffer



Title	Shepherd - Level Translators NES Lab / TU Dresden	
Size A3	Number	Revision
Date: 9.17.2023		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\LevelTranslators.SchDoc		Drawn By: Ingmar

Signal Switches

SEL	Tar1	Tar2
0	VA	VB
1	VB	VA

only VB has current-tracking
-> so SEL=1 enables tracking of Target 1
0 enables tracking of Target 2

GPIO
TGT_PWR_SEL, TGT_IO_EN, TGT_IO_SEL → GPIO0, GPIO1, GPIO2, GPIO3 → CTRL

GPIO
TGT_GPIO0, TGT_GPIO1, TGT_GPIO2, TGT_GPIO3 → GPIO0, GPIO1, GPIO2, GPIO3 → GPIO_A

GPIO
TGT_GPIO4, TGT_GPIO5, TGT_GPIO6, TGT_UARX → GPIO0, GPIO1, GPIO2, GPIO3 → GPIO_B

GPIO
TGT_UATX, TGT_BAT_OK → GPIO0, GPIO1, GPIO2, GPIO3 → GPIO_C

GPIO
TGT_SWD1_CLK, TGT_SWD1_IO, TGT_SWD2_CLK, TGT_SWD2_IO → GPIO0, GPIO1, GPIO2, GPIO3 → PROG

U34 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_GPIO6 → COM1
TGT_UARX → COM2
CTRL2, GND, GND → GND
Out1H → T1_GPIO6
Out1L → T2_GPIO6
Out2H → T1_UARX
Out2L → T2_UARX

U36 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_GPIO0 → COM1
TGT_GPIO1 → COM2
CTRL2, GND, GND → GND
Out1H → T1_GPIO0
Out1L → T2_GPIO0
Out2H → T1_GPIO1
Out2L → T2_GPIO1

U37 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_UATX → COM1
TGT_BAT_OK → COM2
CTRL2, GND, GND → GND
Out1H → T1_UATX
Out1L → T2_UATX
Out2H → T1_BAT_OK
Out2L → T2_BAT_OK

U38 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_GPIO2 → COM1
TGT_GPIO3 → COM2
CTRL2, GND, GND → GND
Out1H → T1_GPIO2
Out1L → T2_GPIO2
Out2H → T1_GPIO3
Out2L → T2_GPIO3

U39 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_SWD1_CLK → COM1
TGT_SWD2_CLK → COM2
CTRL2, GND, GND → GND
Out1H → T1_SWD1_CLK
Out1L → T2_SWD1_CLK
Out2H → T1_SWD2_CLK
Out2L → T2_SWD2_CLK

U40 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_GPIO4 → COM1
TGT_GPIO5 → COM2
CTRL2, GND, GND → GND
Out1H → T1_GPIO4
Out1L → T2_GPIO4
Out2H → T1_GPIO5
Out2L → T2_GPIO5

U41 UD_PI5A4158ZA 100 mA
L5V → VCC, VCC
TGT_IO_SEL → CTRL1
TGT_SWD1_IO → COM1
TGT_SWD2_IO → COM2
CTRL2, GND, GND → GND
Out1H → T1_SWD1_IO
Out1L → T2_SWD1_IO
Out2H → T1_SWD2_IO
Out2L → T2_SWD2_IO

L5V → C122 100nF, C123 100nF, C124 100nF, C125 100nF, C126 100nF → GND
L5V → C127 100nF, C128 100nF → GND

Power Switches

U33 UD_NLAS4684-FC 300 mA
L5V → VCC
V_RailA → TGT_PWR_SELC2
V_FbA → A2
GND → GND
CTRL1 → Out1H → C4 → V_T2
COM1 → Out1L → C1 → V_T1
CTRL2 → Out2H → A4 → V_FB2
COM2 → Out2L → A1 → V_FB1
B1 → GND
@5Vcc: VH >= 2V, VL <= 0.8V

V_T1 → NT2 → V_FB1
V_T2 → NT3 → V_FB2

U35 UD_NLAS4684-FC 300 mA
L5V → VCC
V_RailB → TGT_PWR_SELC2
(current-tracking)
V_FbB → A2
GND → GND
CTRL1 → Out1H → C4 → V_T1
COM1 → Out1L → C1 → V_T2
CTRL2 → Out2H → A4 → V_FB1
COM2 → Out2L → A1 → V_FB2
B1 → GND

Target Ports

P10 P_HDR_2x9_2.54mm_header
GND → GND, V1 → V_T1
T1_GPIO0, T1_GPIO2, T1_GPIO4, T1_GPIO6, T1_UATX → GPIO0, GPIO2, GPIO4, GPIO6, GPIO8
GPIO1, GPIO3, GPIO5, GPIO7, BATOK → T1_GPIO1, T1_GPIO3, T1_GPIO5, T1_UARX, T1_BAT_OK
T1_SWD1_CLK, T1_SWD2_CLK → Prog11, Prog21
Prog12, Prog22 → T1_SWD1_IO, T1_SWD2_IO
L3V3 → V2
GND → GND
C118 100nF
C119 1uF

P11 P_HDR_2x9_2.54mm_header
GND → GND, V1 → V_T2
T2_GPIO0, T2_GPIO2, T2_GPIO4, T2_GPIO6, T2_UATX → GPIO0, GPIO2, GPIO4, GPIO6, GPIO8
GPIO1, GPIO3, GPIO5, GPIO7, BATOK → T2_GPIO1, T2_GPIO3, T2_GPIO5, T2_UARX, T2_BAT_OK
T2_SWD1_CLK, T2_SWD2_CLK → Prog11, Prog21
Prog12, Prog22 → T2_SWD1_IO, T2_SWD2_IO
L3V3 → V2
GND → GND
C120 100nF
C121 1uF

rotation save & "shielded"

LED-Feedback for PWR-State

L3V3 → TargetA D16 2.0V Green → R112 1k → U15A HCT2G04 → TGT_PWR_nSEL
R113 1k → TargetB D17 Green 2.0V
TGT_PWR_SEL → U15A HCT2G04 → TGT_PWR_nSEL
InvertBuffer
GND

Programming-Hints:
- Equalize DACs before switching
- unused GPIO should be switched to Input (target and bbone)
- level translators can be switched to other target for low leakage

Leakage Analysis (max per Pin):

NLAS4684	1-2 nA
NXS0101	1 uA
LSF010x	1-5 uA

Max Current:

Target Switches	300mA
3V3 (unmonitored)	250mA

V_Target -> OPA#388 VoltageBuffers source 30-60mA, current measurement up to 50mA

Programming Target:

SWD	-> nRF52, STM32L4
SBW	-> MSP430, MSP432, CC430

SBW-TDIO, -TCK (nRST/NMI)

LED-Feedback for IO-State

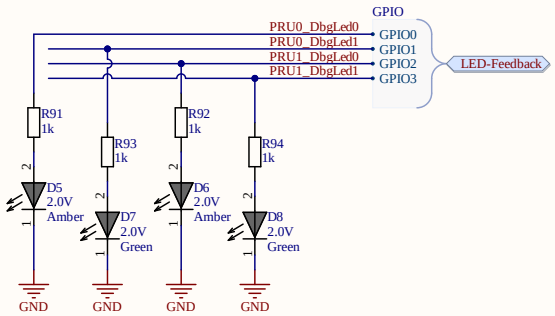
L3V3 → U14 TC7WH08FK
TGT_IO_EN, TGT_IO_SEL → 1A, 1B
U15B HCT2G04 → TGT_IO_nSEL
2A, 2B → GND
1Y → R56 1k → D3 2.0V Amber → TargetA
2Y → R57 1k → D4 2.0V Amber → TargetB
L3V3 → C71 100nF, C72 1uF → GND

Title	Shepherd - Target Interface NES Lab / TU Dresden	
Size: A3	Number	Revision
Date: 9.17.2023		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Targets.SchDoc		Drawn By: Ingmar

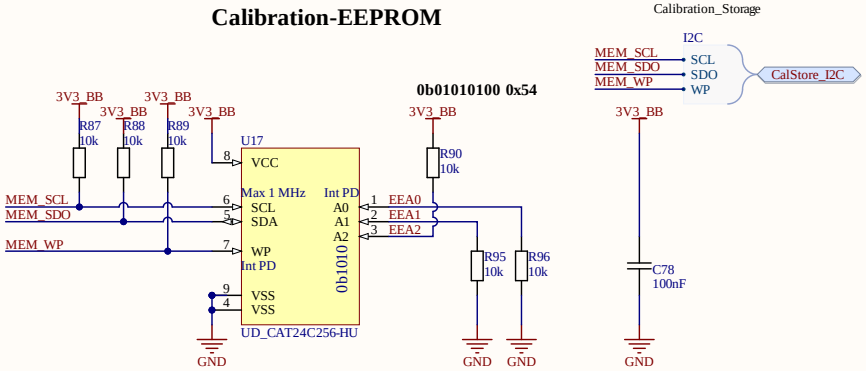
TODO:
Separate into smaller Individual Schem

Possible Changes:
- LED Button could be designed with just 3 Leads, or even 2
- One LED per PRU is enough

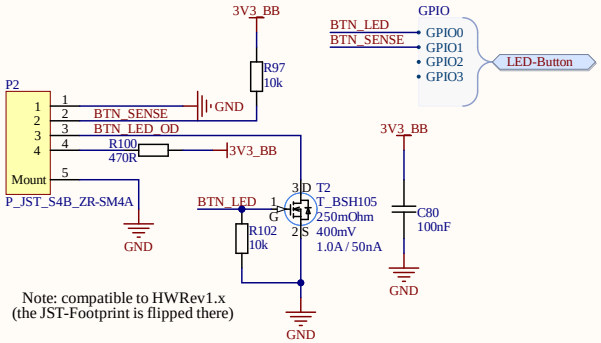
PRU-LED-Feedback



Calibration-EEPROM



Local Control Button

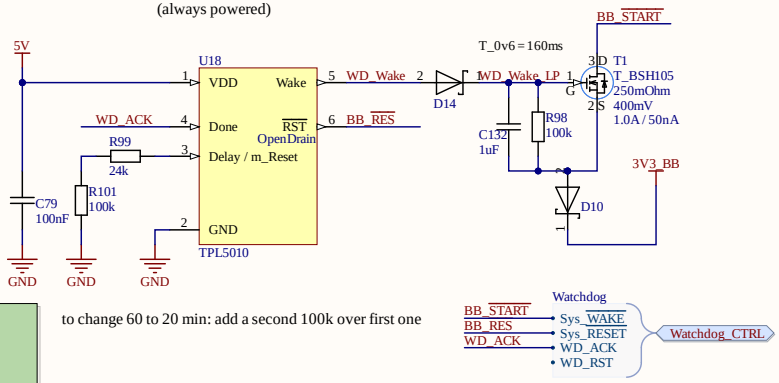


Note: compatible to HWRev1.x
(the JST-Footprint is flipped there)

schematic changed to avoid internal voltages on cable

Watchdog

(always powered)



BB-Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V

nSTART: BB_PCB has nothing discrete except pull-switch to GND, normally 5V Signal
-> use 3V3 as Pull-Down to only get affected by wake-signal when BB is powered off -> seems fine

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & pull-switch to GND

to change 60 to 20 min: add a second 100k over first one

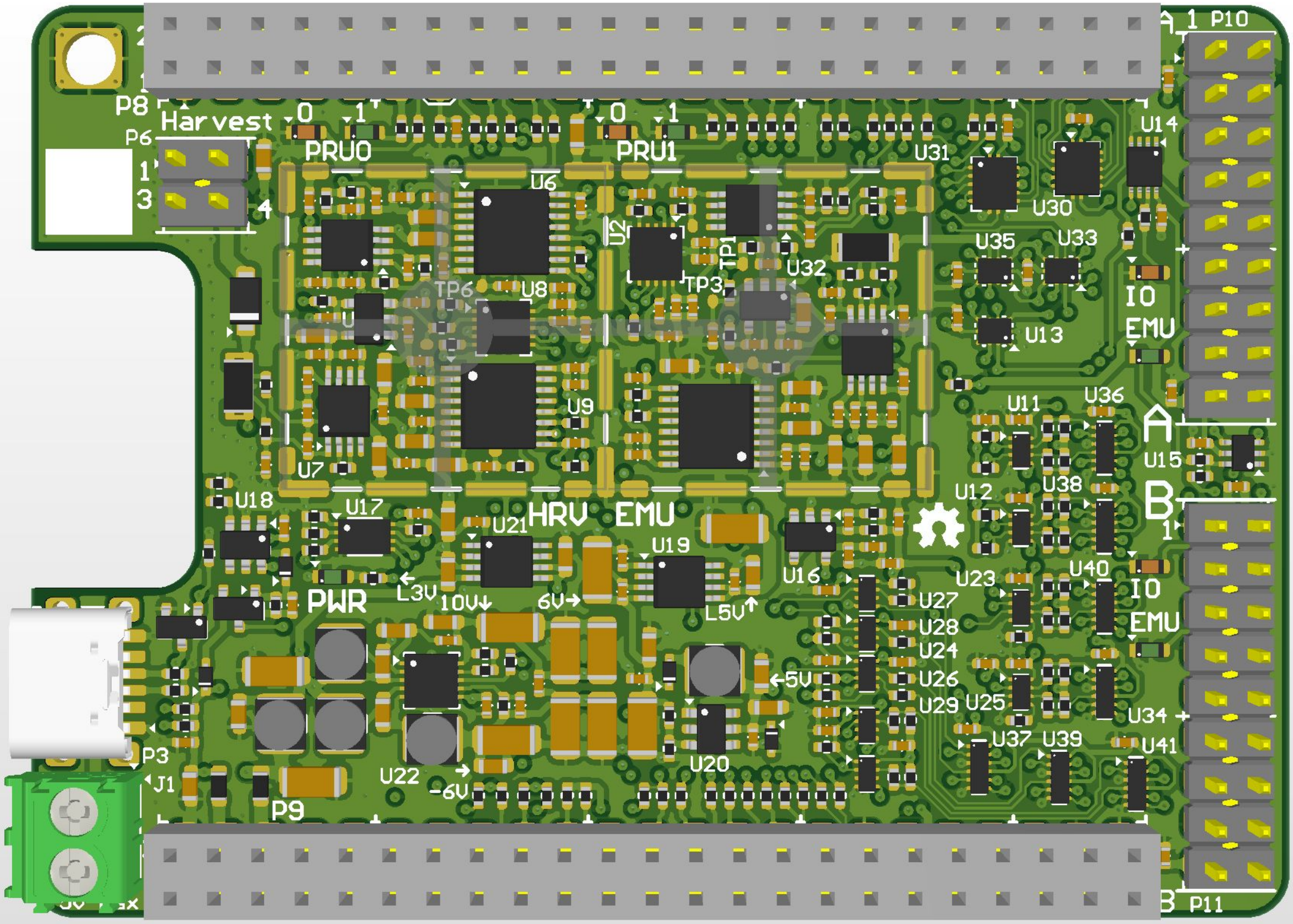
Watchdog - Advantages:
- nodes are in remote rooms, often without access
- Fallback if we can't control POE-Power of ports (most likely)
- with a WD the BB can shut down and be woken up periodically
- routine: BB aks server for tasks, waits or goes to sleep if NOP

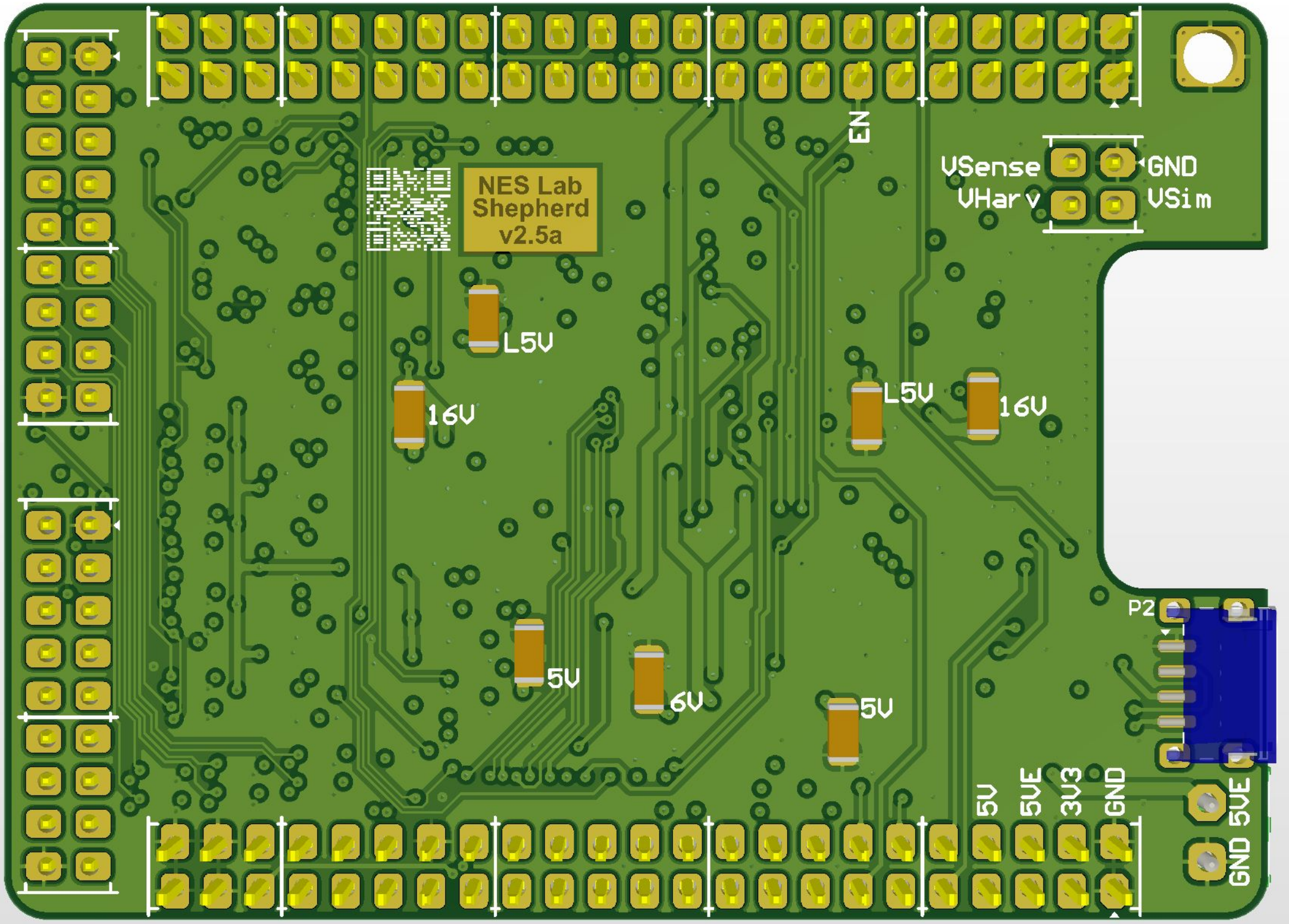
TPL5000 Watchdog behaviour:
- time-delay is configured via resistor (100ms .. 2h)
- "wake" is triggered for 31 ms on timer-match -> LowPass to 150 ms
- wake only reaches BB if 3V3_BB is at GND-Level (BB Shutdown)
- system has to confirm wake by triggering "done"
- if "done" is not triggered before next "wake" a reset occurs

R_Delay	T_Delay
057 kOhm	10 min
077 kOhm	20 min
092 kOhm	30 min
125 kOhm	60 min
150 kOhm	90 min
170 kOhm	120 min

A RTC (i.e. PCF2129 with Linux-Drivers) with alarm-timer and watchdog would be prefered, but both functions are only triggered ONCE without interaction. So if the BB gets woken but fails to boot there will never be a reset.

Title	Shepherd - Misc NES Lab / TU Dresden	
Size: A4	Number	Revision
Date: 9.17.2023		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Misc.SchDoc		Drawn By: Ingmar


P8
Harvest
P6
PRU0
PRU1
U6
U2
TP1
TP3
TP6
U8
U9
U7
U31
U30
U14
U35
U33
U32
U13
IO
EMU
U11
U36
U15
U12
U38
U18
U17
U21
HRV
EMU
U19
U16
U23
U40
U27
U28
U24
U26
U29
U25
U34
U37
U39
U41
PWR
L3V
10V
6V
L5V
5V
U20
U22
-6V
P3
J1
P9
P10
P11
A
B


NES Lab
Shepherd
v2.5a
EN
VSense
VHarv
GND
VSim
L5V
16V
L5V
16V
5V
6V
5V
P2
5V
5VE
3V3
GND
GND
5VE