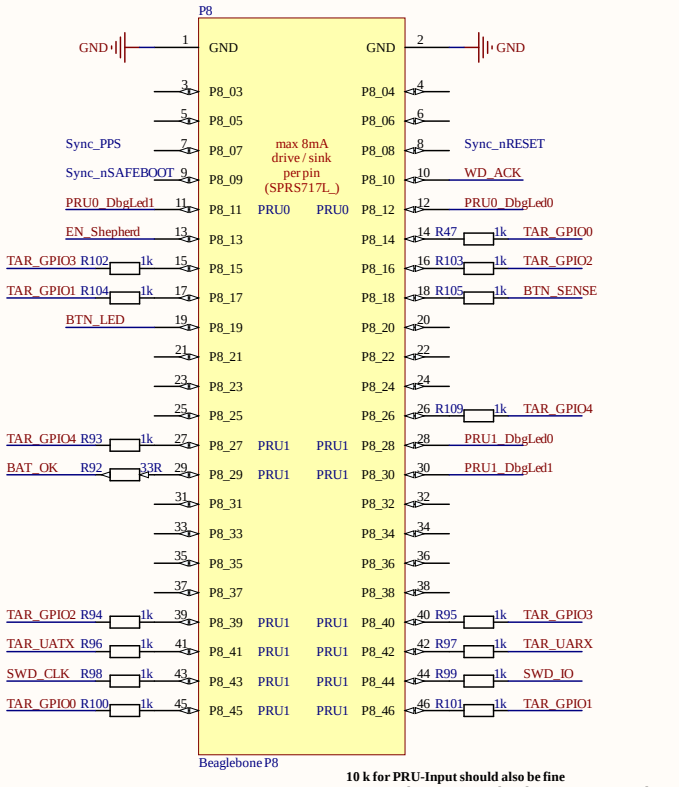
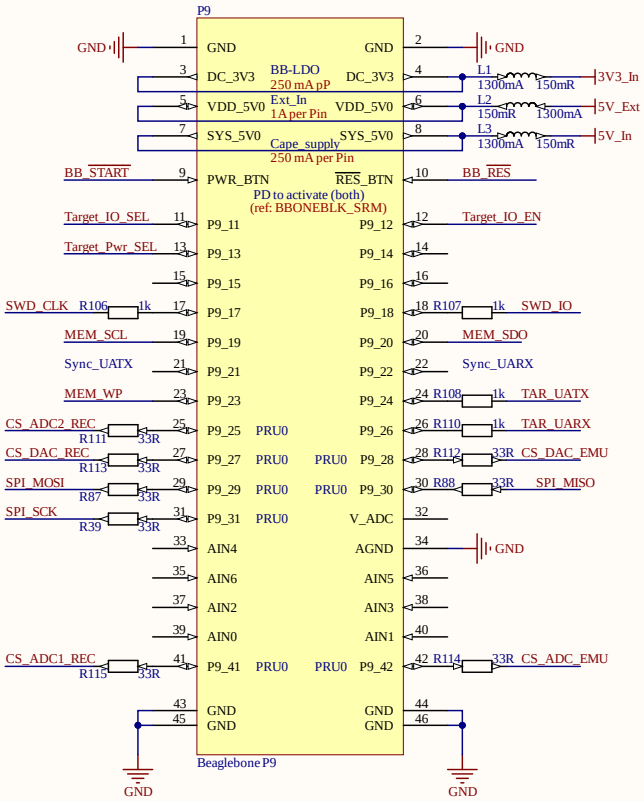
Beaglebone Pinheader P8



10 k for PRU-Input should also be fine
NOTE: order seems messed up, but ensures a proper boot
P8-31:46 are also responsible for bootconfig of beaglebone

Beaglebone Pinheader P9



Pin-Mapping is documented in

concept_hw_beagle_pinout.xls

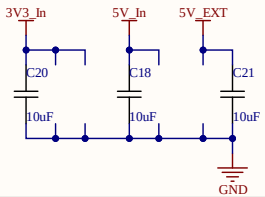
target_io is doubled for pru-timestamping - pru-io is not flexible, no dir-change during runtime

Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V
PWR_BTN	3.74V
nRES_BTN	0.15V

nSTART: BB_PCB has nothing discrete except switch to GND

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & switch to GND

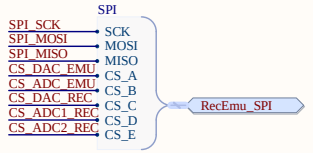


Calibration_Storage

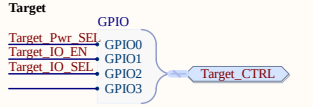
signal-direction is from Host point of view (if in doubt)

Sys_Watchdog

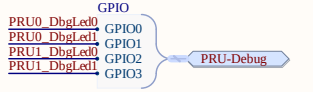
Emulator & Recorder



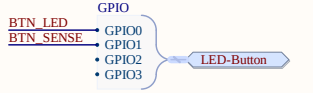
Target



PRU-Debug-Leds



External Button



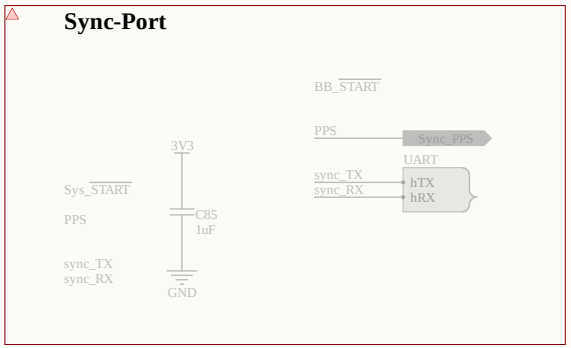
Title	Shepherd - Host Interface NES Lab / TU Dresden	
Size A4	Number	Revision
Date: 2.12.2021		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Host-Interface.SchDoc		Drawn By: Ingmar

SYNC-PORT (GPS, RF-Broadcast, Ext-Trigger, Sys_WakeUp)

GPS or external rf-trigger could also wake system by dedicated alarm-pulse

--> BB-Cape-System stays - so it moves to separate PCB

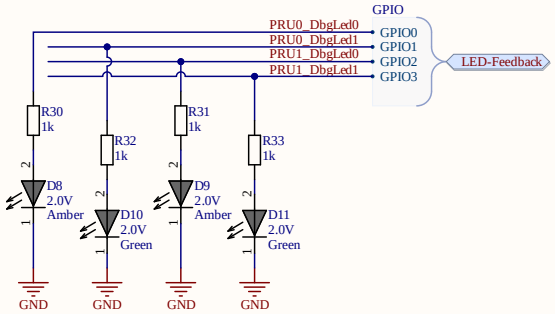
Sync-Port



TODO:
Separate into smaller Individual Schem

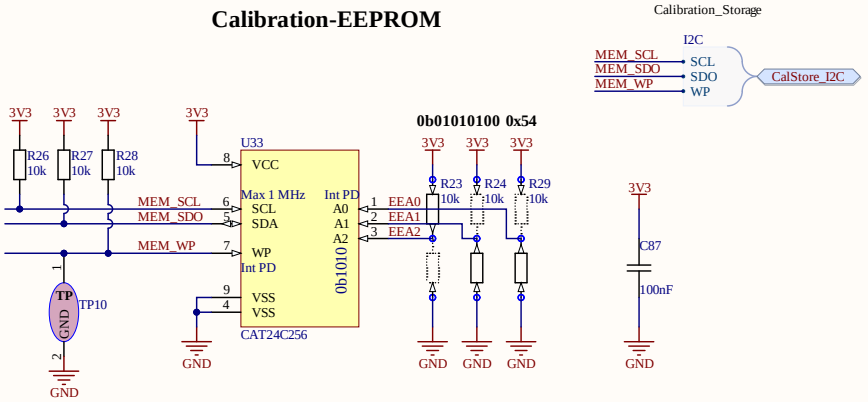
Possible Changes:
- LED Button could be designed with just 3 Leads, or even 2
- One LED per PRU is enough

PRU-LED-Feedback

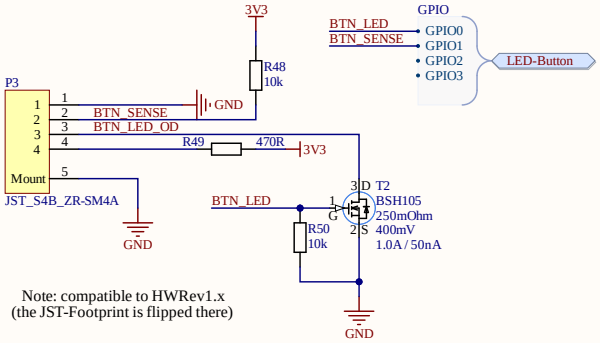


Calibration-EEPROM

Calibration_Storage



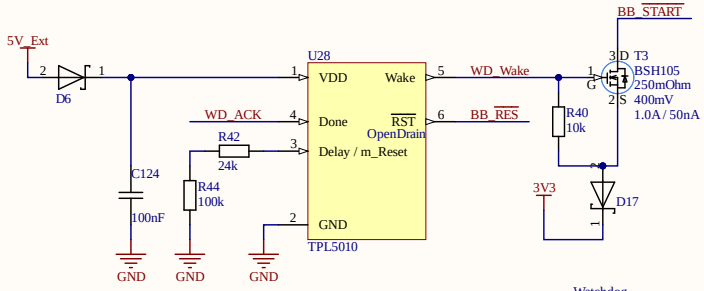
Local Control Button



Note: compatible to HWRev1.x
(the JST-Footprint is flipped there)

schematic changed to avoid internal voltages on cable

Watchdog



change 60 to 20 min: add a second 100k over first one

BB-Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V

nSTART: BB_PCB has nothing discrete except switch to GND
-> use 3V3 as Pull-Down to only get affected by wake-signal when BB is powered off

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & switch to GND

Watchdog - Advantages:
- nodes are in remote rooms, often without access
- Fallback if we can't control POE-Power of ports (most likely)
- with a WD the BB can shut down and be woken up periodically
- BB does not mind a wake-up-signal when already running
- routine: BB aks server for tasks, waits or goes to sleep again

TPL5000 Watchdog behaviour:
- time-delay is configured via resistor (100ms .. 2h)
- "wake" is triggered for 31 ms on timer-match
- system has to confirm wake by triggering "done"
- if "done" is not triggered before next "wake" a reset occurs

057 kOhm	10 min
077 kOhm	20 min
092 kOhm	30 min
125 kOhm	60 min
150 kOhm	90 min
170 kOhm	120 min

A RTC (i.e. PCF2129 with Linux-Drivers) with alarm-timer and watchdog would be prefered, but both functions are only triggered ONCE without interaction. So if the BB gets woken but fails to boot there will never be a reset.

Title	Shepherd - Misc NES Lab / TU Dresden	
Size A4	Number	Revision
Date: 2.12.2021	Sheet of shepherd_v2.PrjPcb	
File: C:\Users\..\Misc.SchDoc	Drawn By: Ingmar	

Routing-HINTS:
- SPI Lines need special care
- equalize length
- avoid long forks
- terminate data & clk if possible

U_Host-Interface
Host-Interface.SchDoc

EN_Shepherd
RecEmu_SPI
Target_CTRL
Target_UART
Target_SWD
Target_GPIO_A
Target_GPIO_B
Watchdog_CTRL
CalStore_I2C
PRU-Debug
LED-Button

U_PowerSupplies
PowerSupplies.SchDoc
EN_Power

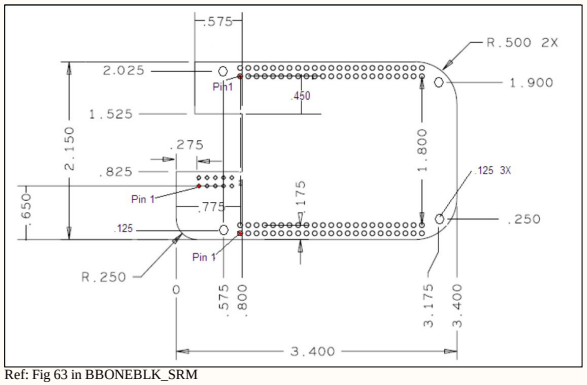
U_Recorder
Recorder.SchDoc
EN_REC
SPI

U_VEmulator
VEmulator.SchDoc
EN_EMU
SPI

M5
SMS-455Cover
M6
SMS-455Frame
M7
SMS-455Cover
M8
SMS-455Frame
1
GND

U_Targets
Targets.SchDoc
CTRL
UART
SWD
GPIO_A
GPIO_B

U_Misc
Misc.SchDoc
Watchdog_CTRL
CalStore_I2C
LED-Feedback
LED-Button



Ref: Fig 63 in BBONEBLK_SRM

PCB Manufacturing Constraints

- Size 54.1 x 75.2 mm, 4 Layer
- 0.25 mm Track Width
- 0.15 mm Copper Clearance
- 0.38 mm Edge Clearance
- 0.35 mm Toolsize / non plated Hole
- 0.25 mm Plated Hole (End-)Size
- 0.125 mm Annular Ring
- 2.54 mm milling radius
- Solder Paste Pads are optimized for a 90 - 110 um Stencil

Assembly (v2r1)

- 2 Variations, recorder / emulator are self-contained and optional
  - with Rec & Emu -> 276 parts, 42 unique
  - with Emu -> 219 parts, 39 unique
- Mech-15 contains Pick and Place Info
  - cross (+) marks origin of part,
  - chamfered edge and circle mark pad 1 of ICs
  - "C" marks cathode of diodes
- Mech-2 contains Top Part Designators
- smallest part 0402
- smallest pitch 0.5 mm, QFN
- only top layer populated

Manual Assembly
- Mech-13 contains info about non-reflow parts (8 items)

Misc

M9
LogoShepherd

M10
LayerWindow

FD1
Fiducial
FD2
Fiducial
FD3
Fiducial

1
Hole
M1
Mounting_Hole
1
Hole
M2
Mounting_Hole
1
Hole
M3
Mounting_Hole
M4 not populated
gives no access to underlaying Hole
GND

BOM-Additions

P1
BeagleBoneGreen

HDR
SOCKET
P6
P_HDR_2x11_2.54mm_LongPinSocket

HDR
SOCKET
P7
P_HDR_2x11_2.54mm_LongPinSocket

HDR
SOCKET
P10
P_HDR_2x12_2.54mm_Header

HDR
SOCKET
P11
P_HDR_2x12_2.54mm_Header

External-BOM

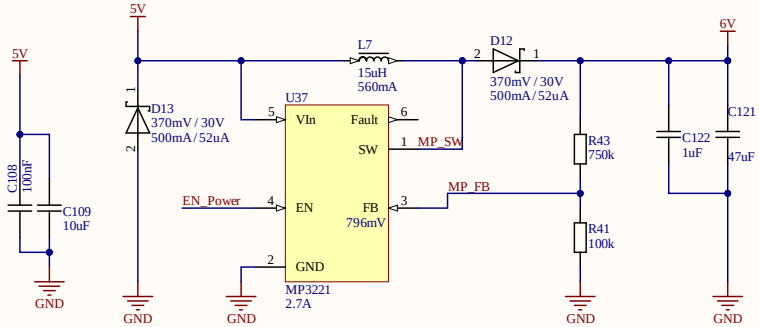
USB-Stick 256 GB
Ethernet Cables
POE-Adapter
uSD-Card (for flashing)

Calibration Resistors
1k-0603-0.05% 667-ERA-3ARW102V
100R-0603-0.05% 754-RG1608N-101-W-T1

Pinheader Connection BBone Variants
2x23 Header -> 77313-802-46LF 1.3 €
2x23 LongPinSocket
Samtec SSQ-123-23-G-D or 03-G-D 6 €
Major League SSHQ-123-D-10-G-LF 3 €
2x11 LongPinSocket & 2x12 Header
Samtec SSQ-111-03-G-D 3 €
Amphenol 10129381-924003BLF 0.4 €
-> third variant is the default one

Title	Shepherd - Overview NES Lab / TU Dresden		
Size A4	Number		Revision
Date:	2.12.2021	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\overview.SchDoc	Drawn By:	Ingmar

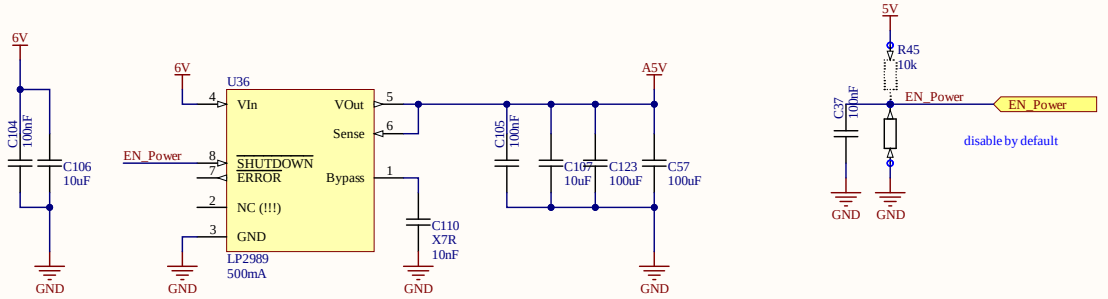
BoostConverter



Output-Ripple-Calculation:
I_out: 0.15;
V_out: 6.0;
V_fw: 0.37;
V_in: 5.0;
f_sw: 1.2e6;
C_out: 111e-6;
dV_out: I_out * (V_out + V_fw - V_in) / (f_sw * (V_out + V_fw) * C_out);
dV_out <= 240 uV

Inductor-Calculation
L: V_in * (V_out + V_fw - V_in) / (f_sw * (V_out + V_fw) * 0.3*I_out);
L 20 uH

UltraLowNoise LDO

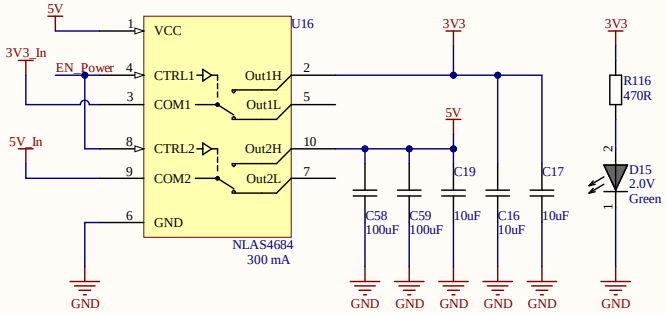


Consumption:
- Disabled < 2 mA
- Enabled 66 mA @ 5 V
- BB 390 mA during boot, 170 to 240 mA later

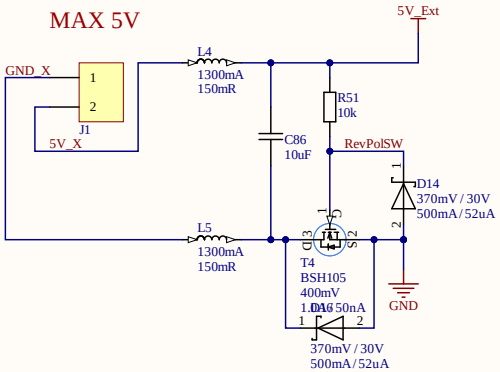
Main Voltages:

A5V	-> 5.000 V	Should be Spot On
6V	-> 6.77 V	[6.63; 6.90] V with 1% Res
10V	-> 9,73 V	[9.56; 9.90] V with 1% Res
-6V	-> -6 V,	[5.94; 6.06] V with 1% Res

Main Power Switch

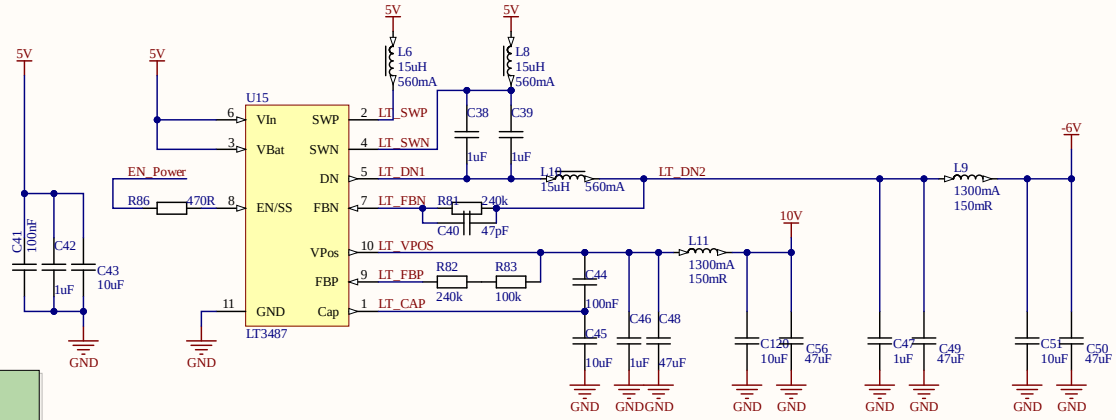


External Power In with OVP



internal MOSFET-Diode needs support

Boost & Inverter



R1=(Vp-1.23V)/25uA
R1=350.8 kOhm (10V)
340kOhm -> 9.73V @1%

R2=-Vn/25uA
R2=240 kOhm (-6V)

Regulator drives at least 50mA on both Outputs

Title	Shepherd - Power Supplies NES Lab / TU Dresden		
Size A4	Number		Revision
Date:	2.12.2021	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\PowerSupplies.SchDoc	Drawn By:	Ingmar

precision DAC

Emulate V_Cap of Converter

Current Sensing

Gain & precision ADC

Harvest V-Matching

OVP

```
# Signal-Propagation-Delay
DAC8562  7-10 us Settling, 0.75 V/us Slew
OPAx388  2 us Settling (0.01%), 5.0 V/us Slew rate
INA190     0.8 us Settling (0.001%), 35 V/us Slew rate
ADS8691  665 ns conversion, 335 ns acquisition

# Noise-Estimate
ADS8691:
- unipolar mode 0 .. 5.12V @ 18bit, LSB = 19.53 uV
- integral nonlin +- 2 LSB
- 90 dB SNR
AD8421:
- Inp. Voltage Noise 3.2 nV/sqrtHz
- Outp. Voltage Noise 60 nV / sqrtHz
OPA388 / OPA2388:
- Noise 7nV/sqrtHz, 100fA/sqrtHz
- no 1/f-Noise: 140 nVpp
DAC8562:
- noise density 90 nV / sqrtHz
- output noise 2.6 uVpp
- crosstalk 5 / 15uV (Ext / Int Reference)
- 16 bit, LSB = 76 uV

InAmpNoise Peak2Peak Voltage with 16kHz BW and variable
Input-Resistor
-> see maxima-sheet "OpAmpNoiseCalculation.wxmx"
InpRes          AD8421    AD8429
0.1 kOhm        2.9 uV    1.76 uV
1 kOhm          5.05 uV   4.72 uV
10 kOhm         14.0 uV   21.1 uV
100 kOhm        48 uV     167 uV

# Signal Ranges
DAC8562 -> 0 .. AVDD (max) ->
            default Gain=1 for VRefExt or 2 for VRefInt (modd
```

SPI: SCK, MOSI, MISO, CS_A, CS_B, CS_C, CS_D, CS_E, CS_DAC_REC, CS_ADC1_REC, CS_ADC2_REC

3V3 R11 10k — RST_rADC — EN_REC — C36 100nF — GND

R34 10k — C90 1nF — RC-Lowpass ~16 kHz — A5V — U34A OPA2388 — V_SenseBuf — TP9 — GND

U35 ADS8691: AIN+, AIN_GND, AVDD, DVDD, CS/CONVST, SCLK, SDI, SDO-0, ALARM/SDO-1/GPO, RVS, RST, REFIO, REFCAP, REFGND, AGND, DGND
1-Ch ADC 18bit; 1 us Acq+Conv; 1 MS/s; 1 MOhm AIn; 0.2 mV offset Error; 90 dB SNR; 50 MHz SPI
A5V 3V3 3V3 — R36 10k — CS_ADC1_REC — SCK — MOSI — MISO — RST_rADC — REFIO_rADC1 — REFCAP_rADC1 — C93 1uF — C94 10uF — C95 10uF — GND

R35 10k — RC-Lowpass ~16 kHz — C91 1nF — U34B OPA2388 — R37 10R — C92 100nF — GND

V_CapBuf — V_HARVEST — V_Sense — P2 HDR_2x2_2.54mm_header — will settle at vMax when unconnected

U32 DAC8562: AVDD, VOut_A, VOut_B, VRef_2V5, SPI SYNC, SPI SCLK, SPI DIN, CLR LDAC, GND, GND
2-Ch DAC 16bit; 7-10 us Settling; 0.75 V/us Slew; 0.1 nV-s Glitch; 90 nV/sqrtHz Noise Density; 2.6 uV p-p Output Noise; 40 mA I_short; 50 MHz SPI
3V3 R21 10k — A5V — CS_DAC_REC — SCK — MOSI — 3V3 R22 10k — CLR_rDAC — GND — C79 100nF — C80 1uF — GND

V_rCap — R38 1k — R12 10k — C64 10nF — RC-Lowpass ~1.6 kHz — D5 — 710mV / 100V 1A / 40nA — 5V

V_rHARV_N — R20 24k — RC-Lowpass ~6.6 kHz — C78 1nF — TP7 TP8 — GND GND — A5V — U27 OPA388 — R14 1M — R15 10k — GND

V_rSH_P — R13 250mW 0.1% 1R — V_rSH_N — T1 BSH105 410mW 400mV 1.0A / 50nA — GND

500 pA Max 1 — 500 pA Max 4 — U25A AD8421B — 100x Gain — V_rCurrentSense

10V — U25B AD8421B: Vs+, RG1, RG2, Ref, Vs- — R80 100R 0.1% — -6V — GND

TP6 — D7 2.0V Amber — GND GND — visual Feedback (max) 7mA@5V

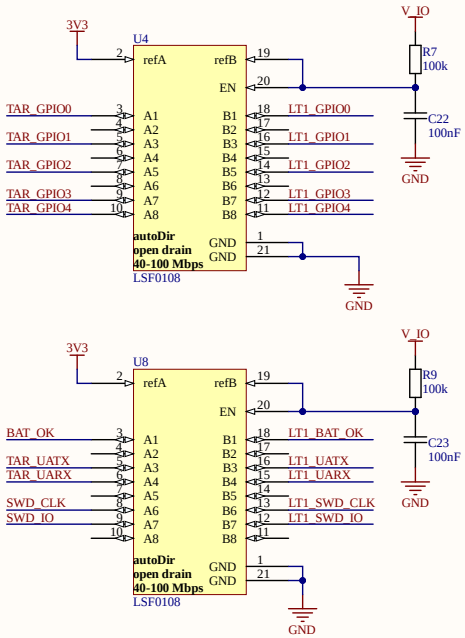
alternative: 1k + 3 LEDs to -6V would always show feedback

U26 ADS8691: AIN+, AIN_GND, AVDD, DVDD, CS/CONVST, SCLK, SDI, SDO-0, ALARM/SDO-1/GPO, RVS, RST, REFIO, REFCAP, REFGND, AGND, DGND
1-Ch ADC 18bit; 1 us Acq+Conv; 1 MS/s; 1 MOhm AIn; 0.2 mV offset Error; 90 dB SNR; 50 MHz SPI
A5V 3V3 3V3 — R19 10k — CS_ADC2_REC — SCK — MOSI — MISO — RST_rADC — REFIO_rADC2 — REFCAP_rADC2 — C65 1uF — C66 10uF — C67 10uF — GND

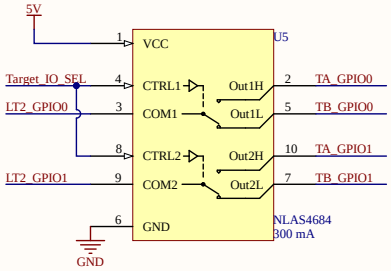
DAC: A5V — C82 1uF — C81 100nF — GND
OPA288: A5V — C83 100nF — C84 1uF — GND
OPA2388: A5V — C96 100nF — C97 1uF — GND
AD8421: 10V — C102 100nF — C103 1uF — GND; -6V — C68 100nF — C69 1uF — GND
Upper ADC: 3V3 — C98 100nF — C99 1uF — A5V — C100 100nF — C101 1uF — GND
Lower ADC: 3V3 — C70 100nF — C71 1uF — A5V — C72 100nF — C73 1uF — GND

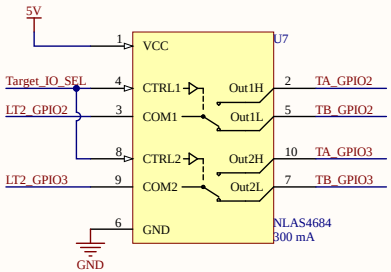
Title	Shepherd - Recorder NES Lab / TU Dresden	
Size: A3	Number	Revision
Date: 2.12.2021	Sheet of shepherd_v2.PrjPcb	
File: C:\Users\..\Recorder.SchDoc	Drawn By: Kai	

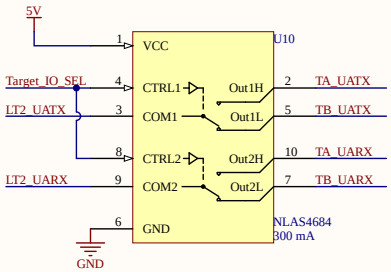
Level Translators

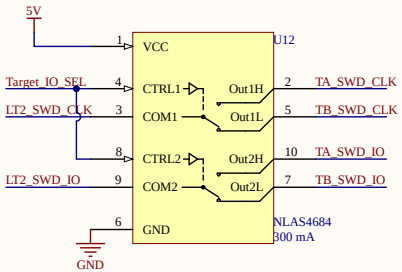


Signal Switches



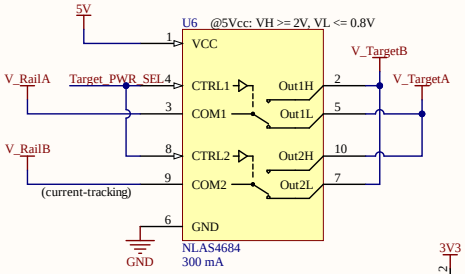


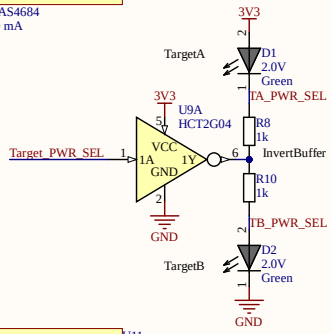


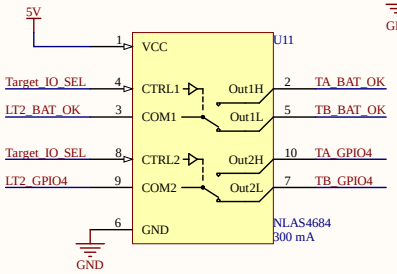


Power Switches

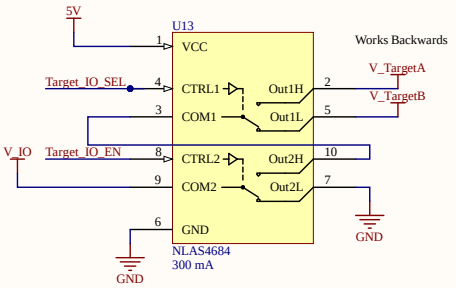
SEL TarA TarB
0 VA VB
1 VB VA
only VB has current-tracking
-> so SEL=1 enables tracking of Target A

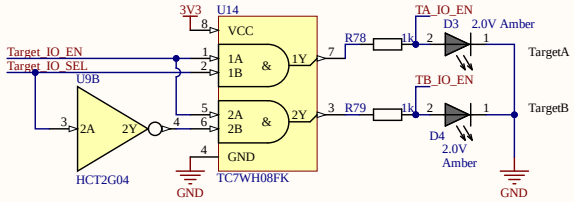




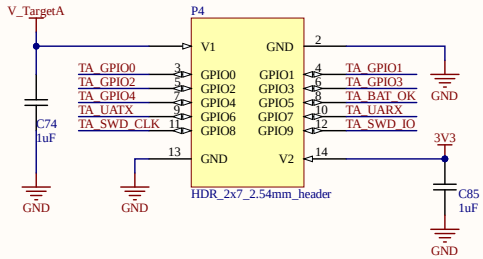


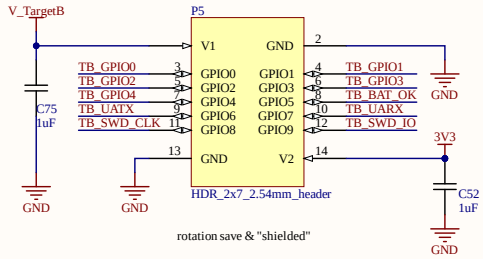
Switch Translator-Power





Target Ports





rotation save & "shielded"

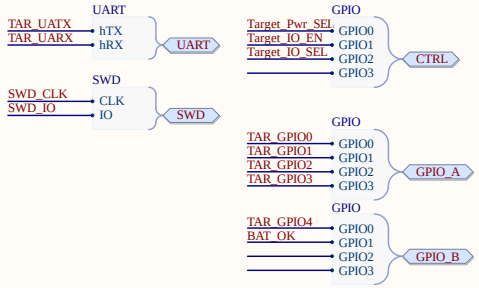
Programming-HINTS:
- Equalize DACs before switching
- unused GPIO should be switched to Input (target and bbone)
- level translators can be switched to other target for low leakage

Leakage Analysis (max per Pin):
NLAS4684 1-2 nA
NXS0101 1 uA
LSF010x 1-5 uA

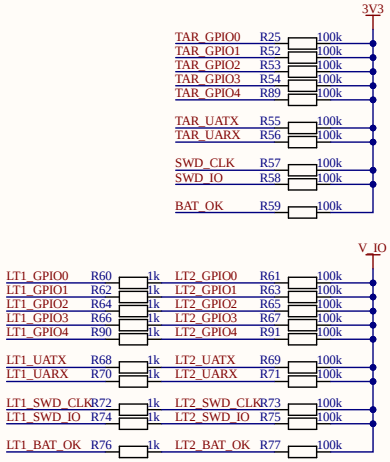
Possible BiDir Level Translation:
TXB -> needs relativly high driving current
TXS -> has internal PU, but relies on VRef-Relation
LSF -> only conducts on lowside, needs external PU
ICs from TI seem to always need special VRef-Relation
Nexperia ICs are new and on order (but offer better specs)

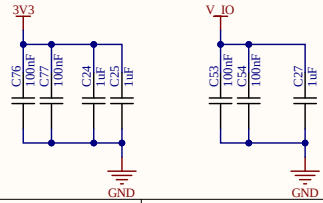
Max Current:
Target Switches 300mA
3V3 (unmonitored) 250mA
V_Target -> OPA#388 VoltageBuffers source 30-60mA, current measurement up to 50mA

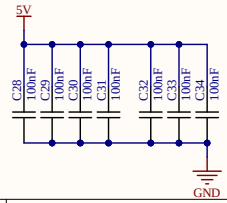
Programming Target:
SWD -> nRF52, STM32L4
SBW -> MSP430, MSP432, CC430
SBW-TDIO, -TCK (nRST/NMI)

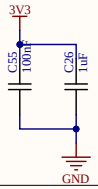


Current Limit & PU









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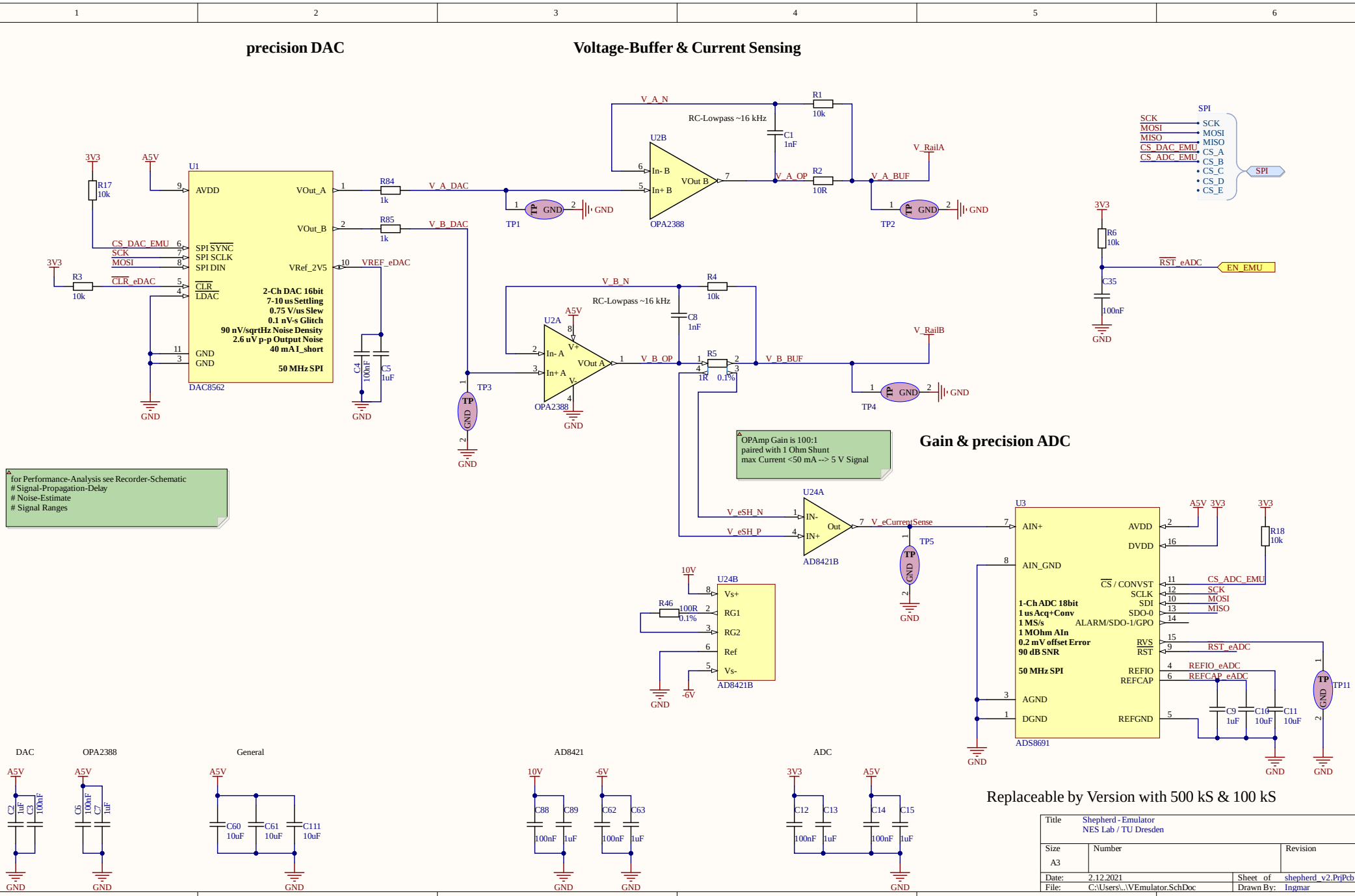
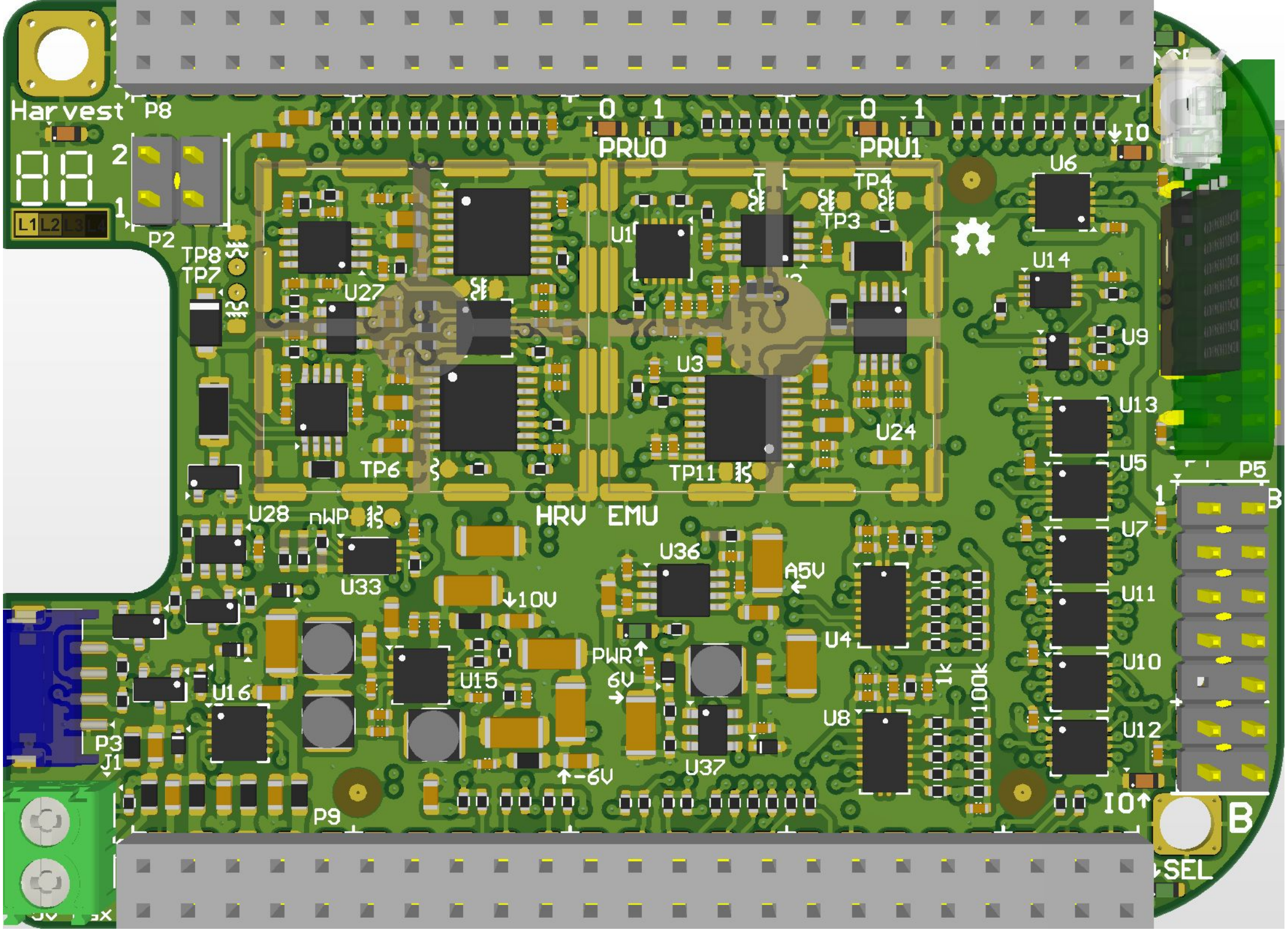
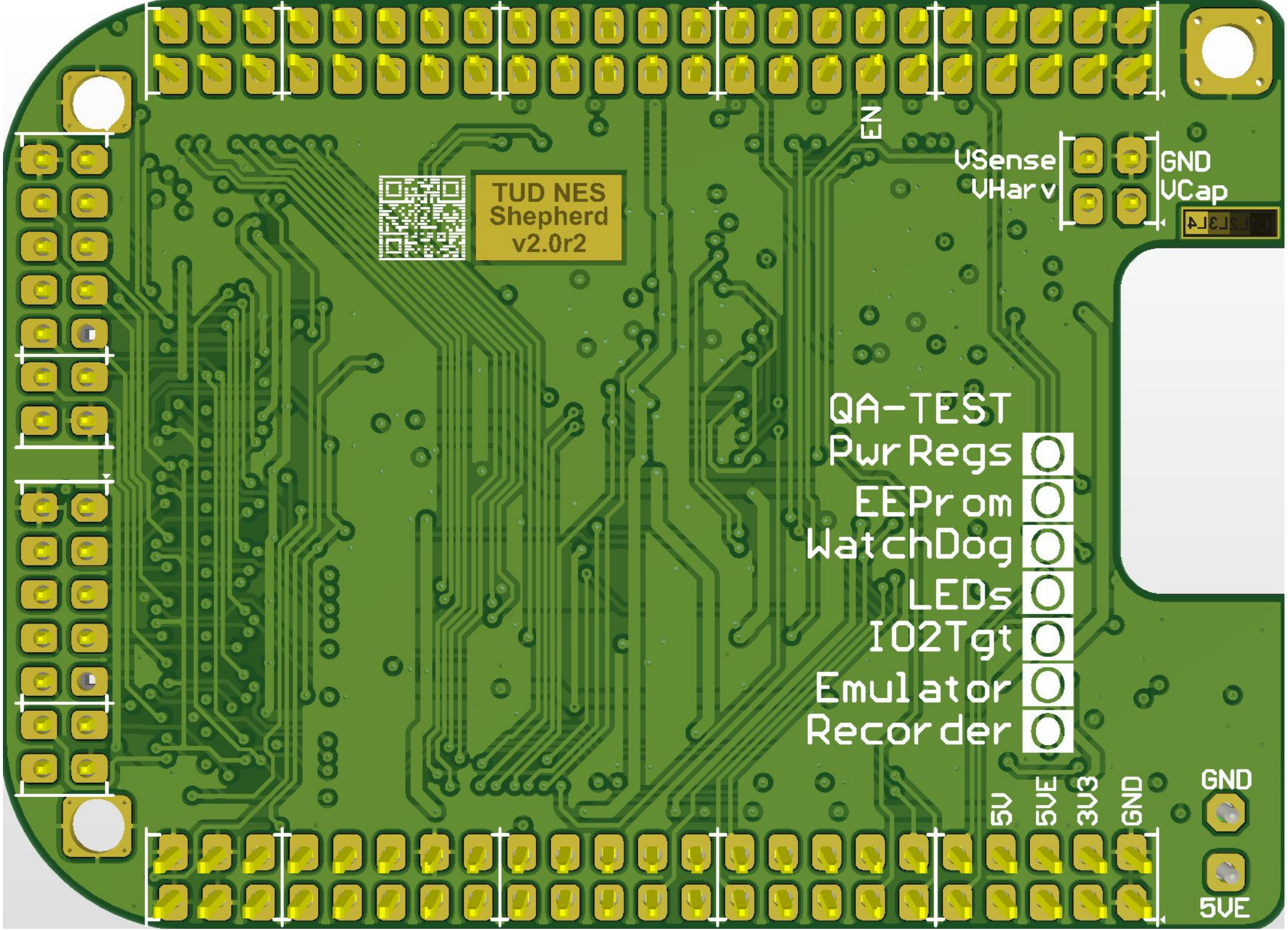
Size A3	Number	Revision
Date: 2.12.2021	Sheet of shepherd_v2.PrjPcb	
File: C:\Users\..\Targets.SchDoc	Drawn By: Ingmar	


precision DAC
Voltage-Buffer & Current Sensing
Gain & precision ADC
U1
DAC8562
2-Ch DAC 16bit
7-10 us Settling
0.75 V/us Slew
0.1 nV-s Glitch
90 nV/sqrtHz Noise Density
2.6 uV p-p Output Noise
40 mA I_short
50 MHz SPI
U2B
OPA2388
U2A
OPA2388
RC-Lowpass ~16 kHz
RC-Lowpass ~16 kHz
U24A
AD8421B
U24B
AD8421B
U3
ADS8691
1-Ch ADC 18bit
1 us Acq+Conv
1 MS/s
1 MOhm AIn
0.2 mV offset Error
90 dB SNR
50 MHz SPI
OPAmp Gain is 100:1
paired with 1 Ohm Shunt
max Current <50 mA --> 5 V Signal
for Performance-Analysis see Recorder-Schematic
Signal-Propagation-Delay
Noise-Estimate
Signal Ranges
SPI
DAC
OPA2388
General
AD8421
ADC
Replaceable by Version with 500 kS & 100 kS
Title
Shepherd - Emulator
NES Lab / TU Dresden
Size
A3
Number
Revision
Date: 2.12.2021
Sheet of
shepherd_v2.PrjPcb
File: C:\Users\..\VEmulator.SchDoc
Drawn By: Ingmar


Harvest
P8
P2
TP8
TP7
U27
U1
TP4
TP3
U6
U14
U9
U3
U24
U13
U5
U7
U11
U10
U12
P5
TP6
TP11
HRV EMU
U28
nWP
U33
U36
A5V
10V
PWR
6V
U15
U16
U4
U8
1k
100k
P3
J1
P9
-6V
U37
PRU0
PRU1
I0
I0
B
SEL


TUD NES
Shepherd
v2.0r2
EN
VSense
VHarv
GND
VCap
QA-TEST
PwrRegs
EEProm
WatchDog
LEDs
I02Tgt
Emulator
Recorder
5V
5VE
3V3
GND
GND
5VE