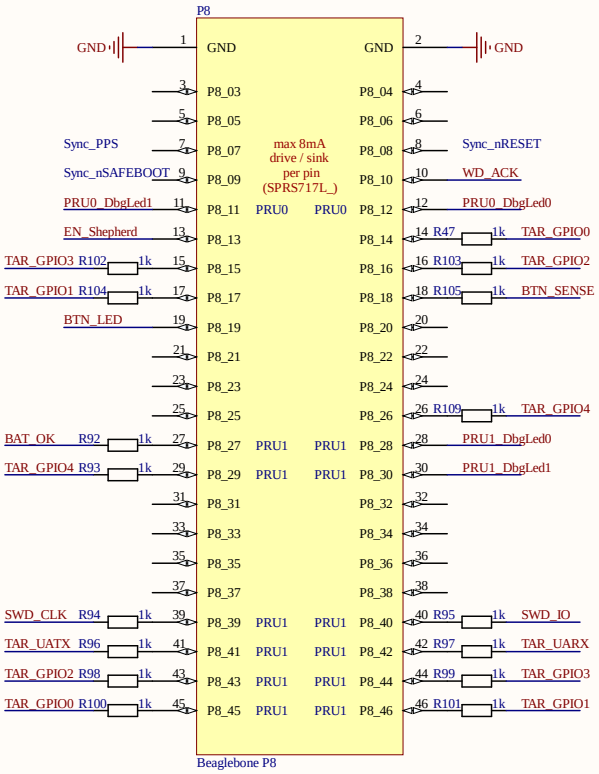
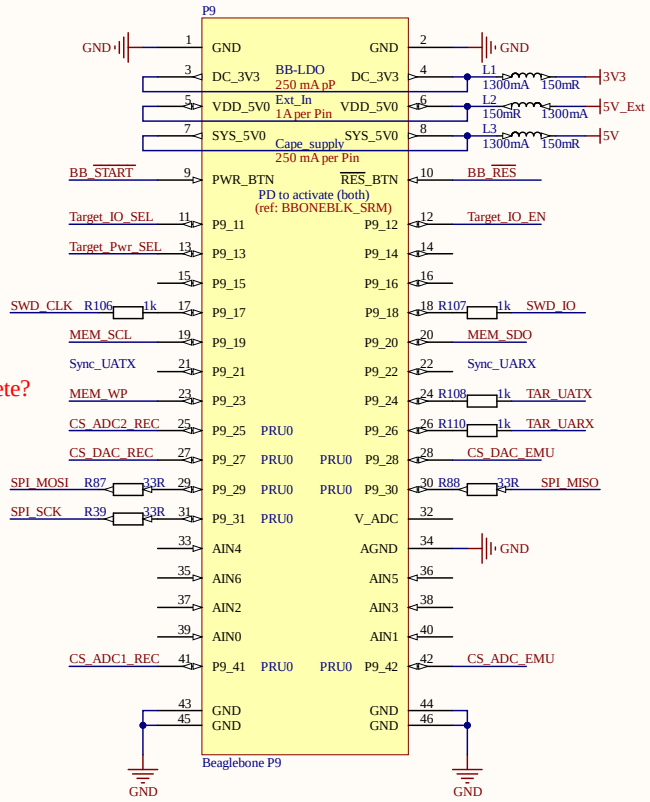
Beaglebone Pinheader P8



Beaglebone Pinheader P9



delete?

Pin-Mapping is documented in

concept_hw_beagle_pinout.xls

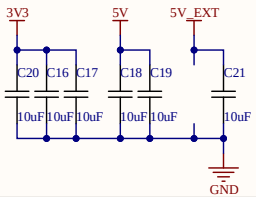
target_io is doubled for pru-timestamping - pru-io is not flexible, no dir-change during runtime

Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V
PWR_BTN	3.74V
nRES_BTN	0.15V

nSTART: BB_PCB has nothing discrete except switch to GND

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & switch to GND



Calibration_Storage
I2C
MEM_SCL, MEM_SDO, MEM_WP → SCL, SDO, WP → CalStore_I2C

signal-direction is from Host point of view (if in doubt)

Sys_Watchdog
Watchdog
BB_START, BB_RES, WD_ACK → Sys_WAKE, Sys_RESET, WD_ACK, WD_RST → Watchdog_CTRL

Emulator & Recorder
SPI
SPI_SCK, SPI_MOSI, SPI_MISO, CS_DAC_EMU, CS_ADC_EMU, CS_DAC_REC, CS_ADC1_REC, CS_ADC2_REC → SCK, MOSI, MISO, CS_A, CS_B, CS_C, CS_D, CS_E → RecEmu_SPI

EN_Shepherd → EN_Shepherd

Target
GPIO
Target_Pwr_SEL, Target_IO_EN, Target_IO_SEL → GPIO0, GPIO1, GPIO2, GPIO3 → Target_CTRL

GPIO
TAR_GPIO0, TAR_GPIO1, TAR_GPIO2, TAR_GPIO3 → GPIO0, GPIO1, GPIO2, GPIO3 → Target_GPIO_A

GPIO
TAR_GPIO4, BAT_OK → GPIO0, GPIO1, GPIO2, GPIO3 → Target_GPIO_B

UART
TAR_UATX, TAR_UARX → hTX, hRX → Target_UART

SWD
SWD_CLK, SWD_IO → CLK, IO → Target_SWD

PRU-Debug-Leds
GPIO
PRU0_DbgLed0, PRU0_DbgLed1, PRU1_DbgLed0, PRU1_DbgLed1 → GPIO0, GPIO1, GPIO2, GPIO3 → PRU-Debug

External Button
GPIO
BTN_LED, BTN_SENSE → GPIO0, GPIO1, GPIO2, GPIO3 → LED-Button

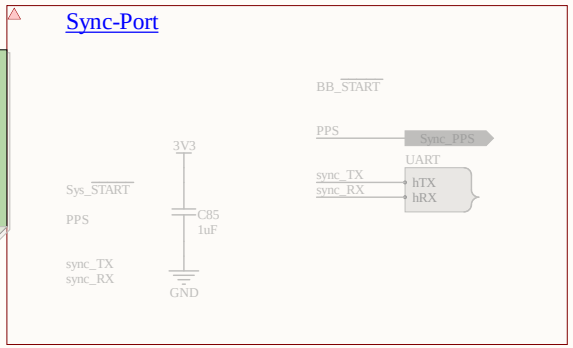
Title	Shepherd - Host Interface NES Lab / TU Dresden	
Size: A4	Number	Revision
Date: 12.17.2020	Sheet of	shepherd_v2.PrjPcb
File: C:\Users\..\Host-Interface.SchDoc	Drawn By:	Ingmar

Sync-Port

SYNC-PORT (GPS, RF-Broadcast, Ext-Trigger, Sys_WakeUp)

GPS or external rf-trigger could also wake system by dedicated alarm-pulse

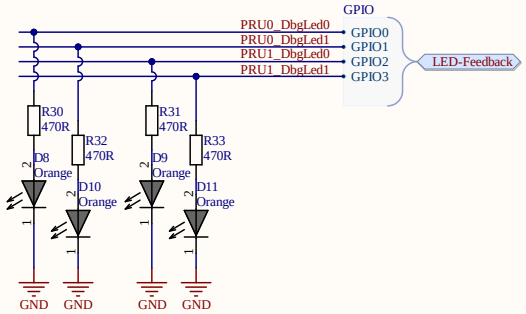
--> BB-Cape-System stays - so it moves to separate PCB



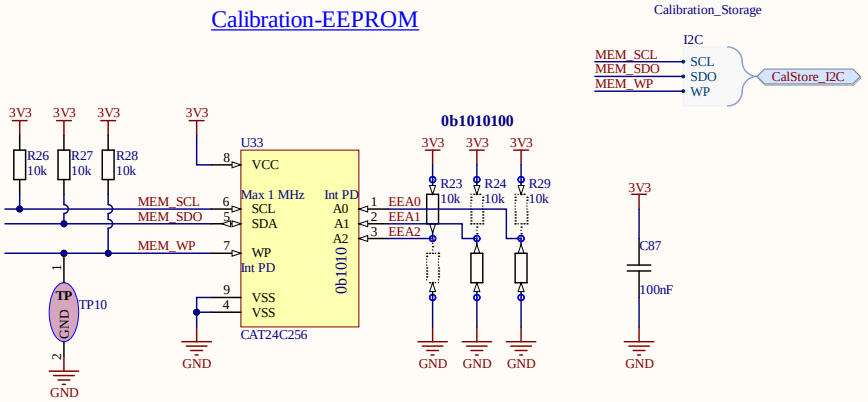
TODO:
Separate into smaller Individual Schem

Possible Changes:
- LED Button could be designed with just 3 Leads, or even 2

PRU-LED-Feedback



Calibration-EEPROM



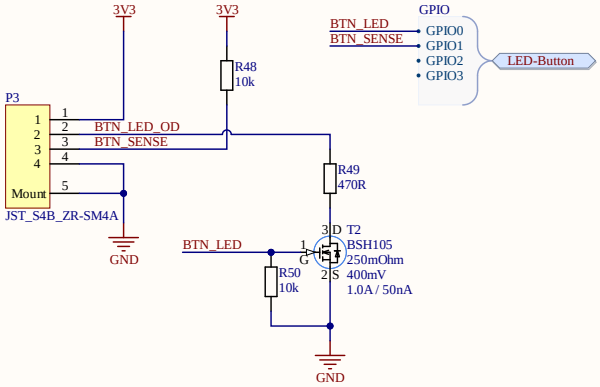
Watchdog - Advantages :
- nodes are in remote rooms, often without access
- Fallback if we can't control POE-Power of ports (most likely)
- with a WD the BB can shut down and be woken up periodically
- BB does not mind a wake-up-signal when already running
- routine: BB aks server for tasks, waits or goes to sleep again

TPL5000 Watchdog behaviour:
- time-delay is configured via resistor (100ms .. 2h)
- "wake" is triggered for 31 ms on timer-match
- system has to confirm wake by triggering "done"
- if "done" is not triggered before next "wake" a reset occurs

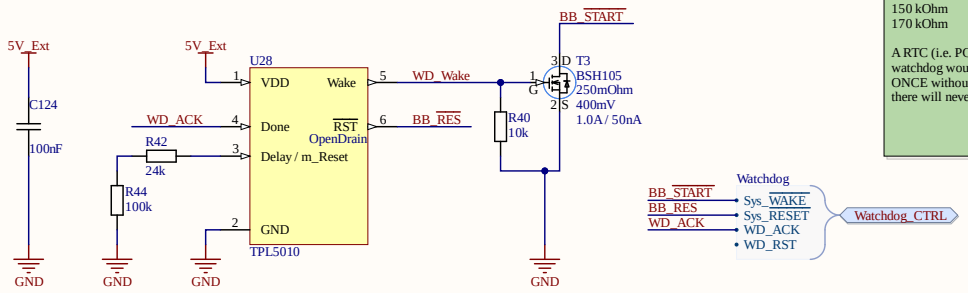
125 kOhm	60 min
150 kOhm	90 min
170 kOhm	120 min

A RTC (i.e. PCF2129 with Linux-Drivers) with alarm-timer and watchdog would be prefered, but both functions are only triggered ONCE without interaction. So if the BB gets woken but fails to boot there will never be a reset.

Local Control Button



Watchdog



Title	Shepherd - Misc NES Lab / TU Dresden		
Size A4	Number		Revision
Date:	12.17.2020	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\Misc.SchDoc	Drawn By:	Ingmar

Routing-HINTS:
- SPI Lines need special care
- equalize length
- avoid long forks
- terminate data & clk if possible

U_Host-Interface
Host-Interface.SchDoc

U_PowerSupplies
PowerSupplies.SchDoc

EN_Shepherd → EN_Power

U_Recorder
Recorder.SchDoc

RecEmu_SPI → EN_REC, SPI

U_VEmulator
VEmulator.SchDoc

EN_EMU, SPI

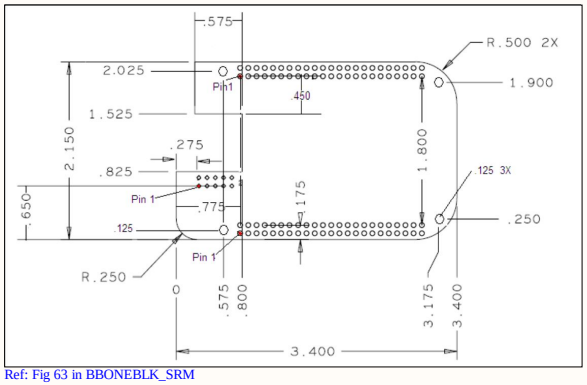
M5 SMS-455Cover
M6 SMS-455Frame
M7 SMS-455Cover
M8 SMS-455Frame
1 GND 1 GND
GND

U_Targets
Targets.SchDoc

Target_CTRL → CTRL
Target_UART → UART
Target_SWD → SWD
Target_GPIO_A → GPIO_A
Target_GPIO_B → GPIO_B

U_Misc
Misc.SchDoc

Watchdog_CTRL → Watchdog_CTRL
CalStore_I2C → CalStore_I2C
PRU-Debug → LED-Feedback
LED-Button → LED-Button



Ref: Fig 63 in BBONEBLK_SRM

Misc

M9 LogoShepherd
M10 LayerWindow

FD1 Fiducial
FD2 Fiducial
FD3 Fiducial

1 Hole M1 Mounting_Hole
1 Hole M2 Mounting_Hole
1 Hole M3 Mounting_Hole
M4 not populated
gives access to underlaying Hole
GND

BOM-Additions

P1 BeagleBoneGreen
HDR SOCKET P6 P_HDR_2x11_2.54mm_LongPinSocket
HDR SOCKET P7 P_HDR_2x11_2.54mm_LongPinSocket
HDR SOCKET P10 P_HDR_2x12_2.54mm_Header
HDR SOCKET P11 P_HDR_2x12_2.54mm_Header

PCB Manufacturing Constraints

- Size 54.1 x 75.2 mm, 4 Layer
- 0.25 mm Track Width
- 0.15 mm Copper Clearance
- 0.38 mm Edge Clearance
- 0.35 mm Toolsize / non plated Hole
- 0.25 mm Plated Hole (End-)Size
- 0.125 mm Annular Ring
- 2.54 mm milling radius
- Solder Paste Pads are optimized for a 130 - 150 um Stencil

Assembly (v2r1)

- 2 Variations, recorder / emulator are self-contained and optional
  - with Rec & Emu -> 276 parts, 42 unique
  - with Emu -> 219 parts, 39 unique
- Mech-15 contains Pick and Place Info
  - cross (+) marks origin of part,
  - chamfered edge and circle mark pad 1 of ICs
  - "C" marks cathode of diodes
- Mech-2 contains Top Part Designators
- smallest part 0402
- smallest pitch 0.5 mm, QFN
- only top layer populated

Manual Assembly
- Mech-13 contains info about non-reflow parts (8 items)

External-BOM

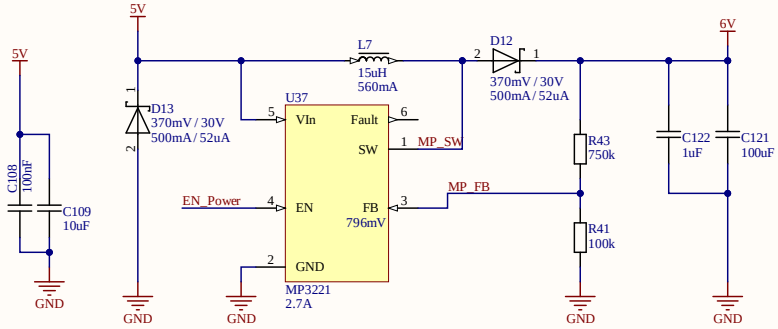
USB-Stick 256 GB
Ethernet Cables
POE-Adapter
uSD-Card (for flashing)

Calibration Resistors
1k-0603-0.05%
667-ERA-3ARW102V
100R-0603-0.05%
754-RG1608N-101-W-T1

Pinheader Connection BBone Variants
2x23 Header -> 77313-802-46LF 1.3 €
2x23 LongPinSocket
Samtec SSQ-123-23-G-D or 03-G-D 6 €
Major League SSHQ-123-D-10-G-LF 3 €
2x11 LongPinSocket & 2x12 Header
Samtec SSQ-111-03-G-D 3 €
Amphenol 10129381-924003BLF 0.4 €
-> third variant is the default one

Title	Shepherd - Overview NES Lab / TU Dresden	
Size A4	Number	Revision
Date: 12.17.2020		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\overview.SchDoc		Drawn By: Ingmar

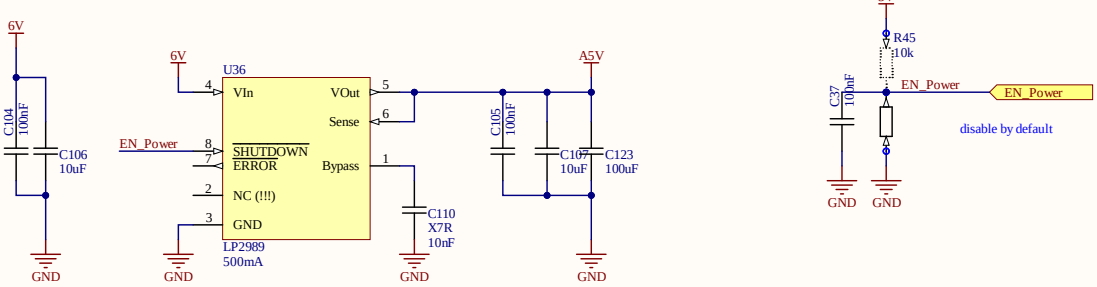
BoostConverter



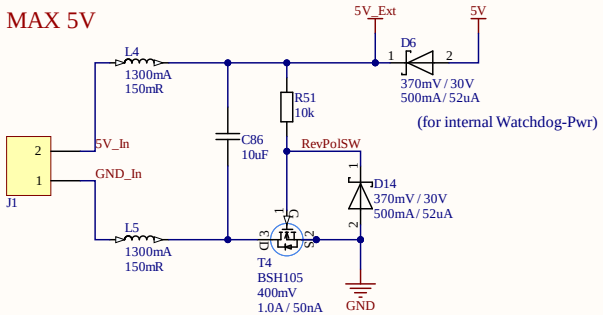
Output-Ripple-Calculation:
I_out: 0.15;
V_out: 6.0;
V_fw: 0.37;
V_in: 5.0;
f_sw: 1.2e6;
C_out: 111e-6;
dV_out: I_out * (V_out + V_fw - V_in) / (f_sw * (V_out + V_fw) * C_out);
dV_out <= 240 uV

Inductor-Calculation
L: V_in * (V_out + V_fw - V_in) / (f_sw * (V_out + V_fw) * 0.3*I_out);
L 20 uH

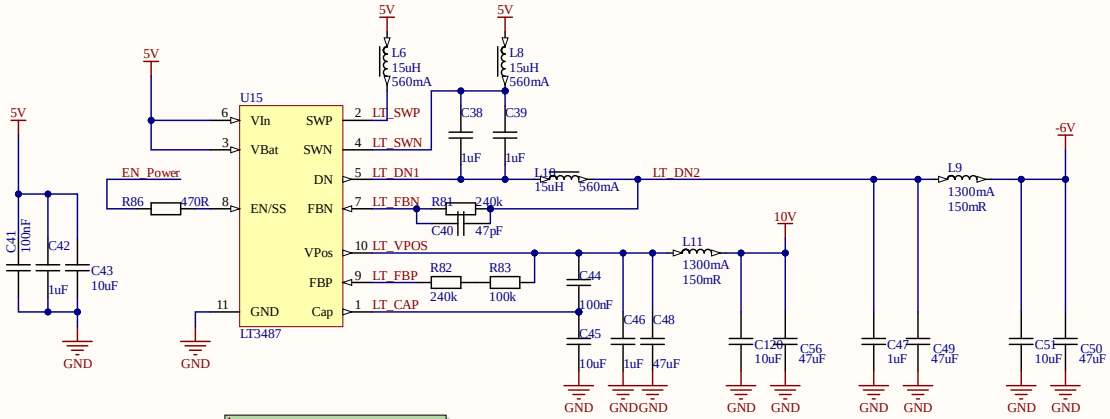
UltraLowNoise LDO



External Power In with OVP



Boost & Inverter



R1=(Vp-1.23V)/25uA
R1=350.8 kOhm (10V)
340kOhm -> 9.73V @1%

R2=-Vn/25uA
R2=240 kOhm (-6V)

Regulator drives at least 50mA on both Outputs

Title	Shepherd - Power Supplies NES Lab / TU Dresden	
Size A4	Number	Revision
Date: 12.17.2020	Sheet of	shepherd_v2.PrjPcb
File: C:\Users\..\PowerSupplies.SchDoc	Drawn By:	Ingmar

precision DAC

Emulate V_Cap of Converter

Current Sensing

Gain & precision ADC

Signal-Propagation-Delay
DAC8562 7-10 us Settling, 0.75 V/us Slew
OPAx388 2 us Settling (0.01%), 5.0 V/us Slew rate
INA190 0.8 us Settling (0.001%), 35 V/us Slew rate
ADS8691 665 ns conversion, 335 ns acquisition

Noise-Estimate
ADS8691:
- unipolar mode 0 .. 5.12V @ 18bit, LSB = 19.53 uV
- integral nonlin +- 2 LSB
- 90 dB SNR
AD8421:
- Inp. Voltage Noise 3.2 nV/sqrtHz
- Outp. Voltage Noise 60 nV / sqrtHz
OPA388 / OPA2388:
- Noise 7nV/sqrtHz, 100fA/sqrtHz
- no 1/f-Noise: 140 nVpp
DAC8562:
- noise density 90 nV / sqrtHz
- output noise 2.6 uVpp
- crosstalk 5 / 15uV (Ext / Int Reference)
- 16 bit, LSB = 76 uV

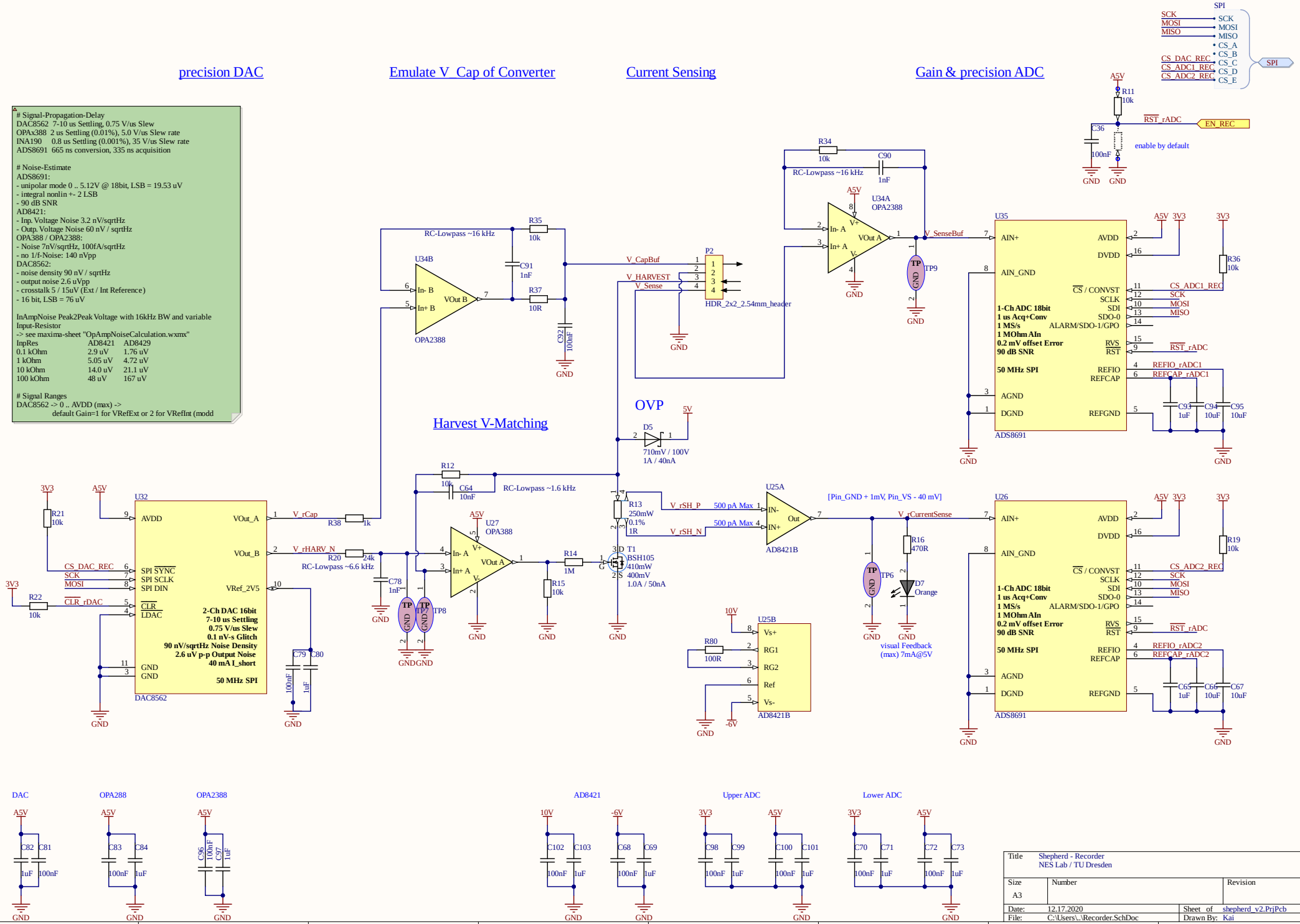
InAmpNoise Peak2Peak Voltage with 16kHz BW and variable Input-Resistor
-> see maxima-sheet "OpAmpNoiseCalculation.wxmx"

InpRes	AD8421	AD8429
0.1 kOhm	2.9 uV	1.76 uV
1 kOhm	5.05 uV	4.72 uV
10 kOhm	14.0 uV	21.1 uV
100 kOhm	48 uV	167 uV

Signal Ranges
DAC8562 -> 0 .. AVDD (max) ->
default Gain=1 for VRefExt or 2 for VRefInt (modd

Harvest V-Matching

OVP



DAC

OPA288

OPA2388

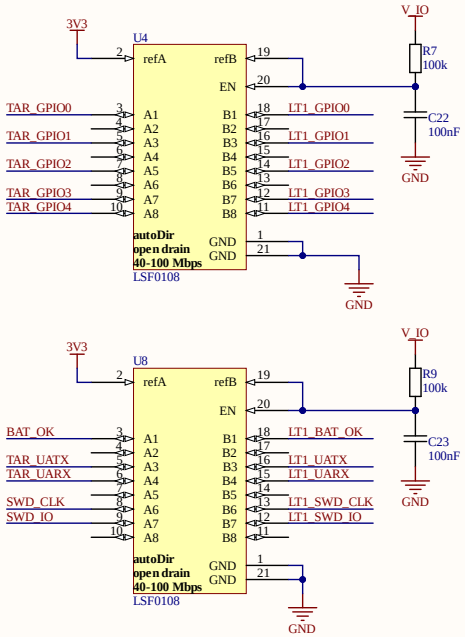
AD8421

Upper ADC

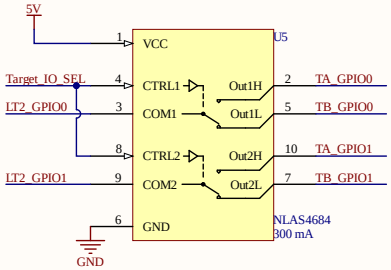
Lower ADC

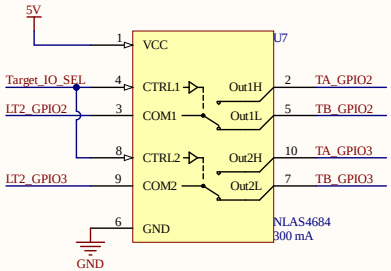
Title	Shepherd - Recorder NES Lab / TU Dresden	
Size A3	Number	Revision
Date: 12.17.2020	Sheet of	shepherd_v2.PrjPcb
File: C:\Users\..\Recorder.SchDoc	Drawn By:	Kai

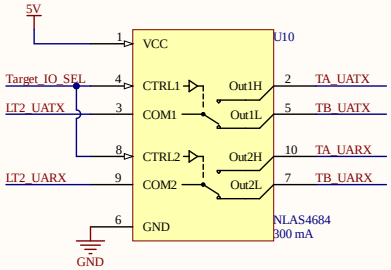
Level Translators

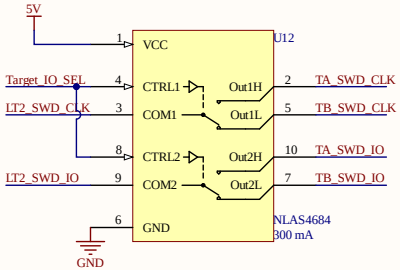


Signal Switches



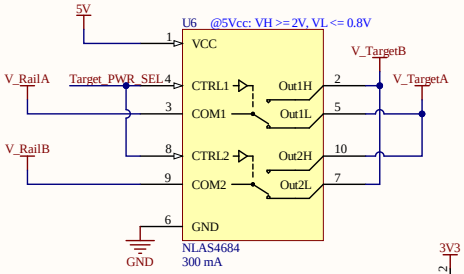


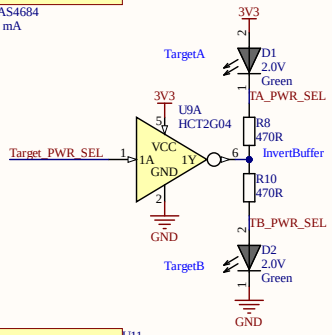


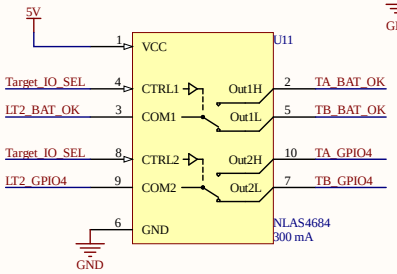


Power Switches

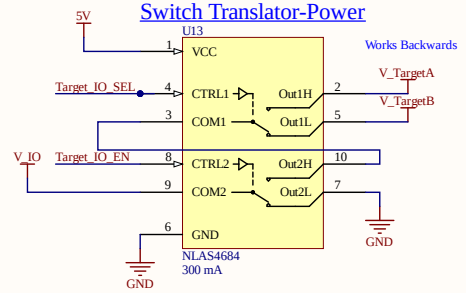
SEL TarA TarB
0 VA VB
1 VB VA
only VB has current-tracking
-> so SEL=1 enables tracking of Target A

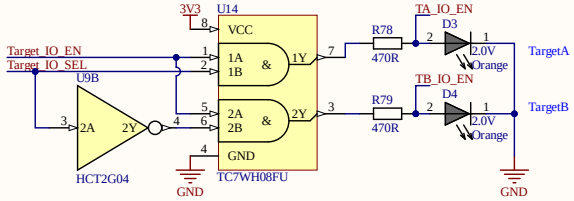




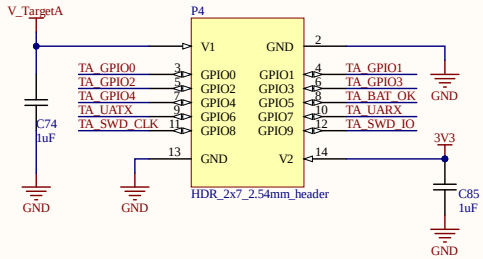


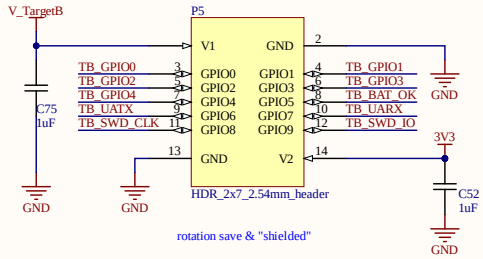
Switch Translator-Power





Target Ports





rotation save & "shielded"

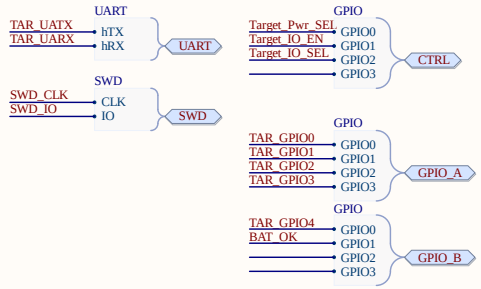
Programming-HINTS:
- Equalize DACs before switching
- unused GPIO should be switched to Input (target and bbone)
- level translators can be switched to other target for low leakage

Leakage Analysis (max per Pin):
NLAS4684 1-2 nA
NXS0101 1 uA
LSF010x 1-5 uA

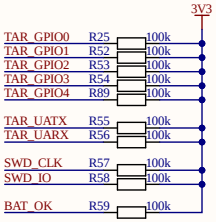
Possible BiDir Level Translation:
TXB -> needs relativly high driving current
TXS -> has internal PU, but relies on VRef-Relation
LSF -> only conducts on lowside, needs external PU
ICs from TI seem to always need special VRef-Relation
Nexperia ICs are new and on order (but offer better specs)

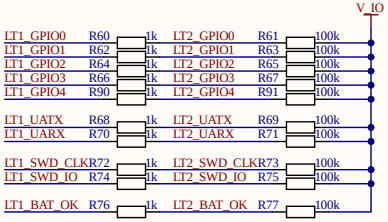
Max Current:
Target Switches 300mA
3V3 (unmonitored) 250mA
V_Target -> OPA#388 VoltageBuffers source 30-60mA, current measurement up to 50mA

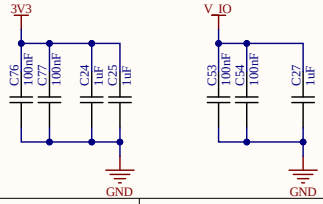
Programming Target:
SWD -> nRF52, STM32L4
SBW -> MSP430, MSP432, CC430
SBW-TDIO, -TCK (nRST/NMI)

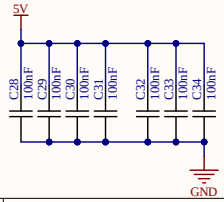


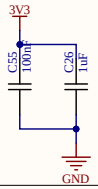
Current Limit & PU









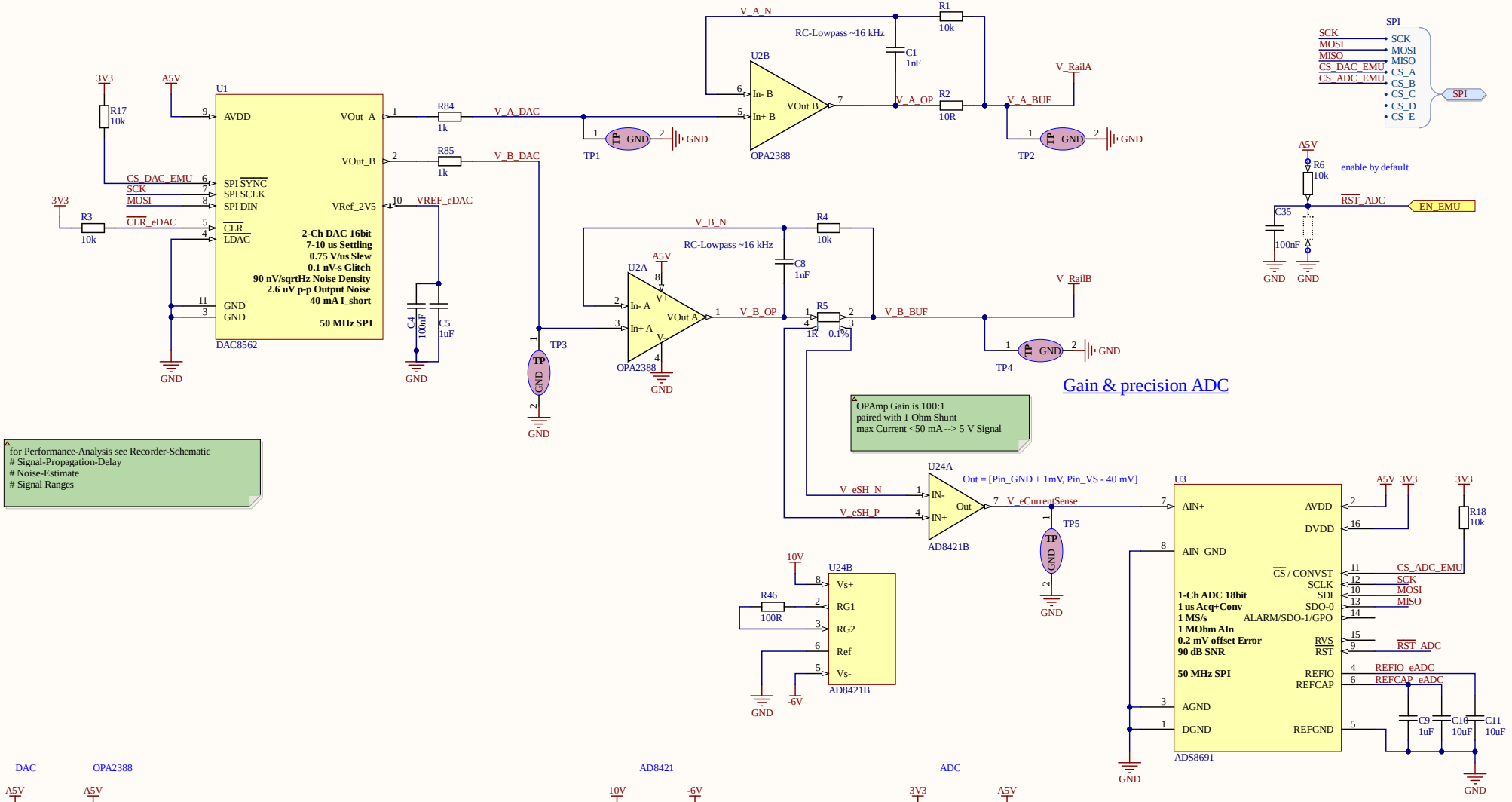


Title	Shepherd - Target Interface NES Lab / TU Dresden		
Size A3	Number		Revision
Date:	12.17.2020	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\Targets.SchDoc	Drawn By:	Ingmar

precision DAC

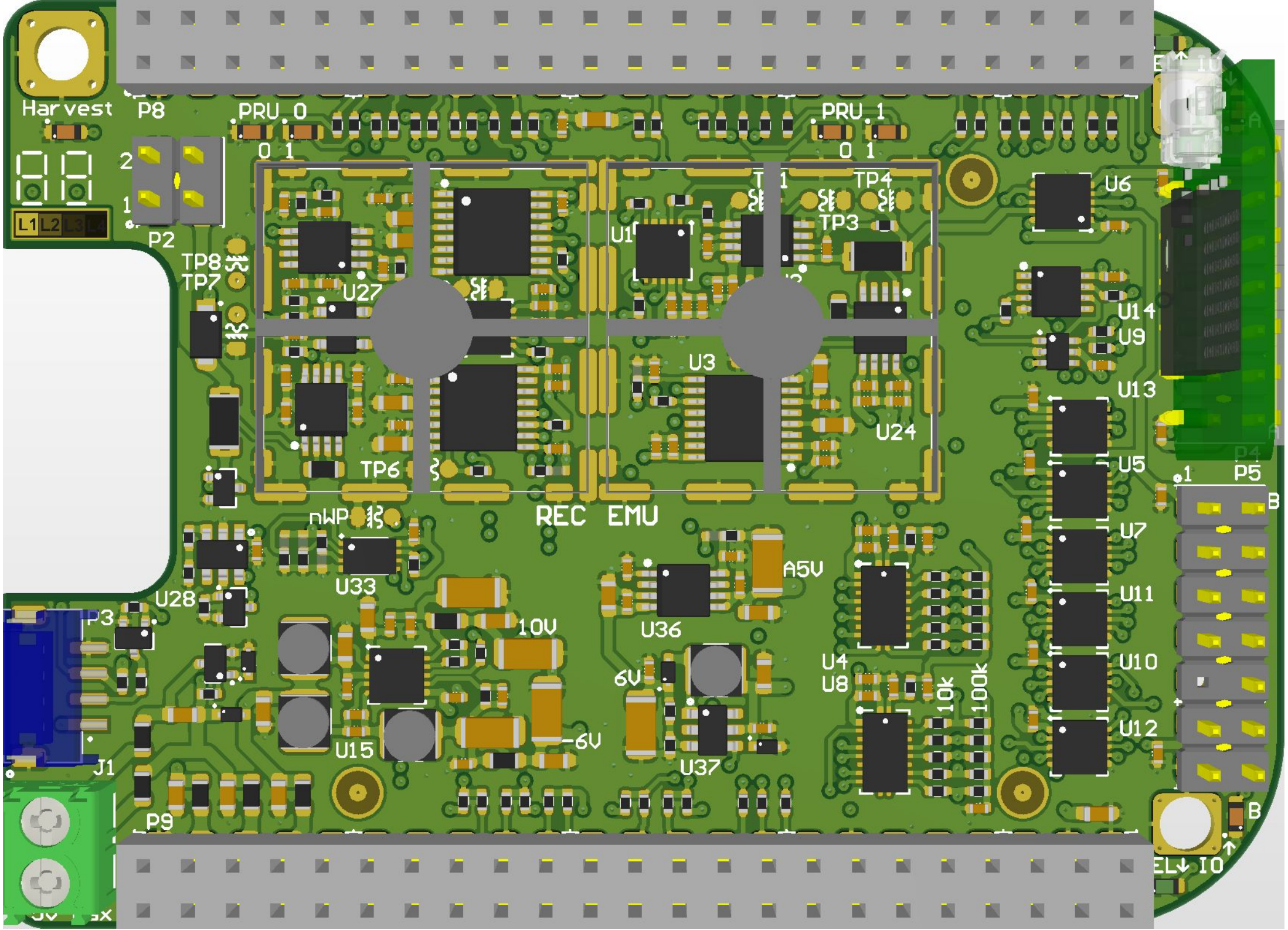
Voltage-Buffer & Current Sensing

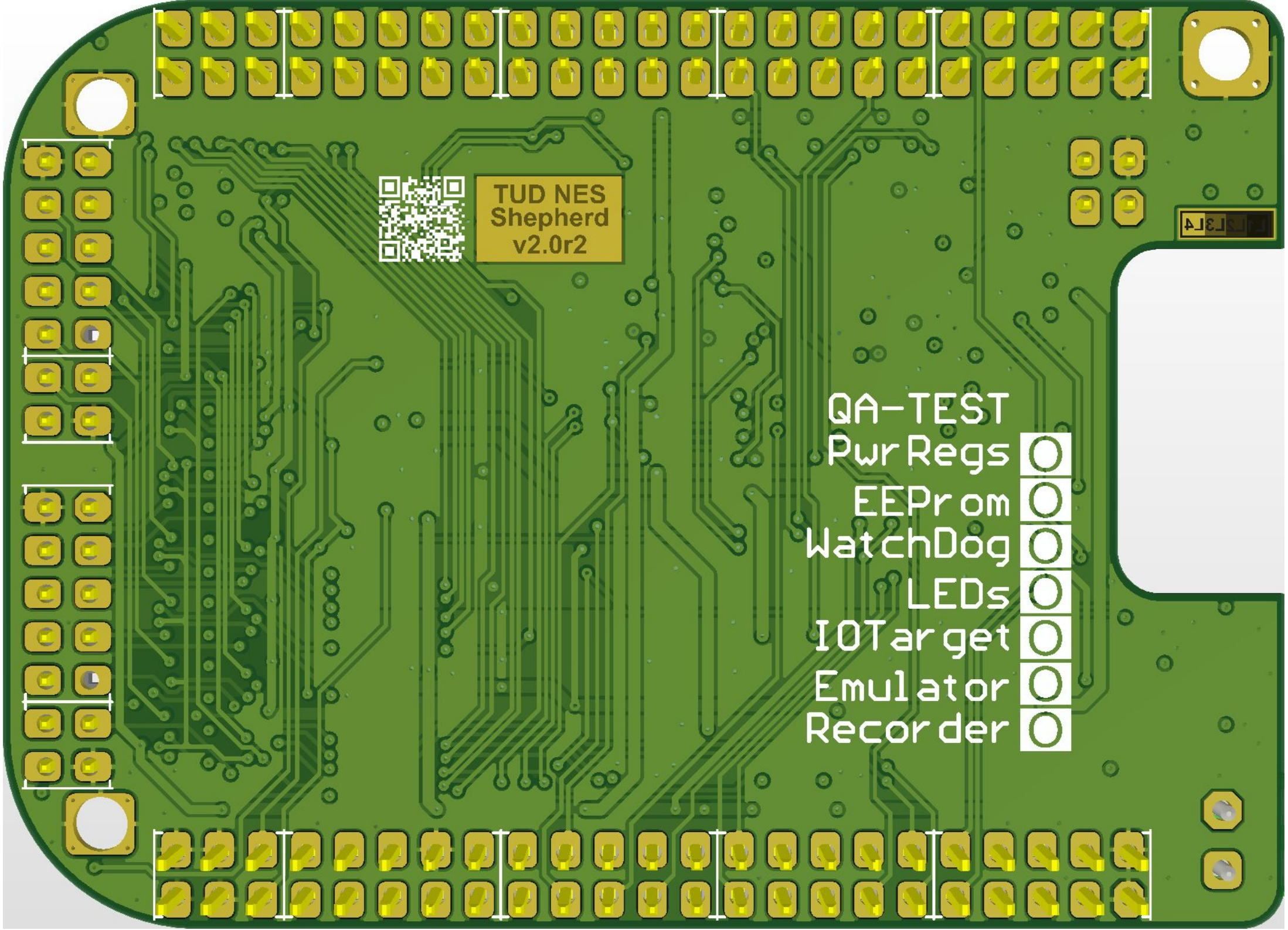
Gain & precision ADC



Replaceable by Version with 500 kS & 100 kS

Title	Shepherd - Emulator NES Lab / TU Dresden	
Size: A3	Number	Revision
Date: 12.17.2020	Sheet of	shepherd_v2.PrjPcb
File: C:\Users\..\VEmulator.SchDoc	Drawn By:	Ingmar


Harvest
P8
PRU_0
PRU_1
P2
TP8
TP7
U27
U1
TP1
TP4
TP3
U6
U14
U9
U3
U24
U13
U5
P5
TP6
REC EMU
nWP
U33
U28
A5V
U36
U7
U11
P3
10V
U4
U8
10k
100k
U10
6V
U12
U15
-6V
U37
J1
P9


TUD NES
Shepherd
v2.0r2
QA-TEST
PwrRegs
EEProm
WatchDog
LEDs
IOTarget
Emulator
Recorder