ECE 350 – Spring 2016

HW 2 - Register File

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1 Design Implementation

To build a register file, multiple submodules needed to be implemented or obtained from the Altera library. The submodules are shown below

1. Altera Library
   (a) DFFE - D Flip Flop with Enable bit
2. Personal Created Modules
   (a) 5 to 32 Decoder
   (b) Register
   (c) Tri State Buffer

The register used a generator loop to generate the 32 DFFE inside it so that it would be able to store all 32 bits. The output of each register is then connected to a Tri State Buffer where a 5 to 32 decoder was used to select the register to read from. In the case of write, a 5 to 32 decoder was used to determine which register to write too. Each bit from the output of the decoder was an input to an AND gate alongside with the ctrl writeEnable signal. This was then connected to each of the register in the generator loop.

2 Timing Waveform

To determine the timing waveform, I fixed the clock cycle. I then did a write operation to clock cycle. I then did a read in the next clock cycle. If there were any glitches as seen by the very small diamond shapes in the output waveform, it represents a distorted wave. In this case, this represents a clock frequency where the register file can't function. If the waveform looks fine, the clock frequency was increased.

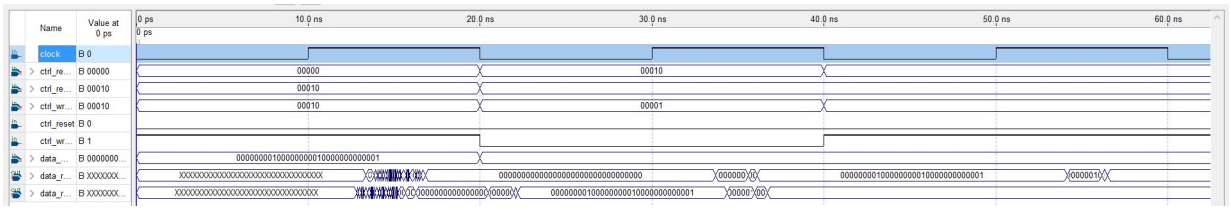

Figure 1: Waveform Vector for Clock Rate = 50MHz