

Introduction to Intel Xeon Phi Workshop

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Outline

① Intel Xeon Phi overview

- Why this enthusiasm with Intel Phi?
- Hardware specs
- Roadmap

② Parallel Strategies

- How easy is it?
- Perfect Candidates
- How to get the maximum performance on Intel Phi

Intel Xeon Phi co-processor overview

Why this enthusiasm about Intel Phi?

- You don't need to learn a new programming language (CUDA,...)
- You don't need to change the code in order to run on MIC.
- But,....
- The Intel MIC CPUs are slow comparing with the current Xeon.
- To get real performance you need to apply some changes.
- Is not easy, but a medium size code can be modified in few hours or days.
- Comparing with other architectures, it's like child's play.

A MAGIC ACT: The SAME CODE works on Xeon TOO!!



¹R. Harrison, "Opportunities and Challenges Posed by Exascale Computing - ORNL's Plans and Perspectives", National Institute of Computational Sciences, May 2011.

Other brands and names are the property of their respective owners



Figure : source www.intel.com

Intel Xeon Phi co-processor overview

System based on coprocessors in TOP500 – June 2013

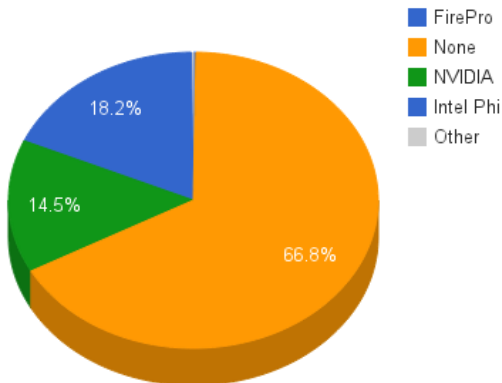


Figure : source Top500 <http://www.top500.org/statistics/list/>

Intel Xeon Phi co-processor overview

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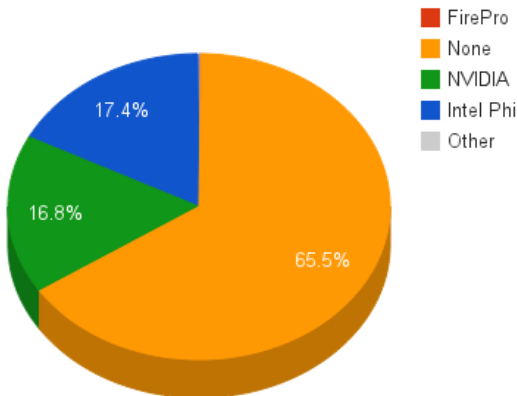
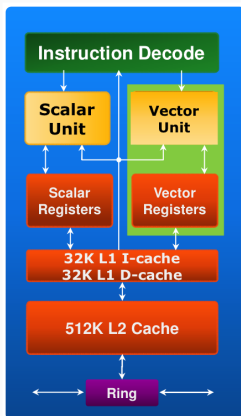


Figure : source Top500 <http://www.top500.org/statistics/list/>

Hardware specs

Hardware specs of 5110P (KNF)



- 60 cores/1.053 GHz/240 threads.
- 30MB cache
- 8 GB memory and 320 GB/s bandwidth.
- GDDR5 x16 channels (5.5Gbit each).
- 300 ns access!
- Linux operating system, IP addressable.
- Built using Intel's 22nm process technology.
- 512-bit Single Instruction, Multiple Data instructions (SIMD).
- 32 vector registers.

Intel Xeon Phi Public Roadmap

Unveiling Details of Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors

Compute: Energy-efficient IA cores²

- Microarchitecture enhanced for HPC³
- **3X Single Thread Performance** vs Knights Corner⁴
- Intel Xeon Processor Binary Compatible⁵

On-Package Memory:

- up to **16GB** at launch
- **1/3X the Space**⁶
- **5X Bandwidth** vs DDR4⁷
- **5X Power Efficiency**⁶

Jointly Developed with Micron Technology

2nd half '15
1st commercial systems

3+ TFLOPS¹
In One Package
Parallel Performance & Density

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. ¹Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle. ²FLOPS = cores x clock frequency x floating-point operations per second per cycle. ³Modified version of Intel® Silvermont microarchitecture currently found in Intel® Atom™ processors. ⁴Modifications include AVX512 and 4 threads/core support. ⁵Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner). ⁶Binary Compatible with Intel Xeon processors using Haswell instruction set (except TSX). ⁷Projected results based on internal Intel analysis of Knights Landing memory vs Knights Corner (GDDR5). ⁸Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.

Conceptual—Not Actual Package Layout

Figure : source http://newsroom.intel.com/servlet/JiveServlet/download/38-32805/ISC14_Raj_Hazra_keynote.pdf

Intel Omni Scale Fabric Roadmap

Announcing

Intel® Omni Scale—The Next-Generation Fabric

- Designed for Maximum Scalability
- Rich Set of Programming Models
- Flexible Configurations
- End-to-End Solution

INTEGRATION

Intel® Omni
Scale Fabric



Starting with
Knights Landing

Intel® Omni
Scale Fabric



Future 14nm
generation



Coming in '15



PCIe
Adapters



Edge
Switches



Director
Systems



Intel Silicon
Photonics



Open
Software
Tools*

Intel® True Scale
Fabric Upgrade
Program Helps Your
Transition



*OpenFabrics Alliance

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Figure : source http://newsroom.intel.com/servlet/JiveServlet/download/38-32805/ISC14_Raj_Hazra_keynote.pdf

Matrix addition processing in scalar and vector mode.

- **SSE** 128-bit (streaming) SIMD / 4 elements at once (2008).
- **AVX** 256-bit SIMD / 8 elements at once (2011).
- **MIC** 512-bit SIMD / 16 elements at once (2012).
- **AVX2** 256-bit SIMD / up to 32 elements at once (Q2 2013).
- **AVX-512** 512-bit SIMD / 16 elements at once (Q2 2015).

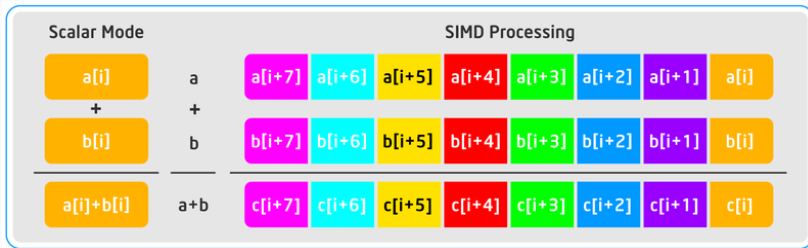
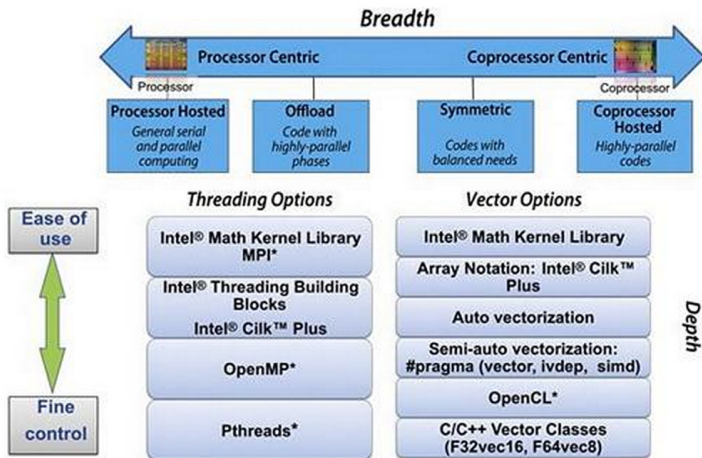


Figure : source: www.intel.com

Parallel Strategies

Figure : source www.intel.com

Perfect Candidates

Perfect Candidates

- Serial applications that need to be run many times.
- Massive parallel applications (OpenMP).
- Massive parallel applications (MPI).
- Massive hybrid parallel applications (MPI+OpenMP).
- Applications that can exploit the vectorial capabilities of MIC.

How to get the maximum performance on Intel Phi

Maximize the performance in the processor first!

- The first advise is to focus in the processor performance
- Audit the loops and find the hot-spots
- Profile the code
- Profile the MPI collectives
- Explore the Vectorization opportunities

Questions & Answers



for more info

Books

- James Jeffers & James Reinders, Intel Xeon Phi Coprocessor High Performance Programming, Newnes, 2013. ISBN: 0124104940
- James Reinders, Parallel Programming and Optimization with Intel® Xeon Phi™ Coprocessors, Colfax 2013. ISBN-13: 978-0-9885234-1-8

Intel website (trainings and workshops)

- <http://software.intel.com/en-us/mic-developer>
- <http://software.intel.com/en-us/intel-mkl>
- <http://software.intel.com/en-us/intel-composer-xe/>