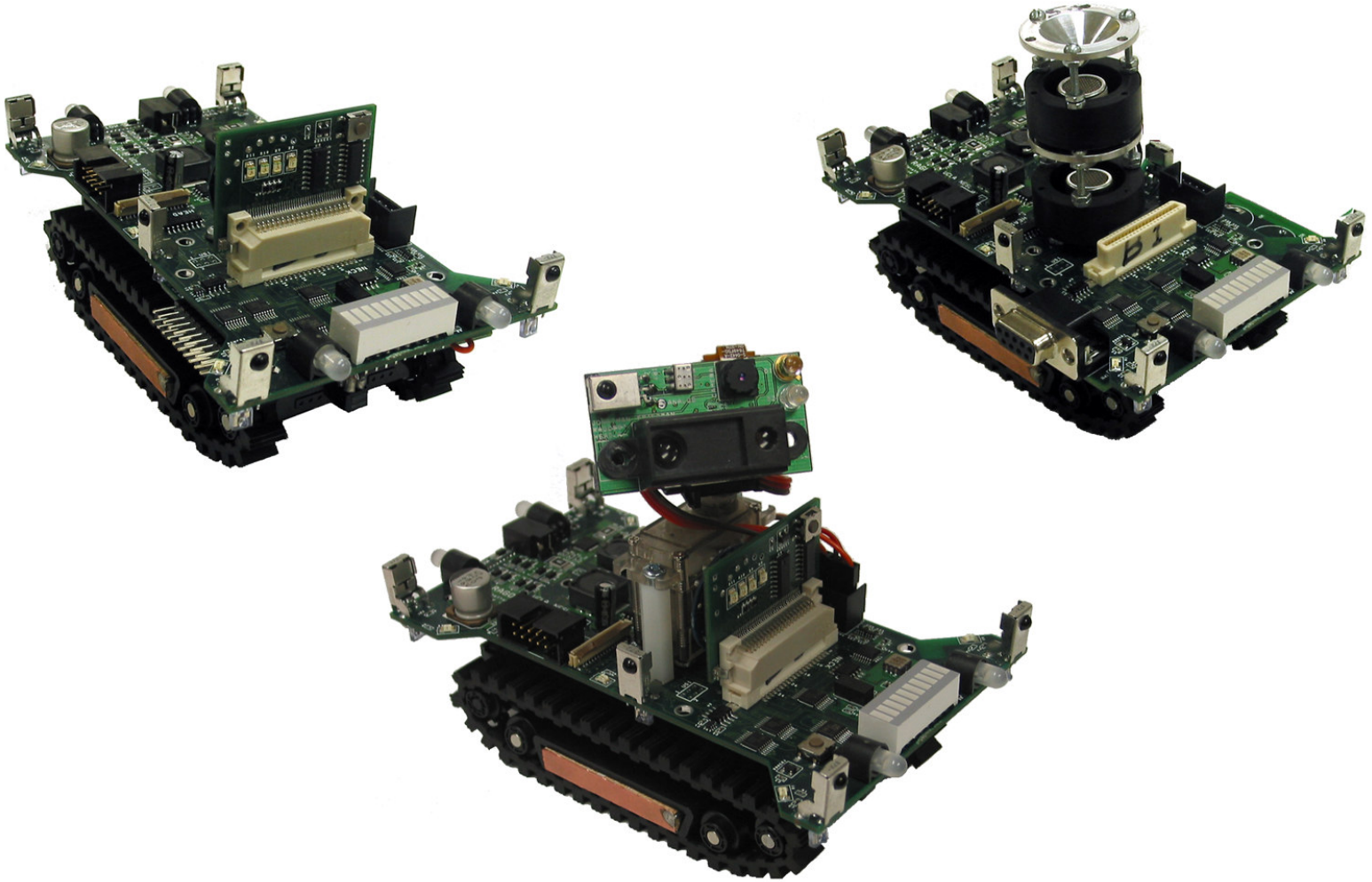
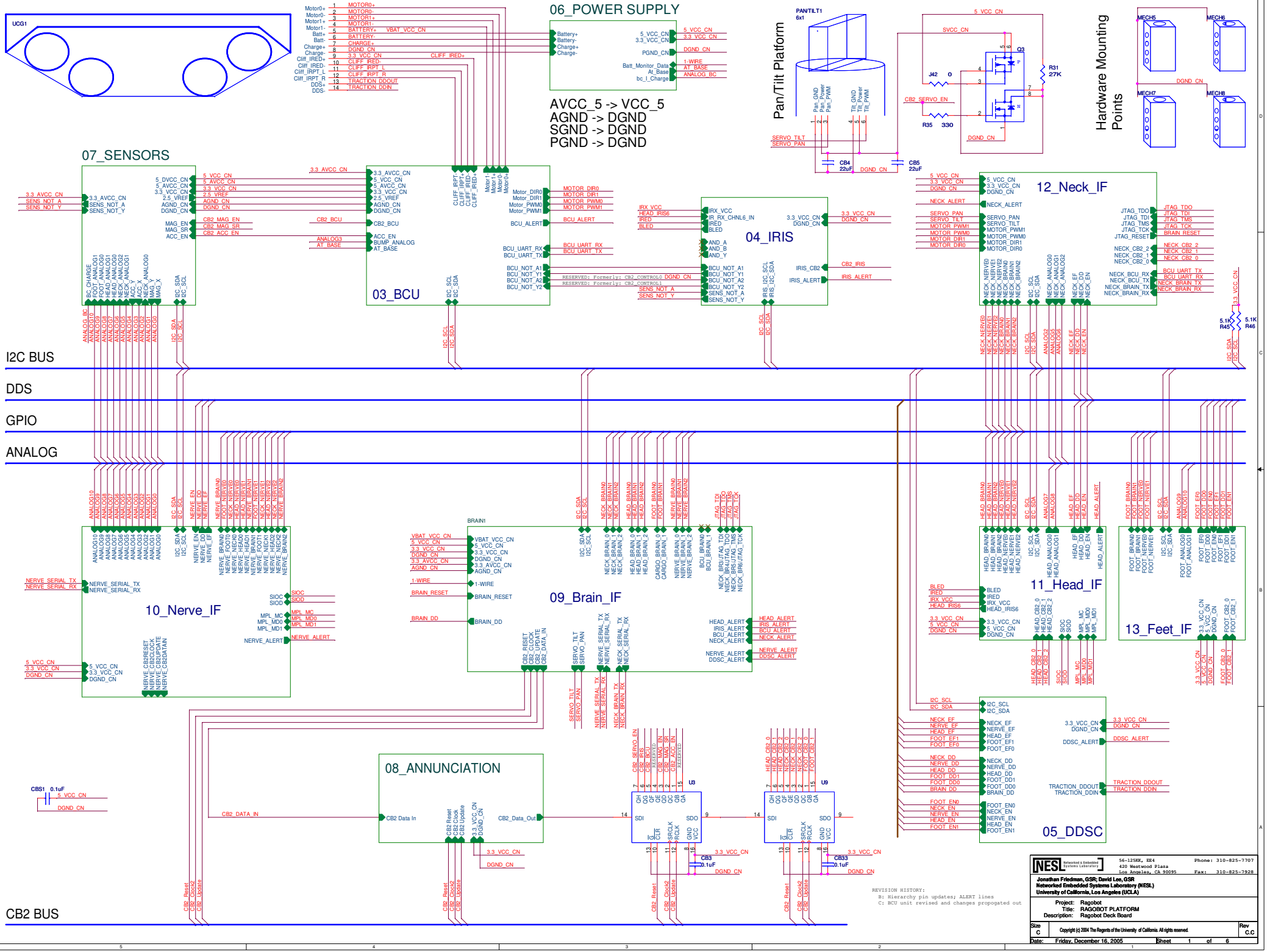


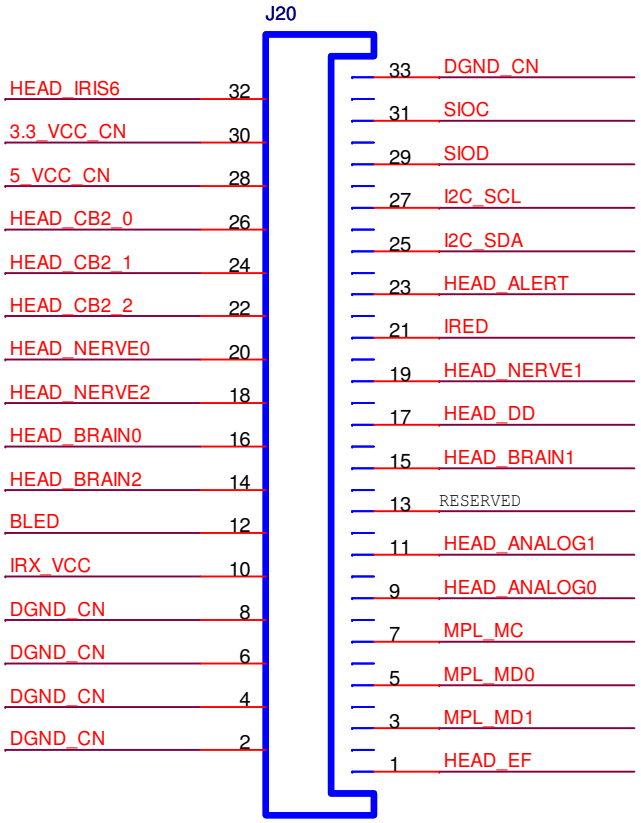
Ragobot

NESL Networked & Embedded Systems Laboratory CENS

Jonathan Friedman, GSR
David Lee, GSR



HEAD I/F



3.3_VCC_CN
5_VCC_CN

DGND_CN

HEAD_EF
HEAD_DD
HEAD_EN

SIOC
SIOD

I2C_SDA
I2C_SCL

HEAD_CB2_0
HEAD_CB2_1
HEAD_CB2_2

HEAD_ANALOG0
HEAD_ANALOG1

HEAD_BRAIN0
HEAD_NERVE0

HEAD_BRAIN1
HEAD_NERVE1

HEAD_BRAIN2
HEAD_NERVE2

IRED
BLED
IRX_VCC
HEAD_IRIS6

MPL_MC
MPL_MD0
MPL_MD1

HEAD_ALERT

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Jonathan Friedman, GSR; David Lee, GSR
Networked Embedded Systems Laboratory (NESL)
University of California, Los Angeles (UCLA)

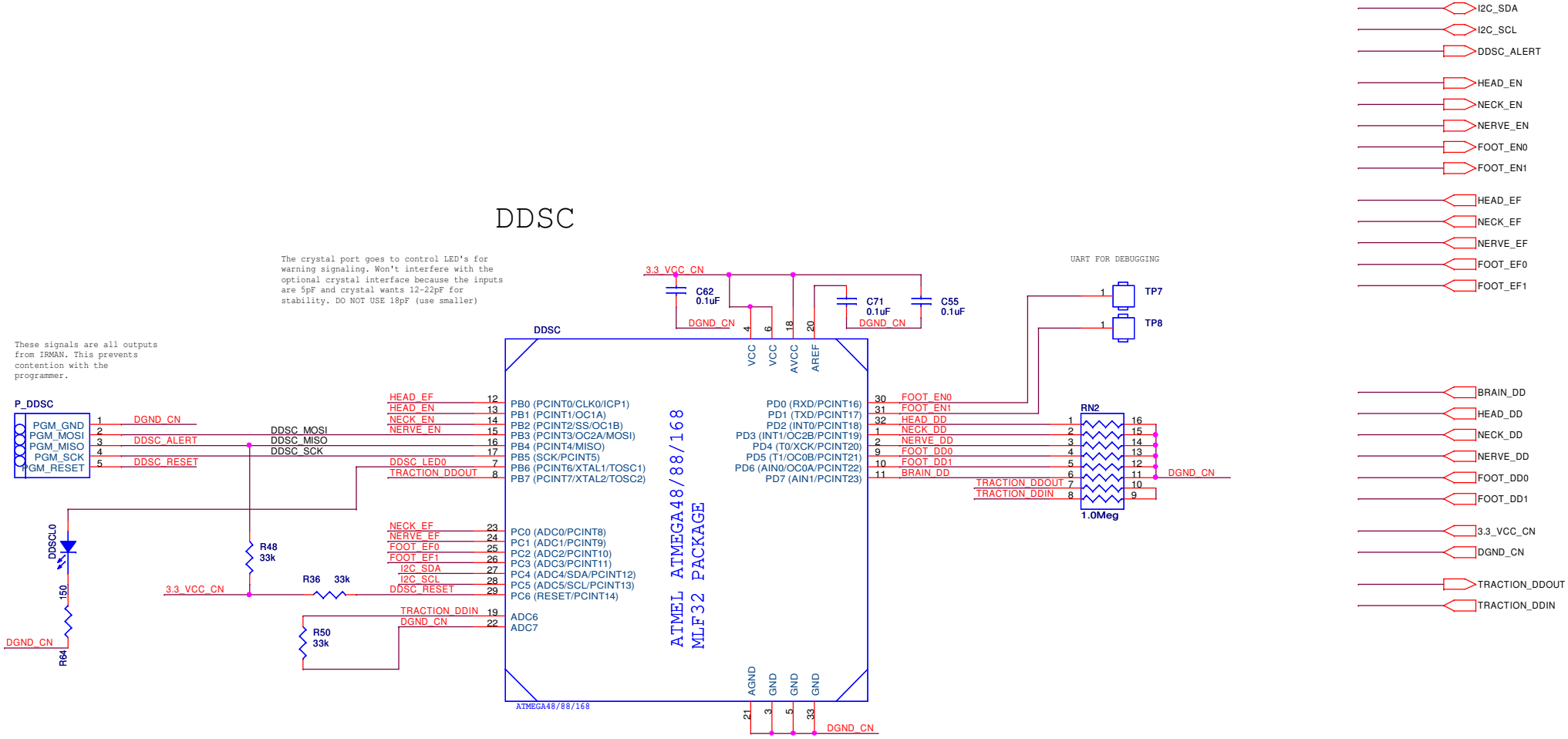
Project: Ragobot
Title: HEAD interface detail
Description: Motile Sensor Interface with support for both dumb and smart cards

Size A

Rev C.A

Date: Friday, December 16, 2005

DDSC



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University of California, Los Angeles (UCLA)

Project:	Ragobot
Title:	DDSC
Description:	Device Discovery Service Controller (hot-swap and plug-and-play)

Size		Rev
B		C.A

Date: Friday, December 16, 2005 Sheet 1 of 6

50 J_NERVE

CARD SOCKET CONNECTOR

GND	1		
MPL0	2	MPL_MC	
+3.3	3		
MPL1	4	MPL_MD0	
GND	5		
MPL2	6	MPL_MD1	
GND	7		
LANE0_A	8	NERVE_BRAIN0	
LANE0_B	9	NERVE_BRAIN1	
LANE0_C	10	NERVE_BRAIN2	
LANE1_A	11	NERVE_HEAD0	
LANE1_B	12	NERVE_HEAD1	
LANE1_C	13	NERVE_HEAD2	
LANE1_D	14	SIOD	
LANE1_E	15	SIOC	
LANE2_A	16	NERVE_NECK0	
LANE2_B	17	NERVE_NECK1	
LANE2_C	18	NERVE_NECK2	
LANE3_A	19	NERVE_FOOT0	
LANE3_B	20	NERVE_FOOT1	
LANE4/CB2_A	21	NERVE_CB2RESET	
LANE4/CB2_B	22	NERVE_CB2CLOCK	
LANE4/CB2_C	23	NERVE_CB2UPDATE	
LANE4_CB2_D	24	NERVE_CB2DATAIN	
DFID_EF	25	NERVE_EF	
RESERVED	26	NERVE_ALERT	
DFID_DD	27	NERVE_DD	
SDA	28	I2C_SDA	
SCL	29	I2C_SCL	
TXD0	30	NERVE_SERIAL_TX	
RXD0	31	NERVE_SERIAL_RX	
GND	32	GND_CN	
LANE5/ANHI_A+	33	AUDIO0+	
LANE5/ANHI_A-	34	AUDIO0-	
LANE5/ANHI_B+	35	AUDIO1+	
LANE5/ANHI_B-	36	AUDIO1-	
ANHO0	37	ANALOG0	
ANHO1	38	ANALOG1	
ANHO2	39	ANALOG2	
GND	40	GND_CN	
ANHO3	41	ANALOG3	
ANHO4	42	ANALOG4	
ANHO5	43	ANALOG5	
ANHO6	44	ANALOG6	
ANHO7	45	ANALOG7	
ANHO8	46	ANALOG8	
ANHO9	47	ANALOG9	
+5.0	48		
ANHO10	49	ANALOG10	
GND	50	GND_CN	

3.3_VCC_CN

5_VCC_CN

R55 330

R56 330

LS1 SPEAKER

LS2 SPEAKER

The MPL bus is extremely high speed serial (~200MHz). Excercize all due care during layout.

VBAT is not connected in this module.

NERVE_EN is not implemented in this version of the RAGOBOT

ULTRASOUND TRANSCIEVERS

Audio was removed at rev.C.B.; Audio subsystem is available on a mini-stereo connector (RCA) out of the NERVE card directly.

3.3_VCC_CN
5_VCC_CN
DGND_CN
ANALOG0
ANALOG1
ANALOG2
ANALOG3
ANALOG4
ANALOG5
ANALOG6
ANALOG7
ANALOG8
ANALOG9
ANALOG10
MPL_MC
MPL_MD0
MPL_MD1
SIOC
SIOD
I2C_SDA
I2C_SCL
NERVE_CB2RESET
NERVE_CB2CLOCK
NERVE_CB2UPDATE
NERVE_CB2DATAIN
NERVE_EF
NERVE_DD
NERVE_EN
NERVE_SERIAL_RX
NERVE_SERIAL_TX
NERVE_BRAIN0
NERVE_BRAIN1
NERVE_BRAIN2
NERVE_HEAD0
NERVE_HEAD1
NERVE_HEAD2
NERVE_NECK0
NERVE_NECK1
NERVE_NECK2
NERVE_FOOT0
NERVE_FOOT1
NERVE_ALERT

REVISION HISTORY:
B: Dropped bus switches. Updated pin wiring. Assigned RESERVED signal to NERVE_ALERT
C: Updated signal names to match David's convention of all data directions being robot-centric; Removed unused signals (except NERVE_EN); Verified all wiring on this page.

D: added drive-limit resistors to UART

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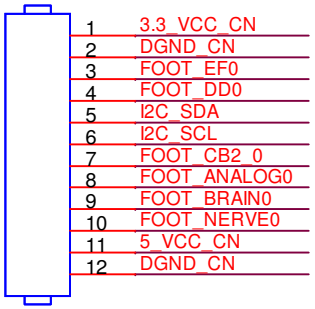
Project: Ragobot
Title: The NERVE Interface
Description: Connectors and wire-terminated components

Size A

Rev C.D

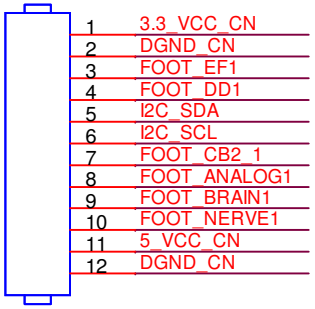
Date: Friday, December 16, 2005 Sheet 1 of 1

FOOT0

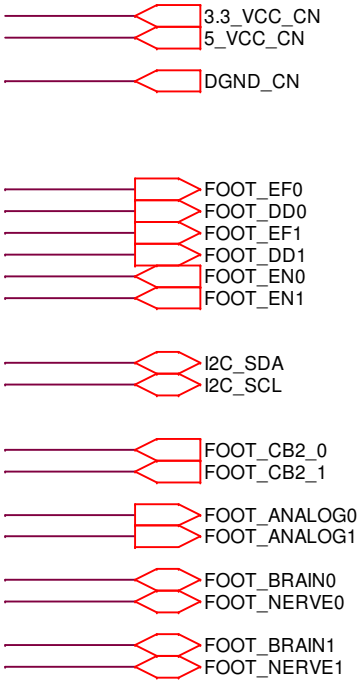


12

FOOT1



12



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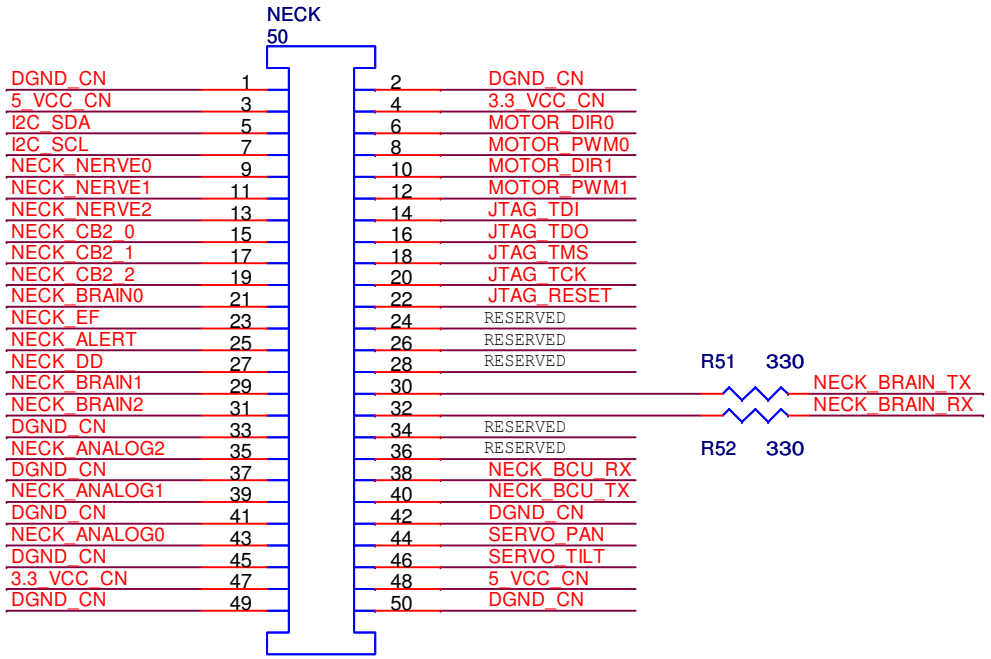
Project: Ragobot
Title: FOOT INTERFACE
Description: Forward and Aft Auxilary Cargo Interfaces

Size A | Rev C.A

Date: Friday, December 16, 2005 | Sheet 1 of 6

NECK I/F



5_VCC_CN
3.3_VCC_CN
DGND_CN

NECK_ANALOG0
NECK_ANALOG1
NECK_ANALOG2

I2C_SDA
I2C_SCL

NECK_CB2_0
NECK_CB2_1
NECK_CB2_2

NECK_DD
NECK_EF
NECK_EN

NECK_BRAIN0
NECK_BRAIN1
NECK_BRAIN2

NECK_NERVE0
NECK_NERVE1
NECK_NERVE2

MOTOR_DIR0
MOTOR_DIR1
MOTOR_PWM0
MOTOR_PWM1

NECK_BRAIN_TX
NECK_BRAIN_RX

NECK_BCU_TX
NECK_BCU_RX

SERVO_PAN
SERVO_TILT

JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG_RESET

NECK_ALERT

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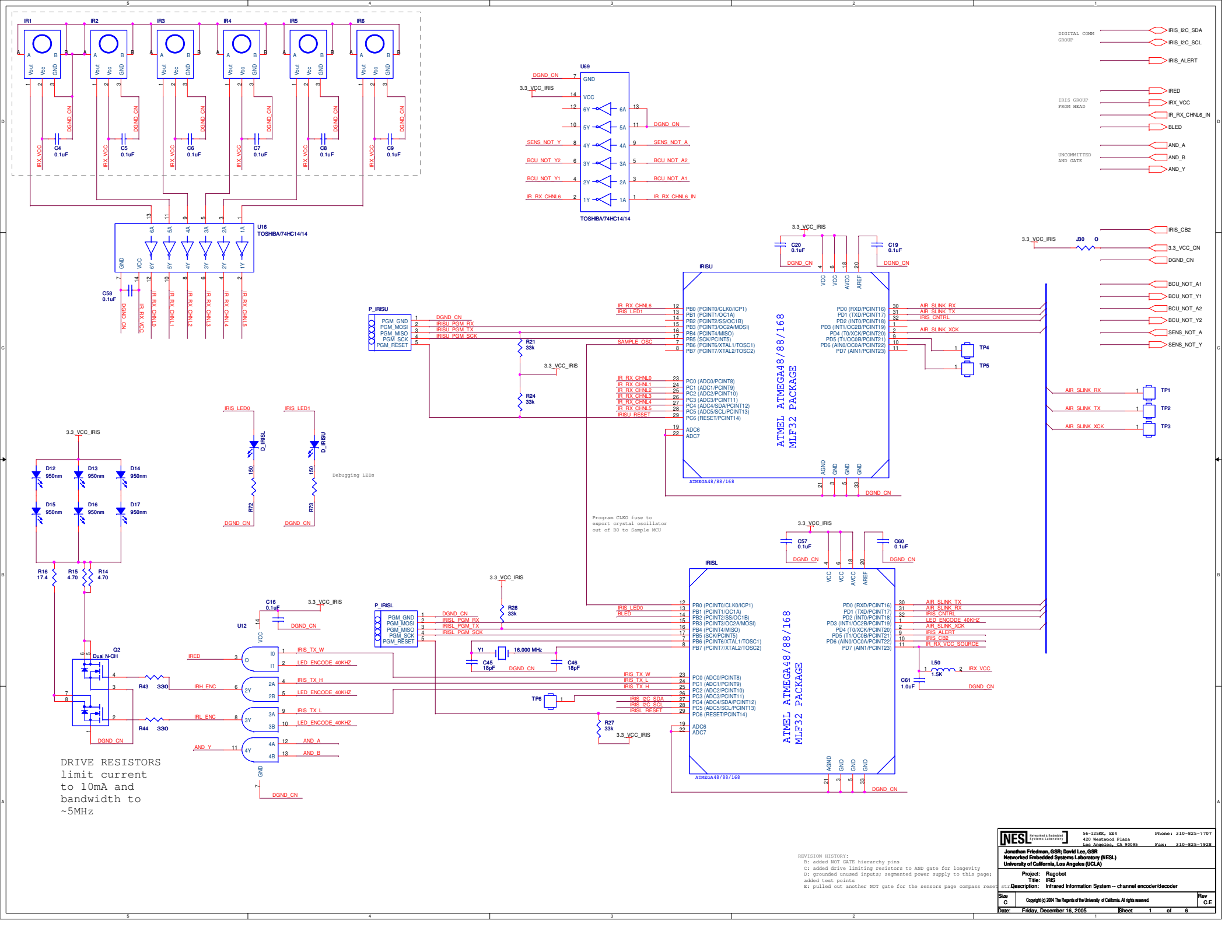
University of California, Los Angeles (UCLA)

Project: Ragobot
Title: NECK Interface
Description: General device expansion interface for all major sub-systems

Date: Friday, December 16, 2005 | Sheet 1 of 6



REVISION HISTORY:
B: added NOT GATE hierarchy pins
C: added drive limiting resistors to AND gate for longevity
D: grounded unused inputs; segmented power supply to this page; added test points
E: pulled out another NOT gate for the sensors page compass reset str

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Project: Ragobot
Title: IRIS
Description: Infrared Information System -- channel encoder/decoder

Size C | Rev C.E
Date: Friday, December 16, 2005 | Sheet 1 of 6

CB2

Deck Lights

Headlights

STATUS INDICATOR

Segment	MV5A164
1	HER
2	HER
3	HER
4	Yellow
5	Yellow
6	Yellow
7	Yellow
8	Green
9	Green
10	Green

Spec'd to light in all three colors. Current divides when both lamps are on so spec'd for 20mA per single color and 10mA each dual.

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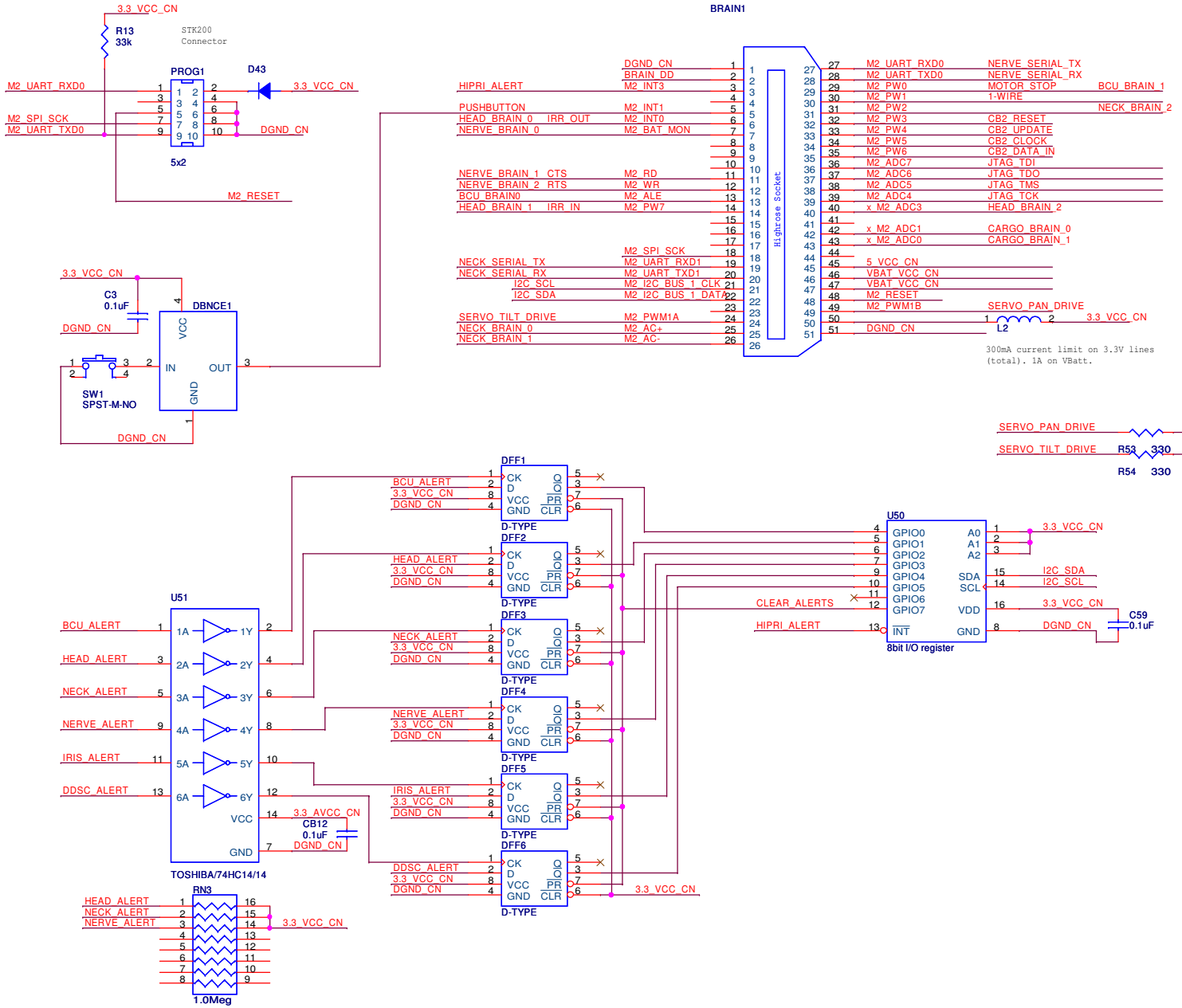
Project: Ragobot
Title: Annuciation
Description: Visual Annunciators for the Ragobot Main Board

Size B | Rev C.B

Date: Friday, December 16, 2005 | Sheet 2 of 6

STK/ISP Module



BRAIN INTERFACE 2.0

POWER DISTRIBUTION
- VBAT_VCC_CN
- 5_VCC_CN
- 3.3_VCC_CN
- 3.3_AVCC_CN
- AGND_CN
- DGND_CN

DIGITAL COMMUNICATIONS
- I2C_SCL
- I2C_SDA
- CB2_RESET
- CB2_UPDATE
- CB2_CLOCK
- CB2_DATA_IN
- 1-WIRE
- NECK_SERIAL_TX
- NECK_SERIAL_RX
- NERVE_SERIAL_RX
- NERVE_SERIAL_TX

SERVO CONTROL
- SERVO_PAN
- SERVO_TILT

INTERRUPT REGISTER
- NECK_ALERT
- HEAD_ALERT
- BCU_ALERT
- NERVE_ALERT
- IRIS_ALERT
- DDSC_ALERT

JTAG
- JTAG_TDI — NECK_BR3/JTAG_TDI
- JTAG_TDO — NECK_BR4/JTAG_TDO
- JTAG_TMS — NECK_BR5/JTAG_TMS
- JTAG_TCK — NECK_BR6/JTAG_TCK

DEVICE DISCOVERY
- BRAIN_DD

GPIO
- HEAD_BRAIN_0
- HEAD_BRAIN_1
- HEAD_BRAIN_2
- NERVE_BRAIN_0
- NERVE_BRAIN_1
- NERVE_BRAIN_2
- BCU_BRAIN0
- BCU_BRAIN_1
- NECK_BRAIN_0
- NECK_BRAIN_1
- NECK_BRAIN_2
- CARGO_BRAIN_0
- CARGO_BRAIN_1

RESET
- M2_RESET — BRAIN_RESET

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David Lee, GSR; Jonathan Friedman, GSR
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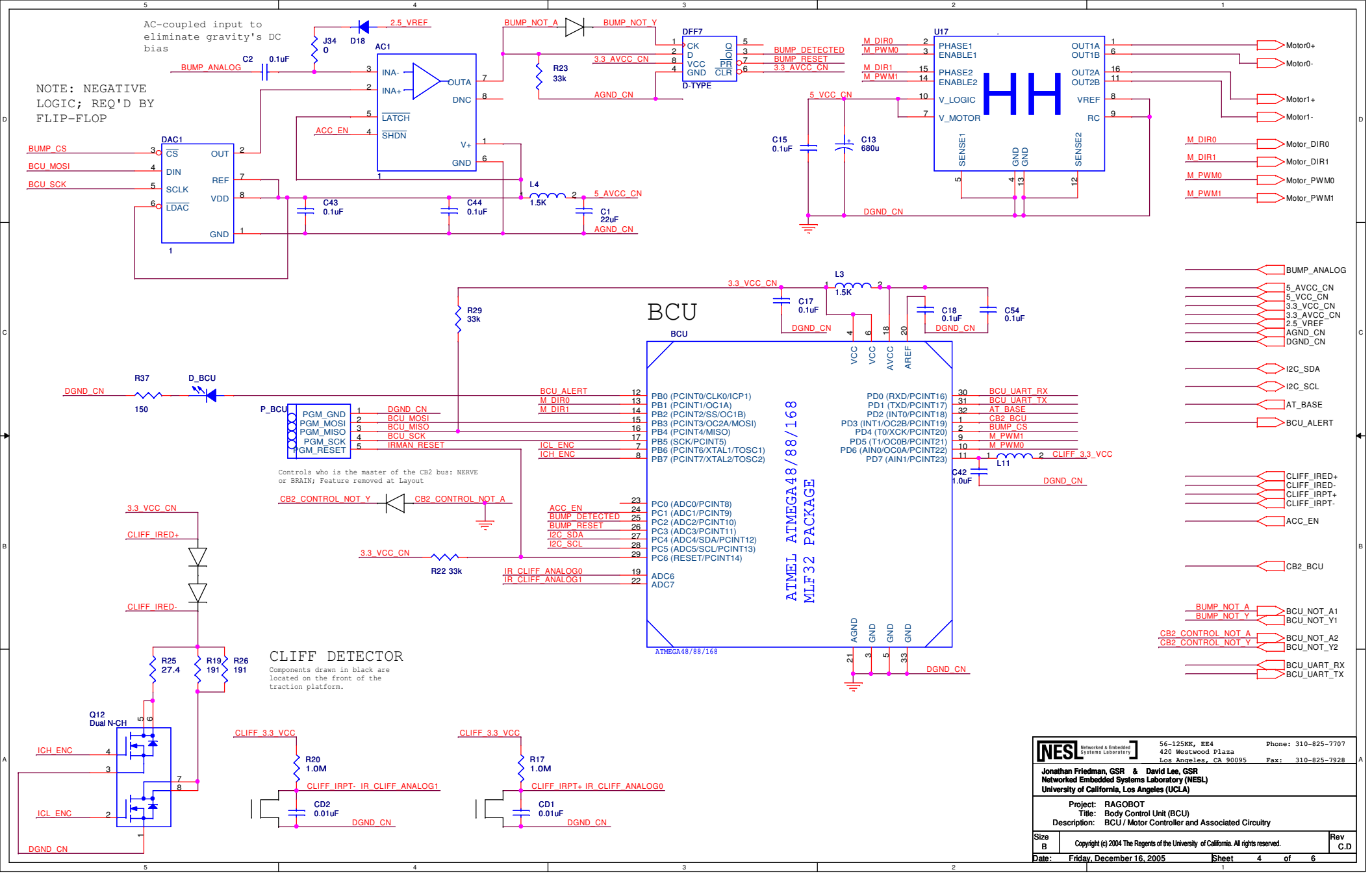
University of California, Los Angeles (UCLA)

Project: Ragobot
Title: Ragobot Brain IF
Description: Brain interface (signal abstraction)

Size B | Rev C.C

Date: Friday, December 16, 2005 | Sheet 3 of 6


AC-coupled input to eliminate gravity's DC bias
NOTE: NEGATIVE LOGIC; REQ'D BY FLIP-FLOP
BCU
ATMEL ATMEGA48/88/168 MLF32 PACKAGE
CLIFF DETECTOR
Components drawn in black are located on the front of the traction platform.
Controls who is the master of the CB2 bus: NERVE or BRAIN; Feature removed at Layout
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Project: RAGOBOT
Title: Body Control Unit (BCU)
Description: BCU / Motor Controller and Associated Circuitry
Size B
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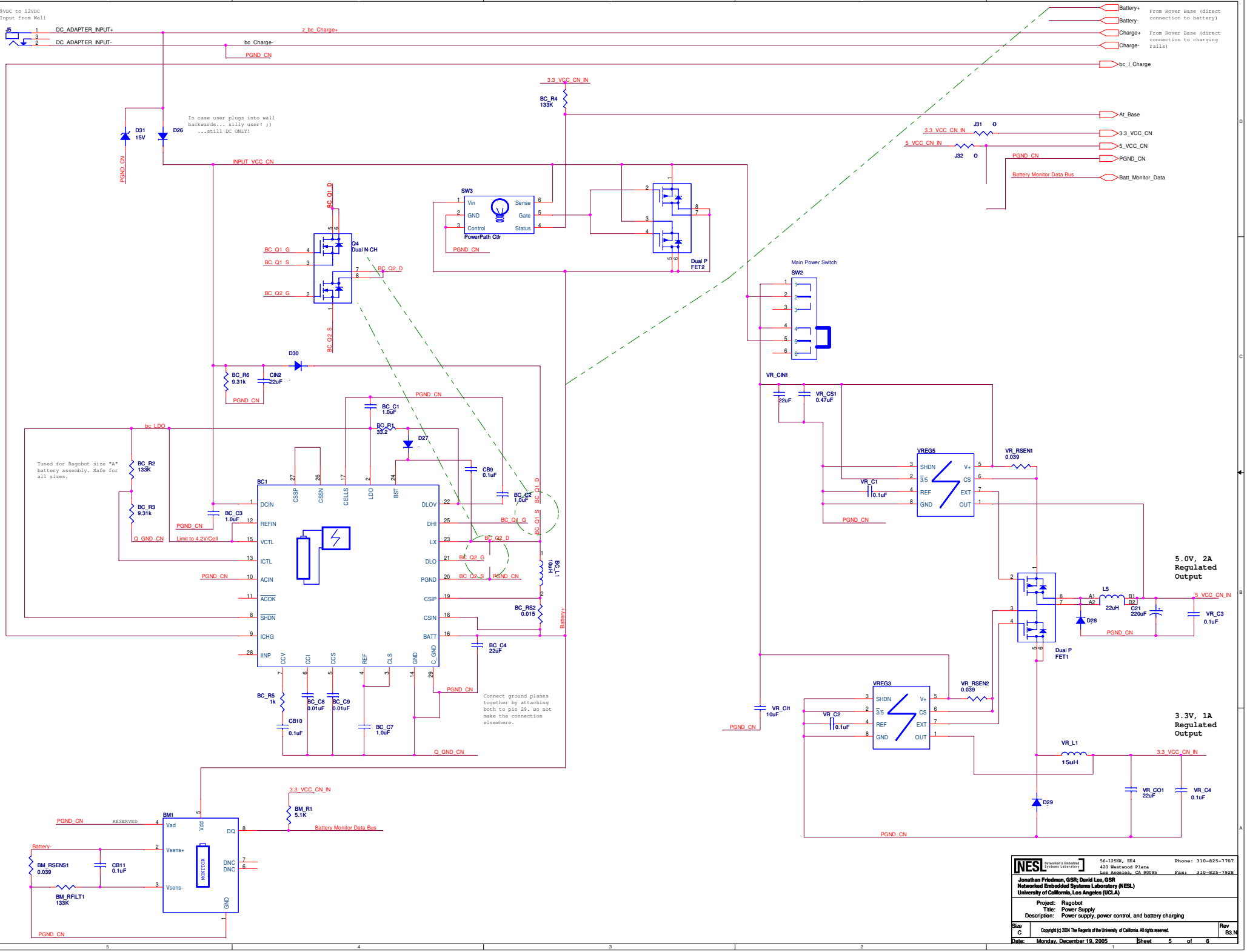
Rev C.D
Date: Friday, December 16, 2005
Sheet 4 of 6



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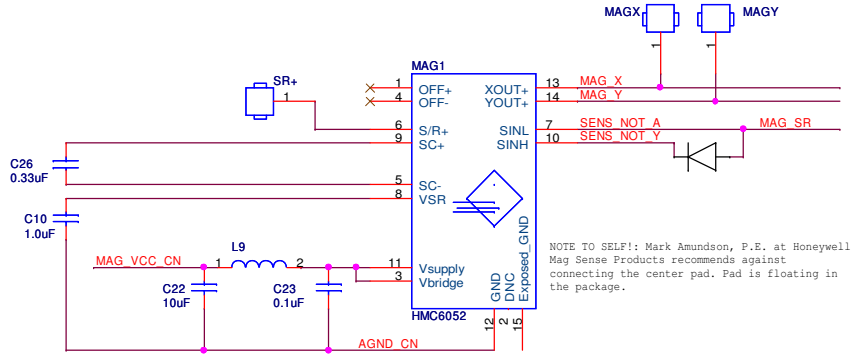
Project: Ragobot
Title: Power Supply
Description: Power supply, power control, and battery charging

Size C | Rev B3.N

Date: Monday, December 19, 2005 | Sheet 5 of 6

Magnetometer



NOTE TO SELF!: Mark Amundson, P.E. at Honeywell Mag Sense Products recommends against connecting the center pad. Pad is floating in the package.

Set/Reset Circuit for the Magnetometer
Note: Set/Reset is needed to realign the magnetic domains of the Permalloy magneto-resistive elements. The Set/Reset Strap needs 1.5A and the resistance of the S/R strap is 3 ohms. 1uF capacitor is used to decouple for the inverter since we are drawing 1.5A at once.

Hierarchical Block IO

SENSOR DATA
- MAG_X
- MAG_Y
- NECK_ANALOG0
- ACC_X
- ACC_Y
- NECK_ANALOG1
- NECK_ANALOG2
- HEAD_ANALOG0
- HEAD_ANALOG1
- FOOT_ANALOG0
- FOOT_ANALOG1
- BC_CHARGE

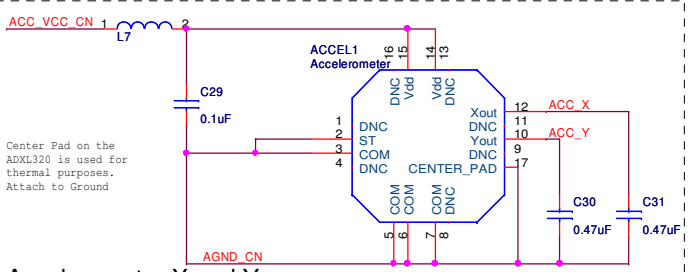
POWER DISTRIBUTION
- 5_DVCC_CN
- 5_AVCC_CN
- 3.3_AVCC_CN
- 3.3_VCC_CN
- DGND_CN
- AGND_CN

DIGITAL COMMUNICATIONS
- I2C_SDA
- I2C_SCL

SENSOR POWER & CONTROL
- 2.5_VREF
- ACC_EN
- MAG_EN
- MAG_SR

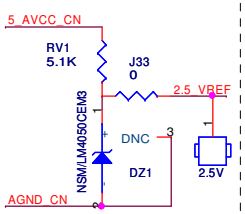
COMPASS RESET STRAP GATE
- SENS_NOT_A
- SENS_NOT_Y

Accelerometer X and Y

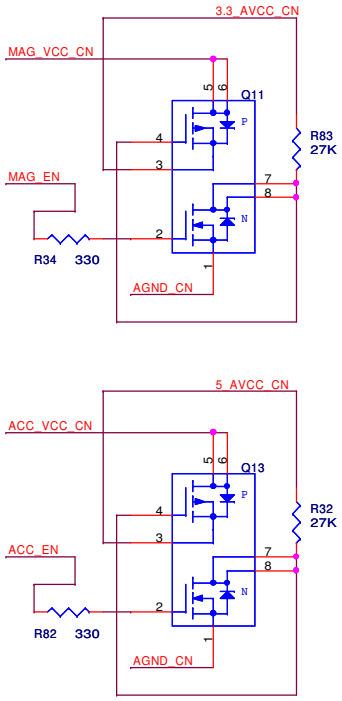


Center Pad on the ADXL320 is used for thermal purposes. Attach to Ground

Mid-scale Reference



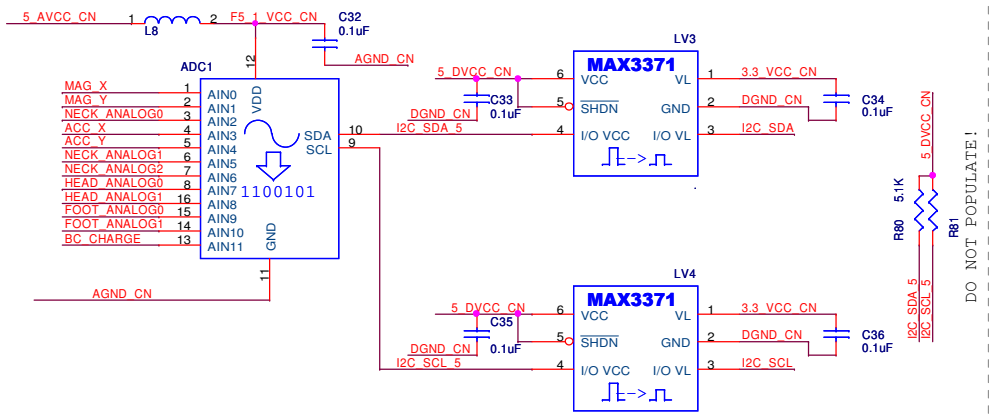
Power Control



NOTE TO SELF!: 5_AVCC and 5_VCC are electrically isolated on the schematic. Attachment point must be implemented in post process.

NOTE TO SELF!: AGND and DGND are electrically isolated on the schematic. Attachment point must be implemented in post process.

ADC with I2C interface



REVISION HISTORY:
- B: added 2.5Vref hierarchy pin
- C: Switched to a high-side power control system
- D: jumpered the 2.5V reference for debugging/measurement
- E: Heavy revision to the compass -- new integrated chip
- F: fixed 5V net name for the i2c pull-ups
- G: I2C Level Translators to 5DVCC net to optimize noise layout.
- H: Changed Vref to 5AVCC to ease routing problems

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Project: Ragobot
Title: Sensors
Description: Sensors on the main Ragobot board

Size B | Rev C.H
Date: Friday, December 16, 2005 | Sheet 6 of 6