ADC REGISTERS

2 Ocak 2025 Perşembe 22:59

1- ADC MUX SELECTION REG: ADMUX

7	6	5	4	3	2	1	0	
REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	ADMUX
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

* **Bit 7&6 : REFS1 & 0** (Reference Voltage Selection Bits)

REFS1	REFS0	
0	0	AREF, internal V_{REF} turned off.
0	1	AV_{cc} with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 1.1V Vref w/ external capacitor at $AREF_{pin}$

* **Bit 5: ADLAR** (ADC Left Adjust Result)
  - 1: Left align the result in the ADCH & ADCL registers.
  - 0: Right " " " .

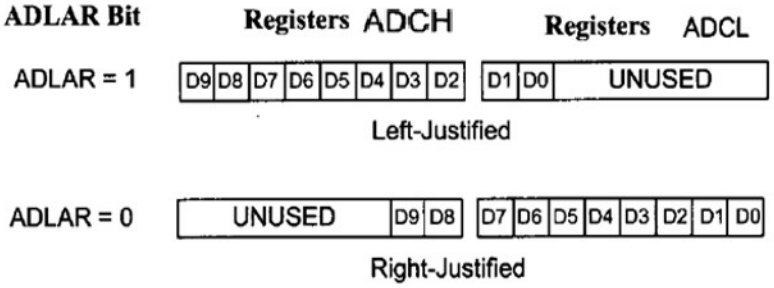
* **Bit 3-0: MUX 3-0** (Analog Channel Selection)

MUX3...0	Single Ended Input
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6

2- ADC DATA REGISTER: ADLAR (ADCH & ADCL)

ADCH AND ADCL REGISTER

After Analog to digital conversion is complete, result 10 bit sits in registers ADCH AND ADCL.



(2)
ADC DATA REGISTER (ADLAR: ADCH & ADCL)

3- ADC CONTROL & STATUS REGISTER A : ADCSRA

7	6	5	4	3	2	1	0
ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

ADCSRA

* **Bit 7 : ADEN** (ADC Enable)
  - 1: Enable ADC
  - 0: Disable ADC to save power

* **Bit 6 : ADSC** (ADC Start Conversion)
  - Writing
    - 1: start a new conversion
    - 0: No effect
  - Reading
    - 1: conversion in progress
    - 0: " completed

* **Bit 5 : ADATE** (ADC Auto Trigger Enable)
  - 1: Enables auto-triggering for continuous conversion
  - 0: Disables "

* Bit 2:0 : ADPS2 - 0 (ADC Prescaler Selection Bits)

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC operates reliability btw 50KHz to 200KHz clk freq.

CPU clock	Prescale	ADC frequency	ADCSRA bits set
1 MHz	4	250 kHz	ADPS1
	8	125 kHz	ADPS1 and ADPS0
	16	62.5 kHz	ADPS2
	32	31.25 kHz	ADPS2 and ADPS0
8 MHz	16	250 kHz	ADPS2
	32	125 kHz	ADPS2 and ADPS0
	64	62.5 kHz	ADPS2 and ADPS1
	128	31.25 kHz	ADPS2 and ADPS1 and ADPS0
12 MHz	64	187.5 kHz	ADPS2 and ADPS1
	128	93.75 kHz	ADPS2 and ADPS1 and ADPS0
16 MHz	64	250 kHz	ADPS2 and ADPS1
	128	125 kHz	ADPS2 and ADPS1 and ADPS0

Bit	7	6	5	4	3	2	1	0	
(0x7A)	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0	
(0x7B)	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	ADCSRB
Read/Write	R	R/W	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ADTS2	ADTS1	ADTS0	Trigger Source
0	0	0	Free running mode
0	0	1	Analog comparator
0	1	0	External interrupt request 0
0	1	1	Timer/Counter0 compare match A
1	0	0	Timer/Counter0 overflow
1	0	1	Timer/Counter1 compare match B
1	1	0	Timer/Counter1 overflow
1	1	1	Timer/Counter1 capture event