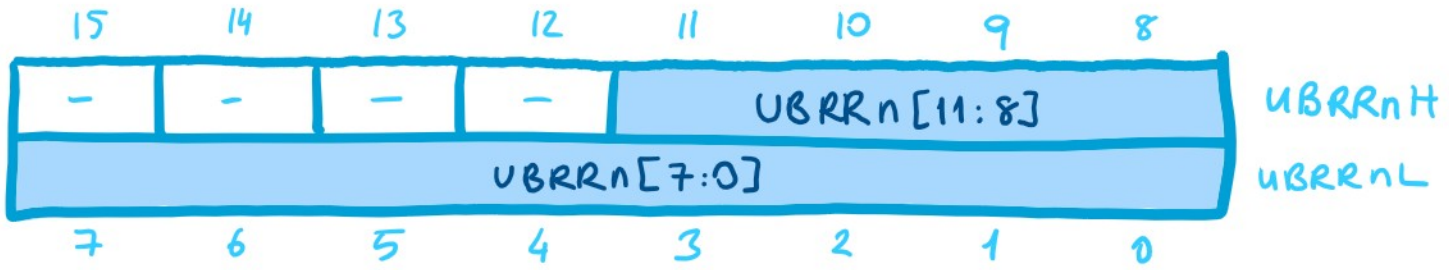
USART REGISTERS

10 Kasım 2024 Pazar 01:15

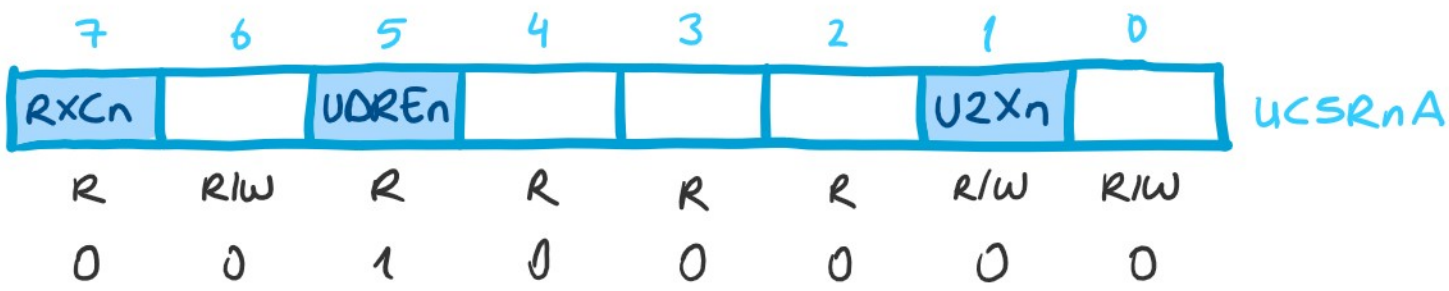
1- USART BAUD RATE REGISTER : UBRRn (UBRR0L & UBRR0H)



Read/ Write	R	R	R	R	R/W	R/W	R/W	R/W
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0

* UBRRn[15:12] → reserved for future usage
* UBRRn[11:0] → 12-bit register holding the BAUD rate.

2- USART CONTROL & STATUS REGISTER0 A : UCSR0A



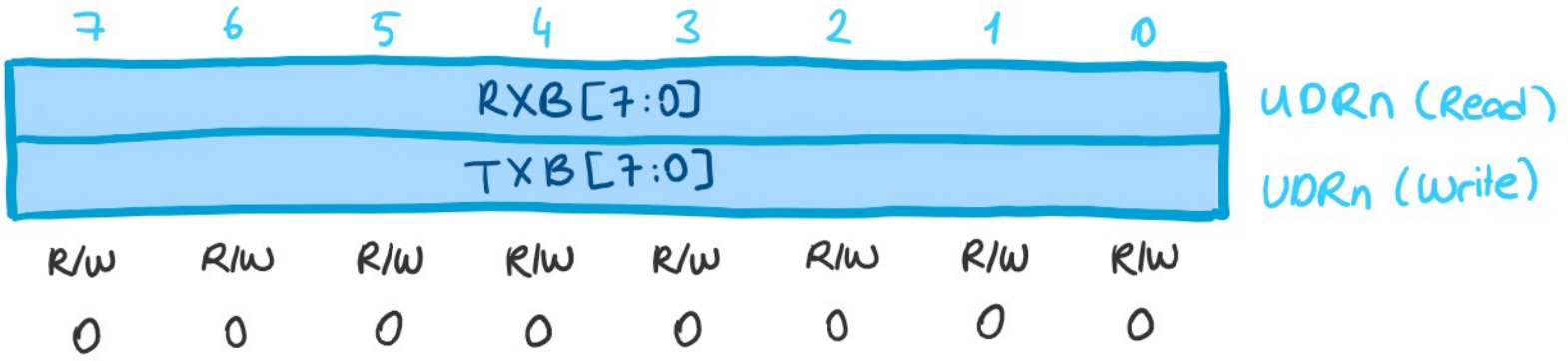
R	R/W	R	R	R	R	R/W	R/W
0	0	1	0	0	0	0	0

* **Bit 1 : U2X0** (double the USART transmission speed)
  - → 1 : double speed mode
  - → 0 : normal mode

* **Bit 5 : UDRE** (USART Data Register Empty)
  - → 1 : UDR0 is empty (new data can be loaded in UDR0 for transmission)
  - → 0 : UDR0 is used (data transmission in progress, do not load new data into UDR0)

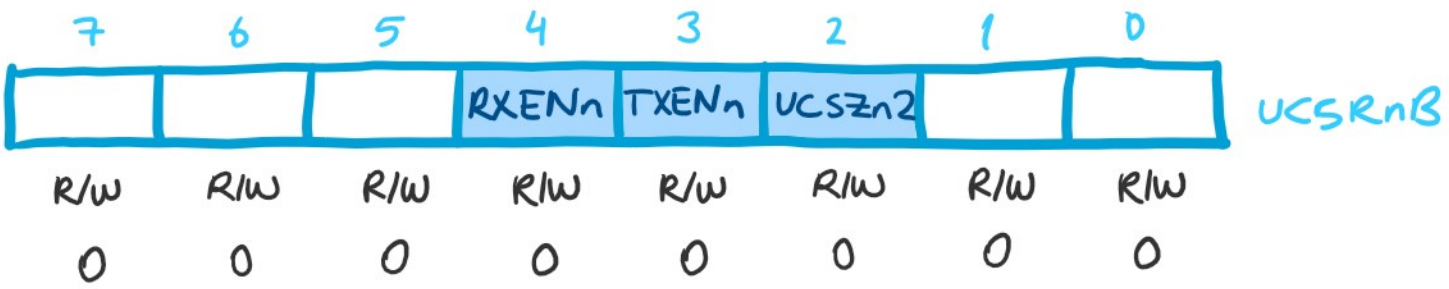
* **Bit 7 : RXC0** (Receive Complete)
  - → 1 : new data has been received in UDR ; ready to be used.
  - → 0 : data reception is in progress.

3- USART DATA REGISTER 0 : UDR0



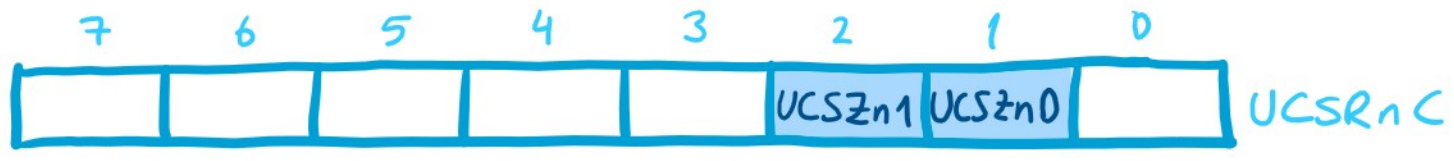
* Writing UDR0 loads data in TXB
* Reading UDR0 returns data from RXB

4- USART CONTROL & STATUS REGISTER 0 B: UCSR0B



* **Bit 3 : TXEN** (Transmitter Enable n)
  - 1: USART Transmitter is enable (overwrites normal op of PD1 for TD)
  - 0: " " " disabled
* **Bit 4 : RXEN** (Receiver Enable n)
  - 1: USART receiver is enable (overwrites normal port op. of PD0 for RxD pin)
  - 0: " " " disabled

5- USART CONTROL & STATUS REGISTER 0 C : UCSR0C



* USART Character Size
* Bit 2 & 1 of UCSR0C (UCSZn 1:0) & Bit 2 of UCSR0B (UCSZn 2) define # of data bits in a frame

define # of data bits in a frame

UCSZn2	UCSZn1	UCSZn0	Character Size
0	0	0	5 bit
0	0	1	6 "
0	1	0	7 "
0	1	1	8 "
1	0	0	Reserved
1	0	1	"
1	1	0	"
1	1	1	9 bit