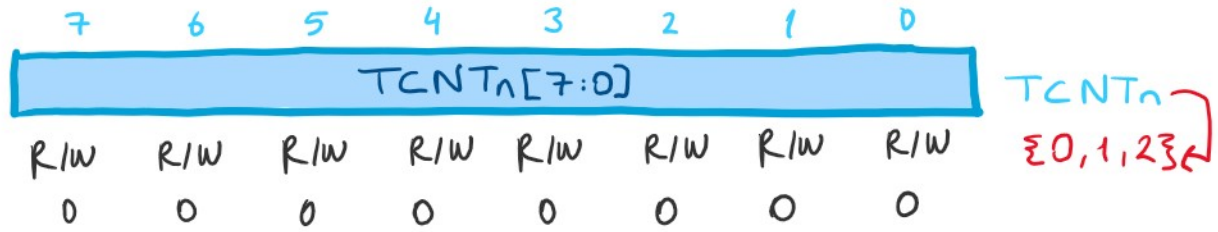
TIMER REGISTERS

23 Aralık 2024 Pazartesi 22:30

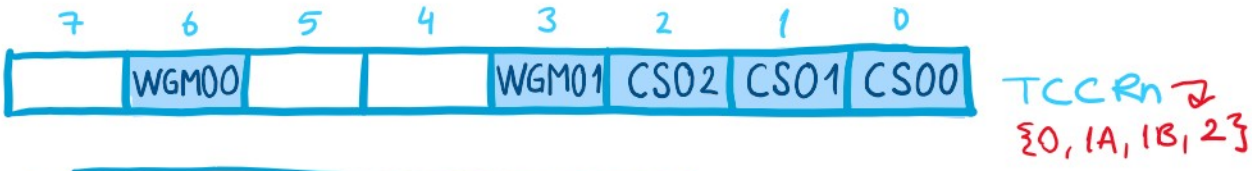
1- TIMER/COUNTER REGISTER : TCNTn → Stopwatch

* The current count can be read any time
* Can be written a value any time.



* Starts from 0 when initialized
* Increments until it overflows (255 for 8-bit)

2- TIMER/COUNTER CONTROL REGISTER: TCCRn



* Bit 6 & 3 : WGM00 & WGM 01 (Waveform Generation Mode)

WGM00	WGM01	Timer0 mode selector bits
0	0	Normal
0	1	CTC (clear timer on Compare Match)
1	0	PWM, phase correct *
1	1	Fast PWM *

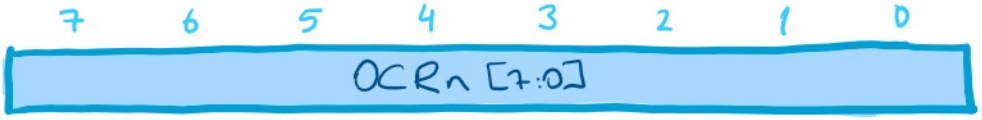
* PWM: Pulse with modulation (Lect. 10)

* Bit 2, 1 & 0 : CS02, CS01 & CS00 (Clock Select Bits)
  - Used in prescaler configuration

CS02	CS01	CS00	Clock Source (Prescaler)
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	clk (No prescaling)
0	1	0	clk/8
0	1	1	clk/64
1	0	0	clk/256
1	0	1	clk/1024
1	1	0	External clk source on T0 pin, Falling Edge.
1	1	1	" " " " " " , Rising Edge

3- OUTPUT COMPARE REGISTER : OCRn → Alarm clock

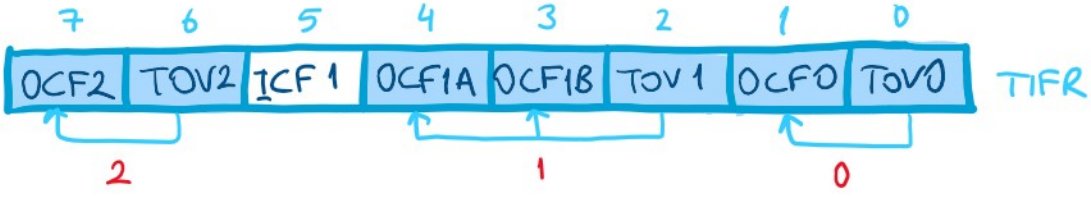
* Store compare value in this register
* When the compare value is reached a compare event triggers the waveform generator



OCRn → {0, 1A, 1B, 2}

* When the timer (TCNTn) equals the value in OCRn, an output compare event is triggered.

4- TIMER/COUNTER INTERRUPT FLAG REGISTER: TIFR



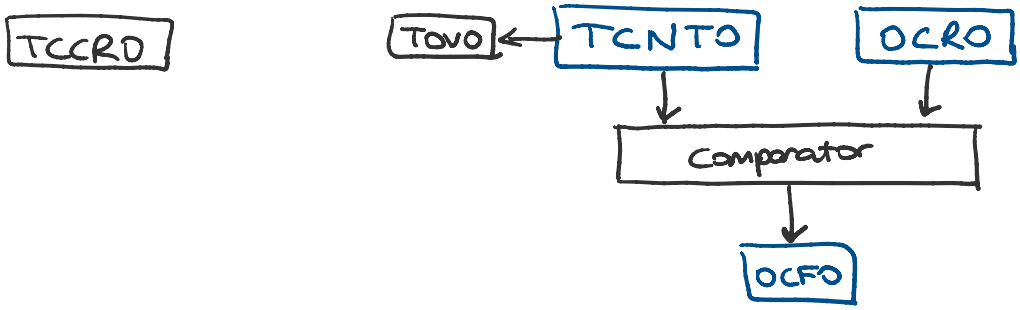
* Bit 7, 4, 3, 1 : OCF2, 1A, 1B & 0 (Output Compare Flag)
  → Set when TCNTn matches OCRn

* **Bit 6,2,0 : TOV 2, 1 & 0** (Timer Overflow Flag)
  - Set when Timer n overflows.

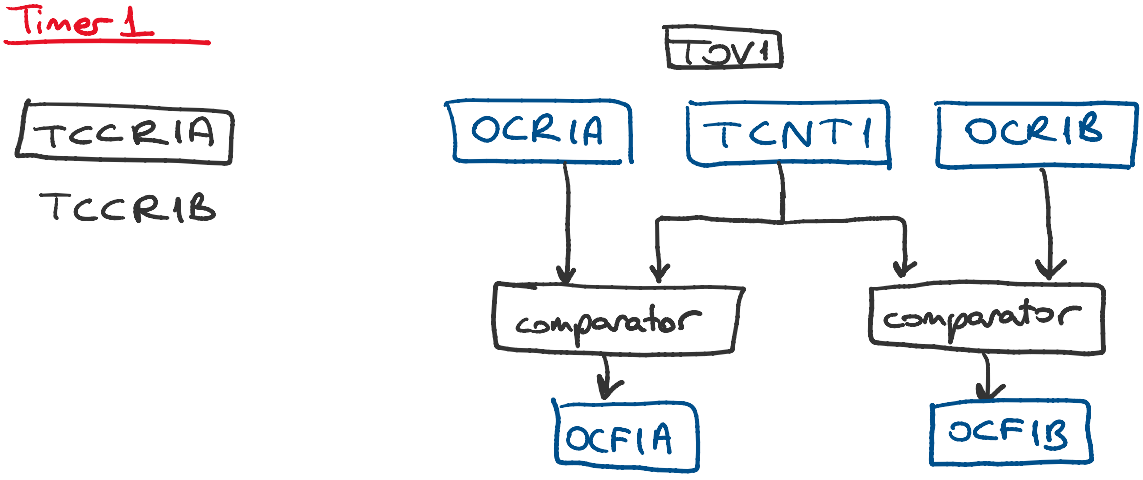
* **Bit 5 : ICF 1** (Input Capture Flag for Timer 1)
  - Indicates an input capture event occured.

Note: ATmega series of AVR chips have three timers.
- 2 with 8-bit (256 step)
- 1 with 16-bit (65356 step)

Timer 0



Timer 1



Timer 2