SPI REGISTERS

10 Kasım 2024 Pazar 02:13

1- SPI CONTROL REGISTER: SPCR

7	6	5	4	3	2	1	0	
SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

* **Bit7: SPIE** (SPI Interrupt Enable)
  - 1: enable interrupts
  - 0: disable interrupts

* **Bit6: SPE** (SPI Enable)
  - 1: enable SPI
  - 0: disable SPI

* **Bit5: DORD** (Data Order)
  - 1: transmit LSB first (start from right) R
  - 0: transmit MSB first (start from left) L

* **Bit 4: MSTR** (Master / Slave Select)
  - 1: Master mode
  - 0: Slave mode

* **Bit3: CPOL** (Clock Polarity)
  - 1: SCK (CLK) is high when the bus is idle (boş)
  - 0: SCK (CLK) " low " " " " "

CPOL	Leading Edge	Trailing Edge
0	Rising	Falling
1	Falling	Rising

* **Bit 2 : CPHA** (Clock Phase)
  - 1: Sample is taken from Trailing Edge
  - 0: " " " " Leading Edge

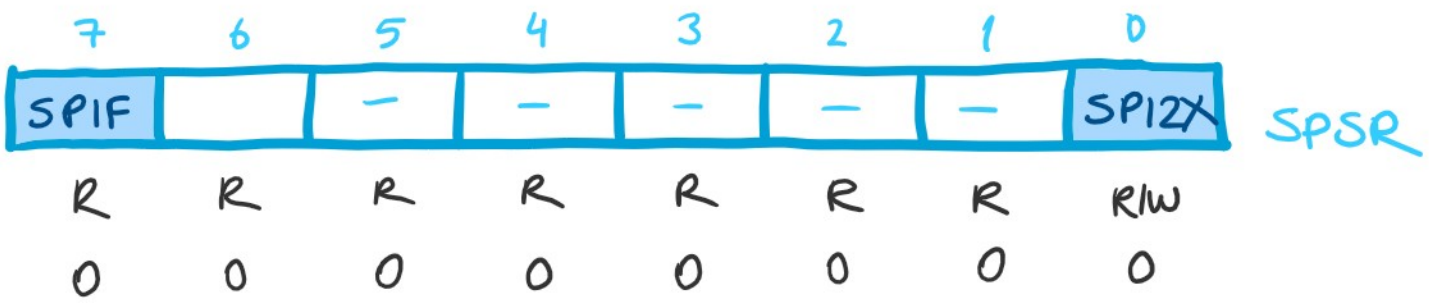
CPHA	Leading Edge	Trailing Edge
0	Sample	Setup
1	Setup	Sample

* **Bit 1,0 : SPR1, SPR0** (SPI Clock Rate Select)

These bits along w/ SPI2X bit in the SPSR register are used to choose the oscillator frequency divider.
f_{osc} = internal clock / freq. of the crystal

SPI2X	SPR1	SPR0	SCK Frequency
0	0	0	$\frac{f_{osc}}{4}$
0	0	1	$\frac{f_{osc}}{16}$
0	1	0	$\frac{f_{osc}}{64}$
0	1	1	$\frac{f_{osc}}{128}$
1	0	0	$\frac{f_{osc}}{2}$
1	0	1	$\frac{f_{osc}}{8}$
1	1	0	$\frac{f_{osc}}{32}$
1	1	1	$\frac{f_{osc}}{64}$

2- SPI STATUS REGISTER: SPSR



* **Bit7: SPIF** (SPI Interrupt Flag)
  - 1: serial transfer is complete
  - 0: " " " not "

* **Bit0: SPI2X** (SPI Double Speed Mode)
  - 1: double speed mode
  - 0: normal mode

3- SPI DATA REGISTER: SPDR