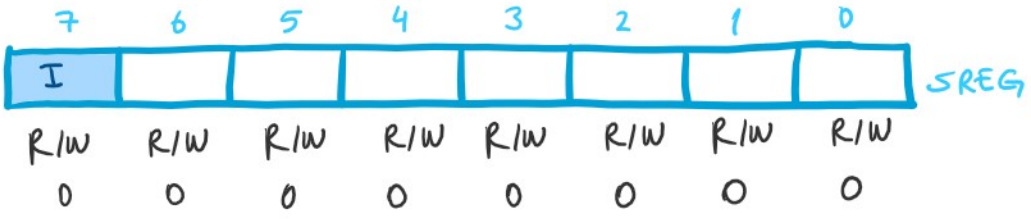
ISR REGISTERS

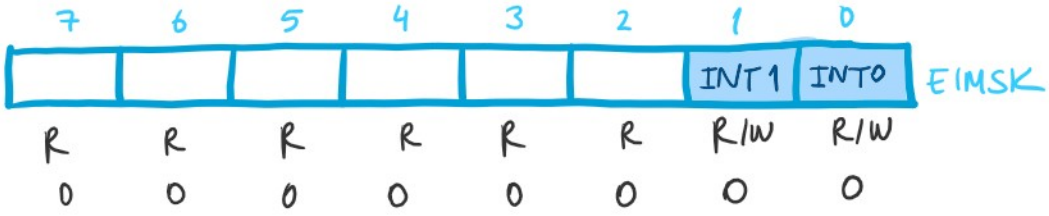
3 Aralık 2024 Salı 16:22

1 - AVR STATUS REGISTER: SREG



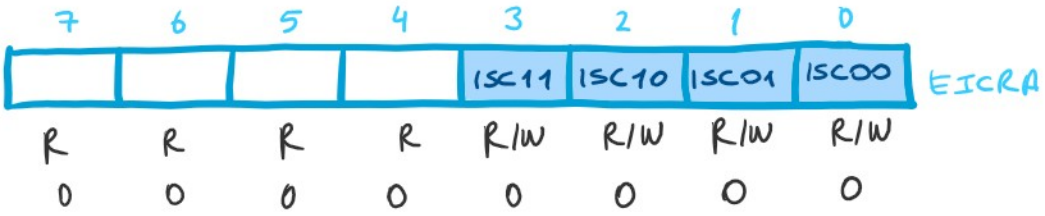
* Bit7: I (Interupt)
  - 0: All interrupts are disabled.
  - 1: Enables interrupts whose respective flag bits are set.

2 - EXTERNAL INTERRUPT MASK REGISTER: EIMSK



* Bit1 & Bit2 : INT1 & INT0
  - 0: Disables external interrupts.
  - 1: Enables " " .(requires I bit in SREG to be set.)

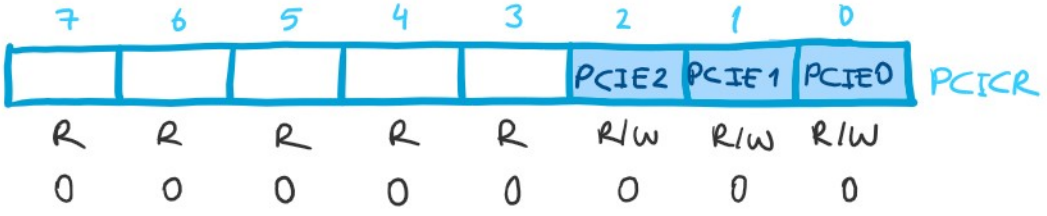
3 - EXTERNAL INTERRUPT CONTROL REGISTER A: EICRA



ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 " " " "
1	1	" rising " " INT1 " " " "

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 " " " "
1	1	" rising " " INT0 " " " "

4- PIN CHANGE INTERRUPT CONTROL REGISTER: PCICR



* Enables specific banks for pin change interrupts:

Bank #	Pins	PCIEn
Bank 0	PB0 - PB7	PCIE0
Bank 1	PC0 - PC7	PCIE1
Bank 2	PD0 - PD7	PCIE2

* Pin 2, 1 & 0: PCIE 2, 1 & 0 (Pin Change Interrupt Enable)
  - 0: Disable specific bank.
  - 1: Enable " ".

5- PIN CHANGE MASK REGISTERS: PCMSKn

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7	6	5	4	3	2	1	0	
7	6	5	4	3	2	PCINT1	PCINT0	PCMSK0 → PortB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	
7	6	5	4	3	2	1	0	
–	14	13	12	11	10	9	8	PCMSK1 → PortC
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	
7	6	5	4	3	2	1	0	
23	22	21	20	19	18	17	16	PCMSK2 → PortD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

All pins are named PCINT - just their number is different -

* 24 Pins: PCINTn (Pin Change Interrupts)
  - 0: Disabled, changes on the pin will not trigger an interrupt.
  - 1: Enabled, any change in the pin state (High to Low / Low 2 H) will trigger an interrupt.