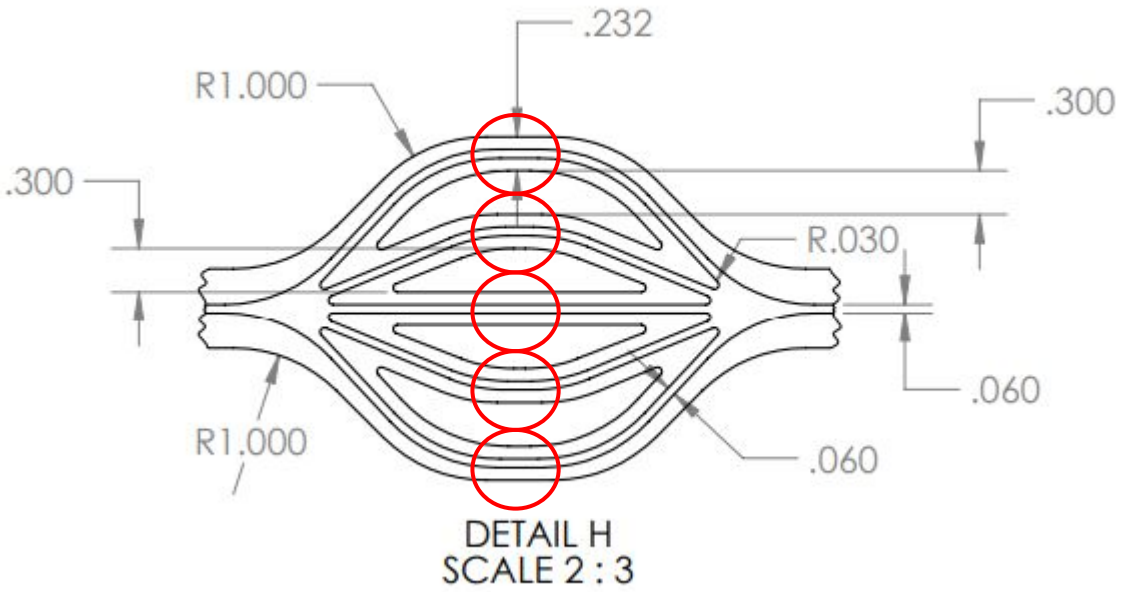
UROP S24

Vanessa Sanchez

The objective of this project is to support Richard's experimental findings.



Solving Our Circuit

Symbolic **C**ircuit **A**nalysis in **M**atlab

The A Matrix:

- (*n*+*m*)×(*n*+*m*) matrix consisting of known quantities.

The x Matrix:

- (*n*+*m*)×1 vector of **unknowns** (**node voltages**, currents through voltage sources)

The z Matrix:

- (*n*+*m*)×1 vector of known quantities (independent current and voltage sources)

We can solve a circuit with the simple matrix manipulation: $x = A^{-1}z$

Struggles

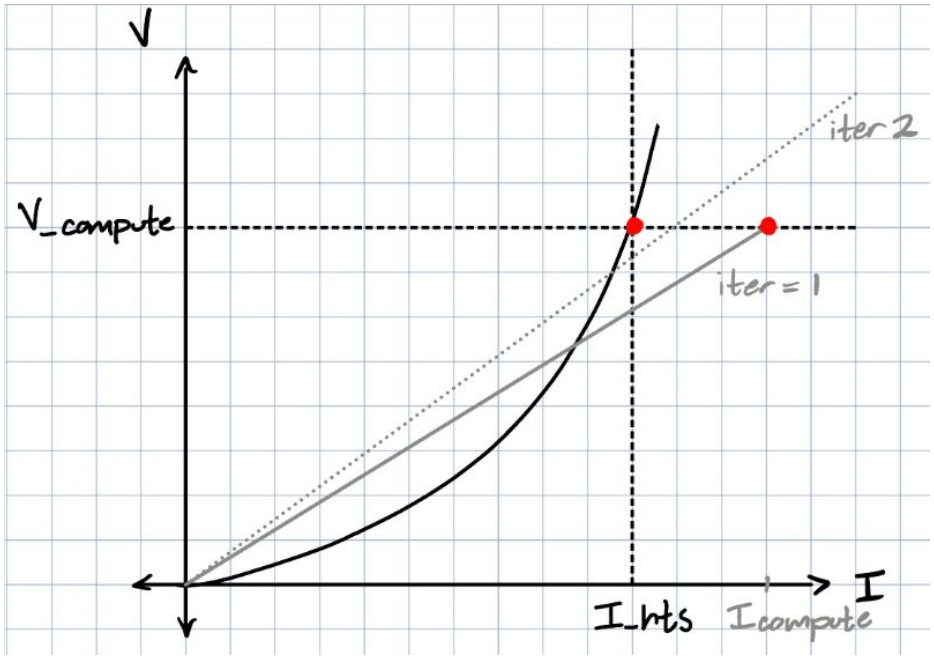
Early Attempts

- Simulink
  - Difficult to work with variable resistors
- Manual Nodal Analysis
  - Not efficient

Code Modifications

- Computational complexity
  - Symbolic analysis became difficult with a 5x5 circuit
- NaN
  - Uniform voltage readings

Updating Resistors



$$\frac{V_{\text{compute}}}{R_{\text{old}}} = I_{\text{compute}}$$

$$V_{\text{compute}} = V_c \left(\frac{I_{\text{HTS}}}{I_c} \right)^n$$

$$I_{\text{HTS}} = I_c \left(\frac{V_{\text{compute}}}{V_c} \right)^{\frac{1}{n}}$$

$$R_{\text{new}} = R_{\text{old}} \left(\frac{I_{\text{compute}}}{I_{\text{HTS}}} \right)$$

Check for convergence

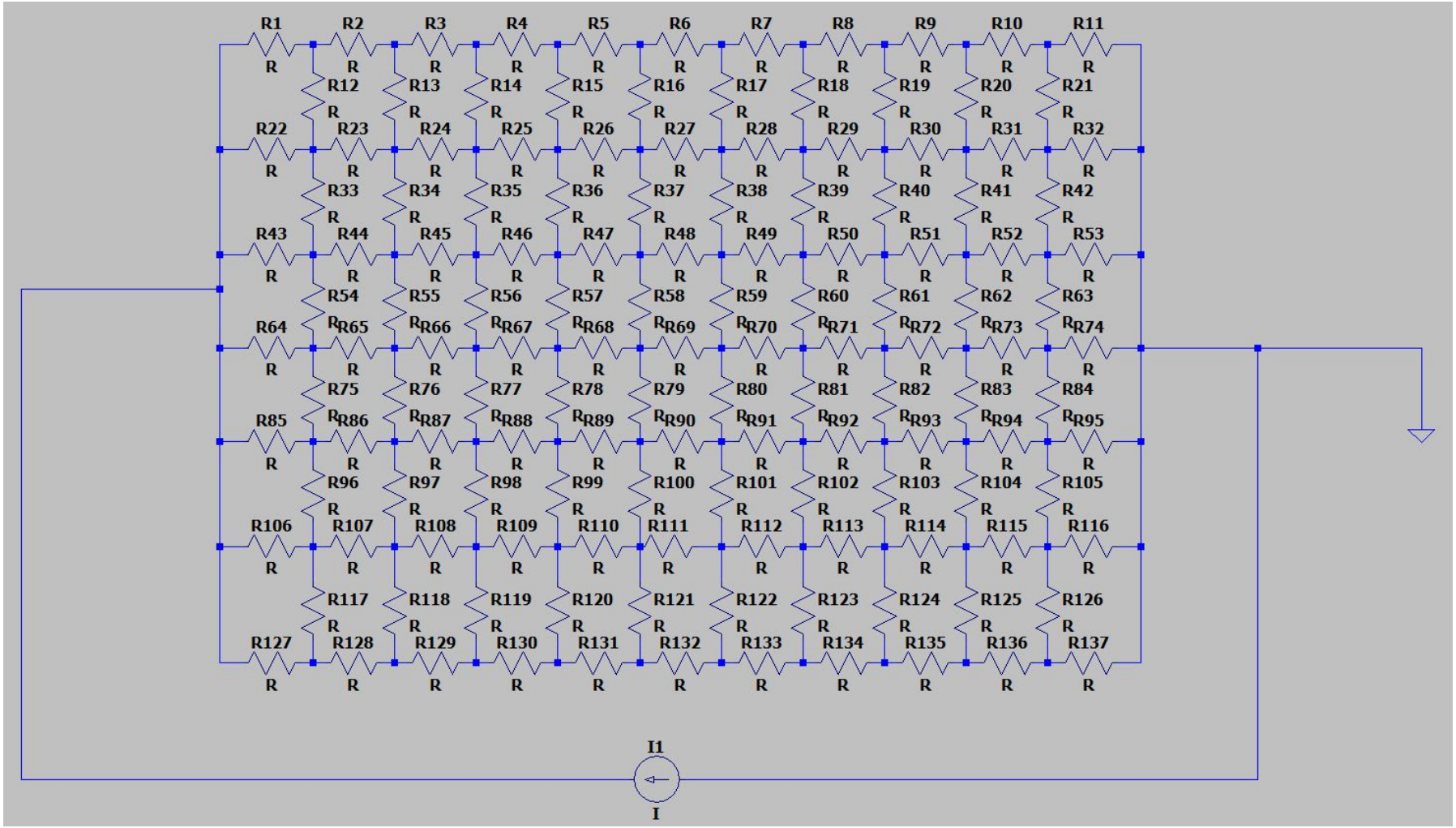
Inputs

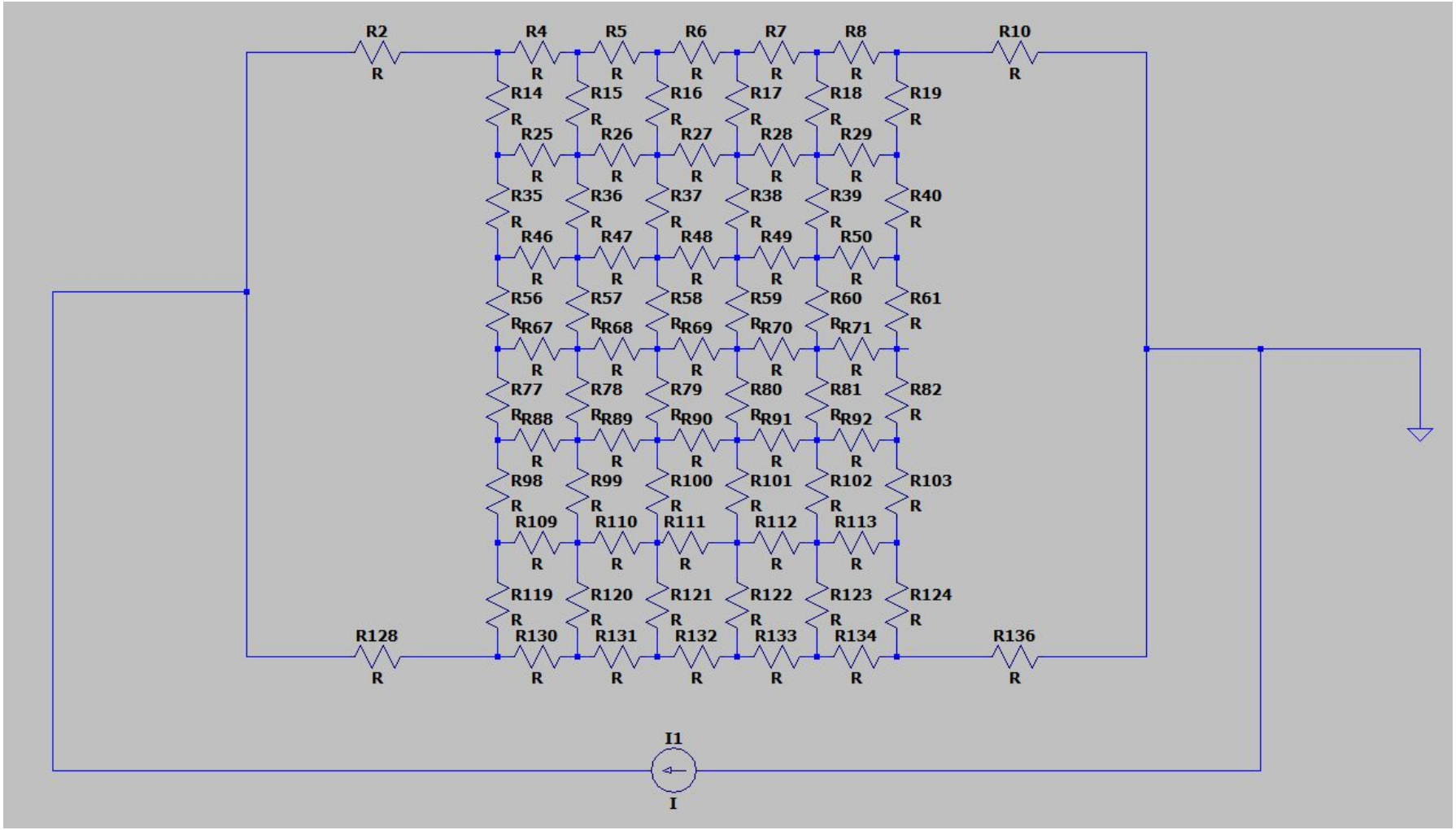
LTSpice Netlist

- Standardized approach that allows for expansion into LTSpice

SPICE Netlist: C:\Users\Vaness Sanchez\Documents\LTspiceXVII\no_block_copy.net

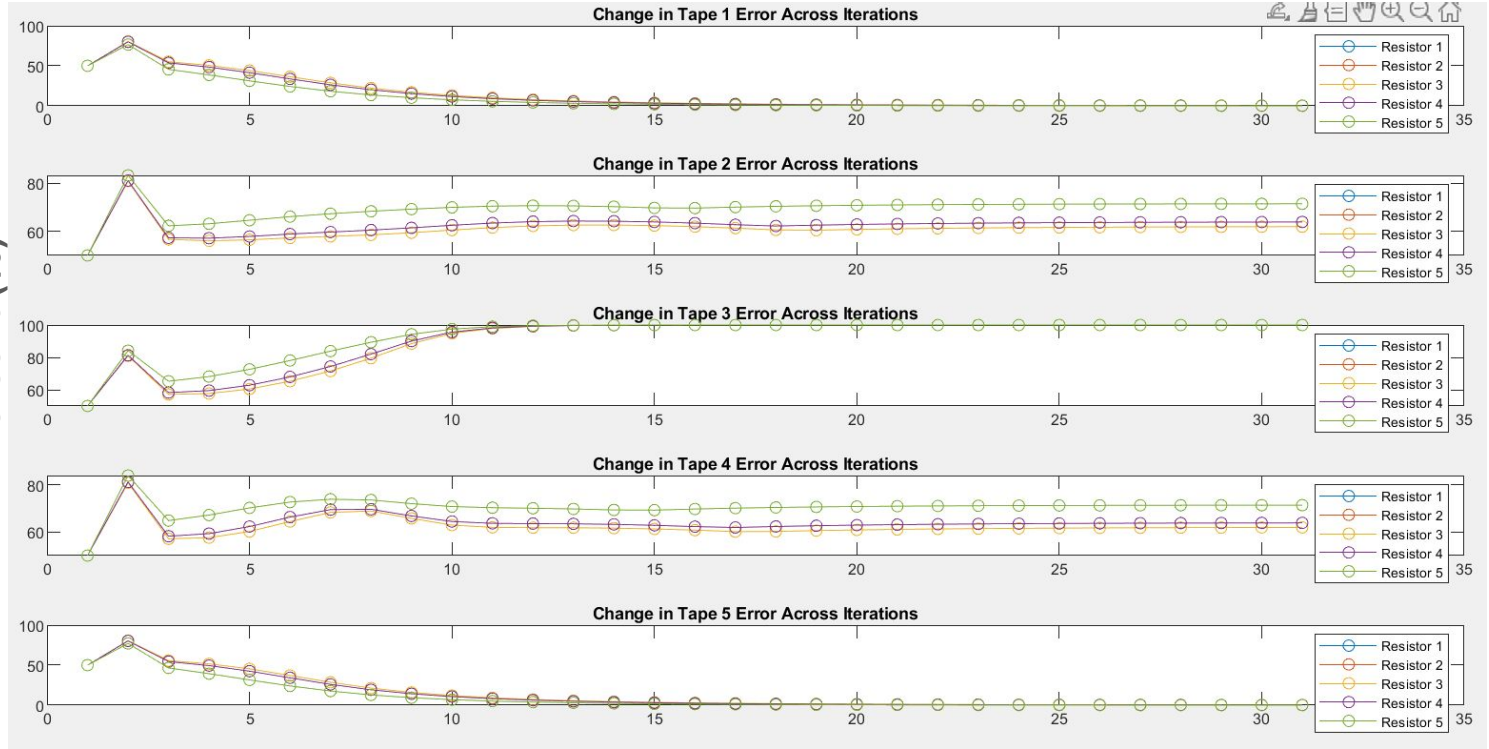
```
* C:\Users\Vaness Sanchez\Documents\LTspiceXVII\no_block_copy.asc
R4 N003 N002 R
R5 N004 N003 R
R6 N005 N004 R
R7 N006 N005 R
R8 N007 N006 R
R15 N003 N009 R
R16 N004 N010 R
R17 N005 N011 R
R18 N006 N012 R
R25 N009 N008 R
R26 N010 N009 R
R27 N011 N010 R
R28 N012 N011 R
R29 N013 N012 R
R36 N009 N015 R
R37 N010 N016 R
R38 N011 N017 R
```


R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11
R12 R13 R14 R15 R16 R17 R18 R19 R20 R21
R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32
R33 R34 R35 R36 R37 R38 R39 R40 R41 R42
R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53
R54 R55 R56 R57 R58 R59 R60 R61 R62 R63
R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74
R75 R76 R77 R78 R79 R80 R81 R82 R83 R84
R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95
R96 R97 R98 R99 R100 R101 R102 R103 R104 R105
R106 R107 R108 R109 R110 R111 R112 R113 R114 R115 R116
R117 R118 R119 R120 R121 R122 R123 R124 R125 R126
R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137
I1
I


R2
R4
R5
R6
R7
R8
R10
R14
R15
R16
R17
R18
R19
R25
R26
R27
R28
R29
R35
R36
R37
R38
R39
R40
R46
R47
R48
R49
R50
R56
R57
R58
R59
R60
R61
R67
R68
R69
R70
R71
R77
R78
R79
R80
R81
R82
R88
R89
R90
R91
R92
R98
R99
R100
R101
R102
R103
R109
R110
R111
R112
R113
R119
R120
R121
R122
R123
R124
R128
R130
R131
R132
R133
R134
R136
I1
I

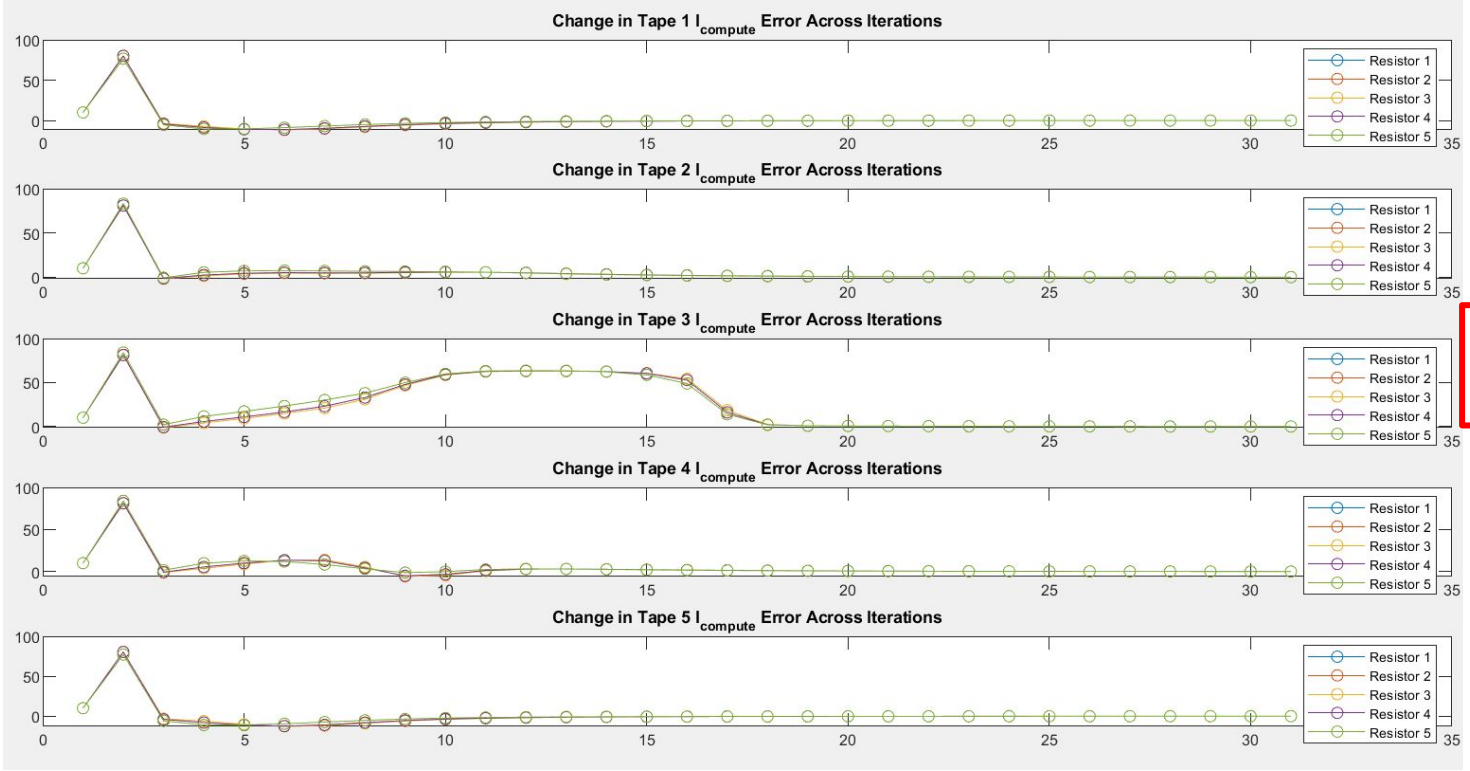
Graphical Validation

Convergence Method 1



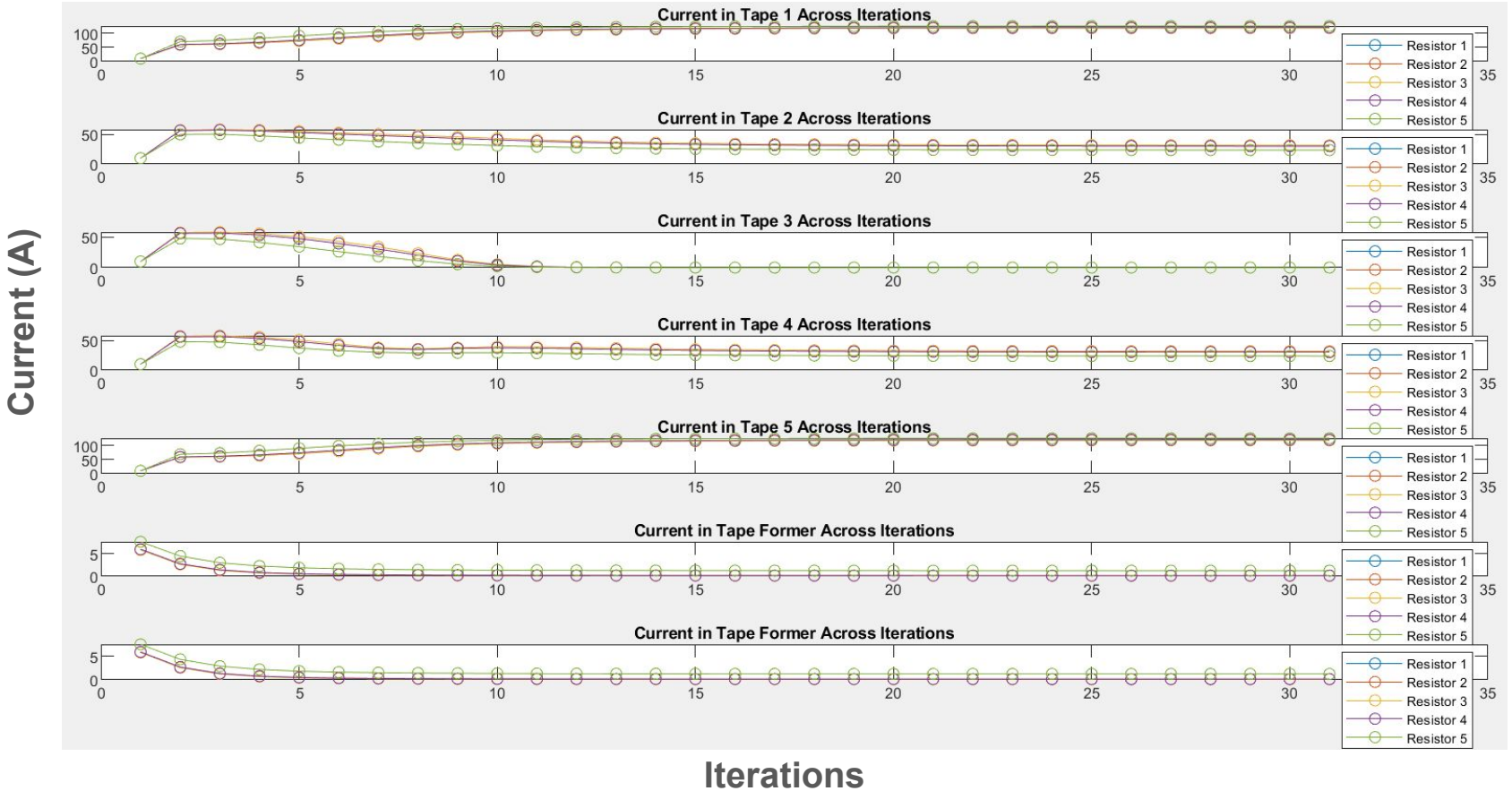
$$\left(\frac{I_{\text{hts old}}(i,j) - I_{\text{compute}}}{I_{\text{hts old}}(i,j)}\right) \times 100$$

Convergence Method 2



$$\left(\frac{I_{\text{compute old}}(i,j) - I_{\text{compute}}}{I_{\text{compute old}}(i,j)}\right) \times 100$$

Converged Current Values

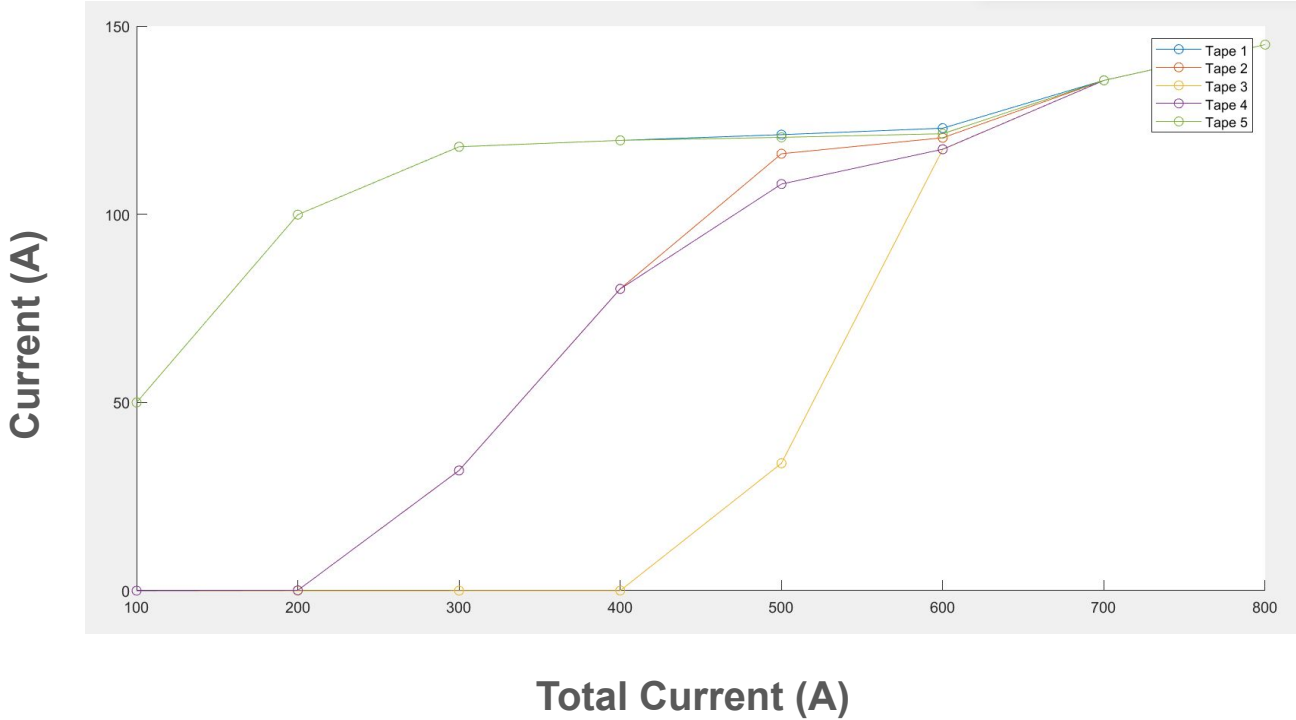


Interpreting Results

Results

No Defect

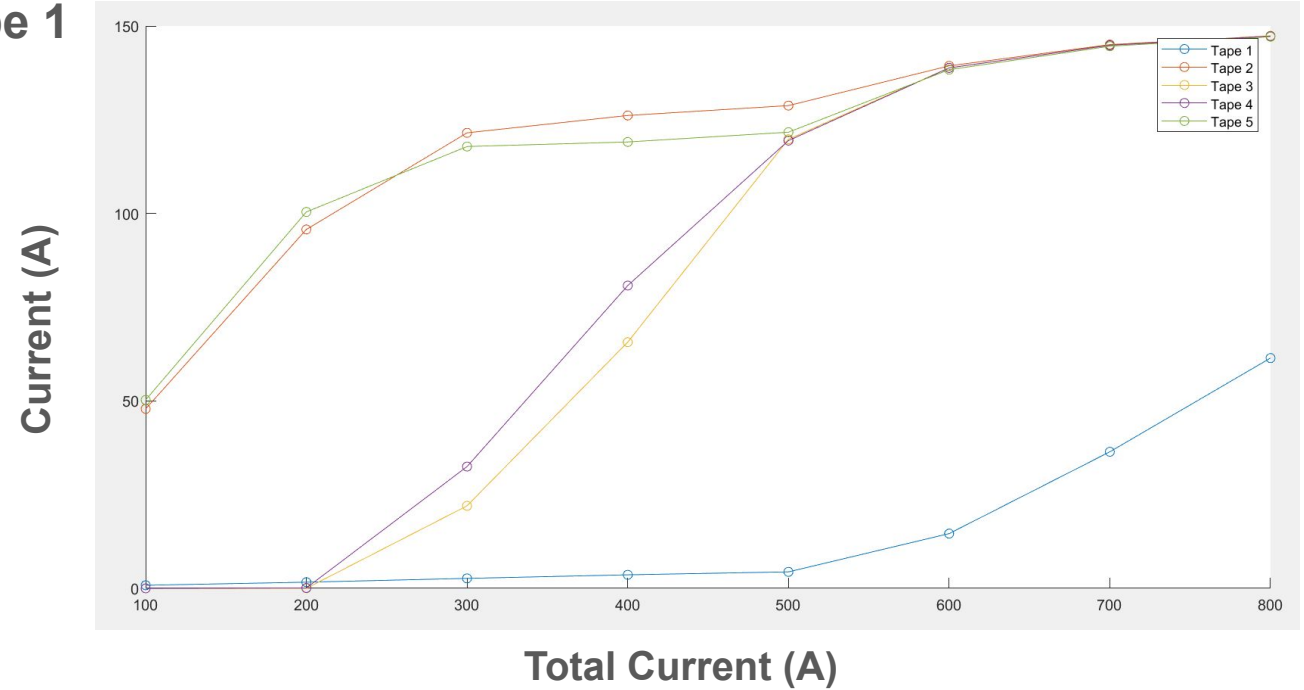
Slice 3 screenshot



Results

Defect in Resistor 3, Tape 1

Slice 3 screenshot



GUI

For a more comprehensive understanding of the results, I created a GUI!