Digital and Comp Org: Another Perspective

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About me

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- Taeyeon CPE31 , Hwang Jisung
- Computer Engineer Student, Kasetsart University
- Interesting in computer system and computer architecture
- Love K-pop [Wanna One / NU’EST / X1 ‘s fanboy]

How do computers really work??

- A question in my mind …
- That’s why i wanted to learn in computer major… so, I study here
- computer architecture answers me 70% of what i’m curious

Outline

- Basic Digital Design
  - Combinational logic circuit / Sequential logic circuit
  - ALU / Memory (RAM,ROM,Register)
  - Logism
- Processor design and simulation
  - ISA (Instruction Set Architect) : Minimal MIPS
  - Minimal MIPS Datapath
  - Real Word Architect : MIPS x86

Basic Digital Design

Combinational Logic Circuit

- A circuit is a network that processes discrete-valued variables, can be viewed as a black block.
- Combinational circuit's output depends only on the current value.
- Boolean equations are perfect for describing digital logic.
    - Sum-of-Product
    - Product-of-Sum
    - Boolean algebra are used to simplify boolean expression
        - Axioms table
        - K-map

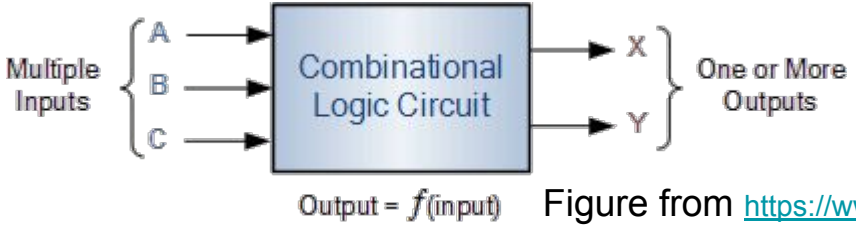
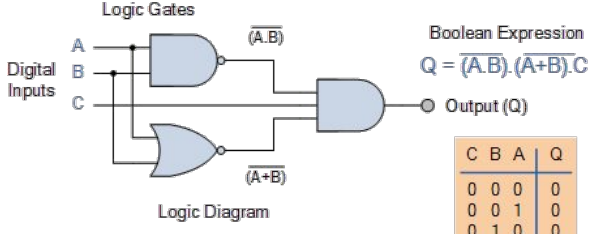


Figure from https://www.electronics-tutorials.ws/combination/comb_1.html



Typical Truth Table

C	B	A	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Classification of Combinational Logic Circuit

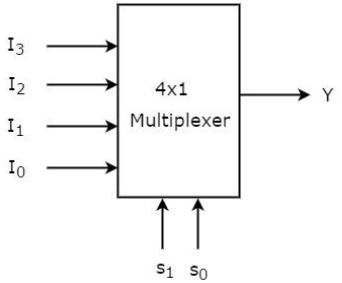
- Arithmetic & Logical Function
  - ALU in processor
- Data Transmission
  - MUX / DEMUX
  - Encoder / Decoder
- Code Converter
  - 7-segment
- Any Function
  - F(Input) = Output

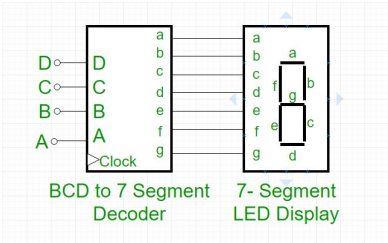
Arithmetic & Logic Function

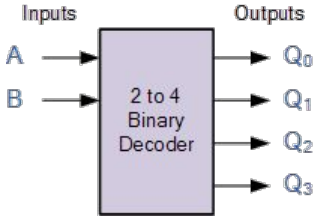
- Adder
  - Half / Full / Carry Propagate / Ripple-carry / Carry-Lookahead
- Substractor
- Comparator

Data Transmission & Code Convertor

- MUX/DEMUX
  - MUX 2 power n inputs, 1 output : Shannon's equation
  - DEMUX 1 input, 2 power n outputs
- Decoder/Encoder
- 7 segment

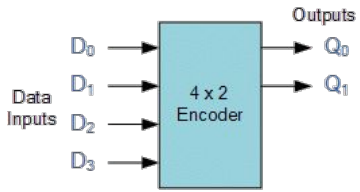






Truth Table

A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Figure from https://www.electronics-tutorials.ws/sequential/seq_1.html
https://www.geeksforgeeks.org/digital-electronics-bcd-7-segment-decoder/

Hardware Description Language

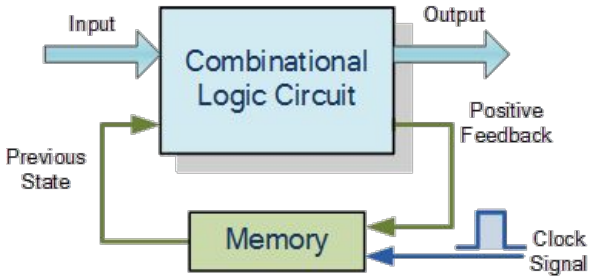
- The language to describe hardware in Module
- HDL is a specialized computer language used to describe the structure and behavior of electronic circuits, and most commonly, digital logic circuits. [Wikipedia]
- VHDL and System Verilog

Try to play : 4-bits Simple ALU

- Combining arithmetic & logic function, data transmission and code converter to simple ALU circuit
- ALU = Arithmetic & Logic Unit : essential to use for executing in processor

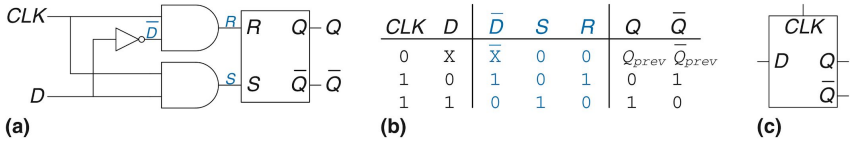
Sequential Logic Circuit

- Unlike Combinational Logic circuits that change state depending upon the actual signals being applied to their inputs at that time, Sequential Logic circuits have some form of inherent “Memory” built in.
- Synchronous Sequential Logic Circuit deals with Clock signal
- Latch and Flip-Flop are basic “Memory” element.
  - Keep the state
- Synchronus Design Method : FSM (Mearly/Moore)



Latch/Flip-Flop and Register

- bistable element, an element with two stable states
- Flip-Flop [D Flip-Flop, T Flip-Flop, JK Flip-Flop]
- D Flip-Flop can be built from two back-to-back D latches controlled by complementary clock
  - In this slide, I will mention a detail only D flip/flop
- Register is a bank of D Flip-Flop share a common CLK
  - so that all bits are updated on the same time



CLK	D	$\bar{D}$	S	R	Q	$\bar{Q}$
0	X	$\bar{X}$	0	0	Q_{prev}	$\bar{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

Figure 3.7 D latch: (a) schematic, (b) truth table, (c) symbol

Figure from David Money H. & Sarah L.H. ,Digital Design and Computer Architecture (2nd Edition)

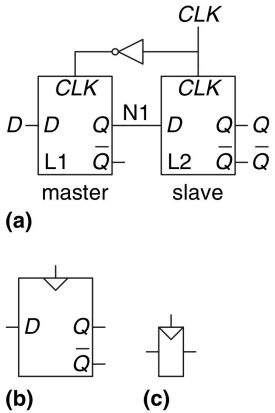
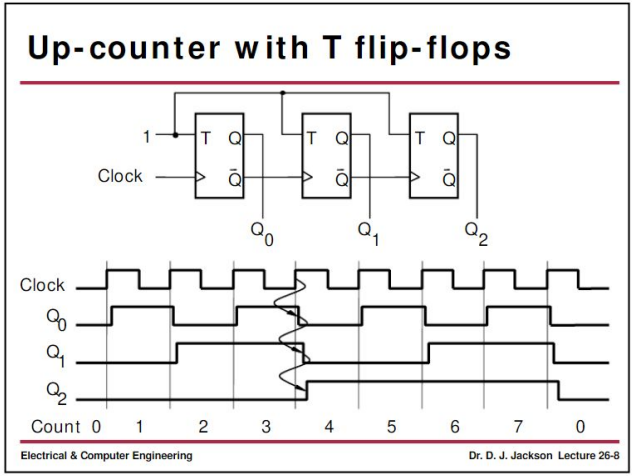


Figure 3.8 D flip-flop: (a) schematic, (b) symbol, (c) condensed symbol

Counter / Shifter

- Use flip-flop (and also clock signal) to implement
- Counter
  - To increment or decrement by 1
  - Often use T flip-flop because a toggle feature
- Shifter



Memory

- Register : a bank of D Flip-Flop share a common CLK
- ROM : Read-Only Memory
  - Control Unit of processor
- RAM : Random Access Memory
  - Memory unit in processor

n bit Register file

- a set of n registers size 32 bits
- MIPS first hierachy memory
  - close to processor the most

FIGURE C.8.7 A register file with two read ports and one write port has five inputs and two outputs. The control input Write is shown in color.

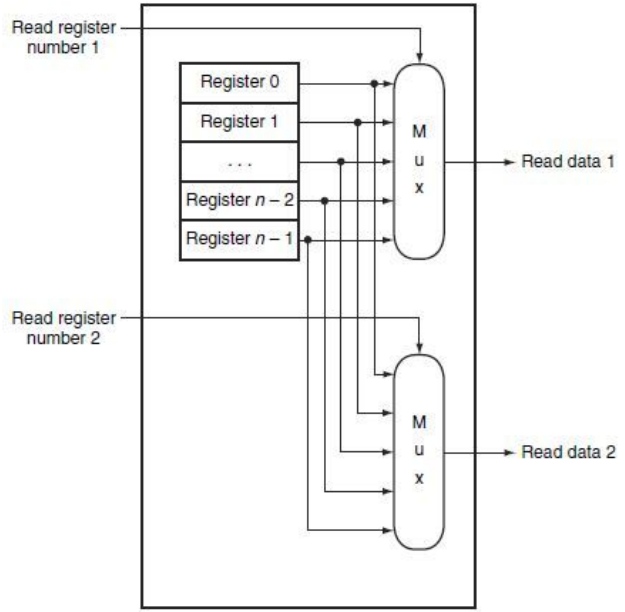


FIGURE C.8.8 The implementation of two read ports for a register file with *n* registers can be done with a pair of *n*-to-1 multiplexors, each 32 bits wide. The register read number signal is used as the multiplexor selector signal. Figure C.8.9 shows how the write port is implemented.

Try to play : 4-bits Simple ALU with Input Memory

- Combining arithmetic & logic function, data transmission and code converter to simple ALU circuit
- Including “Memory” keeping the input. Output changes every falling edge trigger

Processor design and simulation

Processor

- Essential computing components of computer
- Basicly consists of ALU , Memory and Control Unit

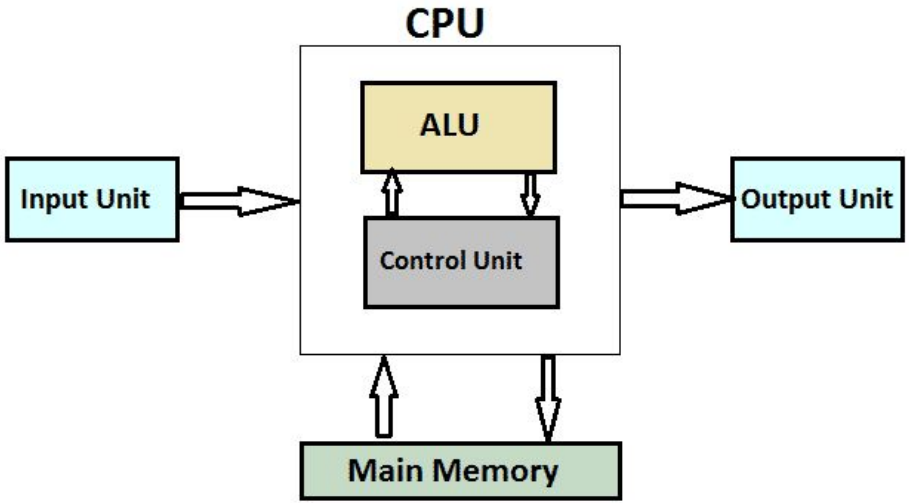


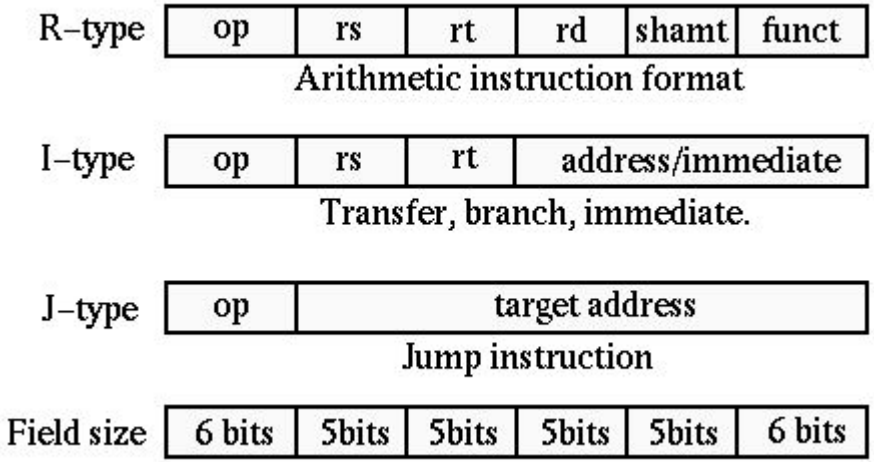
Figure from https://www.it4nextgen.com/what-is-a-cpu-central-processing-unit/

Instruction Set Architecture

- If we have any processor (in form black box), how can you instruct it to do on your demand… what you would like instruct it… it’s instruction …
- An instruction set architecture (ISA) is an abstract model of a computer. It is also referred to as architecture or computer architecture.
- A realization of an ISA is called an implementation. (Wikipedia)

MIPS ISA

- 32-bit Instruction (32-bit 0f 01's)



add $1, $2, $3

addi $1, $2, 0x10

j 0x00000010

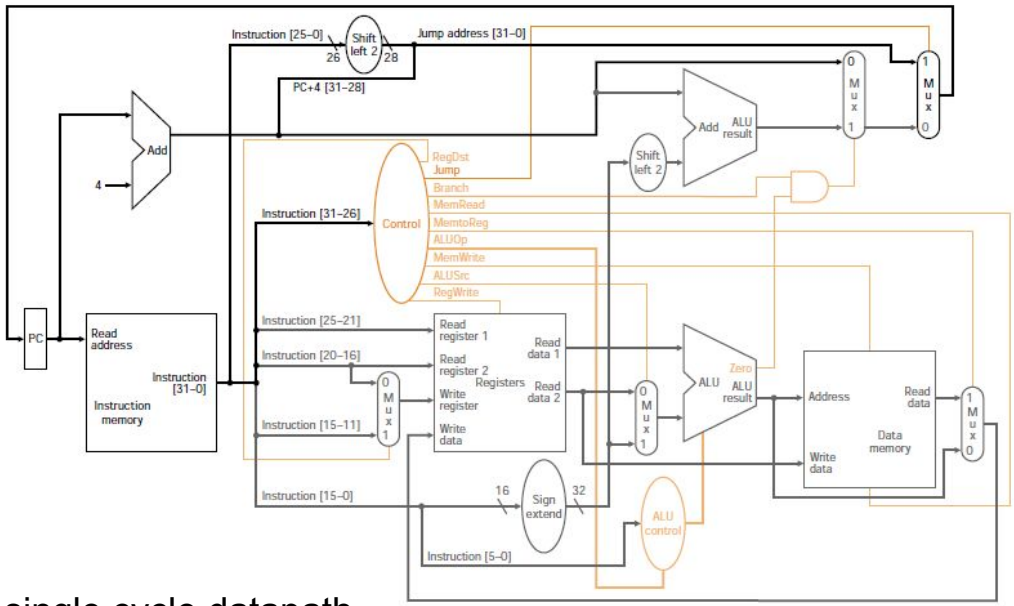
More detail in 01204225 >>

Minimal MIPS Processor

- Minimal version of MIPS (define for this lecture only)
  - MIPS (Microprocessor without Interlocked Pipelined Stages) is a reduced instruction set computer (RISC) instruction set architecture (ISA)
    - detail more in 01204225
- consists of only 5 instructions
  - addu / addiu
  - beq
  - and / andi
- MIPS assembly
  - addu $1, $2, $3 # $1 = $2 + $3
  - addiu $1, $2, 0x10 # $1 = $2 + 0x10
  - beq $1, $2, 0xf8 # branch to PC = PC+4+0xf8 if $1 == $2
  - and $1, $2, $3 # $1 = $2 && $3 (bitwise)
  - andi $1, $2, 0x10 # $1 = $2 && 0x10 (bitwise)

Minimal MIPS single cycle datapath

- 1 instruction per 1 clock cycle



More detail in 01204225 >>

Design a single cycle datapath
https://cseweb.ucsd.edu/classes/su06/cse141/slides/s05-1cyc_data-1up.pdf

Try to implement : Processor implementation

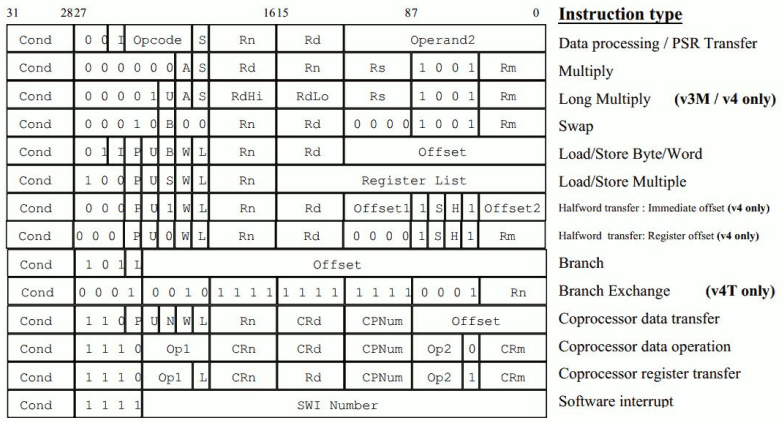
Download mininal_MIPS_single_cycle on http://bit.ly/2pvuG2E

, then follow me to implement

Real Life Architecture

- MIPS
- ARM : Advance RISC Machine
  - Microprocessor and microcontroller
- X86 : Intel CPU More detail >> https://cs.lmu.edu/~ray/notes/x86overview/

ARM Instruction Set Format



Textbook I recommend

- David Money H. & Sarah L.H. ,Digital Design and Computer Architecture (2nd Edition)
- M. Morris M. & Michael D. C ,Digital Design With An Introduction to the Verilog HDL (5th Edition)
- David A. P. & John L. H. ,Compter Organization and Design (5th Edition)