References

- [1] Wireless Semiconductors Market Report, Databeans, 2010.
- [2] G. Purdy, 2010 Outlook & Forecast: Mobile & Wireless Communications, http://www.slideshare.net/FrostandSullivan/2010-outlook-forecast-mobile-wireless-communications, 2009.
- [3] G. Karmakar and L. S. Dooley (Editors), *Mobile Multimedia Communications: Concepts, Applications, and Challenges*, IGI Global, 2008.
- [4] D. Rouffet and P. Sehier, "Convergence and competition on the way towards 4g," in *Proc. of IEEE Radio and Wireless Symposium*, 2007, pp. 277–280.
- [5] G. Delagi, "Harnessing technology to advance the next-generation mobile user-experience," in IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010, pp. 18 –24.
- [6] Ian Kuan and Jonathan Rose, "Measuring the gap between FPGAs and ASICs," in *International Symposium on Field Programmable Gate Arrays*, Feb. 2006.
- [7] R. Tessier, S. Swaminathan, R. Ramaswamy, D. Goeckel, and W. Burleson, "A reconfigurable, power-efficient adaptive viterbi decoder," *IEEE Transactions on VLSI Systems*, vol. 13, no. 4, pp. 484–488, Apr. 2005.
- [8] C. Liang and X. Huang, "SmartCell: An Energy Efficient Coarse-Grained Reconfigurable Architecture for Stream-Based Applications," EURASIP Journal on Embedded Systems, Jan. 2009.
- [9] K. Eguro and S. Hauck, "Issues and approaches to coarse-grain reconfigurable architecture development," in *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines*, Apr. 2003, pp. 111–120.
- [10] C.H. Lam, "The quest for the universal semiconductor memory," in *Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits*, Dec. 2005, pp. 327–331.
- [11] K. Kim and G. Jeong, "Memory technologies for sub-40nm node," in *Proc. of IEEE International Electron Devices Meeting (IEDM)*, Dec. 2007, pp. 27–30.
- [12] J.A. Hutchby, R. Cavin, V. Zhirnov, J.E. Brewer, and G. Bourianoff, "Emerging nanoscale memory and logic devices: A critical assessment," *Computer*, vol. 41, pp. 28–32, May 2008.
- [13] F. Bedeschi, R. Fackenthal, C. Resta, E.M. Donze, M. Jagasivamani, E.C. Buda, F. Pellizzer, D.W. Chow, A. Cabrini, G. Calvi, R. Faravelli, A. Fantini, G. Torelli, D. Mills, R. Gastaldi, and G. Casagrande, "A bipolar-selected phase change memory featuring multi-level cell storage," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 217–227, Jan. 2009.
- [14] R. Bez, "Chalcogenide PCM: A memory technology for next decade," in *Proc. of IEEE International Electron Devices Meeting (IEDM)*, Dec. 2009.
- [15] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y.-C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.-L. Lung, and C. H. Lam, "Phase-change random access memory: a scalable technology," *IBM Journal of Research and Development*, vol. 52, pp. 465–479, July 2008.

- [16] F. Bedeschi et al., "A multi-level-cell bipolar-selected phase-change memory," in *International Solid-State Circuits Conference*, San Francisco, US, Feb. 2008, pp. 428–625.
- [17] T. Nirschl et al., "Write strategies for 2 and 4-bit multi-level phase-change memory," in *International Electron Devices Meeting (IEDM)*, Washington D.C., US, Dec. 2007, pp. 461–464.
- [18] S. Kang et al., "A 0.1-μm 1.8-V 256-Mb phase-change random access memory (PRAM) with 66-MHz synchronous burst-read operation," *Journal of Solid-State Circiuts*, vol. 42, pp. 210–218, Jan. 2007.
- [19] H. Oh et al., "Enhanced write performance of a 64-Mb phase-change random access memory," *Journal of Solid-State Circiuts*, vol. 41, pp. 122–126, Jan. 2006.
- [20] K. Osada et al., "Phase change RAM operated with 1.5-V CMOS as low cost embedded memory," in *Custom Integrated Circuits Conference*, San Jose, US, Sept. 2005, pp. 431–434.
- [21] A. Driskill-Smith et al., "Non-volatile spin-transfer torque ram (stt-ram): An analysis of chip data, thermal stability and scalability," in *Memory Workshop (IMW), 2010 IEEE International,* 2010, pp. 1–3.
- [22] E. Chen et al., "Advances and future prospects of spin-transfer torque random access memory," *Magnetics, IEEE Transactions on*, vol. 46, no. 6, pp. 1873–1878, june 2010.
- [23] A. Raychowdhury, D. Somasekhar, T. Karnik, and V. De, "Design space and scalability exploration of 1t-1stt mtj memory arrays in the presence of variability and disturbances," in *Electron Devices Meeting* (*IEDM*), *IEEE International*, 2009, pp. 1 –4.
- [24] K.-T. Nam et al., "Switching properties in spin transper torque MRAM with sub-50nm MTJ size," in *Proc. of the 7th Annual Non-Volatile Memory Technology Symposium (NVMTS)*, Nov. 2006, pp. 49–51.
- [25] M. Hosomi et al., "A novel nonvolatile memory with spin torque transfer magnetization switching: spin-RAM," in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 459–462.
- [26] T. Keller and L. Hanzo, "Adaptive multicarrier modulation: a convenient framework for time-frequency processing in wireless communications," *Proceedings of the IEEE*, vol. 88, pp. 611–640, 2000.
- [27] R. Becher, M. Dillinger, M. Haardt, and W. Mohr, "Broadband wireless access and future communication networks," *Proceedings of the IEEE*, vol. 89, pp. 58–75, 2001.
- [28] P.F. Marshall, "Extending the reach of cognitive radio," *Proceedings of the IEEE*, vol. 97, pp. 612–625, 2009.
- [29] J. Hagenauer, "The Turbo principle: Tutorial introduction and state of the art," in *Proc. of the International Symposium on Turbo Codes*, Sept. 1997, pp. 1–11.
- [30] M. Shafi et al. (ed.), "Special Issues on MIMO Systems and Applications (I/II)," *IEEE Journal on Selected Areas in Communications*, vol. 21, April/June 2003.
- [31] N. Jayant (ed.), "Special Issue on Gigabit Wireless," Proceedings of the IEEE, vol. 92, Feb. 2004.
- [32] J. Chen, A. Dholakia, E. Eleftheriou, M.P.C. Fossorier, and Xiao-Yu Hu, "Reduced-Complexity Decoding of LDPC Codes," *IEEE Transactions on Communications*, vol. 53, pp. 1288–1299, Agu. 2005.
- [33] Z. Guo and P. Nilsson, "Algorithm and implementation of the k-best sphere decoding for mimo detection," *IEEE Journal on Selected Areas in Communication*, vol. 24, pp. 491–503, March 2006.

- [34] P. Viola and M. Jones, "Rapid object detection using a boosted cascade of simple features," in *Proc. of IEEE International Conference on Computer Vision and Pattern Recognition*, 2001, vol. 1, pp. 511–518.
- [35] H. Rowley, S. Baluja, and T. Kaneda, "Neuro network-based face detection," *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. 20, pp. 23–28, Jan 1998.
- [36] Intel Corporation, Santa Clara, CA. OpenCV Library, "http://sourceforge.net/projects/opencvlibrary,".
- [37] H. Schneiderman and T. Kanade, "A statistical method for 3d object detection applied to faces and cars," in *Proc. of IEEE Conference on Computer Vision and Pattern Recognition*, 2000, pp. 746 –751 vol.1.
- [38] H.A. Rowley, S. Baluja, and T. Kanade, "Neural network-based face detection," *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. 20, no. 1, pp. 23 –38, jan. 1998.
- [39] Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Tinoosh Mohsenin, Mandeep Singh, and Bevan Baas, "An Asynchronous Array of Simple Processors for DSP Applications," in *Proceedings: International Solid State Circuits Conference*, Feb. 2006.
- [40] I. Kuan and J. Rose, "Measuring the Gap Between FPGAs and ASICs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 2, pp. 203–215, Feb. 2007.
- [41] G. Smit, A. Kokkeler, P. Wolkotte, and M. van de Burgwal, "Multi-core architectures and streaming applications," in *Proceedings: ACM International Workshop on System-Level Interconnect Prediction*, 2009, pp. 35–42.
- [42] B. Hutchings, B. Nelson, S. West, and R. Curtis, "Optical Flow on the Ambric Massively Parallel Processor Array (MPPA)," in *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines*, Apr. 2009, pp. 141–148.
- [43] Hyun-Jin Cho, F. Nemati, R. Roy, R. Gupta, K. Yang, M. Ershov, S. Banna, M. Tarabbia, C. Sailing, D. Hayes, A. Mittal, and S. Robins, "A novel capacitor-less dram cell using thin capacitively-coupled thyristor (tcct)," in *Proc. of IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 311 –314.
- [44] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, and E. Faraoni, "New generation of z-ram," in *Proc. of IEEE International Electron Devices Meeting (IEDM)*, 2007, pp. 925 –928.
- [45] S. Natarajan, S. Chung, L. Paris, and A. Keshavarzi, "Searching for the dream embedded memory," *IEEE Solid-State Circuits Magazine*, vol. 1, pp. 34–44, 2009.
- [46] Steve Freudenberger, Tom Gross, and Pete Lowney, "Avoidance and Suppression of Compensation Code in a Trace Scheduling Compiler," *ACM Transactions on Programming Languages and Systems*, vol. 16, no. 4, pp. 1156–1214, 1994.
- [47] Michael Gordon, William Thies, Michal Karczmarek, Jasper Lin, Ali S. Meli, Chris Leger, Andrew A. Lamb, Jeremy Wong, Henry Hoffman, David Z. Maze, and Saman Amarasinghe, "A stream compiler for communication-exposed architectures," in *Proceedings of the International Symposium on Architectural Support for Programming Languages and Operating Systems*, 2002.
- [48] Actel FPGA devices, http://www.actel.com/products/devices.aspx.
- [49] Lattice Nonvolatile FPGA devices, http://www.latticesemi.com/products/fpga/index.cfm.

- [50] CACTI: An integrated cache and memory access time, cycle time, area, leakage, and dynamic power model, http://www.hpl.hp.com/research/cacti/.
- [51] D. Brooks, V. Tiwari, and M. Martonosi, "Wattch: A framework for architectural-level power analysis and optimizations," in *Proceedings of the 27th International Symposium on Computer Architecture (ISCA '00)*. June 2000, ACM Press.
- [52] Sriram Swaminathan, Russell Tessier, Dennis Goeckel, and Wa yne Burleson, "A dynamically reconfigurable adaptive Viterbi decoder," in *Proceedings, ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, Feb. 2002, pp. 227–236.
- [53] Russell Tessier and Heather Giza, "Balancing Logic Utilization and Area Efficiency in FPGAs," in 10th International Conference on Field Programmable Logic and Applications, Villach, Austria, Aug. 2000.
- [54] L. Atieno, J. Allen, D. Goeckel, and R. Tessier, "An adaptive Reed-Solomon errors-and-erasures decoder," in *Proceedings of the ACM/SIGDA International Conference on Field-Programmable Gate Arrays*, Feb. 2006.
- [55] S. Chen, F. Sun, and T. Zhang, "Nonlinear soft-output signal detector design and implementation for MIMO communication systems with high spectral efficiency," in *Proc. of IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2006.
- [56] S. Chen, T. Zhang, and M. Goel, "Relaxed tree search MIMO signal detection algorithm design and VLSI implementation," in *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006, pp. 1147–1150.
- [57] S. Chen, T. Zhang, and Y. Xin, "Relaxed K-best MIMO Signal Detector Design and VLSI Implementation," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, pp. 328–337, March 2007.
- [58] S. Chen and T. Zhang, "Low Power Soft-Output Signal Detector Design for Wireless MIMO Communication Systems," in *International Symposium on Low Power Electronics and Design (ISLPED)*, 2007.
- [59] F. Sun and T. Zhang, "Low power state-parallel relaxed adaptive Viterbi decoder," in *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006, pp. 4811–4814.
- [60] F. Sun and T. Zhang, "Low-power state-parallel relaxed adaptive Viterbi decoder," IEEE Transactions on Circuits and Systems I, vol. 54, pp. 1060–1068, May 2007.
- [61] Y. Liu, T. Zhang, and J. Hu, "Design of voltage overscaled low-power trellis decoders in presence of process variations," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, pp. 439–443, March 2009.
- [62] Y. Xin, A. Mujitaba, and T. Zhang, "Turbo- and LDPC-Coded MIMO-OFDM Systems: A Comparative Study," in Proc. of International Symposium on Personal Indoor and Mobile radio Communications (PIMRC), Sept. 2007.
- [63] Y. Xin, A. Mujitaba, T. Zhang, and J. Jiang, "Bypass Decoding A Reduced Complexity Decoding Technique for LDPC Coded MIMO-OFDM Systems," *IEEE Transactions on Vehicular Technology*, vol. 57, pp. 2319–2333, July 2008.