Control registers definition:

1-7: reserved.

8: Set TLB
8:TLB virtual address lower bits
9:TLB virtual address higher bits
10:TLB physical address lower bits
11:TLB physical address higher bits
12:TLB is base address (head of huge page)
13:TLB write valid

14-19: reserved.

20: Enable completion for host polling

50: h2d DMA
50: DMA host start address higher bits
51: DMA host start address lower bits
52: DMA FPGA HBM start address higher bits
53: DMA FPGA HBM start address lower bits
54: DMA transfer length
55: DMA packet size
56: DMA queue number (*not for QDMA, for queue implemented by logics)
57: polling host memory address for completion higher bits
58: polling host memory address for completion lower bits
59: h2d command input valid (rising edge)

70: c2h DMA
70: DMA host start address higher bits
71: DMA host start address lower bits
72: DMA FPGA HBM start address higher bits
73: DMA FPGA HBM start address lower bits
74: DMA transfer length
75: DMA packet size
76: DMA queue number (*not for QDMA, for queue implemented by logics)
77: polling host memory address for completion higher bits
78: polling host memory address for completion lower bits
79: d2h command input valid (rising edge)

80: pfch_tag for QDMA IP (follow example code)

90: p2p DMA monitor

91: enable monitor (rising edge)

92: p2p completion polling host memory higher bits

93: p2p completion polling host memory lower bits

94: p2p transfer length