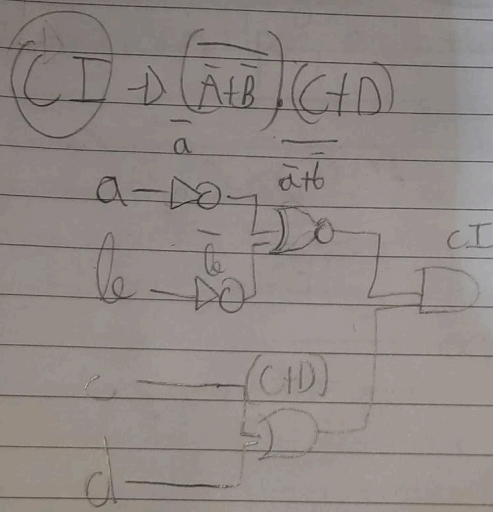
Bagé, 13/04/25 Ely Neto

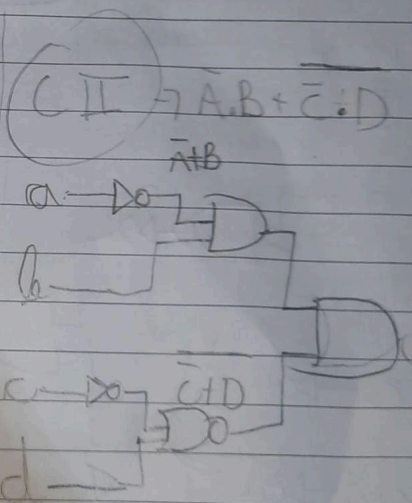
Lista 1 → P. Digital 1 → Prof. Fabio Ramos

① Desenvolva no Logisim as seguintes portas booleanas, utilize do quaisquer portas lógicas:

I) $\bar{A}+\bar{B}\cdot(C+D)$

II) $\bar{A}.B+(\overline{\bar{C}.D})$





b) Transformar as lógicas do item a) para implementar as mesmas, utilizando somente NAND's de duas entradas e inversores. Após, implementar na logisim

$\overline{x+y} = \bar{x} \cdot \bar{y}$

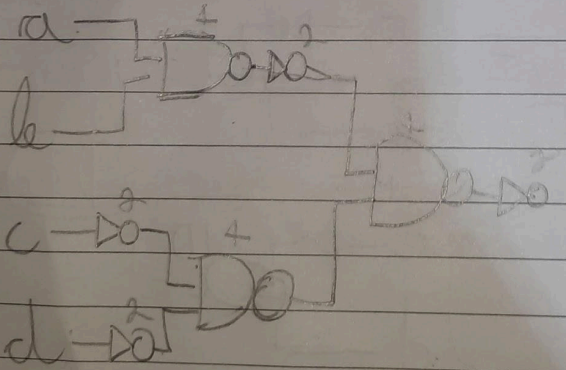
$\overline{x \cdot y} = \bar{x} + \bar{y}$

I) $\overline{\overline{A+B} \cdot (C+D)} =$

$(A \cdot B) \cdot \overline{(\bar{C} \cdot \bar{D})} = (A \cdot B) \cdot (C \cdot D)$

II) $\bar{A} \cdot B + \bar{C} \cdot D = \overline{\overline{(\bar{A} \cdot B) + (\bar{C} \cdot D)}} = \overline{(\bar{A} \cdot B) \cdot (\bar{C} \cdot D)}$

(I)

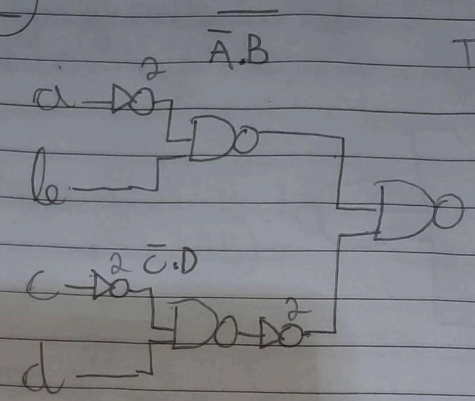


$T = 4 \times 2 + 3 \times 4$

$= 8 + 12 = 20$

(II)

(IT)



$T = 3 \times 2 + 3 \times 4$
$6 + 12 = 18$

c) Transformar as lógicas do item a para implementar as mesmas utilizando somente NOR's de duas entradas e inversores. Após, implementar no Logisim.

$\overline{x \cdot y} = \bar{x} + \bar{y}$
$\overline{x + y} = \bar{x} \cdot \bar{y}$

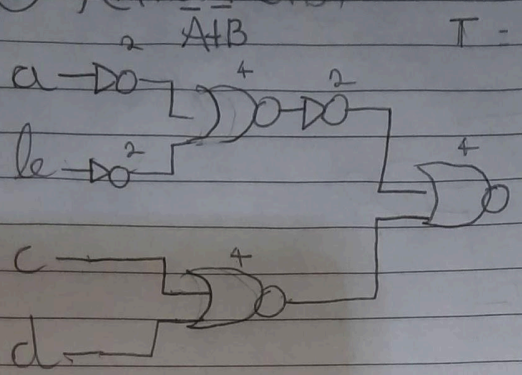
I) $\overline{\bar{A}+\bar{B} \cdot (C+D)}$

↳ $\overline{(\bar{A}+\bar{B}) \cdot (C+D)} \rightarrow \boxed{\overline{(\bar{A}+\bar{B})} + \overline{(C+D)}}$

II) $(\overline{\bar{A}.B}) + \overline{\bar{C}.D}$

↳ $\overline{\bar{A}.B} = \overline{A} + \overline{\bar{B}} + \overline{\bar{C}.D} \rightarrow \boxed{A + \bar{B} + C + D}$

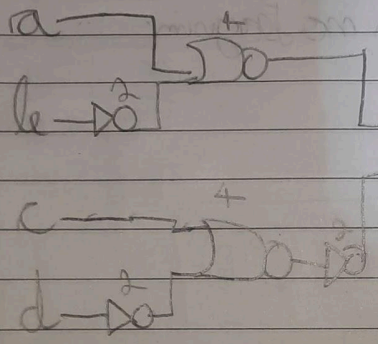
(I) $= \overline{(A+B)} + (C+D)$



$\overline{A+B}$

$T = 3(2) + 3(4) = 6 + 12 = 18$

(II) $= \overline{(A+\bar{B})} + (C+\bar{D})$



$T = 4(2) + 3(4)$

$= 8 + 12 = 20$

d) Diga quantos transistores tem cada implementação do item b) e c) e, portanto, qual delas são menores.

NOR's → ① $\overline{(A+\bar{B})} + \overline{(C+D)}$ ⇒ 18 transistores
→ ② $\overline{(A+B)} + \overline{(C+\bar{D})}$ ⇒ 20 transistores

NAND's → ① $\overline{(A.B)}.\overline{(\bar{C}.D)}$ ⇒ 20 transistores
→ ② $\overline{(\bar{A}.B)}.\overline{(C.\bar{D})}$ ⇒ 18 transistores

Conclusão:

(I) I) com NOR's e c) e II) em NAND's, se provaram ser os circuitos com o menor número de transistores, tendo 18.