CM6327A

USB Single-Chip Audio Solution for Mono Microphone

DESCRIPTION

CM6327A是C-Media为高级VoIP应用设计的新的音频SOC IC。 它拥有高性能的单ADC和I2C接口，允许与各种微处理器和DSP通信。 CM6327A提供低噪音、高质量的语音输入，在录音或广播电话会议或公共演讲时非常重要。 此外，CM6327A集成了所有基本的模拟模块，包括1chADC、PLL、调节器和USB收发器模块，以及允许您自定义产品字符串、PID和VID的EEPROM。 支持8/11.025/16/22.05/32/44.1和48千赫的采样率、高质量的16位分辨率和用户友好的通用输入和输出，用于定制功能。 此外，许多功能可以使用外部EEPROM和MCU编程，这些功能可以通过HID软件接口轻松控制。

The CM6327A is C-Media's new Audio SOC IC designed for advanced VoIP applications. It boasts a high-performance mono ADC, as well as I2C interface, that allows for communication with various microprocessors and DSPs. The CM6327A offers low-noise, high-quality speech input, important when it comes to recording or broadcasting conference calls or public speeches.

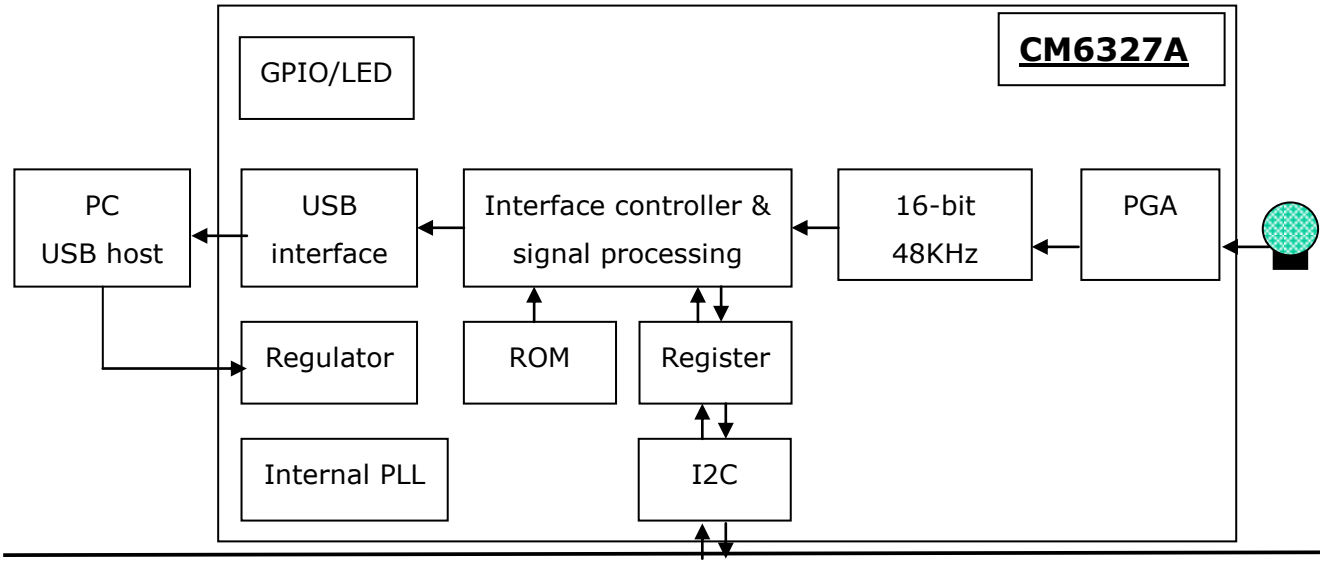
Also, the CM6327A integrates all essential analog modules, including 1-ch ADC, PLL, regulator and USB transceiver modules, along with an EEPROM that allows you to customize the product string, PID and VID. Sampling rates of 8/11.025/16/22.05/ 32/44.1 and 48 KHz, high-quality 16-bit resolutions and user-friendly general purpose inputs and outputs for customized functions are supported. In addition, many features can be programmed using an external EEPROM and MCU, which are easily controlled via the HID software interface.

FEATURES

- USB specification 2.0 full speed-compliant and USB IF-certified
- USB audio device specification 1.0- and USB HID specification 1.1-compliant
- Supports control/interrupt/isochroous data transfers
- USB suspend/resume and remote wake-up support
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz crystal input with on-chip PLL
- Supports series number string for operation system detection
- Serial EEPROM programming interface supports customized VID/PID/product and manufacture strings
- EEPROM interface supports 24C02 data format

?USB规范2.0全速度兼容和USB IF认证
?USB音频设备规范1.0和USB HID规范1.1兼容
?支持控制/中断/中断数据传输，USB暂停/恢复和远程唤醒支持
?嵌入式USB收发器和电源复位电路?单个12MHz晶体输入，片上PLL
?支持操作系统检测的系列号串
?串行EEPROM编程接口支持定制的VID/PID/产品和制造串?EEPROM接口支持24C02数据格式

BLOCK DIAGRAM



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Release Notes

Revision	Date	Description
1.8	2010/4/26	Updated the EEPROM data format Address 0x09: Reserved Address 0x12 (Bit2): Reserved (0: Default) Address 0x13: Reserved
1.9	2012/9/27	Revised format
2.0	2012/10/1	Updated the EEPROM Data Format Address 0x02(Bit3):Reserved Address 0x03(Bit7):Reserved Address 0x0a:Reserved

1 Description and Overview

This is a highly integrated single-chip USB audio solution that is built for a wide range of USB audio controller and applications. Based on our experiences designing and manufacturing PC USB Audio peripherals, as well as recommendations from vendors, C-Media has designed this single-chip solution to make it easier for vendors to integrate their products, and increase their revenues.

The CM6327A is C-Media's new Audio SOC IC designed for advanced VoIP applications. It boasts a high-performance mono ADC, as well as I2C interface, that allows for communication with various microprocessors and DSPs. The CM6327A offers low-noise, high-quality speech input, important when it comes to recording or broadcasting conference calls or public speeches.

The CM6327A integrates all essential analog modules, including 1-ch ADC, PLL, regulator and USB transceiver modules, along with an EEPROM that allows you to customize the product string, PID and VID. Sampling rates of 8/11.025/16/22.05/ 32/44.1 and 48 KHz, high-quality 16-bit resolutions and user-friendly general purpose inputs and outputs for customized functions are supported. Many features can be programmed using an external EEPROM and MCU, which are easily controlled via the HID software interface.

2 Features

- USB spec. 2.0 full speed-compatible and USB IF-certified
- USB audio device class 1.0- and USB HID specification 1.1-compliant
- Supports control/interrupt/isochroous data transfers
- USB suspend/resume and remote wake-up support
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz crystal input with on-chip PLL
- Supports series number string for operation system detection
- Serial EEPROM programming interface supports customized VID/PID/product and manufacture strings for device name changes and configurations
- EEPROM interface support 24C02 data format
- Mono ADC input:
  ADC sampling rate of 8K/11.025K/16K/22.05K/32K/44.1K/48KHz, and 16-bit resolution
  Dynamic range: 96db, THD+N: -89~96db
  Digital linear microphone gain control function (-16db~45db)
  1.0Vrms input swing biased at 2.25V
- Supports Microsoft HID functions
- Supports I2C (master/slave) control interface for external controller used

?USB规格。 2.0全速度兼容和USB IF认证?USB音频设备类1.0-和USB HID规格1。兼容
?支持控制/中断/等中断数据传输
?USB挂起/恢复和远程唤醒支持?嵌入式USB收发器和电源复位电路
?单个12MHz晶体输入与片上PLL
?支持操作系统检测的串联数字串
?串行EEPROM编程接口支持定制的VID/PID/产品和用于设备名称更改和配置的制造字符串?EEPROM接口支持24C02数据格式，MonoADC输入：ADC采样率为8K/11.025K/16K/22.05K/44。1K/48K Hz，16位分辨率动态范围：96db，THDN：-89~96db数字线性麦克风增益控制功能(-16db~45db)1.0Vrms输入摆动偏置在2.25V
?支持Microsoft HID功能?支持外部控制器的I2C（主/从）控制接口

- I2C MCU read/write support 16 bytes data transfer bandwidth
- I2C interface support extra interrupt pin INT
- MCU/EEPROM/GPIO control via HID/vender command interface
- USB audio topology has 1 input terminal, 1 output terminal, 1 selector unit and 1 feature unit
- Supports 2 LED indicator pins:
  1. On/Off/Operation
  2. Recording mute
- Supports 8 GPIO and 2 GPI pins
- Isochronous transfer uses adaptive mode with Internal PLL for synchronization
- Embedded power-on-reset block
- Single 5V power supply with embedded 5V to 3.3V regulator
- Industry standard LQFP-48 pin package
- Compatible with Win2000/WinXP/Vista/Win7/MAC/OSX/Linux/Wii/XBOX360/PS2/PS3
- Supports hardware SDK tool for third-party software development

?I2C单片机读写支持16字节数据传输带宽

?I2C接口支持额外的中断引脚INT?MCU/EEPROM/GPIO控制通过HID/vender命令接口

?USB音频拓扑有1个输入端，1个输出端，1个选择器单元和1个特征单元?支持2个LED指示引脚：1个。 开/关/运行2。 记录静音

?支持8个GPIO和2个GPI引脚?等时传输采用自适应模式与内部PLL同步

?嵌入式电源对复位块?单个5V电源，内嵌5V至3.3V调节器?行业标准LQ FP-48引脚封装

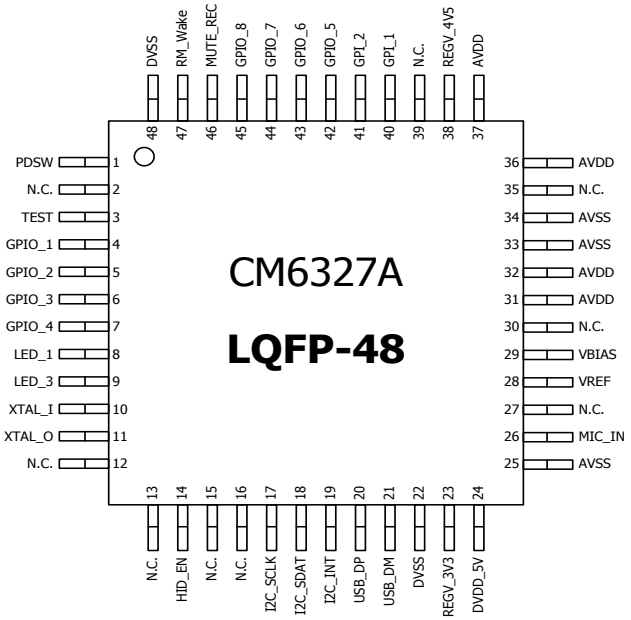
?兼容Win2000/WinXP/Vista/Win7/MAC/OSX/Linux/Wii/XBOX360/PS2/PS3，支持硬件SDK工具进行第三方软件开发

3 Pin Descriptions

3.1 Pin Assignment by Pin Number

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PDSW	13	N.C.	25	AVSS	37	AVDD
2	N.C.	14	HID_EN	26	MIC_IN	38	REGV_4V5
3	TEST	15	N.C.	27	N.C.	39	N.C.
4	GPIO_1	16	N.C.	28	VREF	40	GPI_1
5	GPIO_2	17	I2C_SCLK	29	VBIAS	41	GPI_2
6	GPIO_3	18	I2C_SDAT	30	N.C.	42	GPIO_5
7	GPIO_4	19	I2C_INT	31	AVDD	43	GPIO_6
8	LED_1	20	USB_DP	32	AVDD	44	GPIO_7
9	LED_3	21	USB_DM	33	AVSS	45	GPIO_8
10	XTAL_I	22	DVSS	34	AVSS	46	MUTE_REC
11	XTAL_O	23	REGV_3V3	35	N.C.	47	RM_Wake
12	N.C.	24	DVDD5V	36	AVDD	48	DVSS

3.2 Pin-Out Diagram

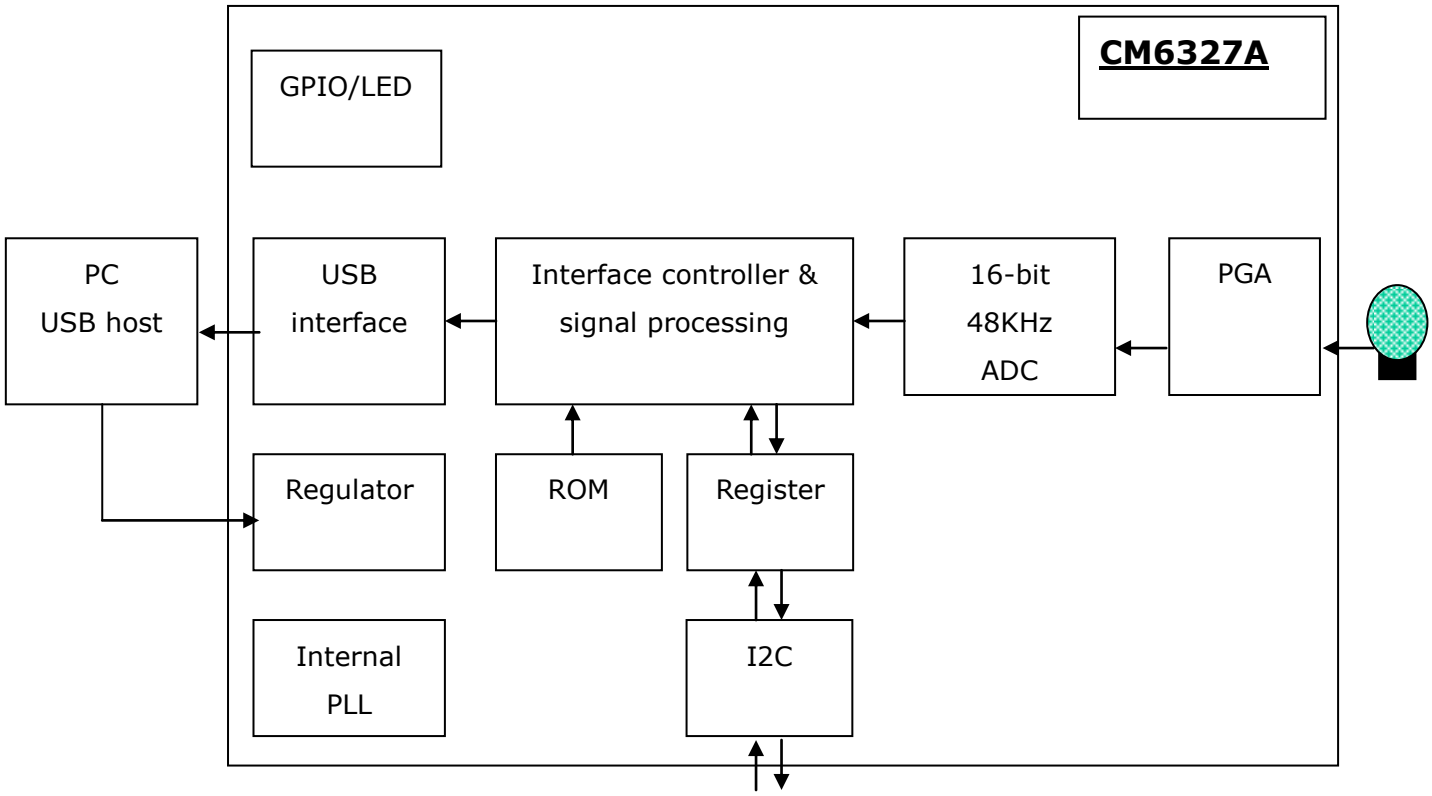


3.3 Pin Signal Descriptions

No.	Symbol	Type	Description
1	PDSW	OD, 5V	Power-down switch output 断电开关输出（0：正常操作；1：暂停） (0: Normal operation; 1: Suspend)
2	N.C.	N.C.	N.C.
3	TEST	DI, PD	Test mode select 测试模式选择（0：正常模式；1：测试模式） (0: Normal Mode; 1: Test Mode)
4	GPIO_1	DIO	General purpose I/O pin 通用I/O引脚
5	GPIO_2	DIO	General purpose I/O pin
6	GPIO_3	DIO	General purpose I/O pin
7	GPIO_4	DIO	General purpose I/O pin
8	LED_1	DO	LED (Play or Record) LED（播放或录制）
9	LED_3	DO	LED (Mute Record) LED（静音记录）
10	XTAL_I	DI	Input pin for 12MHz oscillator 12兆赫振荡器输入针
11	XTAL_O	DO	Output pin for 12MHz oscillator 输出引脚为12MHz振荡器
12	N.C.	N.C.	N.C.
13	N.C.	N.C.	N.C.
14	HID_EN	DI, PU	HID bottom function enable (0: Disable; 1: Enable) HID底部函数启用（0：禁用；1：启用）
15	N.C.	N.C.	N.C.
16	N.C.	N.C.	N.C.
17	I2C_SCLK	OD, DIO	I2C serial clock/EEPROM 24c02 serial clock I2C串行时钟/EEPROM24c02串行时钟
18	I2C_SDAT	OD, DIO	I2C serial data/EEPROM 24c02 serial data I2C串行数据/EEPROM24c02串行数据
19	I2C_INT	DO	I2C interrupt output
20	USB_DP	AIO	USB D+
21	USB_DM	AIO	USB D-
22	DVSS	P	Digital ground
23	REGV_3V3	AO	5V->3.3V regulator output
24	DVDD5V	P	5V power supply to internal regulator
25	AVSS	P	Analog ground
26	MIC_IN	AI	MIC input
27	N.C.	N.C.	N.C.
28	VREF	AO	2.25V reference voltage output

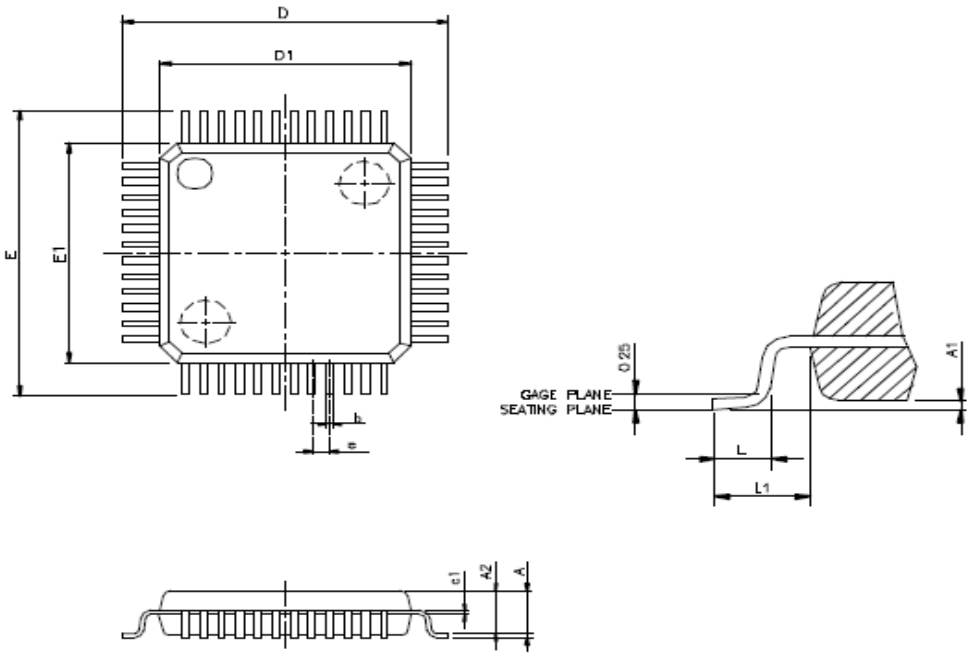
29	VBIAS	AO	MIC bias voltage
30	N.C.	N.C.	N.C.
31	AVDD	P	5V analog power for analog circuit
32	AVDD	P	5V analog power for analog circuit
33	AVSS	P	Analog ground
34	AVSS	P	Analog ground
35	N.C.	N.C.	N.C.
36	AVDD	P	5V Analog power for analog circuit
37	AVDD	P	5V Analog power for analog circuit
38	REGV_4V5	AO	4.5V regulator output
39	N.C.	N.C.	N.C.
40	GPI_1	DI, PU	General purpose input pin (VU)
41	GPI_2	DI, PU	General purpose input pin (VD)
42	GPIO_5	DIO	General purpose I/O pin
43	GPIO_6	DIO	General purpose I/O pin
44	GPIO_7	DIO	General purpose I/O pin
45	GPIO_8	DIO	General purpose I/O pin
46	MUTE_REC	DI, PU	HID MIC Record Mute 麦克风记录静音
47	RM_Wake	DI, PU	Remote wakeup pin to make PC resume from suspend 远程唤醒引脚，使PC恢复暂停
48	DVSS	P	Digital ground

4 Block Diagram



5 Ordering Information

Model Number	Package	Operating Ambient Temperature	Supply Range
CM6327A	48-Pin LQFP, 7mm × 7mm × 1.45mm (Plastic)	0°C to +70°C	DVdd = 5V, AVdd = 5V

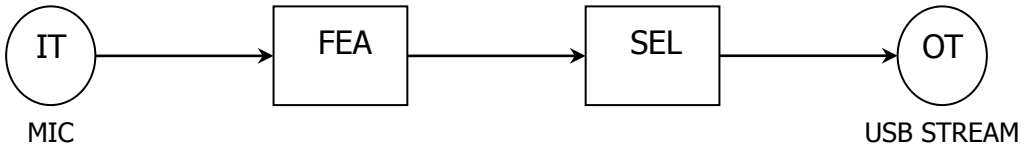


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

6 USB Audio Topology and Descriptions

6.1 USB Audio Topology



6.2 Device Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1-compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	10	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0134	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	03	Manufacturer string descriptor index
15	iProduct	1	01	Product string descriptor index
16	iSerialNumber	1	00 or 03(*)	Serial number string descriptor index
17	bNumConfigurations	1	01	Number of configurations

Note 1: When valid EEPROM is detected, Vendor ID and Product ID will be replaced by the content of the EEPROM

Note 2: iSerialNumber will be valid only if the external EEPROM contains this info

注1：当检测到有效的EEPROM时，供应商ID和产品ID将被EEPROM
注2：I序列号的内容所取代，只有当外部EEPROM包含此信息时才有效

6.3 Configuration Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	007f～00dd	Total length of data returned for this configuration
4	bNumInterfaces	1	03	Number of interfaces supported in configuration: 00: Control 02: ISO-IN 03: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	a0 or 80 or e0 or c0	Bus-powered with remote wakeup support: 8'ha0 (PWRSEL_1 = 1, HID_EN = 1) Bus-powered with no remote wakeup: 8'h80 (PWRSEL_1 = 1, HID_EN = 0) Self-powered with remote wakeup support: 8'he0 (PWRSEL_1 = 0, HID_EN = 1)) Self-powered with no remote wakeup: 8'hc0 (PWRSEL_1 = 0, HID_EN = 0))
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1)

6.4 Standard HID Interface Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface descriptor
2	bInterfaceNumber	1	02	Interface number: 02
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	01	Number of endpoints used by this interface
5	bInterfaceClass	1	03	HID interface class
6	bInterfaceSubClass	1	00	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Interface string descriptor index

Class-specific HID Interface Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version
4	bCountryCode	1	00	No country code
5	bNumDescriptors	1	01	One HID class descriptor
6	bDescriptorType	1	22	Report Descriptor
7	wDescriptorLength	2	0032 / 001a	HID class descriptor length in byte: 50 / 26 bytes (Enable / Disable HID Button)

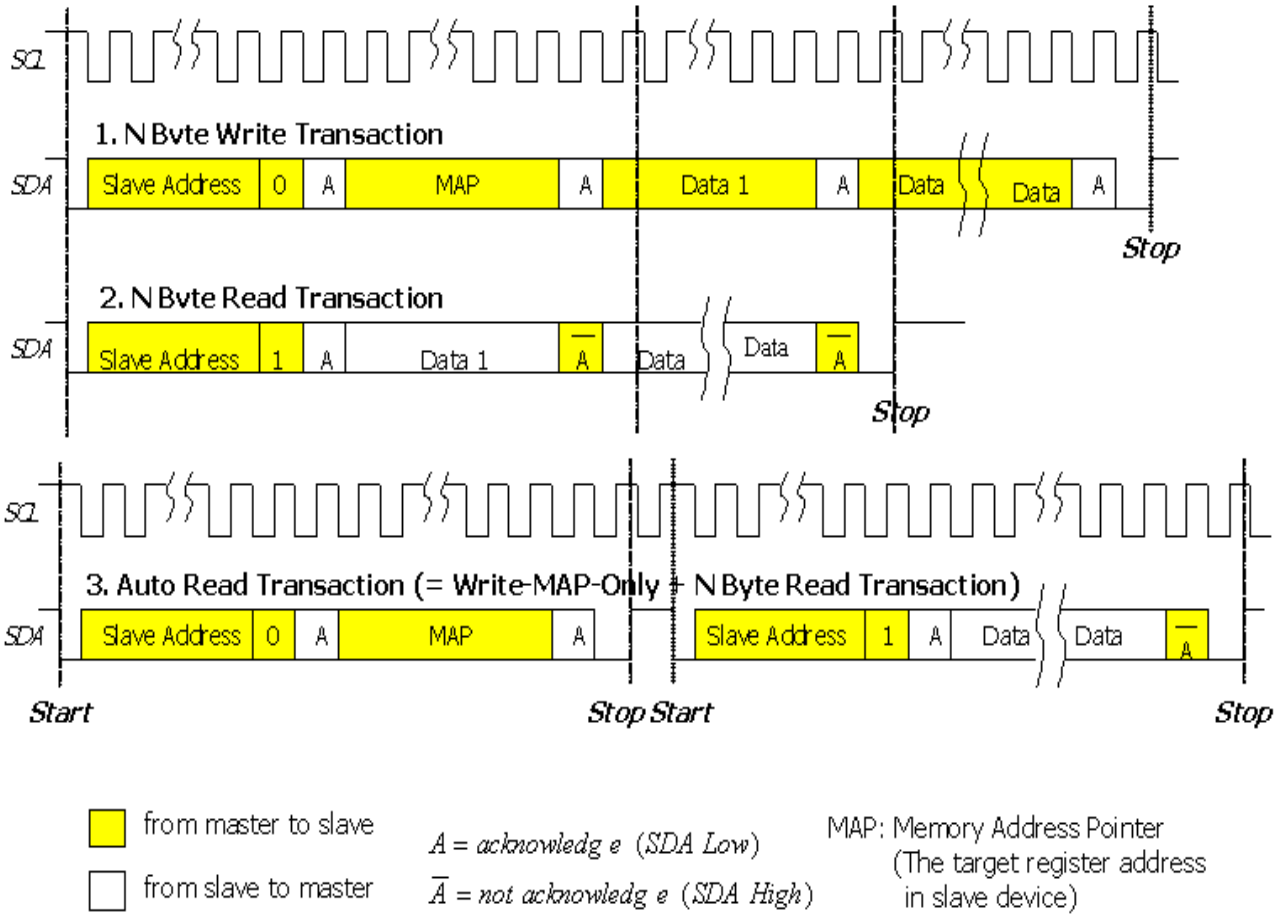
Standard HID Interrupt In Endpoint Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	05	Endpoint descriptor
2	bEndpointAddress	1	87	IN endpoint, endpoint number: 7
3	bmAttributes	1	03	Interrupt endpoint
4	wMaxPacketSize	2	0010	Maximum packet size: 16 bytes
6	bInterval	1	01	1ms

7 Function Block Descriptions

7.1 I2C Interface

7.1.1 Master Mode



from master to slave

from slave to master

A = *acknowledge (SDA Low)*

$\overline{A}$ = *not acknowledge (SDA High)*

MAP: Memory Address Pointer (The target register address in slave device)

7.1.2 Slave Mode

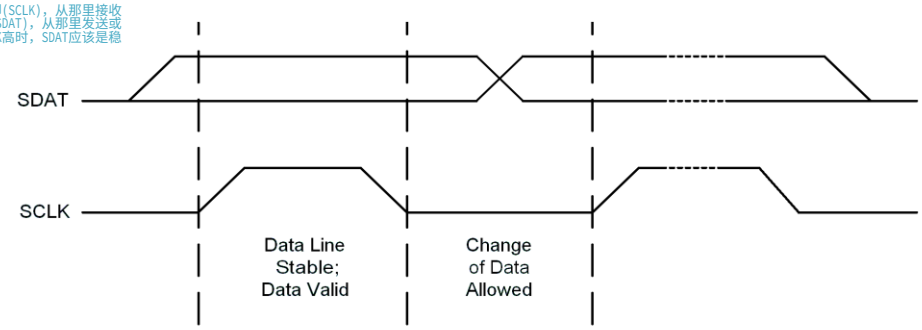
"7-bit slave address = 7'b0111000"

On the MCU serial interface, the CM6327 serves as a slave device with bit rate up to 400Kbps (fast mode). The MCU can write data to the CM6327A or read data from the CM6327A (no size limitations when using the I2C Interface). Since the host side and MCU both have access to all the internal registers, access contention when both host and MCU try to access the same register should be avoided upon application. The CM6327A's 7-bit slave address is assigned as 7'b0111000.

When data is written by the MCU, the CM6327A will NOT transfer any interrupts to the PC until the INT bit of the I2C control register has been set by the MCU. The USB host will keep polling the upward HID report every 1ms. When any button is pressed or released, or there is incoming MCU data, the CM6327A will transfer 16 bytes of HID report to the USB host. 当数据由MCU写入时，CM6327A将不会将任何中断传输到PC，直到MCU设置了I2C控制寄存器的IN T位。 USB主机将每1ms继续轮询向上的HID报告。 当任何按钮被按下或释放，或有传入的MCU数据时，CM6327A将向USB主机传输16字节的HID报告。

In I2C Slave Mode, the CM6327A has one open-drain input pin (SCLK) from where it receives the serial clock from the MCU, and one open-drain I/O pin (SDAT) from where it sends or receives serial signals to/from the MCU. As shown below, SDAT should be stable when SCLK is high, and can transition only when SCLK is low.

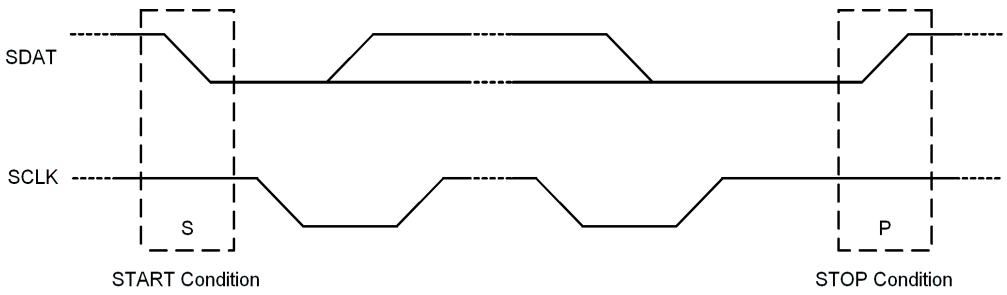
在I2C从模式下，CM6327A有一个开路漏输入引脚(SCLK)，从那里接收来自MCU的串行时钟，以及一个开路漏I/O引脚(SDAT)，从那里发送或接收来自MCU的串行信号。 如下图所示，当SCLK高时，SDAT应该是稳定的，只有当SCLK低时才能过渡。



Bit Transfer on the MCU Interface

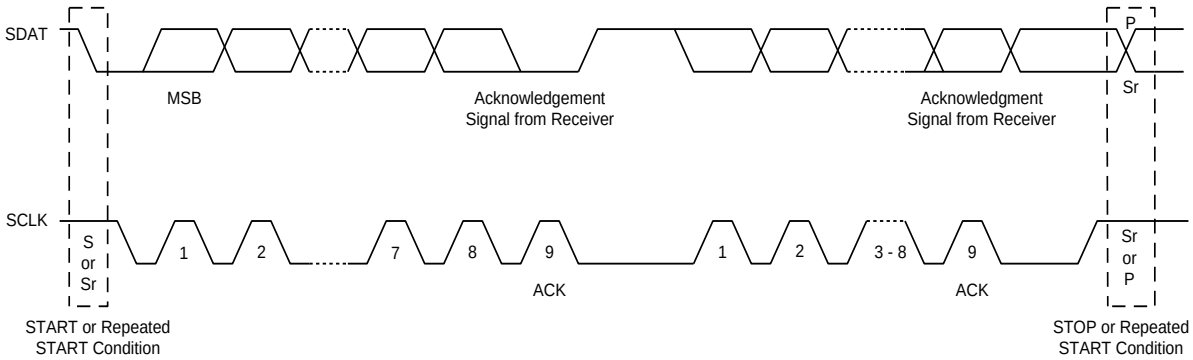
以下所示的START和STOP条件是例外。 每一项交易都是从开始开始的，以停止或另一项开始（重复开始)结束）。

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

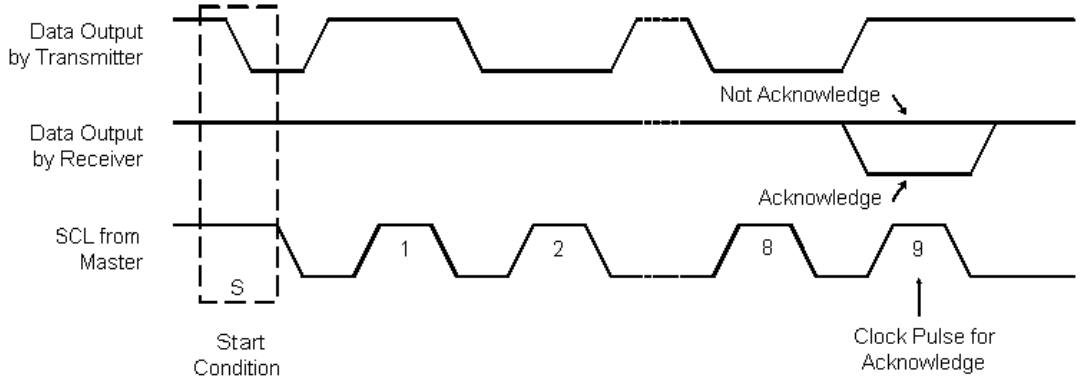


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more details about the acknowledgement bit. Note that SCLK is always driven by the master.



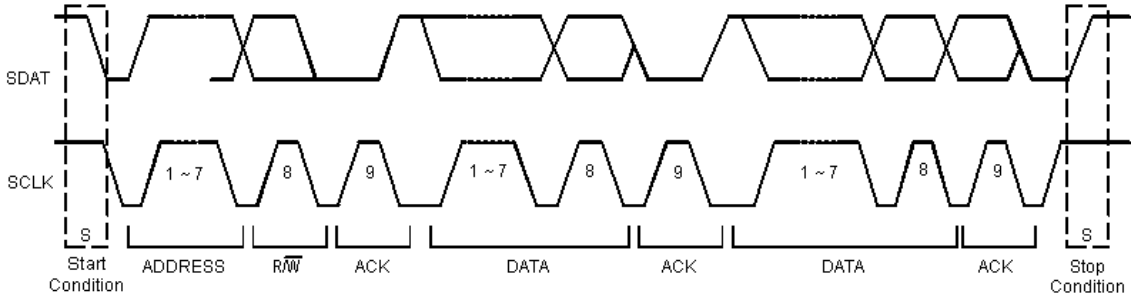
Data Transfer on the MCU Interface



Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, with the 8th bit denoting a read transfer when it's high, or a write transfer when it's low. The first acknowledgement always comes from the CM6327A.

下图显示了完整的数据传输。启动后，MCU应该首先发送一个7位从地址(7'b0111000)，第8位表示高时的读取传输，或低时的写入传输。第一次确认总是来自CM6327A。



A Complete Data Transfer

During the write transfer, the MCU continues acting as the master, and the transfer direction is not changed. The following figure gives an example of one byte write transfer.

写传输过程中，单片机继续充当主，传输方向不变。 下图给出了一个字节写入传输的示例。

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	….	0	Byte N	0	P

	From CM6327A to MCU		From MCU to CM6327A
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N		One byte data	

The CM6327A's slave address is 0x70, which will also tell the CM6327A when it's receiving a write command. CM6327A regards the first coming data byte as the register address. The second data byte is the data content that the MCU writes at the register address. The CM6327A will auto-increment the register address to the next register address for the following data writes.

The figure below shows an example of a read transfer. The MCU read command cannot set the register address, so the MCU must use a write command to set the register address first, and then start the read command. Because the CM6327A auto-increments the register address, the second data byte will be the register data on the next address.

CM6327A的从地址是0x70，当CM6327A收到写命令时也会告诉它。 CM6327A将第一个数据字节视为寄存器地址。 第二个数据字节是MCU在寄存器地址写入的数据内容。 CM6327A将自动将寄存器地址增加到下一个寄存器地址以进行以下数据写入。

下图显示了读取传输的示例。 单片机读取命令不能设置寄存器地址，因此单片机必须先使用写命令设置寄存器地址，然后启动读取命令。 由于CM6327A自动增加寄存器地址，第二个数据字节将是下一个地址上的寄存器数据。

MCU read:

S	0x70	0	addr	0							
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P

	From CM6327A to MCU		From MCU to CM6327A
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte n	One byte of data		

The figure below gives a complete picture of a typical transaction between the MCU and CM6327A. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, with the 8th bit denoting a read transfer when it's high, or a write transfer when it's low.

下面的图给出了MCU和CM6327A之间典型事务的完整图片。开始后，MCU应该首先发送一个7位从地址（7位0111000），第8位表示高时的读取传输，或者低时的写传输。

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	…..	0	Byte N	0	P

MCU read:

S	0x70	0	addr	0								
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P	

	From CM6327A to MCU		From MCU to CM6327A
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte of data		

在写入传输过程中，MCU充当发射机。 CM6327A将把接收到的数据的第一个字节视为起始寄存器地址。 以下数据字节是MCU请求的寄存器的内容。 在读取传输中，需要两个事务。 单片机通过第一个事务重新设置开始寄存器地址，然后改变方向，使MCU在第二个事务中接收数据。

During a write transfer, the MCU acts as the transmitter. The CM6327A will regard the first byte of data received as the start register address. The following DATA bytes are the contents of the registers that the MCU has requested. In a read transfer, two transactions are necessary. The MCU resets the start register address by the first transaction, then direction changes for the MCU to receive data in the second transaction.

7.1.3 EEPROM Data Format

Address	Description
0x00	Magic word (“C”, 8’h43)
0x01	Magic word (“M”, 8’h4D)
0x02	EEPROM Content Setting (EEPROM_OPTION_1) bit0: Manufacture String Valid? (0: No, 1: Yes) bit1: Product String Valid? (0: No, 1: Yes) bit2: Serial Number Valid? (0: No, 1: Yes) bit3: Reserved bit4: Recording (ADC) initial control Valid? (0: No, 1: Yes) bit5: ADC gain range Control Valid? (0: No, 1: Yes) bit6: Disable Selector unit? (0: No, 1: Yes) bit7: Enable Remote Wakeup? (0: Disable, 1: Enable) EEPROM内容设置(EEPROM_OPTION_1) 位0：制造字符串有效？ (0：No，1：Yes) bit1：产品字符串有效？ (0：否，1：是) 位2：序列号有效？ (0：否，1：是) 位3：保留 位4：记录(ADC)初始控制有效？ (0：否，1：是) 位5：ADC增益范围控制有效？ (0：否，1：是) 位6：禁用选择器单元？ (0：否，1：是) bit7：启用远程唤醒？ (0：禁用，1：启用)
0x03	Recording (ADC) initial-L (EEPROM_OPTION_2) bit[5:0]: ADC(unit Fa) initial Volume L-byte (6’h2E ~ 6’h00, 30~ -16dB, -1dB/step) bit6: Mute_fa (ADC) initial Value (0: Un-Mute, 1: Mute) bit7: Reserved 记录(ADC)初始-L(EEPROM_OPTION_2) 位[5：0]：ADC（单位法）初始体积L字节(6‘H2E~6’H00，30~-16DB，-1DB/步骤) 位6：Mute_fa(ADC)初始值（0：未静音，1：静音） 位7：保留
0x04	Recording (ADC) initial-H (EEPROM_OPTION_3) (1)bit[3:0]: ADC (Unit Fa) initial volume H-byte (4’hf ~ 4’h0, 15 ~ 0dB, -1dB/step) Bit[4]: control ADC HP filter by EEPROM (0 : No, 1 : Yes) Bit[5]: ADC HP filter enable (0 : Disable, 1 : Enable) Bit[7:6]: Reserved 记录(ADC)初始-H(EEPROM_OPTION_3)（1） 位[3：0]：ADC(单元Fa)初始体积H字节(4‘hf~4‘h0，15~0dB，-1dB/步骤) 位[4]：通过EEPROM控制ADC HP滤波器（0：否，1：是） 位[5]：ADCHP滤波器启用（0：禁用，1：启用） 位[7：6]：保留
0x05	Recording (ADC) max range Control_L (EEPROM_OPTION_4) bit[7:0]: ADC (Unit fa) max. Volume[7:0] 录音(ADC)最大范围Control_L(EEPROM_OPTION_4) 位[7：0]：ADC(单位FA)最大。卷[7：0]
0x06	Recording (ADC) max. range Control_H (EEPROM_OPTION_5) bit[7:0]: ADC (Unit fa) max. Volume[15:8]
0x07	Recording (ADC) min range Control_L (EEPROM_OPTION_6) bit[7:0]: ADC (Unit fa) min. Volume[7:0]
0x08	Recording (ADC) min. range Control_H (EEPROM_OPTION_7) bit[7:0]: ADC (Unit fa) min. Volume[15:8]
0x09	Reserved

0x0a	Reserved
0x0b	Manufacture string 1 length: this number doesn't include the first 2 bytes of the string descriptor, and its unit is one Unicode word (EEPROM_OPTION_A)
0x0c	Product string 2 length: this number doesn't include the first 2 bytes of the string descriptor, and its unit is one Unicode word (EEPROM_OPTION_B)
0x0d	Serial number string 3 length: this number doesn't include the first 2 bytes of the string descriptor and its unit is one Unicode word (EEPROM_OPTION_C)
0x0e	VID (low byte) (EEPROM_OPTION_D)
0x0f	VID (high byte) (EEPROM_OPTION_E)
0x10	PID (low byte) (EEPROM_OPTION_F)
0x11	PID (high byte) (EEPROM_OPTION_10)
0x12	misce reg (EEPROM_OPTION_11)
	Bit0: Boot gain (volume boot gain 18dB; using digmic boost gain =18dB)
	Bit1: Enable PLL adjustment (0: No, 1: Yes)
	Bit2: Reserved (0 : default)
0x13	Reserved
0x14 ~ 0x4f	Reserved (60 bytes)
0x50 ~0x(50+X-1)	Manufacture string (X bytes): only fill one byte of Unicode in this content, HW will add the other byte 0x00
0x(50+X)~ 0x(50+X+Y-1)	Product string (Y bytes): only fill one byte of Unicode in this content, HW will add the other byte 0x00
0x(50+X+Y)~ 0x(50+X+Y+Z-1)	Serial number string (Z bytes): only fill one byte of Unicode in this content, HW will add the other byte 0x00
Others	Reserved

8 Electrical Characteristics

8.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min. digital supply voltage	- 0.3	V
Dvmax	Max. digital supply voltage	+ 6	V
Avmin	Min. analog supply voltage	- 0.3	V
Avmax	Max. analog supply voltage	+ 6	V
Dvinout	Voltage on any digital input or output pin	-0.3 to +5.5	V
Avinout	Voltage on any analog input or output pin	-0.3 to +5.5	V
T_{stg}	Storage temperature range	-40 to +125	^{0}C
Tj	Junction operating temperature (commercial)	0~+115	^{0}C
ESD (HBM)	ESD human body mode	4000	V
ESD (MM)	ESD machine mode	400	V
Latch Up	Class-3	200	mA

8.2 Operation Conditions

Operation conditions				
	Min	**Typ**	**Max**	**Unit**
Analog supply voltage	4.35	5.0	5.5	V
Digital supply voltage	4.35	5.0	5.5	V
Operation power consumption	-	33	-	mA
Standby power consumption	-	28	-	mA
Suspend mode power consumption	-	410	-	uA
Operating ambient temperature	0	-	70	^{0}C

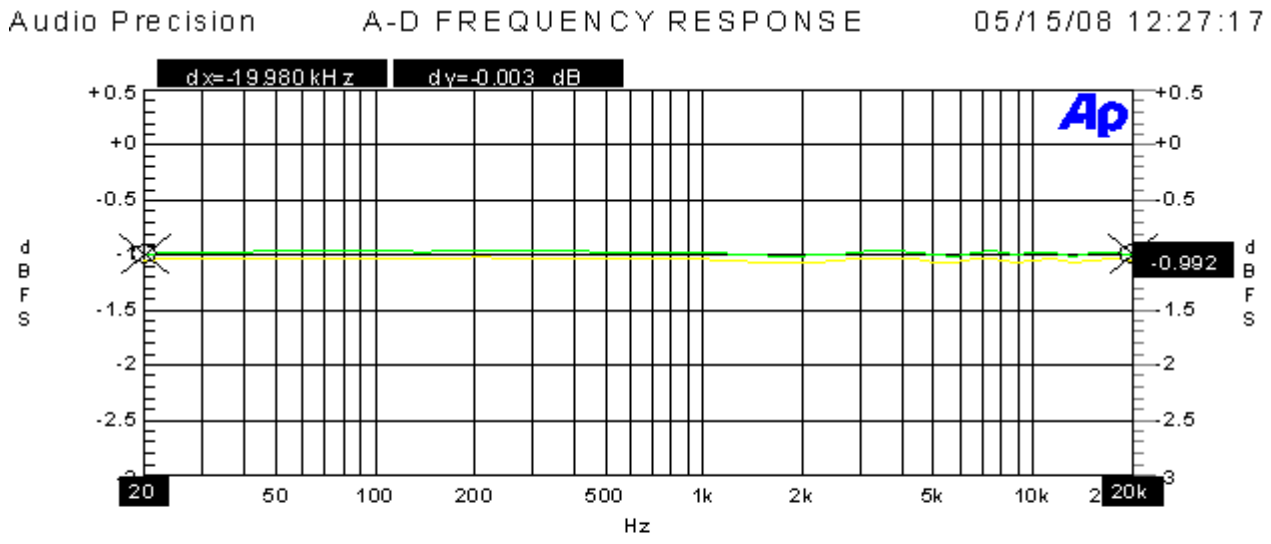
***Notes: Test environment under 25°C, 5.0V, 48K sample rate;**
Max. output is playing 1K full-scale sine wave, typical output is playing music

8.3 Electrical Parameters

	Min	Typ	Max	Unit
THD + N (20 ~ 20KHz)	-89	-	-96	dB
Dynamic range	-	96	-	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency response 44.1KHz	20	-	20K	Hz
Input voltage (rms)	-	1.2	-	Vrms

9 Analog Performance

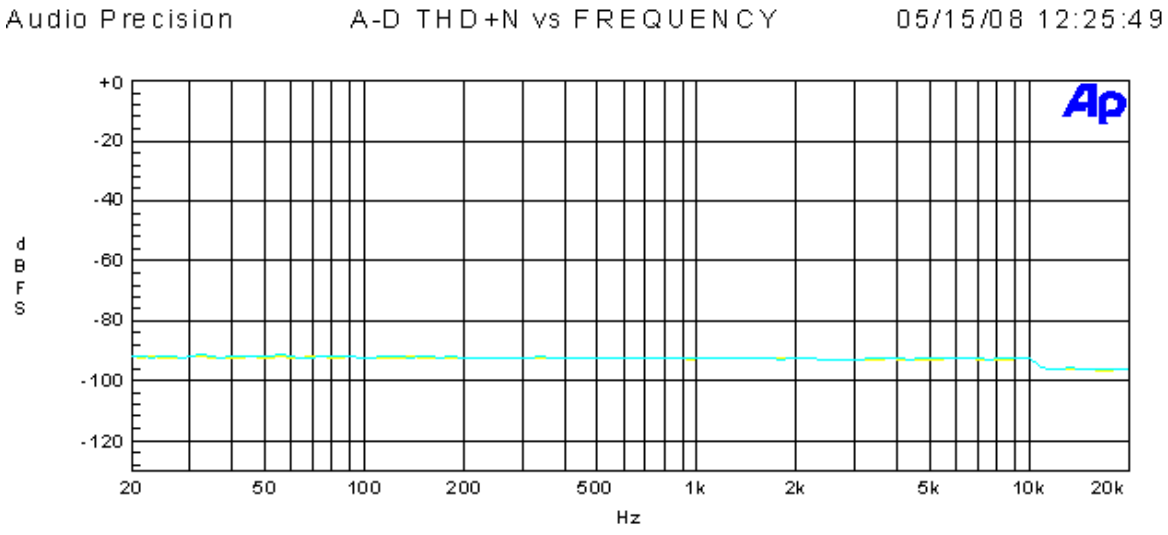
9.1 ADC Frequency Response



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left	
1	2	Green	Solid	1	DSP Anlr.Level B	Right	
1	3	Cyan	Solid	1	DSP Anlr.Level B	Left	

\Vista-A-D Frequency Response.at2c

9.2 ADC THD + N



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	DSP Anlr.THD+N Ampl A	Left	
1	2	Cyan	Solid	1	DSP Anlr.THD+N Ampl B	Left	

\Vista-A-D THD+N.at2c

REFERENCE

- USB specification 2.0-compliant
- USB audio device class specification 1.0-compliant

—End of Datasheet—

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