

MP2162

2A, 6V, 1.5MHz, 17μA I_Q, COT
Synchronous Step Down Switcher
In Ultra-small 2x1.5mm QFN

DESCRIPTION

The MP2162 is a monolithic step-down switch mode converter with built-in internal power MOSFETs. It achieves 2A continuous output current from a 2.5V to 6V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The Constant-On-Time control scheme provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2162 is available in the small QFN8 2.0x1.5mm package and requires a minimum number of readily available standard external components.

The MP2162 is ideal for a wide range of applications including High Performance DSPs, FPGAs, PDAs, and portable instruments.

描述MP2162是具有内置内部功率MOSFET的单片降压开关模式转换器。它具有出色的负载和线路调节能力，可在2.5V至6V输入电压下实现2A连续输出电流。输出电压可低至0.6V。

恒定时间控制方案可提供快速的瞬态响应并简化环路稳定性。故障状态保护包括逐周期电流限制和热关断。

MP2162采用小型QFN8 2.0x1.5mm封装，并且需要最少数量的随时可用的标准外部组件。

MP2162是包括高性能DSP，FPGA，PDA和便携式仪器在内的各种应用的理想选择。

IQ极低：17μA?默认1.5MHz开关频率
EN和电源良好，可用于电源排序
超小型2x1.5mm QFN8封装?2.5V至6V的宽工作输入范围，输出可在0.6V范围内调节
高达2A的输出电流?100% 失落时的占空比
100mΩ 和60mΩ 内部功率MOSFET开关
逐周期过电流保护
打ic模式的短路保护
在低ESR输出电容中稳定应用
无线/网卡?便携式仪器?电池供电的设备
低压I/O系统电源

FEATURES

- Very Low I_Q 17μA
- Default 1.5MHz Switching Frequency
- EN and Power Good for Power Sequencing
- Ultra-small 2x1.5mm QFN8 Package
- Wide 2.5V to 6V Operating Input Range
Output Adjustable from 0.6V
- Up to 2A Output Current
- 100% Duty Cycle in Dropout
- 100mΩ and 60mΩ Internal Power MOSFET Switches
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protect with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors

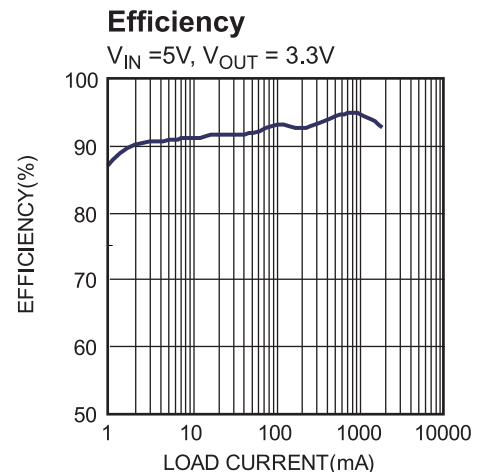
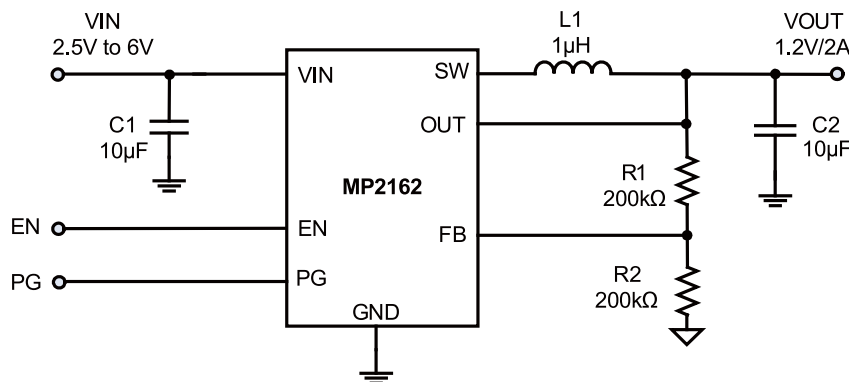
APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery Powered Devices
- Low Voltage I/O Systems Power

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TYPICAL APPLICATION

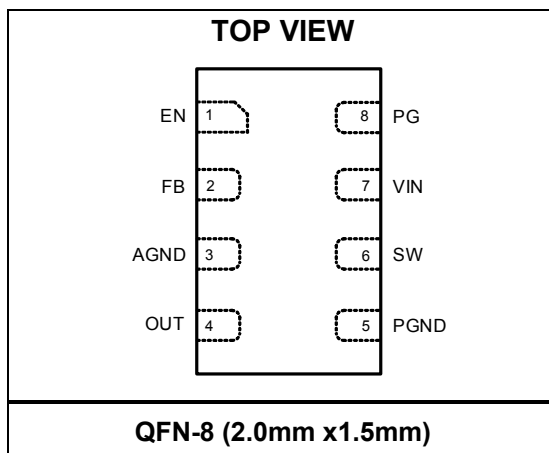


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2162GQH	QFN-8 (2.0mm x1.5mm)	AZ

* For Tape & Reel, add suffix –Z (e.g. MP2162GQH–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage V_{IN}	6.5V
V_{SW}	-0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All Other Pins	-0.3V to 6.5 V
Junction Temperature	150°C
Lead Temperature	260°C
Continuous Power Dissipation ($T_A = +25^\circ\text{C}$) ⁽²⁾	1.14W
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply Voltage V_{IN}	2.5V to 6V
Operating Junction Temp. (T_J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-8 (2.0mm x1.5mm)	110	55... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS ⁽⁵⁾

$V_{IN} = 5V$, $T_A = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	$2.5V \leq V_{IN} \leq 6V$	-3%	0.600	+3%	V/%
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ ⁽⁶⁾	-3.5%		+3.5%	
Feedback Current	I_{FB}	$V_{FB} = 0.6V$		10	50	nA
PFET Switch On Resistance	$R_{DS(on)P}$			100		m Ω
NFET Switch On Resistance	$R_{DS(on)N}$			60		m Ω
Switch Leakage		$V_{EN} = 0V$, $V_{IN} = 6V$ $V_{SW} = 0V$ and $6V$		0	1	μA
PFET Current Limit			2.7	3.2	4.0	A
ON Time	T_{ON}	$V_{IN}=5V$, $V_{OUT}=1.2V$		185		ns
		$V_{IN}=3.6V$, $V_{OUT}=1.2V$		245		
Switching frequency	F_s	$V_{OUT}=1.2V$	-20%	1500	+20%	kHz/%
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ ⁽⁶⁾	-25%	1500	+25%	
Minimum Off Time	$T_{MIN-OFF}$			60		ns
Soft-Start Time	T_{SS-ON}			1.5		ms
Power Good Upper Trip Threshold	PG_H	FB voltage respect to the regulation		+10		%
Power Good Lower Trip Threshold	PG_L			-10		%
Power Good Delay	PG_D			50		μs
Power Good Sink Current Capability	V_{PG-L}	Sink 1mA			0.4	V
Power Good Logic High Voltage	V_{PG-H}	$V_{IN}=5V$, $V_{FB}=0.6V$	4.9			V
Power Good Internal Pull Up Resistor	R_{PG}			550		k Ω
Under Voltage Lockout Threshold Rising			2.15	2.3	2.45	V
Under Voltage Lockout Threshold Hysteresis				260		mV
EN Input Logic Low Voltage					0.4	V
EN Input Logic High Voltage			1.2			V
EN Input Current		$V_{EN}=2V$		1.5		μA
		$V_{EN}=0V$		0		μA
Supply Current (Shutdown)		$V_{EN}=0V$		0	1	μA
Supply Current (Quiescent)		$V_{EN}=2V$, $V_{FB}=0.63V$, $V_{IN}=5V$		17	20	μA
Thermal Shutdown ⁽⁵⁾				150		$^{\circ}C$
Thermal Hysteresis ⁽⁵⁾				30		$^{\circ}C$

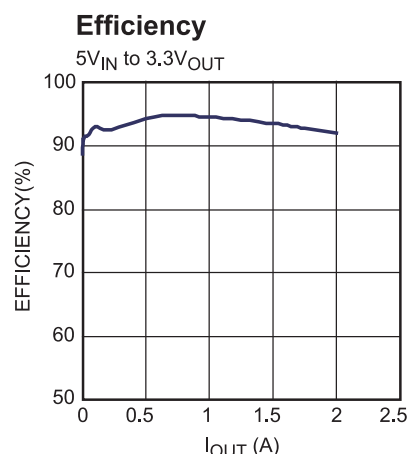
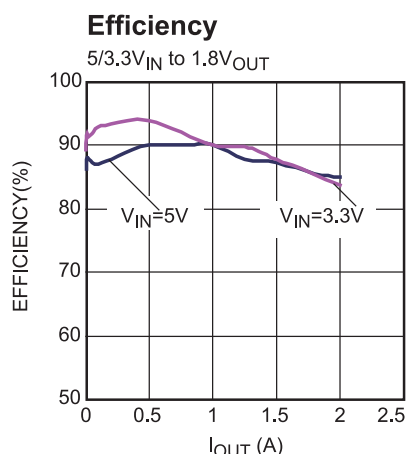
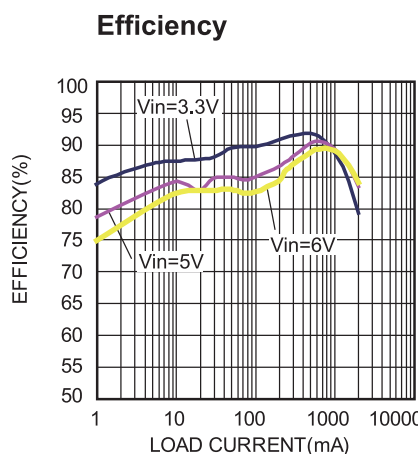
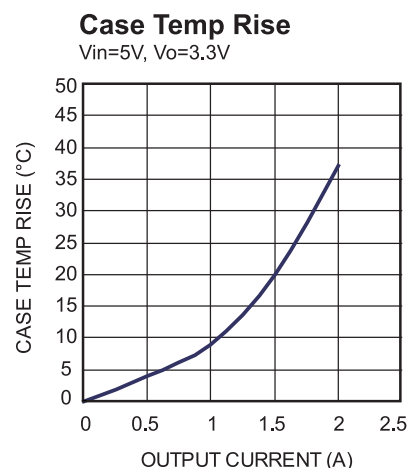
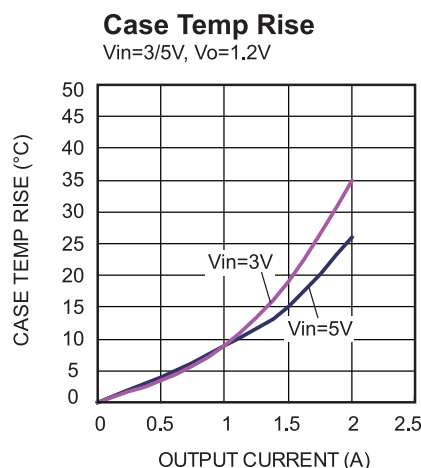
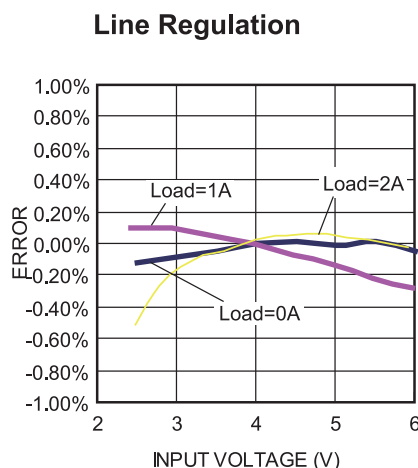
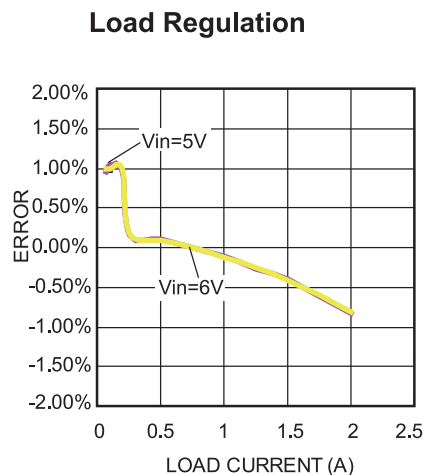
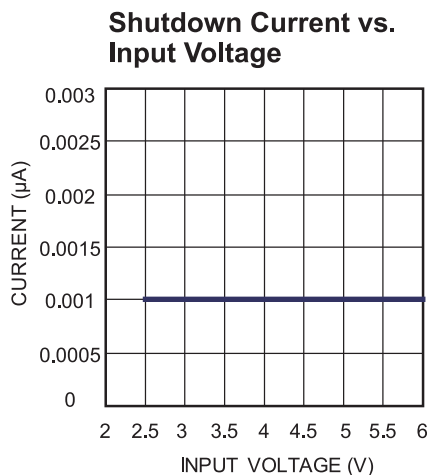
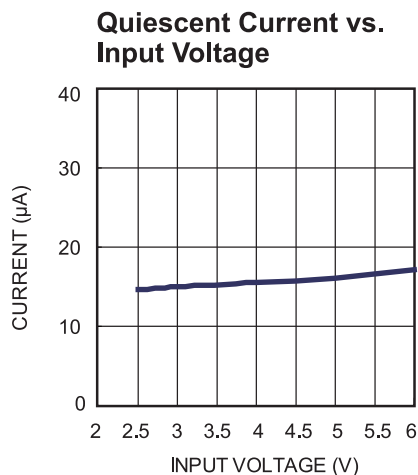
Notes:

5) Guaranteed by design.

6) Guaranteed by characterization test.

TYPICAL PERFORMANCE CHARACTERISTICS

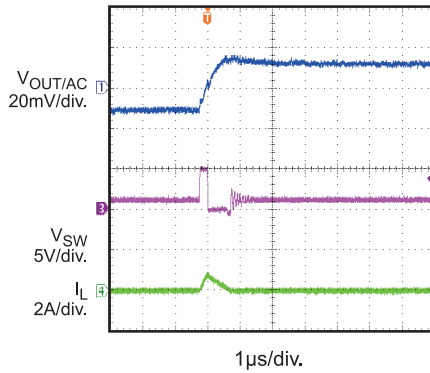
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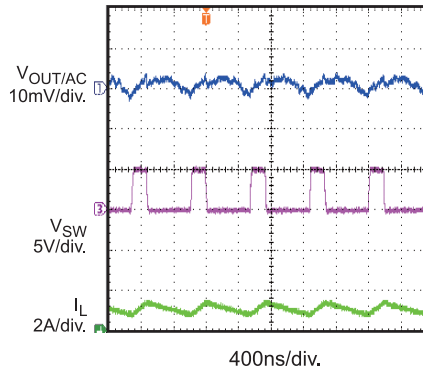
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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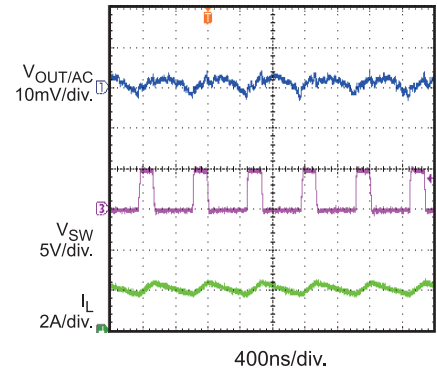
Output Ripple
 $I_{OUT}=0A$



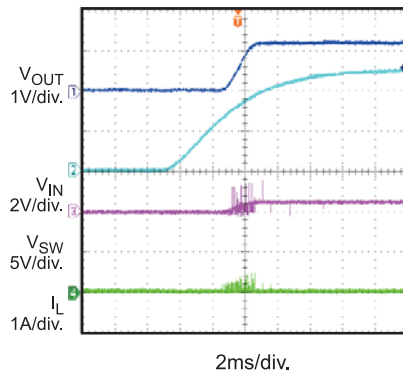
Output Ripple
 $I_{OUT}=1A$



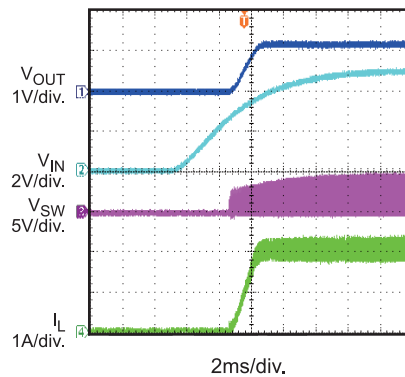
Output Ripple
 $I_{OUT}=2A$



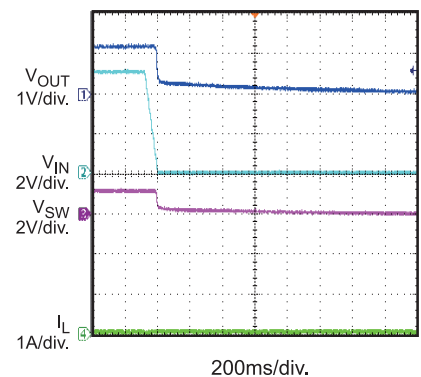
VIN Power Up
without Load



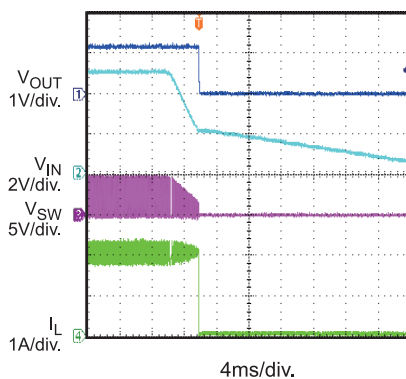
VIN Power Up
with 2A Load



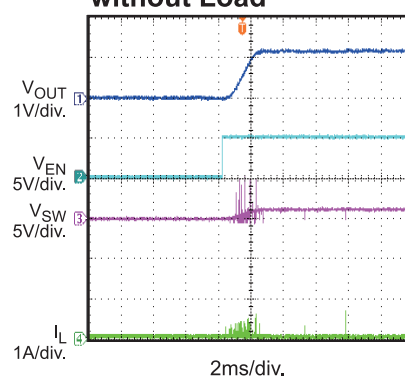
VIN Shut Down
without Load



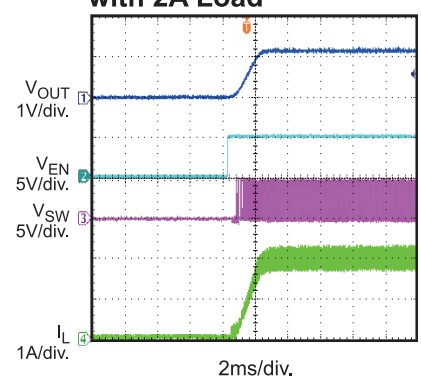
VIN Shut Down
with 2A Load



EN Start Up
without Load

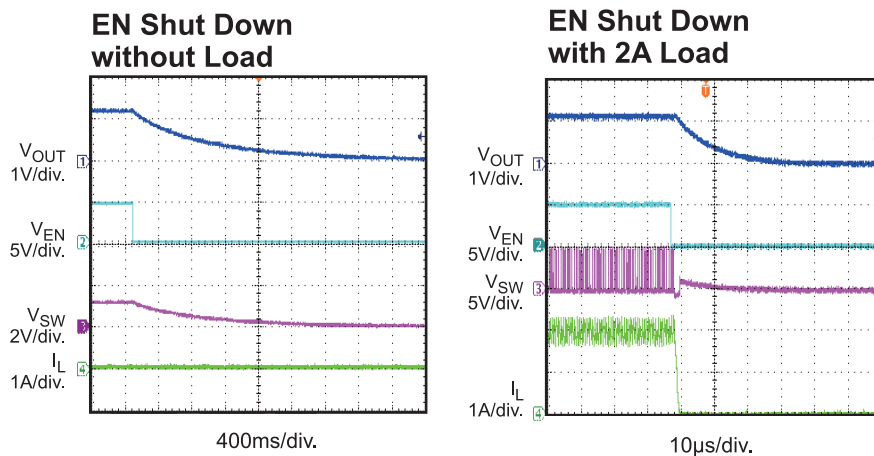


EN Start Up
with 2A Load



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 1.0\mu H$, $T_A = +25^\circ C$, unless otherwise noted



PIN FUNCTIONS

电源正常指示器。该引脚的输出是漏极开路，带有内部上拉电阻至VIN。当FB电压在调节电平的10%以内时，PGOOD上拉至VIN，如果FB电压超出该调节范围，则它为LOW。

Pin #	Name	Description
8	PG	Power Good Indicator. The output of this pin is an open drain with internal pull up resistor to VIN. PGOOD is pulled up to VIN when the FB voltage is within 10% of the regulation level, if FB voltage is out of that regulation range, it is LOW.
7	VIN	Supply Voltage. The MP2162 operates from a +2.5V to +6V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
6	SW	Switch Output 开关管输出
5	PGND	Power ground 电源地
4	OUT	Input sense pin for output voltage 输入检测引脚，用于输出电压
3	AGND	Analogy ground for internal control circuit 内部控制电路的模拟地
2	FB	Feedback pin. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. 反馈针。从输出到GND的外部电阻分压器（分接至FB引脚）设置输出电压。
1	EN	On/Off Control 开/关控制

电源电压。MP2162的工作电压范围为+ 2.5V至+ 6V。需要使用C1来防止在输入端出现大的电压尖峰。

BLOCK DIAGRAM

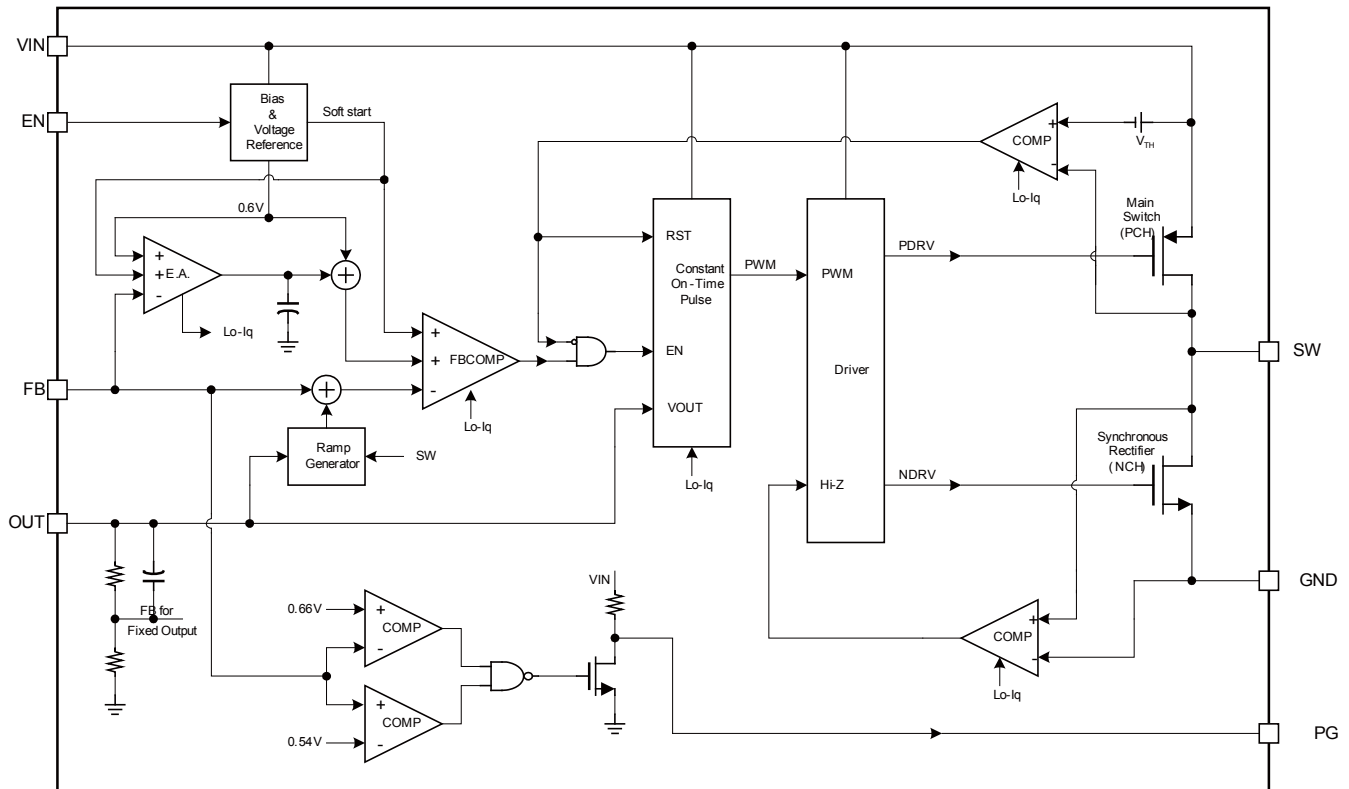


Figure 1: MP2162 Block Diagram

MP2162使用恒定的导通时间控制和输入电压前馈来稳定整个输入范围内的开关频率。在轻负载下，MP2162采用专用的低压侧开关和电感器电流控制来消除开关节点上的振铃并提高效率。

与固定频率PWM控制相比，恒定导通时间控制的优点是控制回路更简单，瞬态响应更快。通过使用输入电压前馈，MP2162在输入和输出电压范围内保持接近恒定的开关频率。开关脉冲的接通时间可以估算为：

OPERATION

MP2162 uses constant on-time control with input voltage feed forward to stabilize the switching frequency over full input range. At light load, MP2162 employs a proprietary control of low side switch and inductor current to eliminate ringing on switching node and improve efficiency.

Constant On-time Control

Compare to fixed frequency PWM control, constant on-time control offers the advantage of simpler control loop and faster transient response. By using input voltage feed forward, MP2162 maintains a nearly constant switching frequency across input and output voltage range. The on-time of the switching pulse can be estimated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.667\mu s$$

To prevent inductor current run away during load transient, MP2162 fixes the minimum off time to be 60ns. However, this minimum off time limit will not affect operation of MP2162 in steady state in any way.

Light Load Operation

In light load condition, MP2162 uses a proprietary control scheme to save power and improve efficiency. The MP2162 will turn off the low side switch when inductor current starts to reverse. Then MP2162 works in discontinuous conduction mode (DCM) operation.

The DCM mode happens only after low side switch turned off by ZCD circuit. Considering the ZCD circuit propagation time, the typical delay is 30ns. It means the inductor current still fall after the ZCD is trigger during this delay. If the inductor current falling slew rate is fast (V_o voltage is high or close to V_{in}), the low side MOSFET is turned off at the moment inductor current may be negative. This phenomena will cause MP2162 can not enter DCM operation. If the DCM mode is required, the off time of low side MOSFET in CCM should be longer than 60ns. It means the maximum duty is 90% to guarantee DCM mode at light load.

For example, V_{IN} is 3.4V and V_{OUT} is 3.3V, the off time in CCM is 20ns. It is difficult to enter

DCM at light load. And using smaller inductor can improve it and make it enter DCM easily.

Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 2.3V, MP2162 can be enabled by pulling EN pin to higher than 1.2V. Leaving EN pin float or pull down to ground will disable MP2162. There is an internal 1Meg Ohm resistor from EN pin to ground.

当输入电压大于欠压锁定阈值 (UVLO) (通常为2.3V) 时，可以通过将EN引脚拉至高于1.2V来使能MP2162。EN引脚悬空或下拉至地面将禁用MP2162。从EN引脚到地之间有一个内部1Meg欧姆电阻。

Soft Start

MP2162 has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at startup. The soft start time is about 1.5ms typical.

Power GOOD Indicator

MP2162 has an open drain with 550kΩ pull-up resistor pin for power good indicator PGOOD. When FB pin is within +/-10% of regulation voltage, i.e. 0.6V, PGOOD pin is pulled up to V_{IN} by the internal resistor. If FB pin voltage is out of the +/-10% window, PGOOD pin is pulled down to ground by an internal MOS FET. The MOS FET has a maximum $R_{ds(on)}$ of less than 100 Ohm.

Current limit

MP2162 has a typical 3.2A current limit for the high side switch. When the high side switch hits current limit, MP2162 will touch the hiccup threshold until the current lower down. This will prevent inductor current from continuing to build up which will result in damage of the components.

Short Circuit and Recovery

MP2162 enters short circuit protection mode also when the current limit is hit, and tries to recover from short circuit with hiccup mode. In short circuit protection, MP2162 will disable output power stage, discharge soft-start cap and then automatically try to soft-start again. If the short circuit condition still holds after soft-start ends, MP2162 repeats this operation cycle till short circuit disappears and output rises back to regulation level.

在轻载条件下，MP2162使用专用的恒导通时间控制来稳定整个输入范围内的开关频率并提高效率。当电感器电流开始反向时，MP2162将关闭低压侧开关，然后MP2162进入不连续导通模式 (DCM) 工作。DCM模式仅在电感电流开始反向且电压开关延迟后才发生。考虑到ZCD电路的传播时间，典型延迟为30ns。这意味着在此延迟期间触发ZCD之后，电感器电流仍会下降。如果电感器电流的下降斜率很快 (V_o 电压高或接近 V_{in})，则低侧MOSFET可能为负时，低侧MOSFET会关闭。这种操作将导致MP2162无法进入DCM操作。如果需要DCM模式，则CCM中低侧MOSFET的关断时间应大于60ns。这意味着最大负载为90%，以确保在轻负载下的DCM模式。

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 can not be too large neither too small considering the trade-off for stability and dynamic. Choose R1 to be around 120kΩ to 200kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.

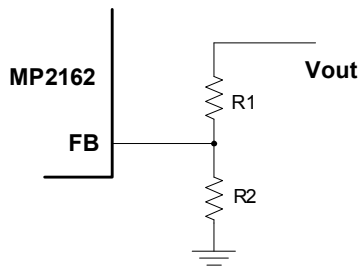


Figure 2: Feedback Network

Table 1 lists the recommended resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

A 0.68μH to 2.2μH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltage, 47μF may be needed for more stable system.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small and high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2} \right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout

Proper layout of the switching power supplies is very important, and sometimes critical for proper function. For the high-frequency switching converter, poor layout design can result in poor line or load regulation and stability issues.

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

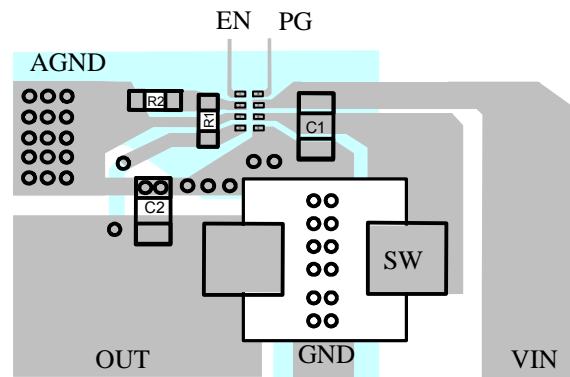


Figure 3: PCB Layout Recommendation

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	5V
V_{OUT}	1.2V
f_{SW}	1500kHz

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

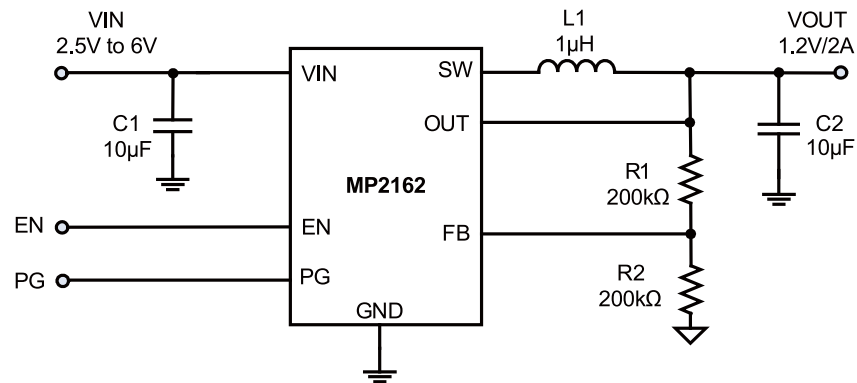
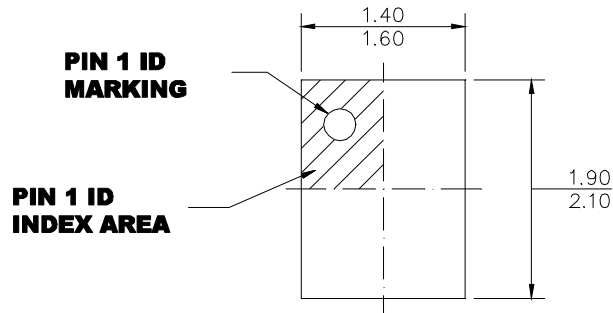


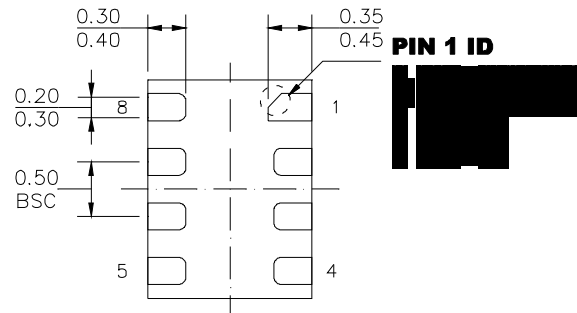
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

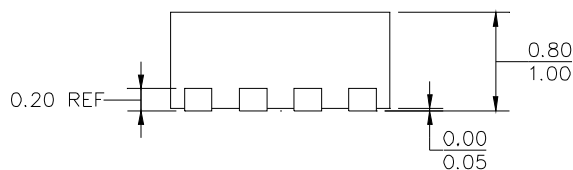
QFN-8 (2.0mm X1.5mm)



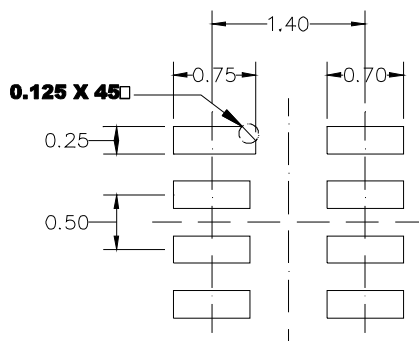
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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