VLSI
TECHNOLOGY
VERILOG TRAINING

CURRICULUM

» Introduction to VLSI

- What is VLSI
- VLSI Design Flow
- ASIC
- SoC

SECTION A:

» Fundamentals of Digital Design

FUNDAMENTALS

- Basic Digital Circuits
- Logic gates & Boolean Algebra
- Number System
- Digital Logic Families

» Combinational Logic Design

- Multiplexers
- MUX based design for digital circuits
- Demultiplexers/Decoders
- Adders/Sub tractors
- BCD Arithmetic & ALU
- Comparators & Parity Generator
- Code Converters/Encoders
- Decoders
- Multipliers/Divider

» Sequential Logic Design Priciples

- Bistable Elements,
- Latches and Flip-Flops
- Counters and its application
- Synchronous Design Methodology
- Impediments to Synchronous Design
- Shift Registers
- Design Examples & Case studies

SECTION B:
» Advanced Digital Design

- Synchronous/Asynchronous Sequential Circuits
- ASM charts
- Finite state machine
- Mealy and Moore machine
- State reduction technique
- Sequence Detectors
- Clock Dividers
- Synchronizers & Arbiters
- FIFO & Pipelining

» MINOR PROJECT
Lab Sessions on ModelSIM

SECTION C:
VERILOG

- **Overview of Digital Design with Verilog® HDL**
  Evolution of CAD, emergence of HDLs, typical HDL-based
  design flow, why Verilog HDL?, trends in HDLs.
- **Hierarchical Modeling Concepts**
  Top-down and bottom-up design methodology, differences between modules and module instances,parts of a simulation, design block, stimulus block.
- **Basic Concepts**
  Lexical conventions, data types, system tasks, compiler directives.
- **Modules and Ports**
  Modules definition, port declaration, connecting ports, hierarchical name referencing.
- **Gate-Level Modeling**
  Modeling using basic Verilog gate primitives, description of and/or and Buf/not type gates, rise, fall and turn-off delays, min, max and typical delays.
- **Dataflow Modeling**
  Continuous assignments, delay specification, expressions, operators, operands, operator types.
- **Behavioral Modeling**
  Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.
- **Tasks and Functions**
  Differences between tasks and functions, declaration, invocation, automatic tasks and functions.
- **Useful Modeling Techniques**
  Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

» Advanced Verilog Topics

- **Timing and Delays**
  Distributed, lumped and pin-to-pin delays, specify blocks, parallel and full connection, timing checks, delay back-annotation.
- **Switch-Level Modeling**
  MOS and CMOS Switches, bidirectional switches, modeling of power and ground, resistive switches, delay specification on switches.
- **User-Deined Primitives**
  Parts of UDP, UDP rules, combinational UDPs, sequential UDPs Shorthand symbols.
- **Logic Synthesis with Verilog HDL**
  Introduction to logic synthesis, impact of logic synthesis, Verilog HDL constructs and operators for logic synthesis, synthesis design flow, verification of synthesized circuits, modeling tips, design partitioning.
- **Advanced Verification Techniques**
  Introduction to a simple verification flow, architectural modeling, test vectors/testbenches,simulation acceleration emulation, analysis/coverage, assertion checking, formal verification, semi-formal verification, equivalence checking.