Hardware Synthesis Laboratory

Final Project Report

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1. Summarize IC Datasheet

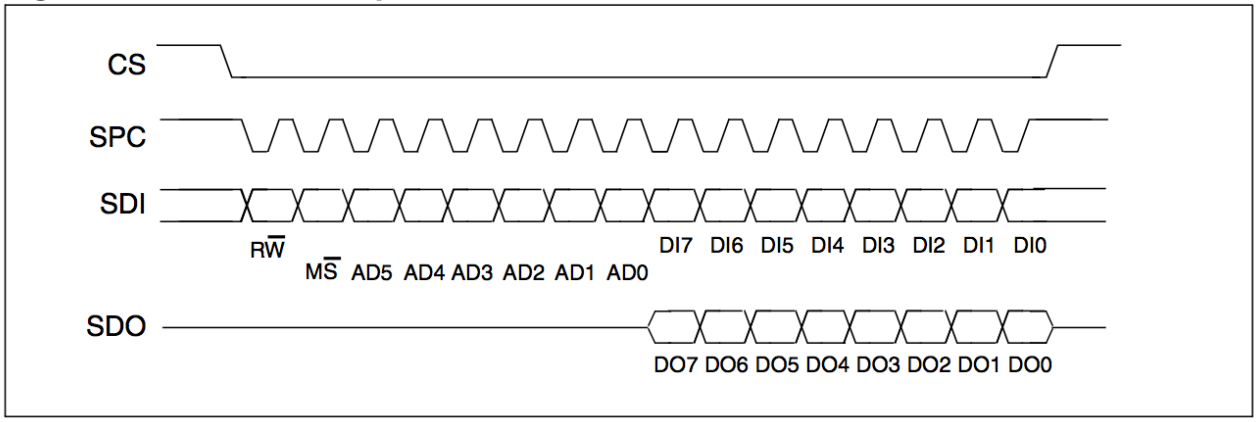
1.1 LIS302DL — Accelerometer

Scoping of LIS302DL

> The LIS302DL has dynamically user selectable full scales of +-2g/+-8g and it is capable of measuring acceleration with an output rate of 100Hz to 400Hz.

For LIS302DL. It's use SPI bus interface for data communication. There are main 4 wire that we might concern: CS, SPC (Clock), SDI (Input), SDO (Output)

Figure 6. Read & write protocol



Format of data is descriptive below the paragraph. If we need to read data use 1 for bit 0 and use 0 for bit 1 in otherwise and sent the data in bit 8-15 if write mode is enabled.

> ***bit 0***: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.
>
> ***bit 1***: MS bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.
>
> ***bit 2-7***: address AD(5:0). This is the address field of the indexed register.
>
> ***bit 8-15***: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).
>
> ***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Necessary register for this project.

Table 18. CTRL_REG1 (20h) register

DR	PD	FS	STP	STM	Zen	Yen	Xen

CTRL_REG1 is control register. There are PD bit mode for setting the power mode of IC, and Zen, Yen, Xen for enable/disable accessing the data for X, Y, Z axis.

OutX	r	29	010 1001	output	
--	r	2A	010 1010		Not Used
OutY	r	2B	010 1011	output	
--	r	2C	010 1100		Not Used
OutZ	r	2D	010 1101	output	

Here are a address list for those 3 axis register.

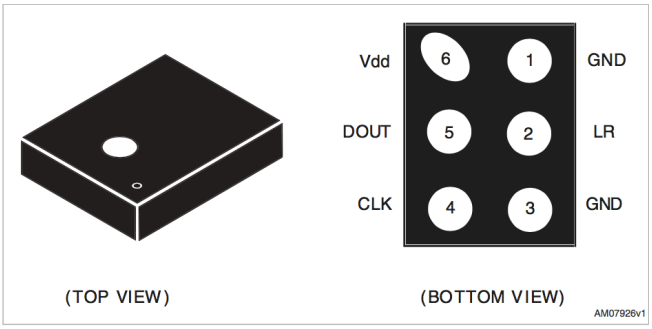
1.2 MP45DT02 — Digital Microphone

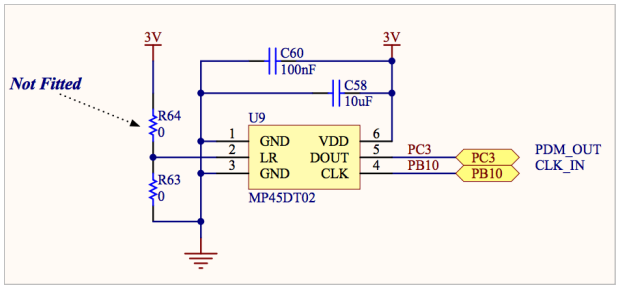
MP45DT02 use I2S for communication the data.

The STM32F4 controls the audio DAC through the I2C interface and processes digital signals through an I2S connection or an analog input signal.

- The sound can come independently from different inputs:
  - ST MEMS microphone (MP45DT02): digital using PDM protocol or analog when using the low pass filter

For data reading, we can just read directly from PC3, because all port (1,2,3,6) already connected to the board. The thing we need to implement is getting data from PC3 and config clock to PB10 (Which can be automatic config by STM32CubeMX)





1.3 CS43L22 — Speaker

I2C protocol are control port operation for CS43L22.

System Features

- I²C™ Control Port Operation

CS43L22 initial sequence.

4.9 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable.
2. Bring $\overline{\text{RESET}}$ high.
3. The default state of the “Power Ctl. 1” register (0x02) is 0x01. Load the desired register settings while keeping the “Power Ctl 1” register set to 0x01.
4. Load the required initialization settings listed in Section 4.11.
5. Apply MCLK at the appropriate frequency, as discussed in Section 4.6. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the “Power Ctl 1” register (0x02) to 0x9E.
7. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.11 Required Initialization Settings

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0x80 to register 0x47.
3. Write ‘1’b to bit 7 in register 0x32.
4. Write ‘0’b to bit 7 in register 0x32.
5. Write 0x00 to register 0x00.

In my project, I use a beep sound sending through speaker.

4.2.1 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, MSTxVOL[7:0], will affect the beep volume, DAC volume may alternatively be controlled using the PCMxVOL[6:0] bits.

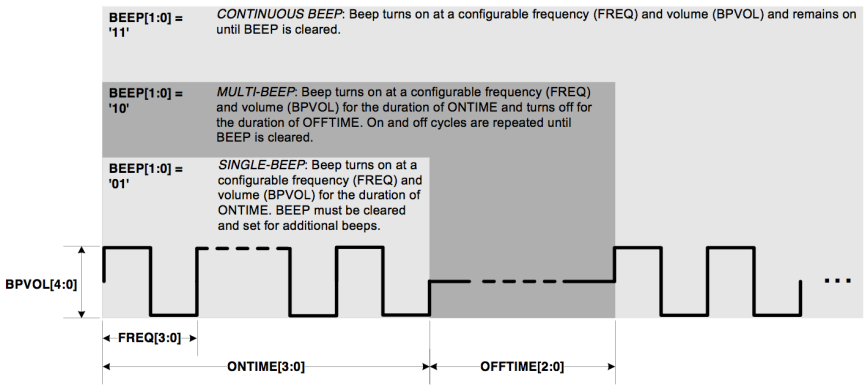


Figure 6. Beep Configuration Options

Beep sound configuration.

7.17 Beep & Tone Configuration (Address 1Eh)

7	6	5	4	3	2	1	0
BEEP1	BEEP0	BEEPMIXDIS	TREBCF1	TREBCF0	BASSCF1	BASSCF0	TCEN

7.17.1 Beep Configuration

Configures a beep mixed with the HP/Line and SPK output.

BEEP[1:0]	Beep Occurrence
00	Off
01	Single
10	Multiple
11	Continuous
Application:	"Beep Generator" on page 22

Notes:

1. When used in analog pass through mode, the output alternates between the signal from the Passthrough Amplifier and the beep signal. The beep signal does not mix with the analog signal from the Passthrough Amplifier.
2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration.

7.17.2 Beep Mix Disable

Configures how the beep mixes with the serial data input.

BEEPMIXDIS	Beep Output to HP/Line and Speaker
0	Mix Enabled; The beep signal mixes with the digital signal from the serial data input.
1	Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input.
Application:	"Beep Generator" on page 22

Note: This setting must not change when BEEP is enabled.

Beep frequency for adjusting the sound pitch.

7.15 Beep Frequency & On Time (Address 1Ch)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

7.15.1 Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	Frequency *(Fs = 12, 24, 48 or 96 kHz)*	Pitch
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	"Beep Generator" on page 22	

The data transmission control part is not much complex because the STM32F4 already provided I2C API. Just use the API function and everything is done for you. By the way, the some condition and data pattern isn't known yet. You must read the I2C data interface below before.

The upper 6 bits of the address field are fixed at 100101. To communicate with the CS43L22, the chip address field, which is the first byte sent to the CS43L22, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS43L22 after each input byte is read and is input to the CS43L22 from the microcontroller after each transmitted byte.

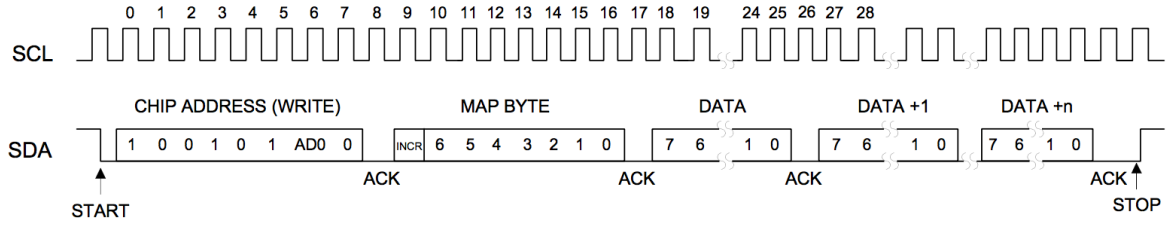
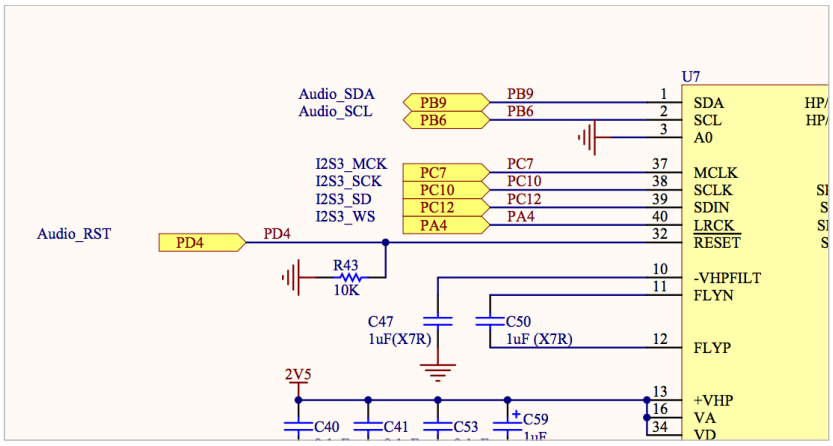


Figure 16. Control Port Timing, I²C Write

Pin set data sheet.



Pin Name	#	Pin Description
SDA	1	**Serial Control Data** (*Input/Output*) - SDA is a data I/O in I²C Mode.
SCL	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0	3	**Address Bit 0 (I²C)** (*Input*) - AD0 is a chip address pin in I²C Mode.
$\overline{\text{RESET}}$	32	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	33	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port.
VD	34	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	35	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
MCLK	37	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	38	**Serial Clock** (*Input/Output*) - Serial clock for the serial audio interface.
SDIN	39	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	40	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.