Design Tips for Use with Avago Smart Eight-Character Alphanumeric LED Displays

Application Brief D-001

Introduction

New equipment designs are utilizing eight character, smart, alphanumeric, LED displays from the HDSP-211X, HDSP-213X, HDSP-253X, and HDSP-250X families as an effective means of transferring information across the man/machine interface. These smart LED displays have on-board CMOS ICs that provide all of the logical functions needed to accept, store, decode ASCII or user defined information, and drive the eight character LED matrix.

This application brief provides tips on accomplishing an effective design utilizing these LED displays.

Toggle CHIP ENABLE and WRITE Together to Load Data

WRITE (WR) and READ (RD) determine if data is either loaded into or read from either the ASCII RAM or the User Definable Character (UDC) RAM. Data is read into one of these two display RAMs when WR pulse makes a transition from logic low (true) to logic high. Data is read from one of these two RAMs when RD makes a transition from logic low (true) to logic high.

CHIP ENABLE (CE) must be toggled through a transition from logic high to logic low (true) and back to logic high for each character loaded into or read from one of the display character RAMS. The actual data transfer occurs at the rising edge of a CE pulse transition from logic low (true) to logic high. CE cannot be held at logic low (true) continuously while attempting to transfer data by toggling only WR or RD. When CE is held at logic low (true), the internal IC RAM address lines are open to the external address input bus. Any noise or data change on the external address input bus while CE is at logic low will cause data within the display RAMs to be relocated to other addresses within those RAMS, scrambling the data, regardless of the logic levels of WR and RD.

The most effective interface design is to electronically connect CE and WR together to write data to the display, and electronically connect CE and RD together to read data from the display, so they toggle as double pole double throw switches.

Thus, to load data into a display character RAM, the character address and data are first established to be true and stable on the external address and data input buses. Then, CE and WR are electrically toggled together from logic high to logic low (true) and back to logic high to load and latch the data into the selected character RAM. Similarly, CE and RD should be toggled together from logic high to logic low (true) and back to logic high to read data from a selected character RAM.

Synchronized Display System Clocks

In a display system that uses more than one alphanumeric LED display device, it is desirable to have all of the display clocks synchronized. This facilitates data loading and eliminates any possibility of visual abnormality due to differences in display on-board IC clock frequencies.

For systems operating within a narrow ambient temperature range, such as with office equipment where the ambient is room temperature, it is effective to have the clock of one display act as the master clock device.

The CLOCK INPUT/OUTPUT (CLK) of the master clock device can be electrically connected to the CLOCK INPUT/OUTPUTs (CLK) of the slave clock devices. CLOCK SELECT (CLS) on the master clock device is set to logic 1, activating the output of its internal clock. The CLOCK SELECTs (CLS) on the slave clock devices are set to logic 0, deactivating their internal clocks and accepting the master clock input frequency. One master clock device can drive up to 10 slave clock devices.

For operation in environments with wide operating temperature ranges, such as in industrial, aerospace, and military applications, it is necessary to use an external, temperature compensated master clock. This is necessary because the frequency of the on-board CMOS IC clock is not temperature stable, varying widely with temperature. This external master clock should drive all of the LED display devices. All the display devices should have CLS set to logic 0 to accept the external master clock frequency. The external master clock frequency should be set at 57 kHz.

Loading User Definable Characters into the UDC RAM

To assure the correct placement of data into the User Definable Character (UDC) RAM, it is recommended that the character data be loaded in reverse order, the last character position loaded first and first character position loaded last. This asssures character address location stability of the data within the UDC RAM should the display RESET function be activated. Then during the RESET function, the on-board IC overwrites the first character location in the UDC RAM with the last character data that was loaded into the RAM. Thus, loading the first character position data last will assure that first character data (which was the last data to be loaded) is rewritten into the first character address location within the UDC RAM should display RESET be actvated.

Separate the Logic and LED Supply Grounds

These smart alphanumeric LED displays have two ground pins, one for logic ground, GND (LOGIC), and one for LED supply current ground, GND (SUPPLY). These two grounds should be separate from each other all the way back to the power supply. The logic ground pin carries minimal logic signal currents and should be connected to the same ground servicing other logic IC devices on the pc board. The LED supply ground should be a separate return path from logic ground. The LED supply ground can carry up to 802 mA per display device, being switched at a nominal 256 Hz rate as the display on-board IC refreshes the LED character matrix. This 802 mA occurs when a 20-dot character, such as the pound sign (#), is illuminated in all eight characters. Thus, the maximum possible total LED supply current would be 802 mA times the number of alphanumeric LED display devices in the display system.

Zero Inductive Impedance Required for LED Supply Ground

The LED supply ground path must return this high level of LED current back to the power supply without a voltage drop. Any voltage drop on the LED supply ground return could show up as 256 Hz noise throughout the electronic system. To prevent noise at 256 Hz from showing up throughout the electronic system, the inductive impedance of the LED supply ground return path back to power supply should be as close to zero as possible at the frequency of 256 Hz.

Power Supply Must Withstand Large Current Surges

The power supply must be designed to provide the maximum peak LED drive current for the display system. The power supply must also be able to withstand the large peak current surges caused by the strobing of the LED matrices within the alphanumeric LED display devices. As the peak LED current demand of illuminated character string in the display system changes, the power supply must be able to maintain a constant, stable source voltage while experiencing this constantly changing high peak current loading.

On-Board CMOS IC Maximum Junction Temperatures

There are two maximum IC junction temperatures to consider, one for IC operating parameters and the CMOS IC Absolute Maximum Temperature Rating. The first maximum temperature is T_J (IC) MAX = 125° C for operating parameters.

The operating parameters for the display on board ICs have been characterized up to an IC junction temperature of 125° C and are listed on device data sheets. The second maximum temperature is the CMOS IC Absolute Maximum Junction Temperature, T_J (IC) ABSOLUTE MAX = 150° C. The on-board CMOS ICs will function with reduced performance up to the 150° C absolute maximum rating. The IC parameters have not been characterized for IC junction temperatures between 125° C and 150° C.

Thermal Resistance Design of the Printed Circuit Board

The junction temperature of the display on-board CMOS IC is much higher than the junction temperatures of the individual LEDs within the eight character LED matrix. Therefore, to assure reliable operation, it is necessary to design for as low a thermal resistance, pc temperatures of the individual LEDs within the eight character LED matrix. Therefore, to assure reliable operation, it is necessary to design for as low a thermal resistance, printed circuit (pc) board-to-ambient on a per LED device basis as practical. The primary thermal path from the display on-board IC to the pc board is through the device leads, primarily the V_{DD} and Ground leads. Effective low thermal resistance design can be achieved by using large metal lands instead of thin traces in the pc board layout. For example, assuming a worst case power dissipation of 1.865 W per LED device, a "#" sign illuminated in all eight characters, the thermal resistance, display-to-ambient through the pc board, Rq_{PC-A}, should be less than 25° C/W on a per device basis to assure reliable operation in an ambient temperature of 50° C. The IC junction temperature does not exceed 125° C. The alphanumeric LED device thermal resistance IC-to-pin is $R\theta_{IC-PIN}$ = 15° C/W.

$$T_J\,(IC) = T_A + (R\theta_{J-A})\,(P_{LED\ DEVICE})$$
$$= 50°\,C + (25°\,C/W + 15°\,C/W)\,(1.865\,W)$$
$$= 50°\,C + (40°\,C/W)\,(1.865\,W)$$
$$T_J\,(IC) = 125°\,C$$

Note:

$$R\theta_{J-A} = R\theta_{PC-A} + R\theta_{IC-PIN}$$

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