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MICRO II COMPUTER

PRELIMINARY

ENGINEERING NOTES



GARRETT MANUFACTURING LIMITED

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Micro II



WHAT IT IS:

The MICRO II COMPUTER is a COMPLETE computer with a basic memory capacity of 256 words and a complement of 16 instructions, 3 of which have indirect addressing capability. This is a GENERAL PURPOSE machine and is therefore suitable for a wide range of applications covering such fields as RESEARCH, TEACHING, and INDUSTRY.

Teaching institutions find the MICRO II ideal for economically demonstrating—MACHINE LANGUAGE PROGRAMMING, INTERFACING TECHNIQUES, FLOWCHARTING, COMPUTER ORGANIZATION and many other aspects of digital technology.

Similarly industry has found that the MICRO II is capable of solving simple PROCESS CONTROL problems at an exceedingly MODERATE price.

A complete line of accessories is available with the MICRO II, thus enabling the user to "custom tailor" his digital system.



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SPECIFICATIONS:

MEMORY	<ul style="list-style-type: none"> • 256 words • expandable (decoded internally for 2K) • bipolar 	INSTRUCTION SET
WORD LENGTH	• 8 bits to the word	STR store AC ADD add (2's compl) JMP - jump CLR clear AC CMP complement AC RTL rotate AC left RTR rotate AC right ORS OR data switches into AC NOP no operation HLT halt SNO skip if no overflow SNA skip if non-zero AC SZS skip if sign bit=0 SFG skip if device flag set INP input data to device from AC OUT output data to device from AC
EXECUTION TIME/ INSTRUCTION	• <1.0 μ sec	STR, ADD, JMP are memory reference instructions with indirect addressing capability.
ORGANIZATION	<ul style="list-style-type: none"> • parallel • synchronous control 	SFG, INP, OUT instructions pertain to INPUT/OUTPUT devices.
REGISTERS	<ul style="list-style-type: none"> • IR—Instruction Register—8 bits • PC—Program Counter—8 bits • MDR—Memory Data Register—8 bits • MAR—Memory Address Register—8 bits • AC—Accumulator—8 bits + 1 bit for overflow • MSR—Memory Selection Register—4 bits with expansion capability 	

INPUT/OUTPUT

- Up to seven different input and / or output devices may be addressed.
- Data may be transferred into the machine via panel data loading switches or peripheral equipment, i.e. paper tape, cassette recorder, or keyboard.
- Inputs and outputs are brought out to:
 - (a) jacks mounted on the front panel of the machine
 - (b) cable connectors mounted on the side of the machine

DISPLAYS

- Data contained in the Accumulator, Program Counter, and Instruction Registers is displayed by Light Emitting Diodes mounted on the front panel of the machine. The overflow bit is also displayed.
- Visible displays are provided for the POWER ON mode and the RUN mode.

PANEL SWITCHES

- Front panel switches are provided for the following functions:
 - (a) Data loading (8 switches)
 - (b) Single stepping
 - (c) Start
 - (d) Run / Stop
 - (e) Load Address
 - (f) Load Data
 - (g) Display
 - (h) Power ON / OFF

OPERATING FEATURES

- Single Step facility
- Program Counter is incremented automatically as data is loaded into memory.
- Display button allows verification of the program.

POWER REQUIREMENTS

- 5 Vdc, regulated to $\pm .25\%$ at 3 Amperes.
- MICRO II (P) picks up power from the MDL-1000 main frame.

ACCESSORIES

- keyboards (a) numerical
(b) operator (specify keytops)
- ribbon cables and connectors
- 5 Vdc auxiliary power supply for MICRO II (GDM 1508)
- Instructional software
- all modules and options available with the MDL-1000 Digital Laboratory Simulator.
- *paper tape read-in and read-out machine
- *quarter punch card reader
- *magnetic tape cassette recorders

*Available Soon



MODEL CONFIGURATIONS

MICRO II MODEL	CONFIGURATION	LOCATION OF PERIPHERAL CONNECTOR	POWER PICKUP
P	MDL1000* Mainframe Mount	Right Hand Side	Banana Jacks Allowing Power Pickup From MDL1000 or Separate Connector on Rear.
R	Standard Rack Mount	Rear	Separate Connector on Rear
RP	Standard Rack Mount With Power Supply	Rear	Separate Connector on Rear
D	Desk Top	Rear	Separate Connector on Rear
DP	Desk Top With Power Supply	Rear	Separate Connector on Rear

* MDL1000 - Modular Digital Lab By Garrett Manufacturing Ltd.,
Capable of Accepting up to 43 Digital Modules Having
Various Simple to Complex Standard Logic Functions.



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DISPLAYS

Accumulator

The ACCUMULATOR (AC) contents are displayed in binary form by 8 LIGHT EMITTING DIODES (LED's). The most significant bit (MSB) is in position "7" and the least significant bit (LSB) is in position "0". The ACCUMULATOR contains the data currently being processed by the computer. The ACCUMULATOR contents are not affected by depression of the following manual pushbutton controls: LOAD ADDRESS, LOAD DATA and DISPLAY.

Program Counter

The contents of the PROGRAM COUNTER (PC) are displayed via 8 LED's. The MSB is in position "7", and the LSB is in position "0". The PC displays only addresses. It normally indicates the address of the next instruction to be accessed or the address in which data will be entered via the data switches on the front panel. The PC is incremented automatically after each instruction execution or by the depression of any of the following pushbuttons with the RUN/STOP switch in the STOP mode: DISPLAY, LOAD ADDRESS, LOAD DATA and START. This register can be pre-set to any address by either manually loading a new address or by a JUMP instruction while executing a program.



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Instruction Register

The contents of the INSTRUCTION REGISTER (IR) are displayed by 8 LED's. The MSB is in position "7"; the LSB is in position "0". In the normal RUN mode, the IR is a holding register for the instruction currently being executed. The IR is updated with a new instruction from memory each time an execution cycle is initiated. When single stepping a program, with the computer in the STOP mode, the IR displays the last instruction executed. If the computer halts during program execution, the IR displays the last instruction executed. When loading data into memory from the data switches, the IR displays the last data loaded into memory. When the DISPLAY pushbutton is depressed, the IR displays the contents of the memory location defined by the address displayed in the PROGRAM COUNTER prior to the depression of the DISPLAY button.

Run Light

One LED is used to indicate that the computer is in an execution cycle. The light will blink momentarily when a manual control switch is depressed. The light will remain on as long as the computer is executing instructions.



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Overflow Light

One LED is used to indicate a carry or overflow condition in the accumulator.



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REGISTERS

1) Memory Address Register (MAR)

This is a holding register for the address of the current instruction being accessed. This register is updated with a new address each time an instruction execution is initiated.

2) Memory Data Register (MDR)

This is a temporary holding register for the direct address derived from an indirect memory reference instruction before the direct address is loaded into the MAR.

3) Instruction Register (IR)

This is a register that contains the current instruction being executed. This register is updated with a new instruction (from memory) each time an execution cycle is initiated.

4) Memory Selection Register (MSR)

This register contains the necessary decoding logic to select the desired memory bank. This register is enabled only with an OUT instruction together with device address 000.



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5) Accumulator (AC)

This is a holding register for the current data being processed.

Data may be ORed into the AC via the X bus lines or Added into the AC via the Y bus lines.



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CONTROLS

Data Switches

The DATA SWITCHES consist of a bank of eight (8) switches with the MSB in position "7" and the LSB in position "0". With the switches in the up state, 1's are entered into the computer, in the down position, 0's are entered. To enter information into the computer, the DATA SWITCHES are pre-set to the appropriate positions and then either the LOAD DATA or LOAD ADDRESS switch is depressed.

Run/Stop Switch

With this switch in the STOP position, the computer is under manual control. In this mode, the computer may be single stepped through a program, instruction by instruction, by depressing the START/STEP pushbutton. In the STOP mode, data may be entered or viewed at will, by depressing the appropriate switch.

If a complete program is to be executed automatically, the switch is set to the RUN position and the START pushbutton is depressed. In the RUN mode, execution may be manually interrupted at any time by returning the switch to the STOP position.



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Start/Step Pushbutton Switch

This pushbutton has two major functions dependent upon the state of the RUN/STOP switch.

- (1) If the RUN/STOP switch is in STOP position, depression of START will allow the computer to execute only the instruction associated with the address displayed in PC. After this single execution the computer will halt again awaiting further manual instructions. This procedure may be repeated as many times as required.
- (2) If the RUN/STOP switch is in the RUN position, depression of the START pushbutton will allow the computer to sequentially execute a complete program. Prior to the depression of START, the PC must be initialized to the address of the first instruction to be executed.

Load Address Pushbutton Switch

This pushbutton is used with the computer in the manual (STOP) mode. This control loads the PC with the address determined by the data switch settings. The address of the data switches will be immediately displayed in the PC. When loading a sequential program, only the initial address must be loaded. The PC is then automatically incremented after each LOAD DATA command.



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Load Data Pushbutton Switch

This pushbutton is used with the computer in the manual (STOP) mode. Depression of the pushbutton loads the data determined by the data switches into the memory defined by the address displayed in the PC. The loaded data will then immediately appear in the IR and the PC will increment by one.

Display

This pushbutton is used with the RUN/STOP switch in the STOP mode. Depression of this pushbutton causes the contents of memory, at the address displayed in the PC (prior to depression), to be displayed in the IR. The PC increments by 'one' after the use of this control.

Example Use of Manual Controls

Suppose the Accumulator (AC) is to be cleared. The instruction required is 11000000. The instruction may be loaded into any memory address not being used for other instructions. Assume the instruction is to be loaded in address 10110001. The procedure is as follows:



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1. Set RUN/STOP switch to STOP.
2. Set 10110001 (ADDRESS) on the DATA switches.
3. Depress LOAD ADDRESS switch.
 - The PC will display 10110001
4. Set 11000000 (clear instruction) on the DATA switches.
5. Depress LOAD DATA switch.
 - The IR will display 11000000
 - The PC will now display 10110010
(Note that it has been incremented by one).
6. Reload the ADDRESS of the instruction (i.e. 10110001) into the PC as per steps 2 & 3 above.
 - The PC will now contain 10110001.
 - The IR will remain unchanged.
7. To execute this one instruction depress the START/STEP switch.
 - The AC will now contain 00000000
 - The PC will now contain 10110010
 - The IR will now contain 11000000



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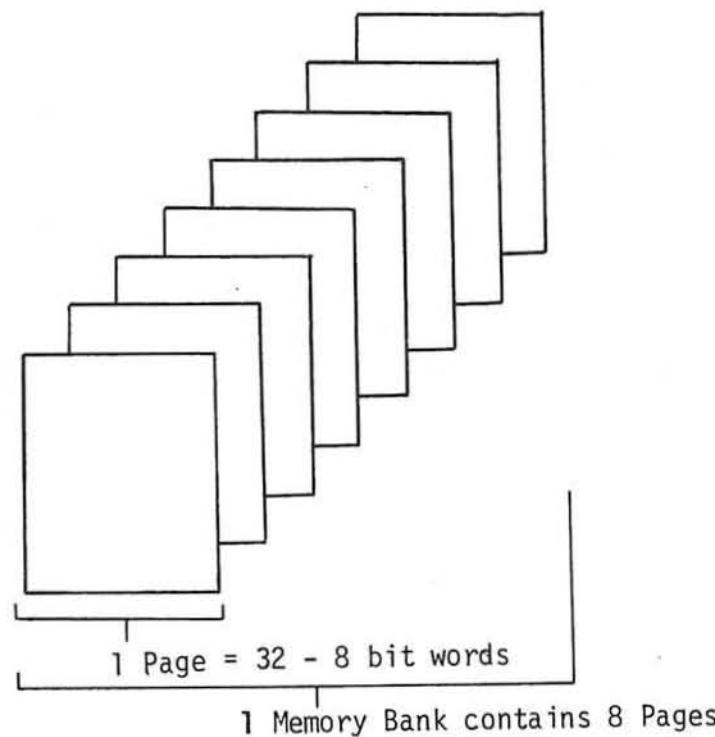
MEMORY ORGANIZATION

The MICRO II's memory is divided into memory banks with each bank divided into eight pages, each page having 32 words. Therefore, each bank has 256 8-bit words. Each 8-bit address may be divided into two sections: the page number and word number.

$A_7 \ A_6 \ A_5$	$A_4 \ A_3 \ A_2 \ A_1 \ A_0$
Page Number	Word Number

The pages are: (0 to 7)

000, 001, 010, 011, 100, 101, 110, 111



Each page has the following words: (0 to 31)

00000, 00001, 00010, 11111.



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Direct and indirect addressing are both unrestricted within each page. If a memory reference instruction operates upon a different page from the current one, then indirect addressing must be used. Program instructions may be loaded consecutively within any number of pages keeping in mind the restrictions on memory reference instructions.

The Micro II is internally decoded for 7 additional memory banks (up to 2048 words). To access the additional memory banks the reader is referred to the section titled "Memory Expansion".

Addressing Modes (Direct, Indirect)

In the MICRO II COMPUTER, two modes of addressing may be used: direct and indirect. With direct addressing, the 5 LBS's in the memory reference instruction are sent to the memory address register (MAR), and the word specified by the MAR is fetched to the processor. With indirect addressing, the address part of the instruction is first used to fetch a word from storage and place it in the memory data register (MDR). Next the MDR contents are placed in the MAR and the MAR used to fetch the new word into the processor.



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The Need for Indirect Addressing

In the MICRO II computer, there are three memory referencing instructions:

JUMP 00*AAAAA

STORE 01*AAAAA

ADD 10*AAAAA

The two most significant bits are the operation code of the instruction word, while the five least significant bits are the memory location of the word to be operated upon.

With a five bit addressing capability it is only possible to address 32 words (00000 to 11111). Thus with a memory capable of holding more than 32 words it is impossible to address any word beyond memory location 31.

The * portion of the instruction is the means by which addressing of any memory location up to 255 (11111111) is accomplished.

When a "0" is detected in the * portion of the memory reference instruction, the address part is identified as a "direct" address. The data word at that 5 bit address is operated upon as specified by the op code.

A "1" in the * portion of a memory reference instruction indicates to the computer that it must use the 8 bit word at the 5 bit address specified in the instruction as the address of the data word to be operated upon.



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COMPARISON

DIRECT

5 bit address specifies the address of an 8 bit data word.

INDIRECT

5 bit address specifies the address of an 8 bit word which specifies the address of an 8 bit data word to be operated upon.

Indirect Addressing

Example - Data in the Accumulator is to be stored in a memory location beyond the range of a 5 bit address (not within the current page).

MEMORY ADDRESS

Decimal	Binary	Contents	Meaning
10	<u>0 0 0</u> <u>0 1 0 1 0</u> Page Word	<u>0 1 1</u> <u>1 1 1 1 1</u> Store Word Address	Word in location 10 of Page 000 states; store the contents of the accumulator in the address specified in location 31 of the current page. (000)
31	<u>0 0 0</u> <u>1 1 1 1 1</u> Page Word	<u>1 1 0</u> <u>1 1 1 0 1</u> Page Location	The data in location 31 of page 000 specifies the 8 bit address into which the data of the accumulator must finally be placed, this address being page 6 (110) location 25 (11101).
25	<u>1 1 0</u> <u>1 1 1 0 1</u> Page Word	<u>D D D D D D D D</u> Data	

NOTE:- The indirect address indicator only appears in the original memory reference instruction.



Direct Addressing

Example - Data in the Accumulator is to be stored in a memory location within the range of a 5 bit address.

ADDRESS

Decimal	Binary	Contents	Meaning
1	0 0 0 0 0 0 0 1 Page Word	0 1 0 0 0 1 0 1 Op Code Word Address	Store the contents of the accumulator in the address specified by the 5 LSB's (00101)
5	0 0 0 0 0 1 0 1 Page Word	D D D D D D D D Data	The data originally in the accumulator is stored in memory address 5, (00101)

NOTE:- When using direct addressing, the page in which the 5 bit address is to be found is assumed to be the same page number in which the memory reference instruction is located. There is an exception to this rule which is discussed in the "Instruction" section under the subtitle "Memory Reference Instructions", Note iii.



Memory Expansion and Selection

The basic MICRO II COMPUTER is supplied with one memory bank. Up to eight memory banks may be accommodated within the computer case. Each additional memory bank card is simply plugged into the appropriate card edge connector in the rear of the unit. One of the cards (Memory Selection Register) has a row of eleven slide switches, coded alphabetically A, B, C, D, E, F, G, H, J, K and L. The number of memory banks in the unit determine which switches are ON (in the UP position).

<u>Number of Memory Cards</u>	<u>Switches in "ON" State (UP)</u>
1	ADG
2	BDG
3	CFG
4	BEG
5	BEH
6	BEJ
7	BEL
8	BEK

When the computer is first turned on, memory selection is a random event and the slide switches make certain that a legal memory card is always selected. After the unit has been turned on, memory bank initialization (selection) may be accomplished with the following procedure:



iii) OUT

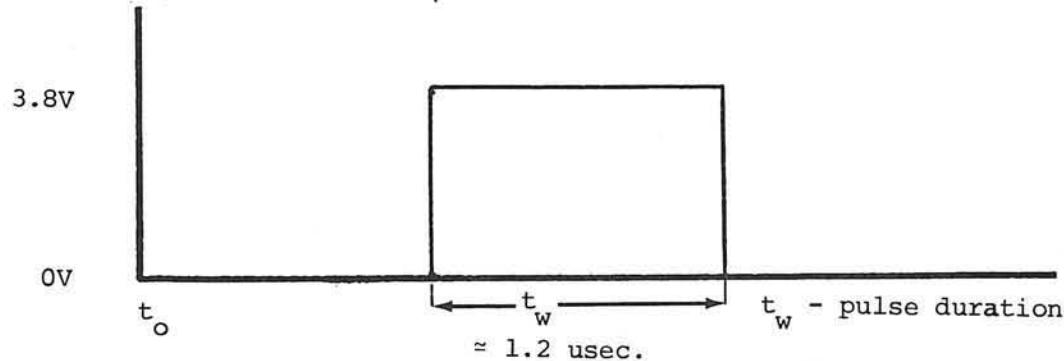
This instruction allows the computer to output data to the device specified by the device address code. A clock signal, OUTc, is available at a connector to clock the output data into the device when the computer is ready to output. (See timing chart for I/O instructions).



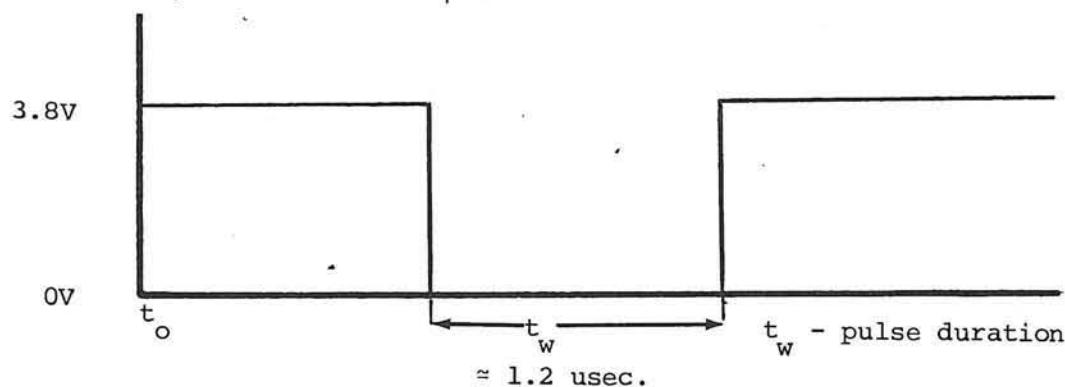
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TIMING CHART FOR I/O INSTRUCTIONS

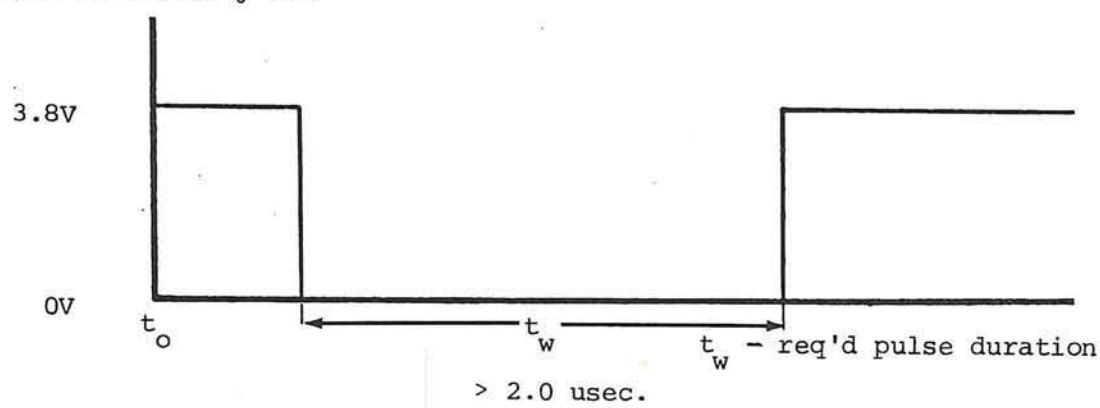
- INg - This pulse is generated by the INP (Input) instruction
- Is normally LO
- Is not an open collector output



- OUTc - This pulse is generated by the OUT (Output) instruction
- Is normally HI
- Is not an open collector output



- FLAG - This pulse must be generated by the peripheral equipment.
It tells the computer to skip if the Flag Bit is set LO.
This pulse must be greater than 2 usec in width.
- Must be normally HI.



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COMPUTING TIMES

The MICRO II COMPUTER has an internal clock frequency of 2 MHz. The computer was designed to operate at clock frequencies up to 20 MHz. The 2 MHz clock frequency was chosen as a compromise between speed and noise effects. With this clock frequency the time for any execution is less than 500 nanoseconds. The times given below include both the execution time and the time required for fetching or jumping. The time given below is the maximum total time it takes for the computer to leave and return to its initial state.

<u>INITIAL STATE</u>	<u>MODE</u>	<u>TYPE OF INSTRUCTION</u>	<u>ADDRESSING</u>	<u>TIME (us)</u>
t_0	Manual	DISPLAY, LOAD DATA, LOAD ADDRESS		2
t_0	Manual (single step- ping)	REG		2.5
t_0	Manual (single step- ping)	REG	Direct	3.0
t_0	Manual (single step- ping)	REG	Indirect	4.0
t_1	Auto	REG		1.5
t_1	Auto	REG	Direct	2.0
t_1	Auto	REG	Indirect	3.0

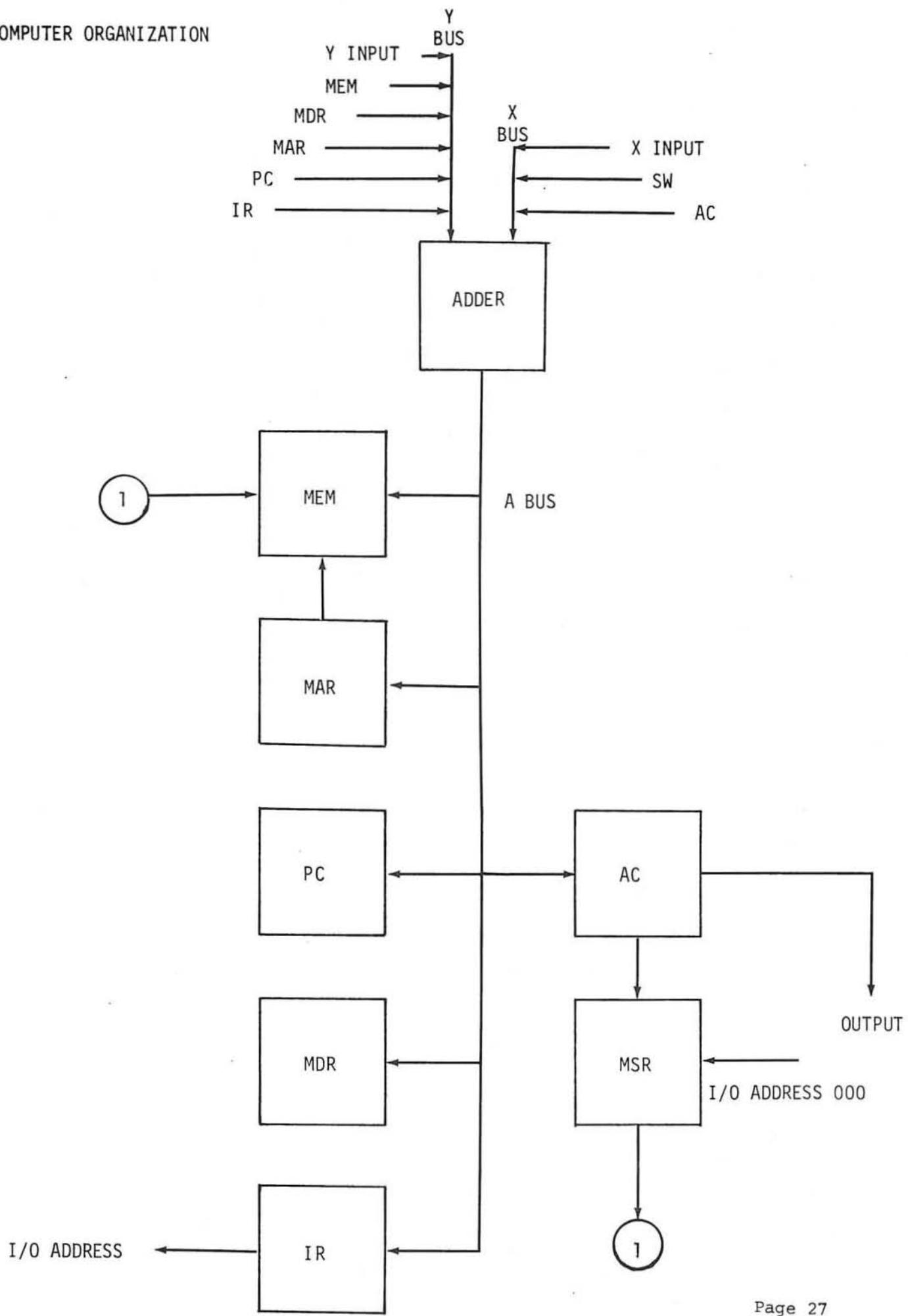
NOTE:- REG = any instruction except ADD, JMP, STR

REG = ADD, JMP, STR

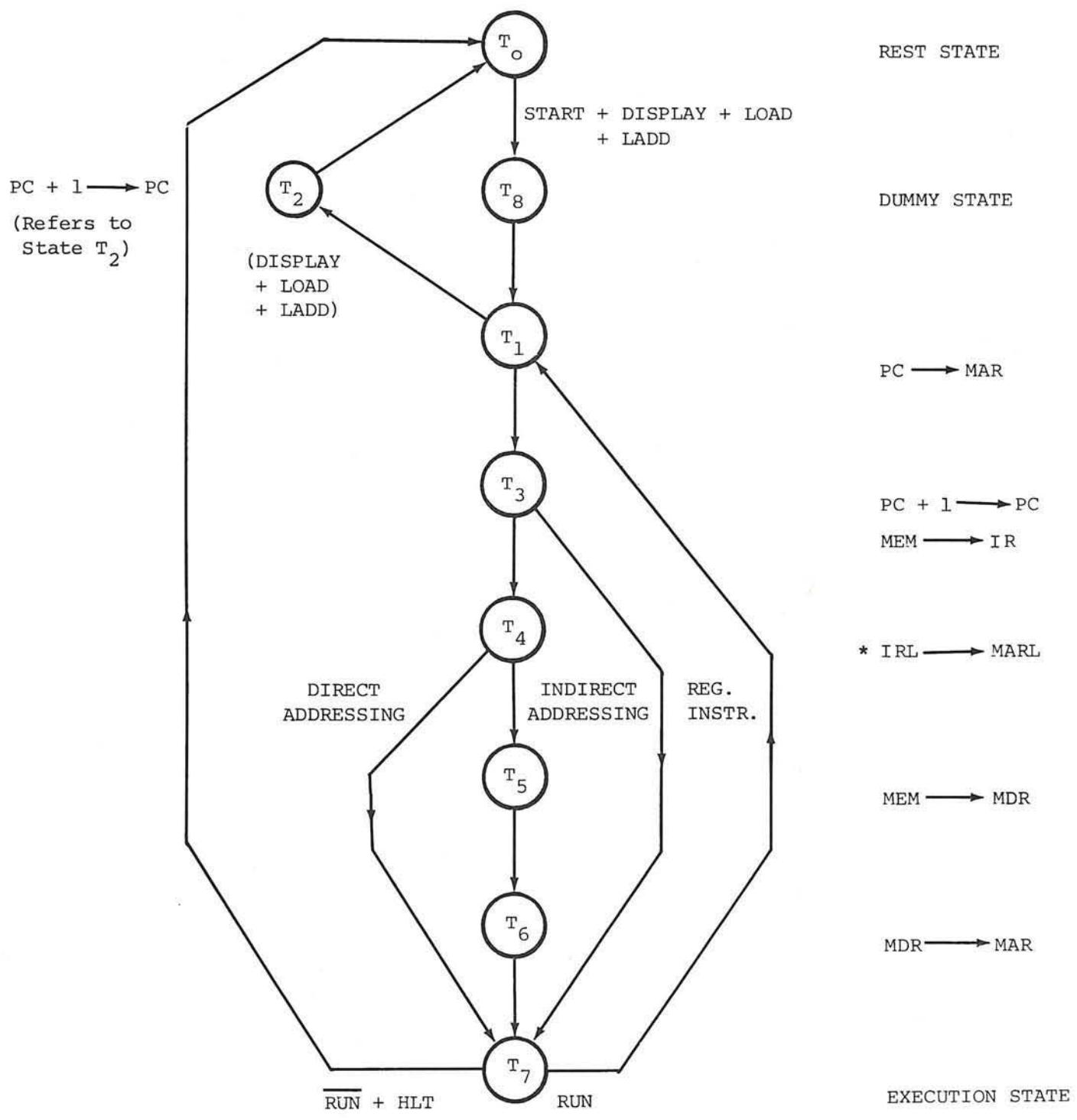


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COMPUTER ORGANIZATION



STATE DIAGRAM



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INPUT/OUTPUT FACILITIES

A connector on the MICRO II provides for all the I/O facilities.

Up to seven external devices may be directly addressed by using the device address bus lines located at the connector as D₂ D₁ D₀ output.

- 1) Data inputed to the computer on the X bus is OR-ed into the AC with the current AC contents and the result placed in the AC. The data presented to the X bus must be in its complemented form.
- 2) Data inputed to the computer on the Y bus is added to the current AC contents and the result placed in the AC. The data presented to the Y bus must be in its complemented form.
- 3) The AC or output bus contains the current true data in the AC and may be outputed to a device. (See Note 6).
- 4) The D₂ D₁ D₀ bus lines contain the true device address of the device being accessed during an I/O instruction.
- 5) A computer generated gate signal, INg, is available to gate data into the computer from a device when the computer is ready to accept data. This line is normally at logical 0 and goes to logical 1 when the computer is inputing data (during INP instruction).
- 6) A computer generated clock signal, OUTc, is available for an external device to clock the computer outputs into an interface. This signal is generated only when valid data is present at the AC bus output during execution of an OUT instruction. This line is normally at a logical 1 level and goes to logical 0 when the computer is ready to output data.



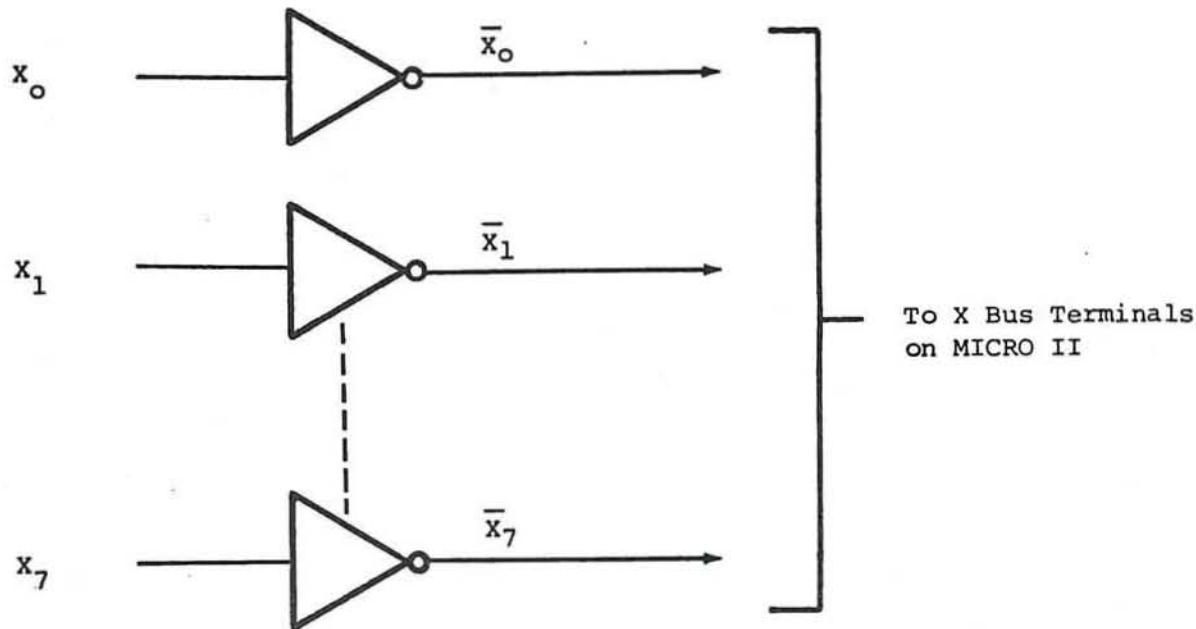
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- 7) An input line, FLAG, is available to be used in conjunction with the SFG instruction. The peripheral equipment must generate the signal for this line. Normally FLAG is held at a logical 1 until such time as the peripheral equipment is ready to INPUT data to and/or OUTPUT data from the computer, whereupon the signal is brought L0. Hence if there is an SFG instruction associated with a particular I/O device whose flag is set "L0", the computer will skip to the next instruction.



INTERFACE CONNECTIONS

X Bus Interface



- NOTES:
1. Use open collector gates when tying to X-Bus.
 2. Pull up resistors are not required, they are already present within the computer.
 3. Data must be inverted when tying into X-Bus.

Y Bus Interface

Same as X Bus.

Accumulator Output Bus

The outputs of the accumulator are the TRUE outputs. All outputs are buffered, (fanout = 10), and do not require pull up resistors. i.e., outputs are not open collector.

Device Address Lines

The outputs of the device addresses, \$D_2\$, \$D_1\$, \$D_0\$ are the true outputs.

These outputs are buffered, (fanout = 10), and are not open collector outputs.



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TYPICAL INTERFACE CIRCUIT

Problem Statement

It is required to interface between a temperature sensor and the MICRO II computer, and also between the MICRO II and a magnetic Tape Deck.

Specifications

Temperature Sensor - range 0°F - 100°F
voltage output 0V-10V

Magnetic Tape Deck - Will be run in the "continuous mode"
- Requires a STOP WRITE COMMAND signal
- Generates a FLAG when ready to accept data

Solution

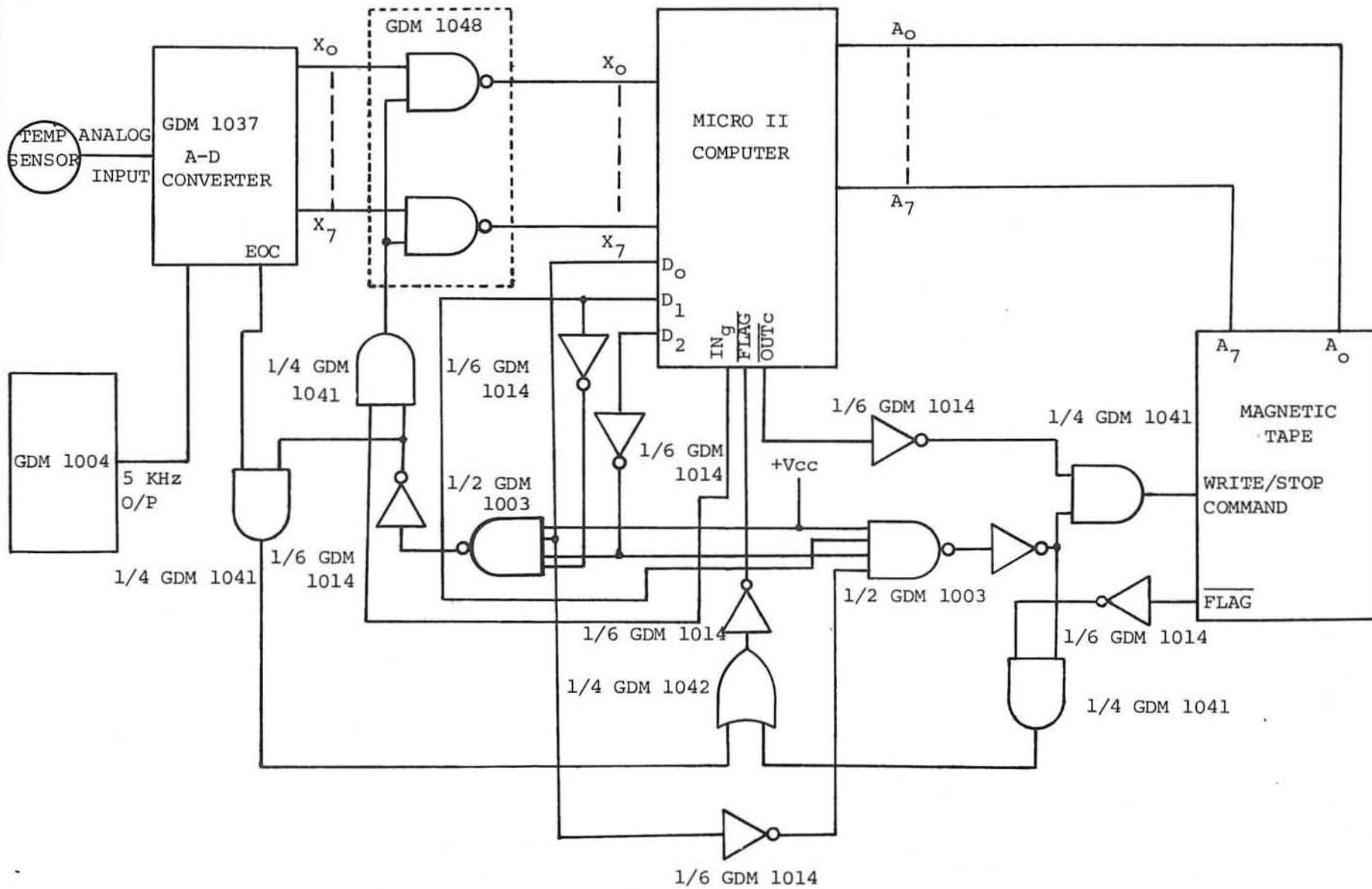
The Interface for the temperature sensor will be defined as device 001. Similarly, the interface for the magnetic tape will be defined as device 010. Referring to Figure 1, we have arranged it such that information from the A-D converter will be transferred to the X Bus lines if and only if device 001 is addressed concurrent with an input (IN_g) instruction. The magnetic tape on the other hand will accept information from the accumulator output lines only when device 010 and an OUT_c signal is present. In both cases, we have written our program such that information is not transferred unless the particular device FLAG bit is set. As may be seen, we have used the EOC from the A-D converter with FLAG of the Magnetic Tape unit to generate the FLAG for the MICRO II.



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POINTS TO NOTE:

1. Open collector gates are required to transfer data from a device to the MICRO II.
2. In order for the input data to be compatible with the MICRO II, it must be inverted.
3. Since EOC for the A-D converter is HI when conversion is complete, it must be inverted if it is to be used as FLAG.
4. The accumulator outputs are in their TRUE buffered form and need no conditioning if they are tagged into TTL compatible logic.
5. The Device Address lines are also in their TRUE buffered form.



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Sample Programs

Example 1 -

A simple program to add two numbers follows. Suppose the decimal numbers, 35 and 120 are to be added together and the result stored in memory.

<u>Address</u>	<u>Contents</u>	<u>Mnemonic</u>	<u>Description</u>
00000000	11000000	CLR	Clear the AC
00000001	10010000	ADD	Add the contents of address 16 to the AC
00000010	10010001	ADD	Add the contents of address 17 to the AC
00000011	01010010	STR	Store the AC in address 18
00000100	11011000	HLT	Halt, stop execution
00010000	00100011		The number 35
00010001	01111000		The number 120

If the preceding program were executed by the MICRO II COMPUTER, the displays would have the following contents:

- 1) AC 10011011 the answer (155)
- 2) PC 00000101
- 3) I.R. 11011000

if address 00010010 were displayed, the IR would display
10011011 (the answer 155).



If the program were single stepped, beginning at address 00000000,
the displays would have the following contents.

<u>NUMBER OF DEPRESSIONS OF STEP SWITCH</u>	<u>DISPLAYS</u>
1	AC 00000000 PC 00000001 IR 11000000
2	AC 00100011 PC 00000010 IR 10010000
3	AC 10011011 PC 00000011 IR 10010001
4	AC 10011011 PC 00000100 IR 01010010
5	AC 10011011 PC 00000101 IR 11011000



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Example 2 -

Use this as an example for indirect addressing.

The preceding program used direct memory reference instructions,
the following program uses indirect memory reference instructions.

The two numbers 35 and 120 are to be added. The indirect address
for number 35 is address 128. The indirect address for number 120
is address 129.

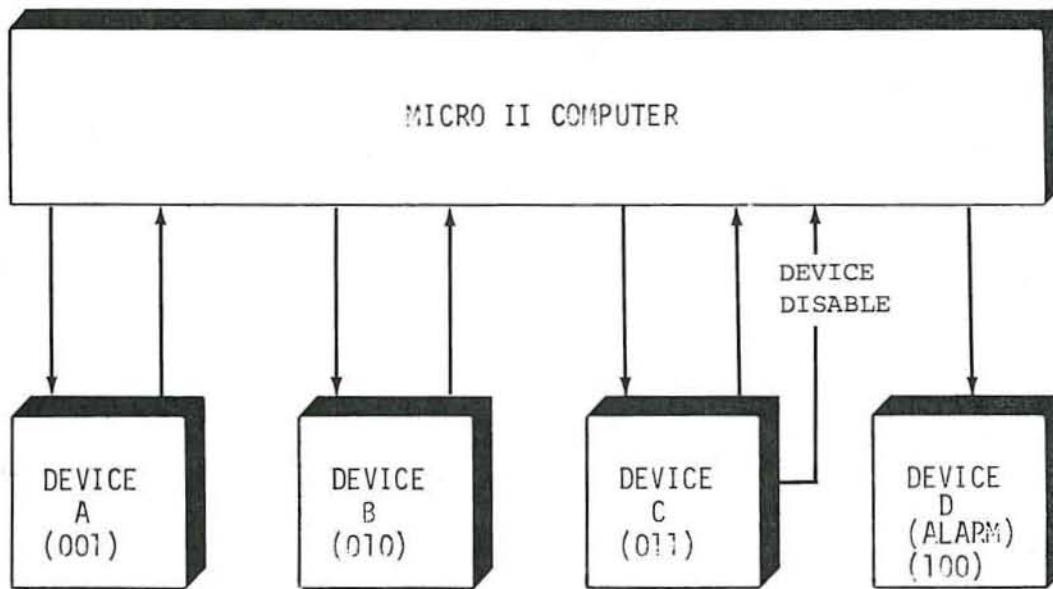
The program is as follows:

<u>Address</u>	<u>Contents</u>	<u>Mnemonic</u>	<u>Description</u>
00000000	11000000	CLR	Clear AC
00000001	10110000	ADD	Add the contents of indirect address 16
00000010	10110001	ADD	Add the contents of indirect address 17
00000011	01010010	STR	Store AC in direct address 18
00000100	11011000	HLT	Halt
00010000	10000000		Address 128
00010001	10000001		Address 129
10000000	00100011		The number 35
10000001	01111000		The number 120



Example of a Process Control Application

In a hypothetical industrial process three machines (or devices) are to be constantly monitored by a computer. Each device has a sensor that outputs the present state of the device with an eight bit data word. The sensor outputs the data word to the computer upon command from the computer. The sensor is also able to accept a data word from the computer which it uses to correct the state of the device if the computer has detected an error. Devices A and B are fast processes and require constant monitoring while device C is a very slow process but the most important. The computer only services device C when device C's sensor outputs a flag bit to the computer requesting servicing. This flag bit causes the computer to output data to disable devices A and B and service device C. When device C no longer outputs a flag bit the computer then services devices A and B and will not service device C until another flag bit is initiated.

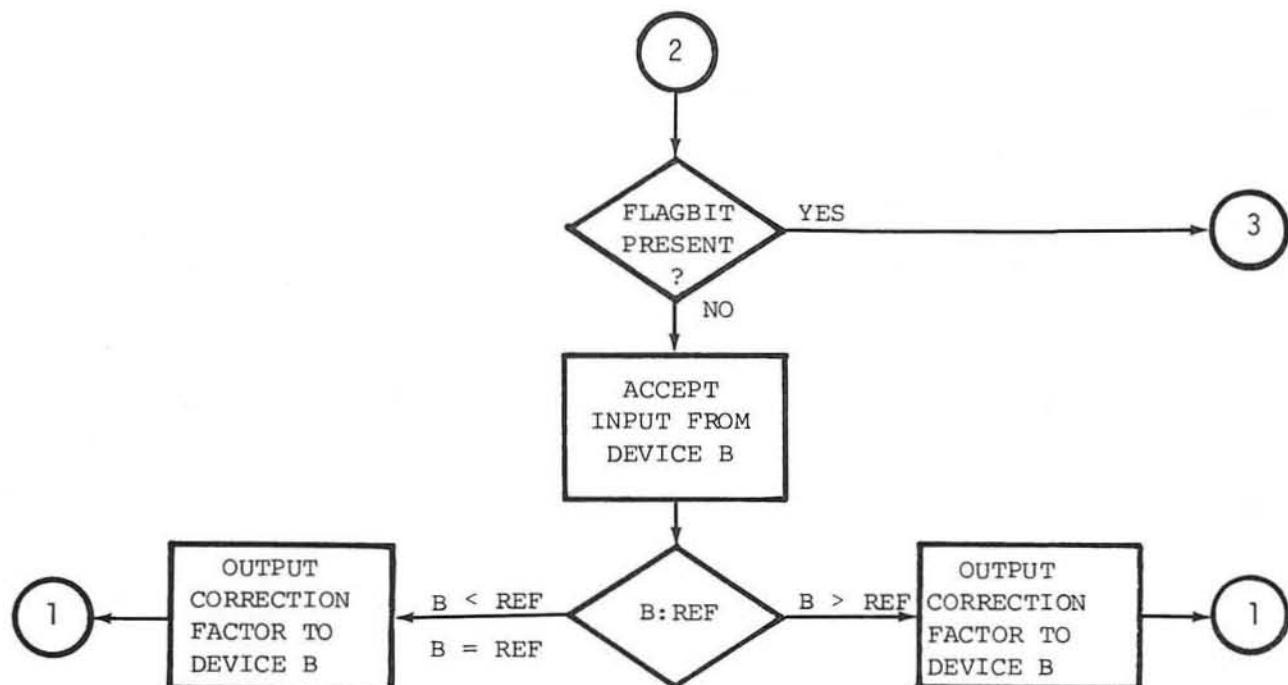
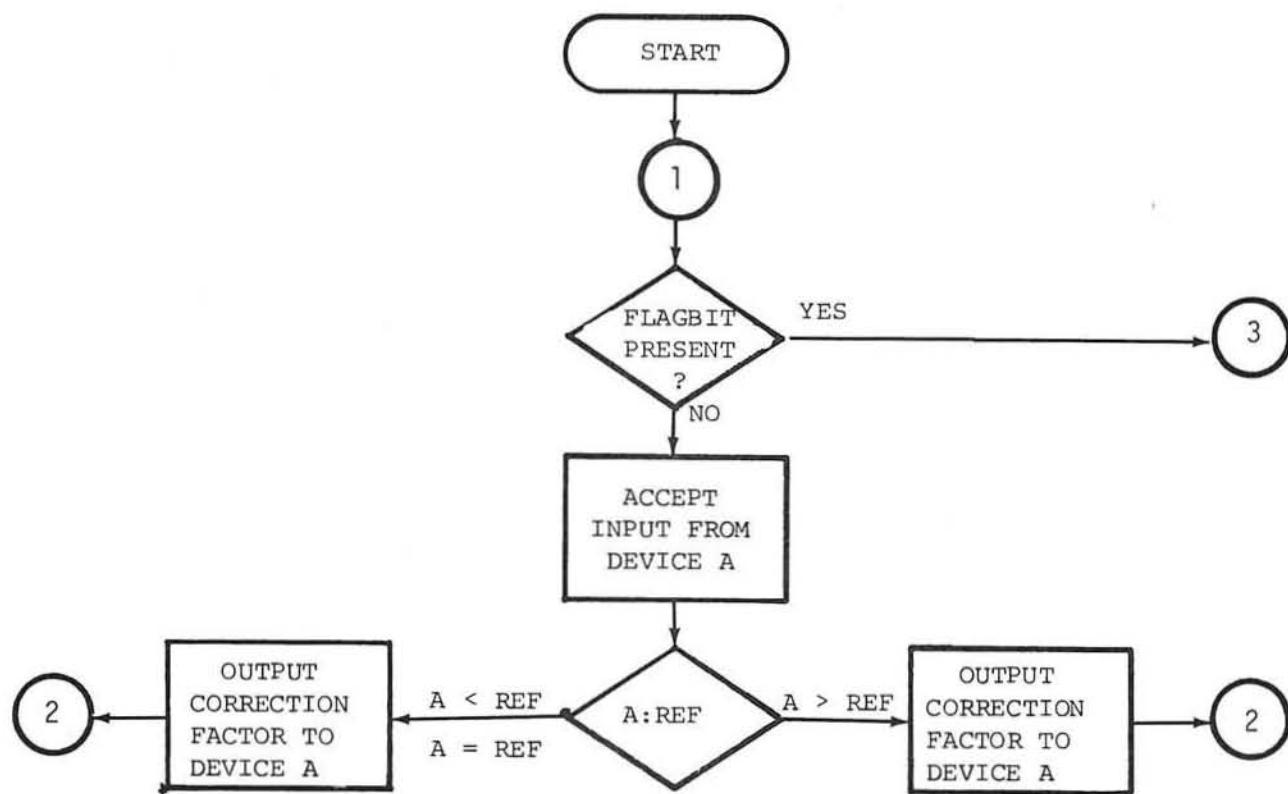


In servicing a device, the computer accepts a data word, compares the data with an internal reference for the device, computes whether the data is greater than the reference, or less than or equal to the reference and then outputs the appropriate correction factor to align the device with the reference. When servicing device C, in addition to the above, if the data word from the device is greater than the reference, an alarm is enabled (device D).

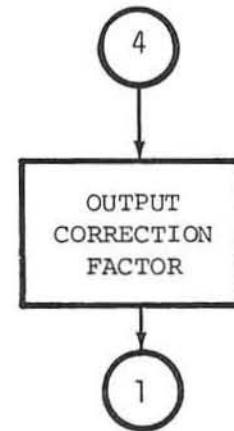
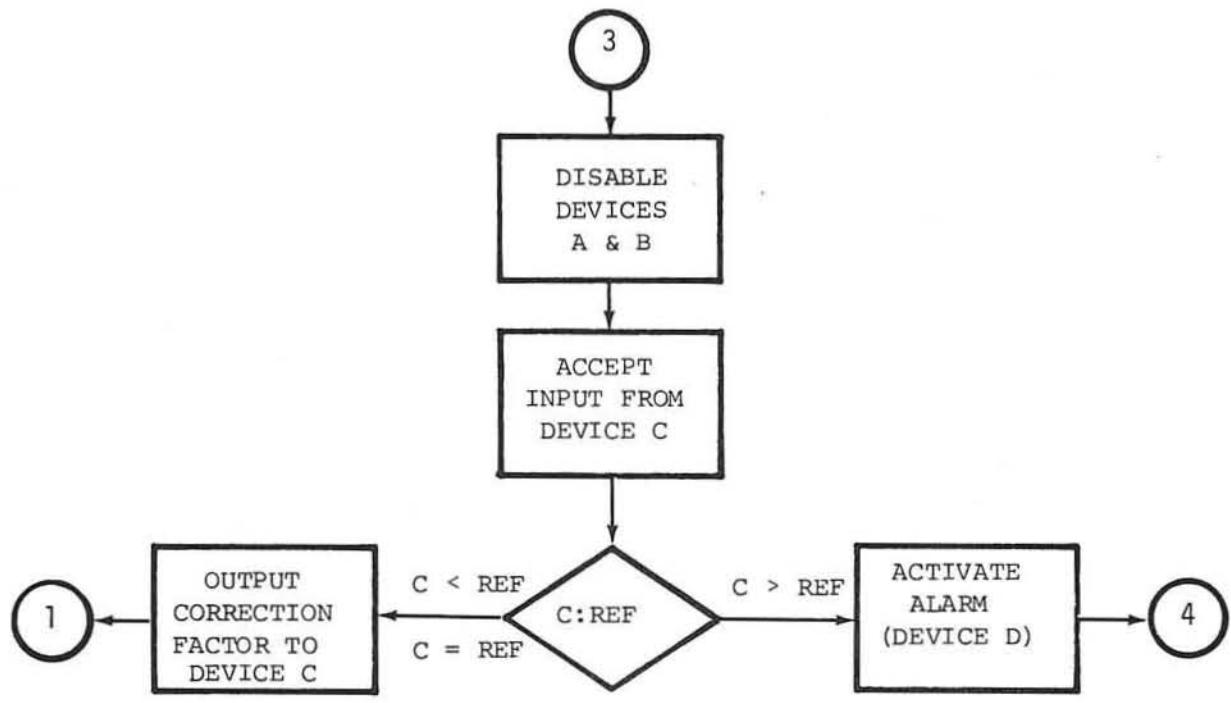


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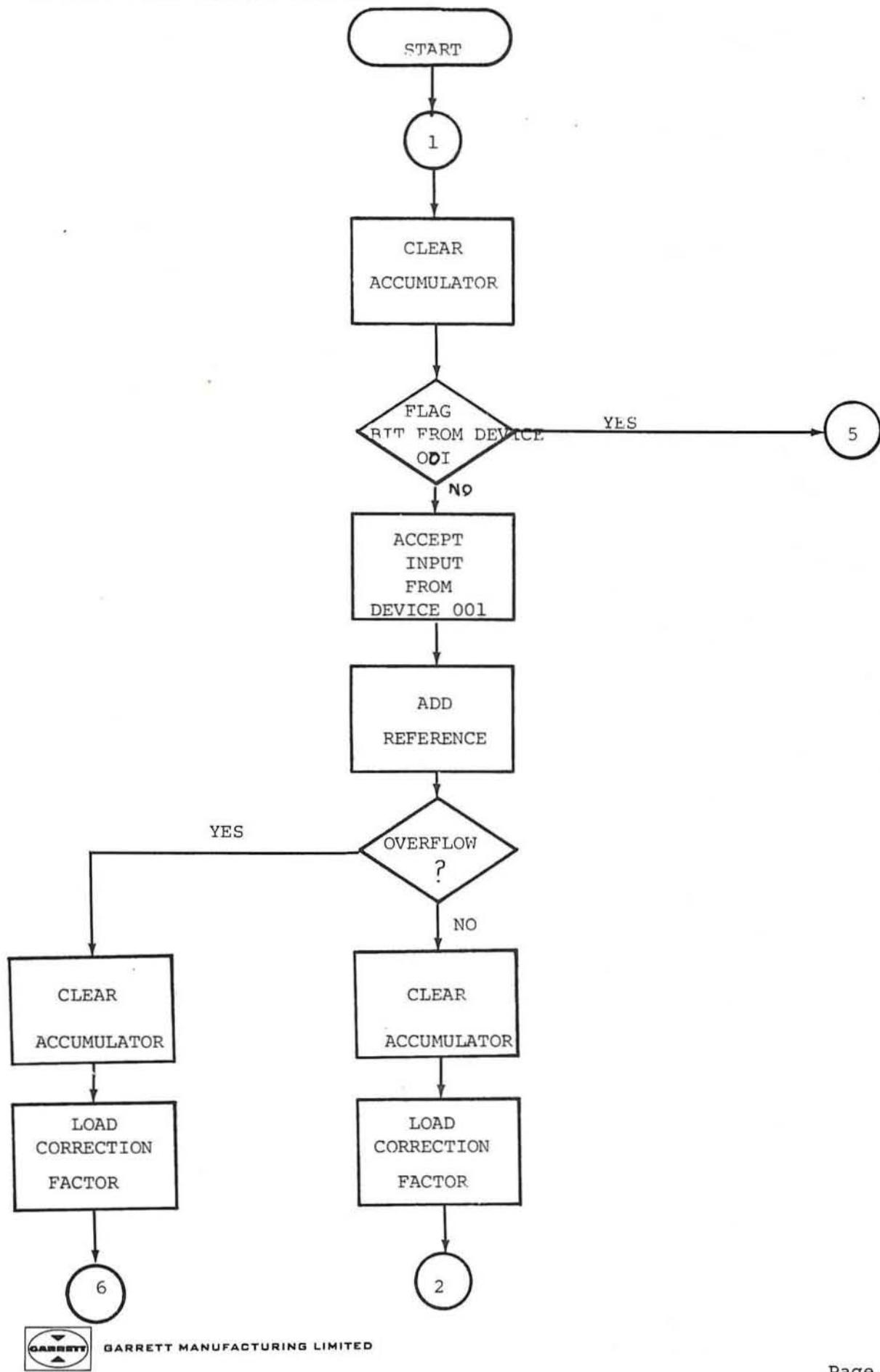
A flow chart illustrating a possible computer program follows:



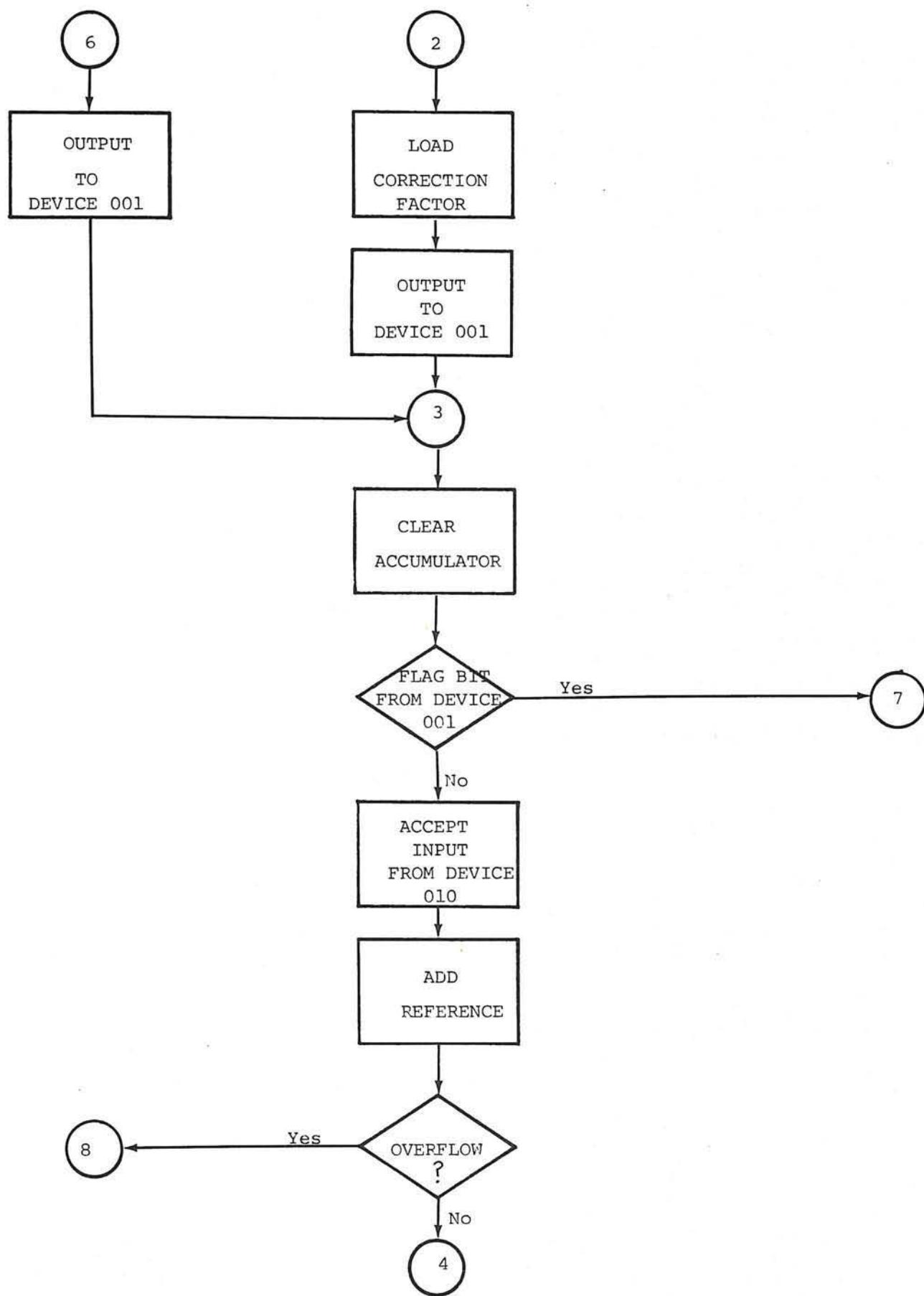
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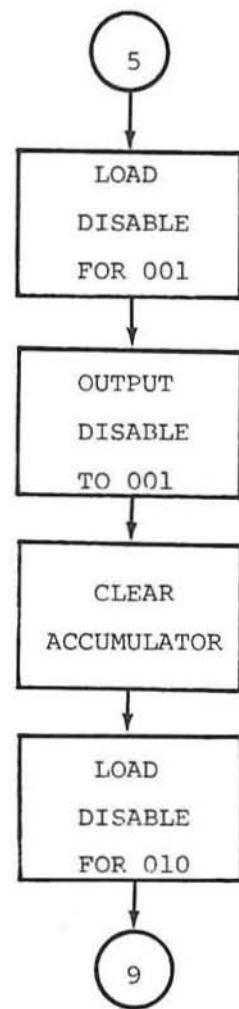
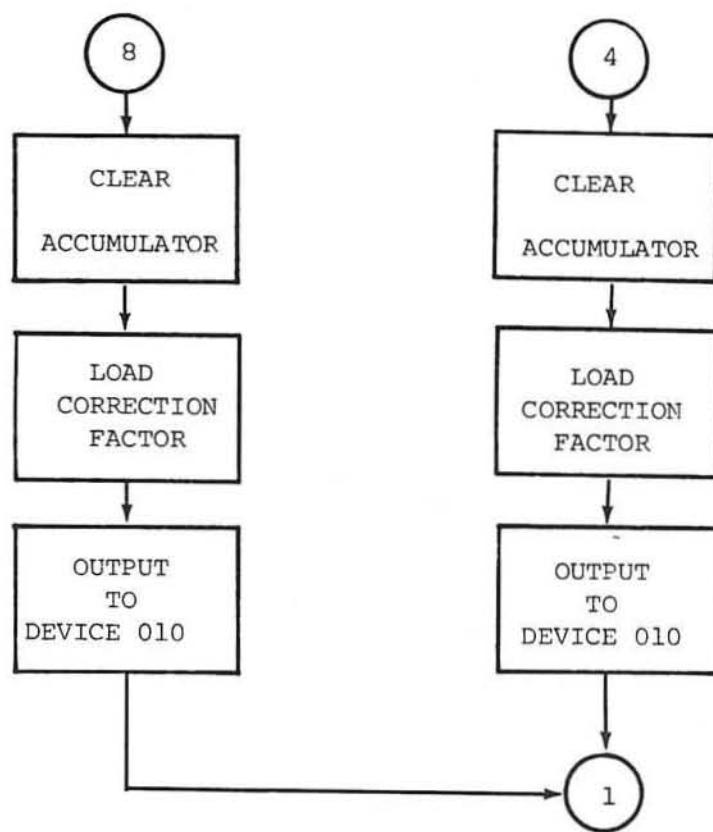
A flow chart illustrating the flow of data between the computer and the devices under control follows.

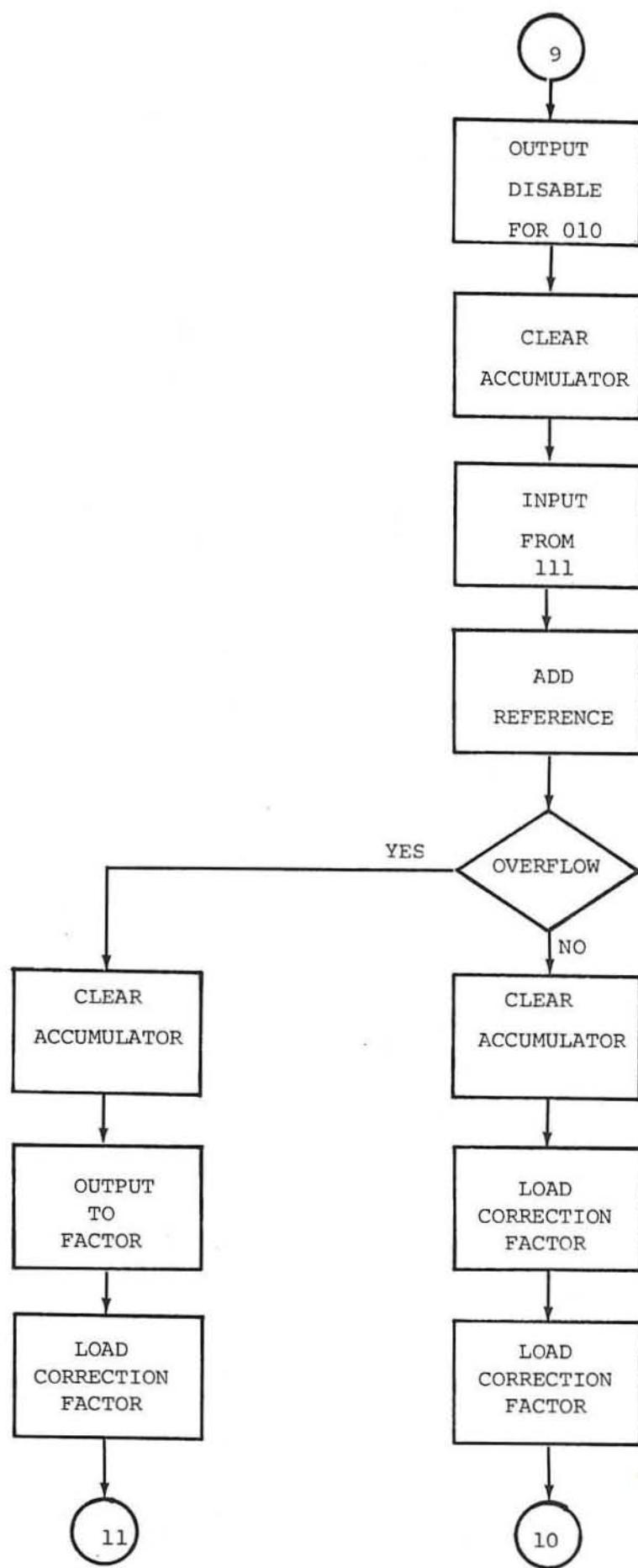


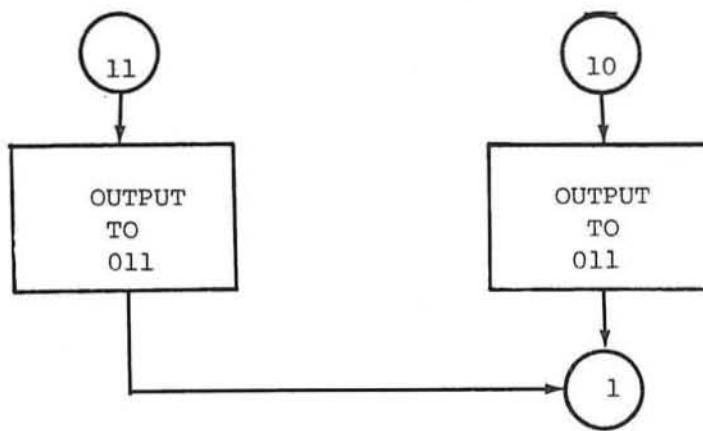
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A possible program to implement the previous two flow charts follows below:

<u>ADDRESS</u>	<u>CONTENTS</u>	<u>MNEMONIC</u>	<u>COMMENT</u>
00000000	11000000	CLR	Clear AC
00000001	11101011	SFG	Checking for Flag bit
00000010	00000100	JMP	Jump to 4, no flag bit
00000011	00111111	JMP	Indirect jump to 31, if flag bit present
00000100	11110001	INP	Input data from 001
00000101	10011110	ADD	Add reference
00000110	11011100	SNO	Skip next instruction if input data is <u><</u> reference
00000111	00001001	JMP	Jump if input is greater than reference
00001000	00001101	JMP	Jump if input data is less or equal to reference
00001001	11000000	CLR	Clear AC
00001010	10011101	ADD	Add correction factor
00001011	11111001	OUT	Output data to 001
00001100	00010000	JMP	Jump to 16
00001101	11000000	CLR	Clear AC
00001110	10011100	ADD	Load correction factor
00001111	11111001	OUT	Output Data to 001
00010000	11101011	SFG	Check for flag bit from 011
00010001	00010011	JMP	Jump to 14 if no flag
00010010	00000011	JMP	Jump to 3 if flag set
00010011	11000000	CLR	Clear AC
00010100	11110010	INP	Input data from 010
00010101	10011011	ADD	Add reference



NOTES:-

- (1) When comparing input data with a reference, the reference (in its complemented form) is added to the input data. If the input is greater than the reference, an accumulator overflow condition will exist.
- (2) A device disable is assumed to have the following data word:
00000000.
- (3) The alarm, device 100, is assumed to be activated whenever its device code appears on the device address bus.
- (4) Computer generated INg and OUTc must be used to gate data into and out of the computer.
- (5) All input data must be gated into the computer in its complemented form.



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POWER SUPPLIES

The Micro II requires a single ended power supply with an output of 5 ± 0.25 volts. The required current is defined by:

$$I = 1.5 + 0.9 n$$

where I is the required current in amperes, and n is the number of memory cards installed in the computer.

When operated from the MDL-1000 power supply, the memory must be limited to 1 card (i.e. 256 words).

The power supply which is supplied with models MICRO II RP and MICRO II DP has the required current output to supply up to 8 memory cards.

If another power supply is used, it may be connected to the 4 pin plug on the rear panel of the computer. The required cable connector is a Cinch-Jones P/N S-304-FHE. Pin connections are shown in Figure 2. Note that two pins are paralleled for each power lead.

Important

The MICRO II is protected from power supply overvoltage and reversed polarity but this protection can be effective only if the power supply is provided with some form of current limiting. If a fuse is used, it should be a buss type AGX (fast acting) of the appropriate current rating.

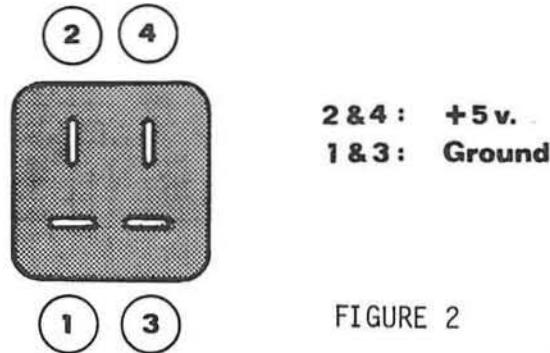


FIGURE 2



PIN CONNECTIONS FOR PERIPHERALS

Peripherals to be connected with the MICRO II computer are interfaced via a connector mounted on the side of the MICRO II P and the rear of the MICRO II R, RP, D, DP.

<u>PIN NUMBER</u>	<u>FUNCTION</u>	<u>PIN NUMBER</u>	<u>FUNCTION</u>
1	*	21	*
2	*	22	*
3	*	23	AC6
4	AC7	24	AC4
5	AC5	25	AC2
6	AC3	26	AC0
7	AC1	27	Y6
8	Y7	28	Y4
9	Y5	29	Y1
10	Y0	30	Y3
11	Y2	31	X1
12	X0	32	X3
13	X2	33	X5
14	X4	34	X7
15	X6	35	D1
16	D0	36	FLAG
17	D2	37	OUTC
18	ING		
19	SPARE		
20	*		



The connector mounted on the MICRO II is a Cannon type CE 9456-6.
The mating connector is a Cannon Type DC-37S.

*These pin connections are internally wired to the computer and reserved for use with peripherals and as such no attempt should be made to use them.

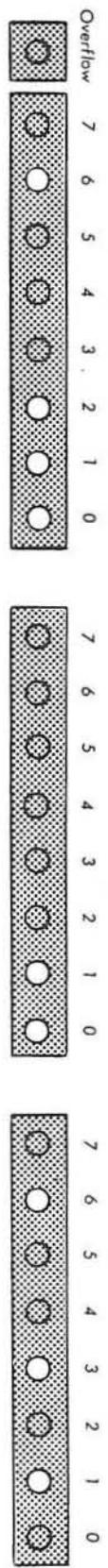
Note that the AC lines are the outputs.





MICRO COMPUTER

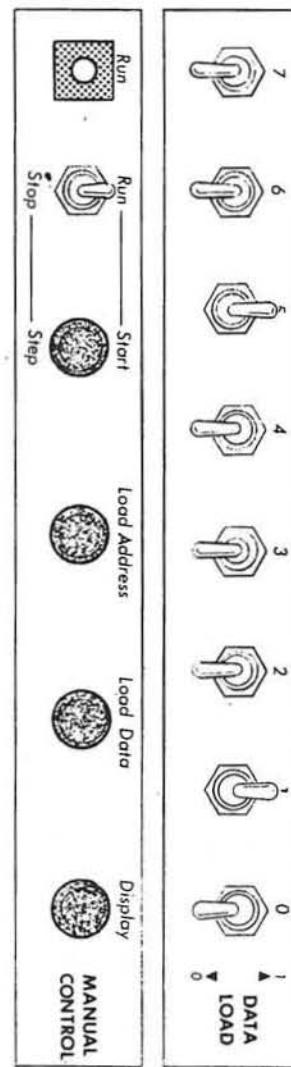
POWER



ACCUMULATOR

PROGRAM COUNTER

INSTRUCTION REGISTER



OUT	IN	FLAG	2	1	0	DEVICE ADDRESS
0	0	0	0	0	0	X INPUTS
1	0	0	0	0	0	Y INPUTS
0	1	0	0	0	0	Z INPUTS
0	0	1	0	0	0	0
0	0	0	0	0	0	OUTPUTS
0	0	0	0	0	0	0
0	0	0	0	0	0	0

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