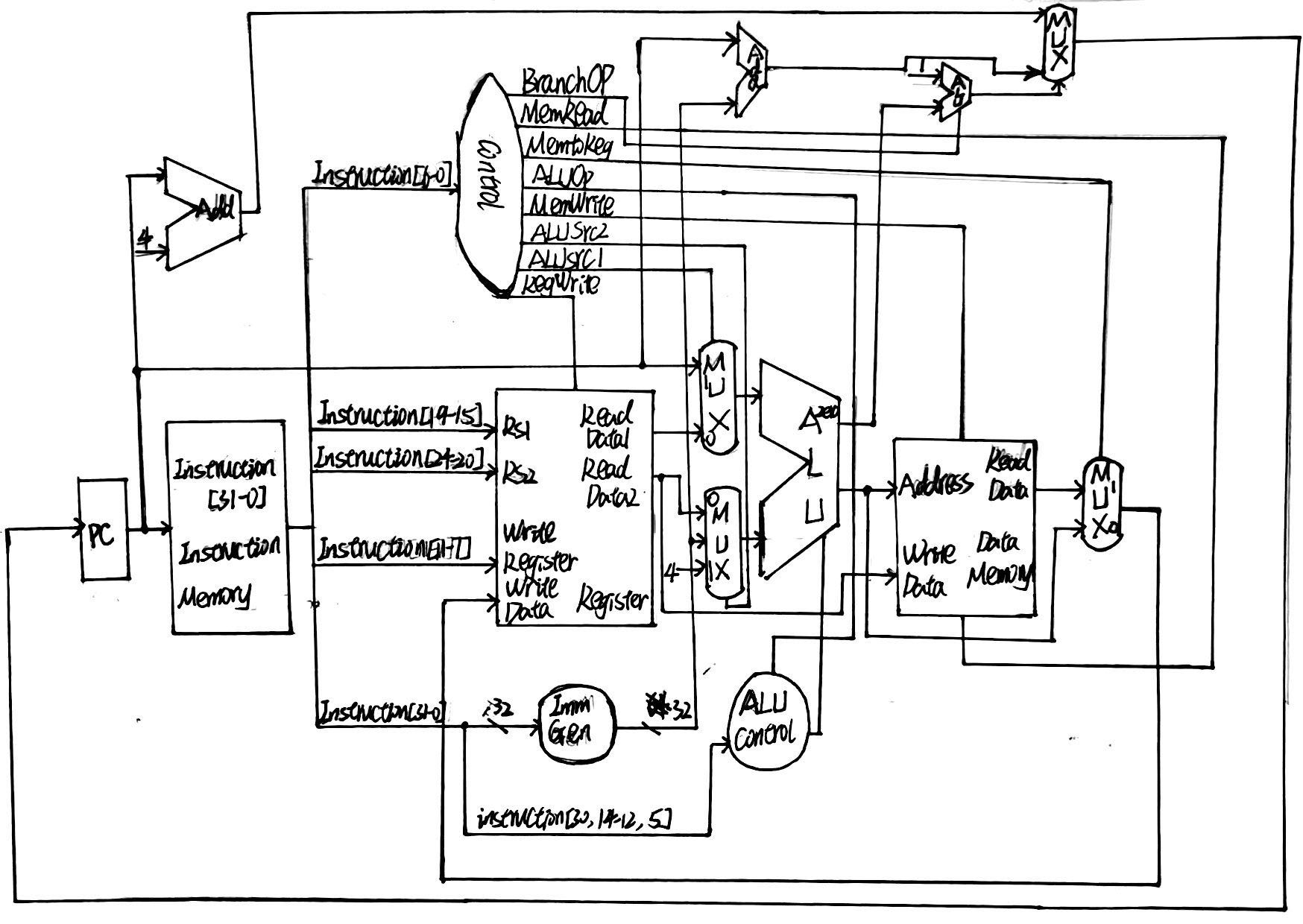
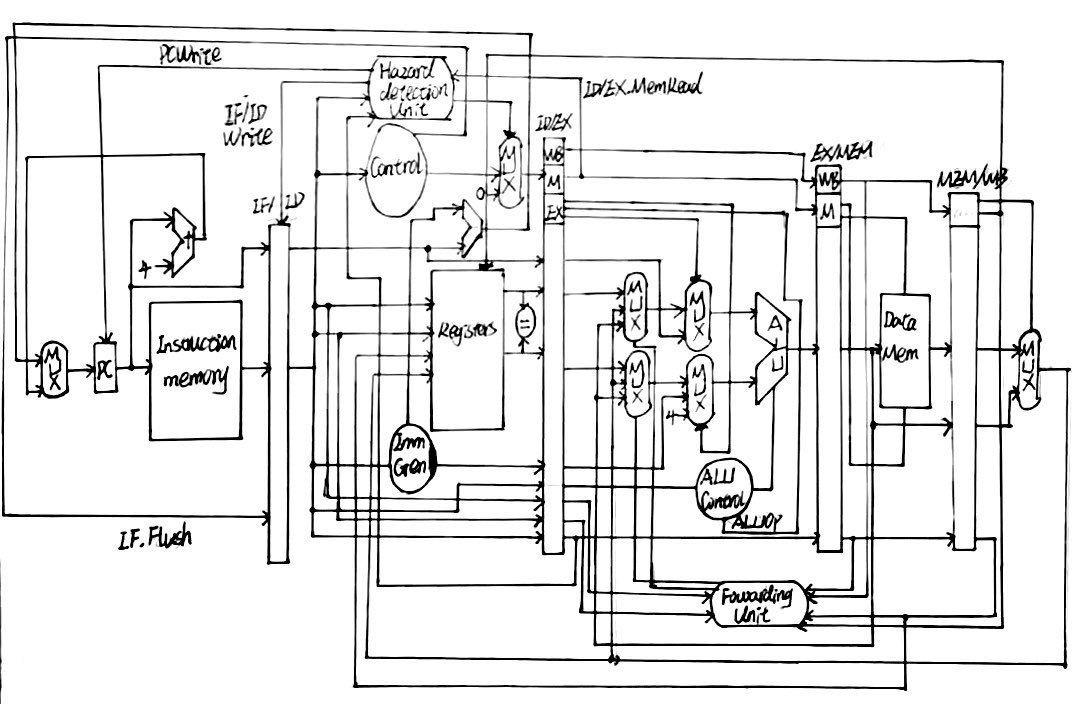
1. Draw the schematic for a single stage processor and fill in your code in the to run the simulator. (20 points)



In combinational logic ImmGen, the specified bits are combined according to the type of instruction and signed expanded to form an immediate number. For branch instructions, the immediate number is shifted left by one bit, so the left-shift combinational logic is omitted.

2) Draw the schematic for a five stage pipelined processor and fill in your code to run the simulator. The processor should be able to take care of RAW and control hazards by stalling and forwarding. (20 points)



In combinational logic ImmGen, the specified bits are combined according to the type of instruction and signed expanded to form an immediate number. For branch instructions, the immediate number is shifted left by one bit, so the left-shift combinational logic is omitted.

1. Measure and report average CPI, Total execution cycles, and Instructions per cycle for both these cores by adding performance monitors to your code. (Submit code and print results to console or a file.) (5 points)

4) Compare the results from both the single stage and the five stage pipelined processor implementations and explain why one is better than the other. (5 points)

Pipelined processors can execute more quickly when there are more instructions to be executed because they can take advantage of almost every part of the data path and execute more compactly, whereas non-pipelined processors always have more or less part of the logic idle each cycle.

5) What optimizations or features can be added to improve performance? (Extra credit 1 point)

If there are two instructions lw followed by sw and rd in lw is equal to rs1 or rs2 in sw, then sw needs to stall for one cycle to wait for lw to read the data. Bypass logic can be added to the MEM stage to bypass the data removed from the WB stage to the MEM stage. When sw needs the data read by the previous instruction in the MEM phase, it can get it directly from the bypass logic, avoiding a stall.