BOM_NOTE:
Replace INA250A3 with INA250A1
and OPA2188 with OPA2192.
These parts were chosen so that I don't have to create
symbols for the specific parts required since these
replacements are logically and physical similar.

U1
TPL0102-100PWR
I2C_SCL
I2C_SDA
VSTEER_A0
VSTEER_A1
SCL
SDA
A0
A1
A2
HA
WA
LA
HB
WB
LB
VSS
GND
VDD
VREF_V_STEER
VSTEER_WA
VSTEER_WB
VSTEER_WA_BUF
U3.1
U3.2
OPA2188AIDR
P5V0
GND
R16 1k
R18 1k
R17 1k
R19 1k
C8 0.1u
C7 0.1u
DEFAULT ADDR: 0x50
DNI: R16, R18

U10.1
U10.2
DCDC_VREF_TRIM
P4
Header-Male-2.54_1x3
C11 0.1u
ILIM_CTRL_R
D1
BAS16-7-F
D2
1N4148TA
ILIM_CTRL
ILIM_CTRL_D
R8 100
CAD_NOTE:
Make Overlapping Footprint
for D1 and D2, only one of
them will be mounted.

DESIGN NOTE:
If the MCU controlling this devices either doesn't have pullup on its I2C bus or
if it doesn't support 5V on its I2C pins then un-mount R9 and R10 (also R22 if using INA_ALERT_N).
For devices running with 5V should be able to work fine with I2C bus upto 400Khz

U6
TPL0102-100PWR
ILIM_CTRL_A0
ILIM_CTRL_A1
VREF_I_LIMIT
ILIM_CTRL_WA
ILIM_CTRL_WB
ILIM_CTRL_WA_BUF
U9.1
U9.2
ILIM_STEER
R9 1k
R10 1k
R12 1k
R14 1k
R13 1k
R15 1k
C9 0.1u
C10 0.1u
DEFAULT ADDR: 0x51
DNI: R13, R14

CURRENT_SENSE_VOUT
CURRENT_SENSE_VOUT_R
R23 10
R24 1k
C12 100nF
DESIGN NOTE:
U10 may not be required in here.
We could have directly driven the
ILIM and VTRIM from U9 and U3,
respectively.

DESIGN NOTE:
C12 and R24 are place holders to either scale
or add a low pass filter to I to V converter if necessary

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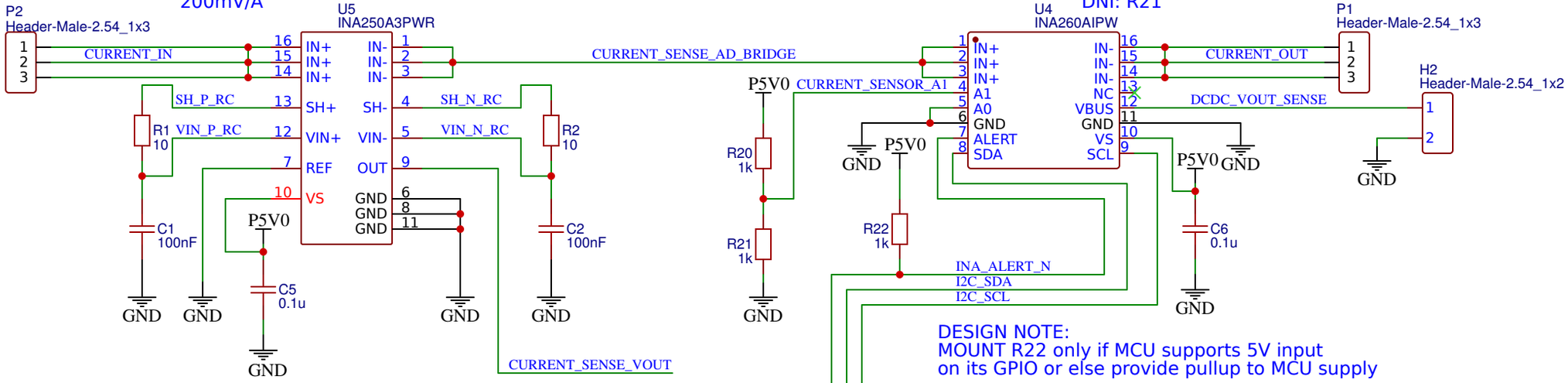
DESIGN NOTE:
For P1 and P2 we can not only use standard 2.54mm hdr
but also 2.54mm screw terminal jack. Each pin can carry
upto 6.25A so 3 pins should be good for 10A even after derating

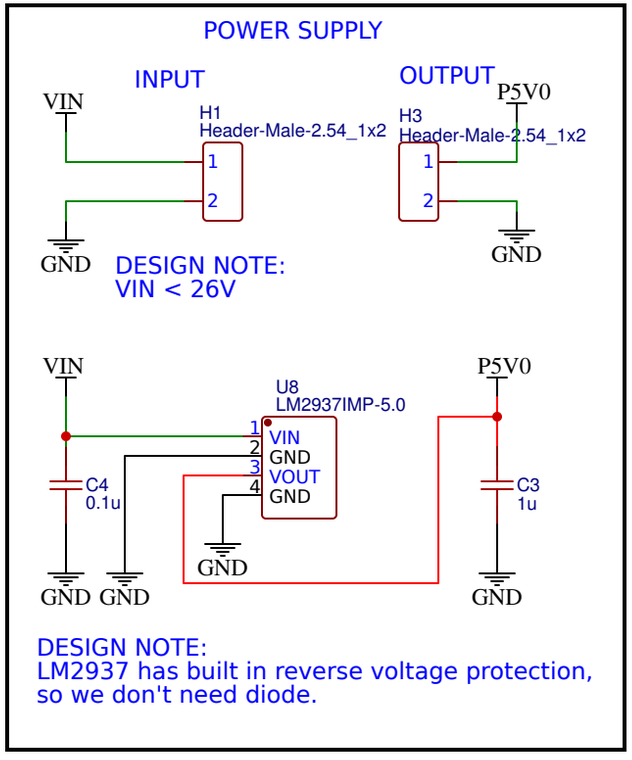
I to V converter INA250A1
200mV/A

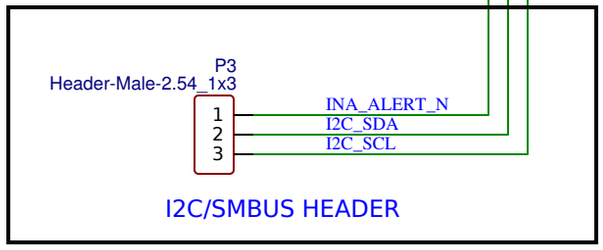
DEFAULT ADDR: 0x44
DNI: R21



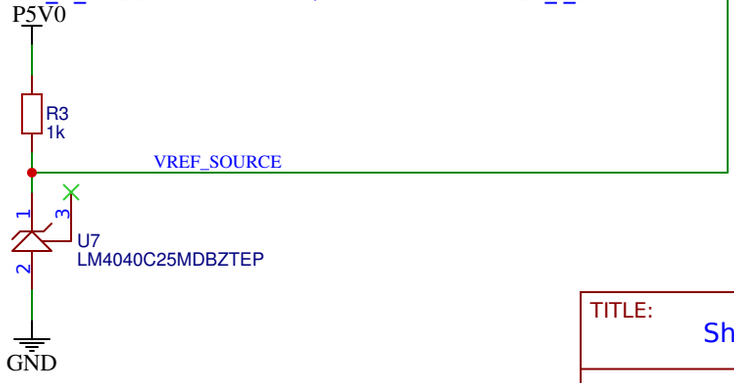
Design Note:
LPF designed for 160KHz 3db point, we can instead not mount
the caps and instead mount a TVS diode to protect the chip
from more than 36V transients that can occur due to inductive loads.

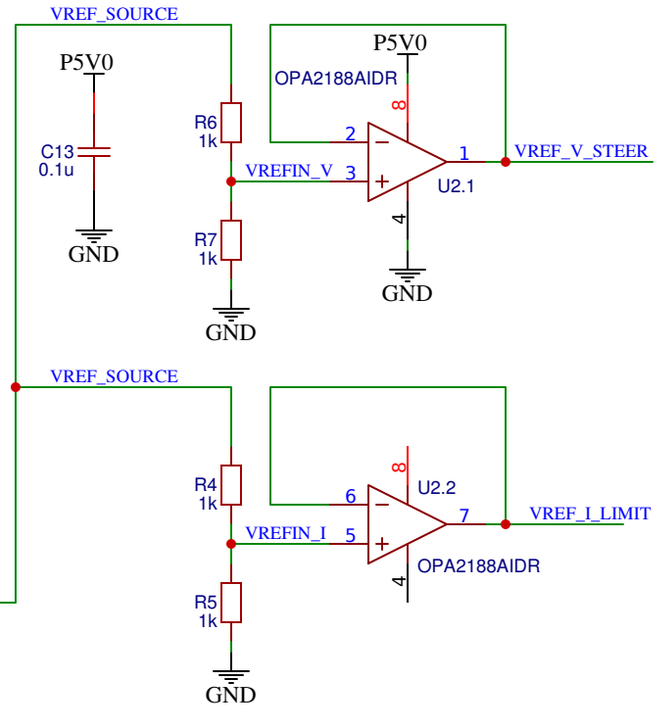
DESIGN NOTE:
MOUNT R22 only if MCU supports 5V input
on its GPIO or else provide pullup to MCU supply





DESIGN NOTE:
Tune R6/R7 values to achieve required reference
for VREF_V_STEER and Tune R4/R5 values for VREF_I_LIMIT





TITLE: Sheet_2		REV: 1.0
EasyEDA	Company: Your Company	Sheet: 1/1
	Date: 2019-05-24 Drawn By: neutronstriker	