CSCI160 COMPUTER ARCHITECTURE I HUNTER COLLEGE CITY UNIVERSITY OF NEW YORK

Spring 2022 Monday and Wednesday 5:35 PM to 6:50 PM IN PERSON in the Hunter West 3rd Floor Student Dining Room. However, in order to prepare for potential contigencies, several lectures throughout the semester will take place on BlackBoard Collaborate TBA SYLLABUS

GRADESCOPE [entry code 4PBYXW]

INSTRUCTOR

Genady Maryash gmaryash@hunter.cuny.edu office hours Monday and Thursday 4:15 PM to 5:15 PM to on BlackBoard Collaborate.

TUTORS

Steven calendly.com/steven-palomino/csci160-office-hours

Shafali calendly.com/shafali-gupta21/csci-160-office-hours-shafali

Daniel calendly.com/daniel-elkik26/160-office-hours

Andy calendly.com/andy-mina30/office-hours/

TEXTBOOK

Digital Design, 6th Edition eText, Mano, Ciletti ISBN-9780134529561. It can be purchased at a discounted price (\$54.99) direct from the publisher through **Vitalsource.com** in order for the chapter links to work. Do not buy any other electronic version of this edition of the book. Of course, you may be able to find prior editions of this book for less – you will simply have to match the reading assignments to those older edditions.

OTHER RESOURCES

Circuit Builder Simulator

COURSE OUTLINE

DATE	TOPIC	READINGS	SLIDES
1/31	Introduction	Syllabus	
2/2	Binary Numbers	1.2 Binary Numbers	Class 1
2/7	Radix Conversions	1.3 Number Base Conversions1.4 Octal and Hexadecimal	Class 2

DATE	TOPIC	READINGS	SLIDES
		Numbers	
2/9	HW Review &	TEST 1	
2/14	Complements of Numbers	1.5 Complements of Numbers1.6 Signed Binary Numbers	Class 3
2/16	Binary Codes	1.7 Binary Codes1.9 Binary Logic	Class 4
2/23	Boolean Algebra	2.2 Basic Definitions	Class 5
2/28	Axioms	2.3 Axiomatic Definition	Class 6
3/2	Functions and Proofs	2.4 Theorems and Properties2.5 Boolean Functions	Class 7
3/7	More Boolean Algebra	2.7 Other Logic Operators Test 2	Class 8
3/9	Logic Gates	2.8 Digital Logic Gates	Class 9
3/14	Midterm Review	Midterm Review	
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3/16	Canonical vs Standard	2.6 Canonical and Standard Forms	Class 10
3/21	Midterm Exam		
3/23	Gate Level Minimisation	<ul><li>3.2 The Map Method</li><li>3.3 Four-Variable K-Map</li><li>TB K-Map Method</li></ul>	Class 11 K-Map Torus
ONLINE 3/28	<b>BB COLLABORATE</b> 5-Var K-map	4.3 Analysis of Combinational Circuits	TB KMaps Class 12
3/30	7-Segment Display	3.5 Don't-Care Conditions	Class 13

DATE	TOPIC	READINGS	SLIDES
4/4	Tabulation Method	Quine-McCluskey Tabular Method	Class 14
4/6	Prime Implicant Table	Prime Implicant Table  Test 3	Class 15
4/11	More P.I.T., Adders	4.4 Design Procedure	Class 16
4/13	Subtractors	4.5 Binary Adders and Subtractors	Class 17
	SPRING	BREAK	
4/25	Comparator & Controlled Input	4.11 Multiplexers	Class 18 FlipFlops
4/27	<b>Test 4</b> Flip-Flops, Clock	5.4 Storage Elements: FlipFlops	Class 19
5/2	Racing Fix JK Flip-Flop	Racing Problem Animation  J K FlipFlop Animation	Class 20
5/4	State Diagrams	Four-Variable K-Map Review	Class 21
5/9	State Equasions, Finate State Machines	5.5 Analysis of Clocked Sequential Circuits	Sequetial Circuit & Equations  State Table for Circuit  State_Table_and_Diagram  Equasions_and_FSMs  Input_Equasions  States_D_FlipFlop  In_Mealy_FSM_output_is_function
5/11			
5/16	Exam Review		
5/18	Final Exam	Wednesday	5:20 – 7:20

# **Instructor Evaluations:**

Computer: www.hunter.cuny.edu/te
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Smartphone: www.hunter.cuny.edu/mobilete