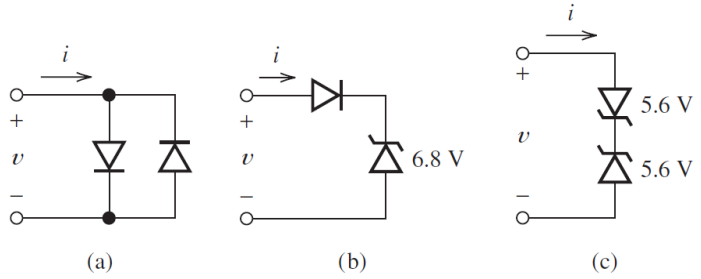
ECE 100, Winter 2022 **Assignment #5**
Electrical and Electronic Circuits Prof. Y. Zhang
University of California, Los Angeles TAs: S. Pei, R. Karmarkar

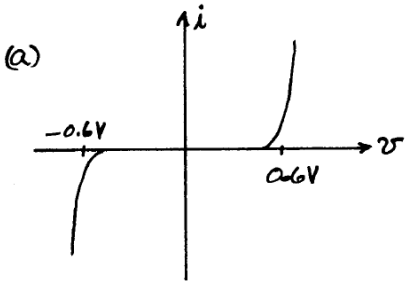
Due **Tuesday, February 22nd 2022, by 6 pm** to Gradescope.
100 points total.

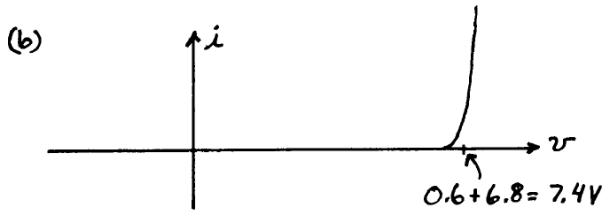
Diode – Lecture 11

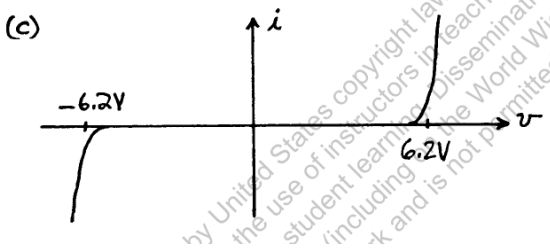
Q1 (10 points)
Sketch i versus v to scale for the circuits show below. The reverse-breakdown voltages of the Zener diodes are shown. Assume voltages of 0.6 V for all diodes including the Zener diodes when current flows in the forward direction.



S1







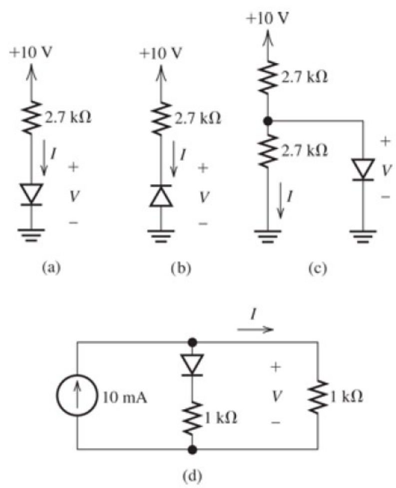
Q2 (10 points)
Two ideal diodes are placed in series, pointing in opposite directions. What is the equivalent circuit for the combination? What is the equivalent circuit if the diodes are in parallel and pointing in opposite directions?

S2

The equivalent circuit for two ideal diodes in series pointing in opposite directions is an open circuit because current cannot flow in the reverse direction for either diode.

The equivalent circuit for two ideal diodes in parallel pointing in opposite directions is a short circuit because one of the diodes is forward conducting for either direction of current flow.

Q3 (10 points)
Find the values of I and V for the circuits of Figure below, assuming that the diodes are ideal.



S3

(a) The diode is on, $V = 0$ and $I = \frac{10}{2700} = 3.70$ mA.

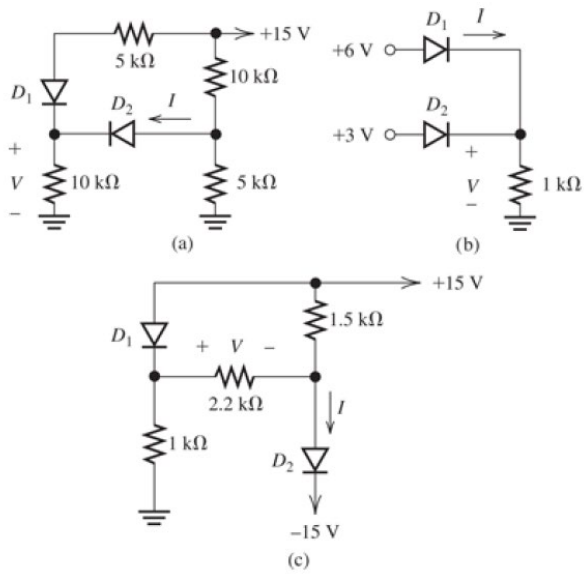
(b) The diode is off, $I = 0$ and $V = 10$ V.

(c) The diode is on, $V = 0$ and $I = 0$.

(d) The diode is on, $I = 5$ mA and $V = 5$ V.

Q4 (10 points)

Find the values of I and V for the circuits of Figure below, assuming that the diodes are ideal.



S4

(a) D_1 is on and D_2 is off. $V = 10$ volts and $I = 0$.

(b) D_1 is on and D_2 is off. $V = 6$ volts and $I = 6$ mA.

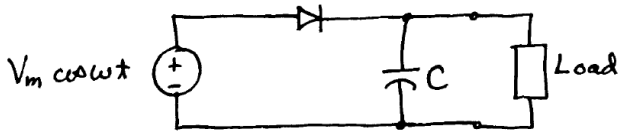
(c) Both D_1 and D_2 are on. $V = 30$ volts and $I = 33.6$ mA.

Q5 (10 points)

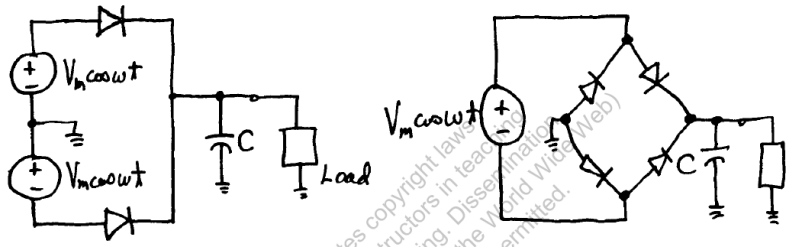
P9.49. Draw the circuit diagram of a half-wave rectifier for producing a nearly steady dc voltage from an ac source. Draw two different full-wave circuits.

S5

Half-wave rectifier with a capacitance to smooth the output voltage:

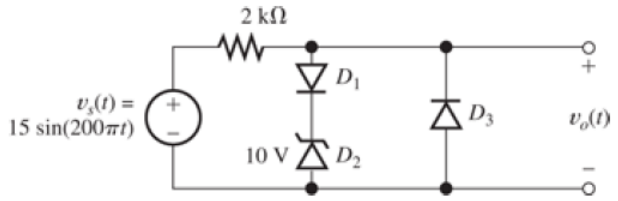


Full-wave circuits:



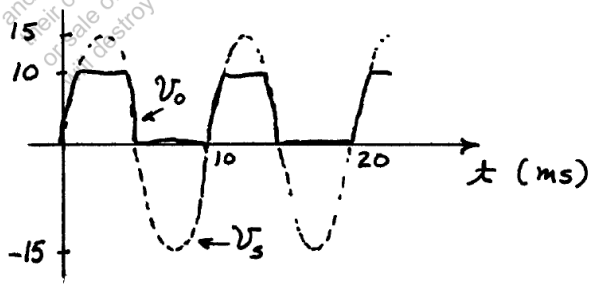
Q6 (10 points)

P9.63. Sketch to scale the output waveform for the circuit shown in **Figure P9.63**. Assume that the diodes are ideal.



S6

Refer to Figure P9.63 in the book. When the source voltage is negative, diode D_3 is on and the output $v_o(t)$ is zero. For source voltages between 0 and 10 V, none of the diodes conducts and $v_o(t) = v_s(t)$. Finally when the source voltage exceeds 10 V, D_1 is on and D_2 is in the breakdown region so the output voltage is 10 V. The waveform is:



Diode – Lecture 12

Q7 (10 points)

We have a junction diode that has i_D=0.2 mA for v_D = 0.6 V. Assume that n=2 and V_T = 0.026 V. Use the Shockley equation to compute the diode current at v_D = 0.65 V and at v_D = 0.70 V.

S7

For $v_D = 0.6$ V, we have

$$i_D = 0.2\times10^{-3} = I_s\left[\exp(v_D/nV_T) - 1\right]$$
$$\cong I_s \exp(v_D/nV_T)$$

Thus, we determine that:

$$I_s \cong \frac{i_D}{\exp(v_D/nV_T)} = \frac{0.2\times10^{-3}}{\exp(0.6/(2\times0.026)} = 1.950\times10^{-9}\text{A}$$

Then, for $v_D = 0.65$ V, we have

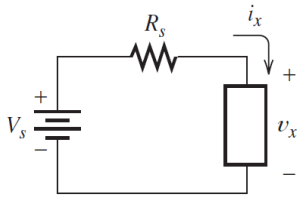
$$i_D = I_s[\exp(0.650/0.052) - 1] = 0.5321\text{ mA}$$

Similarly, for $v_D = 0.700$ V, we find $i_D = 1.369$ mA.

Q8 (10 points)

$i_x = [\exp(v_x) - 1]/10$

v_x and i_x Ω. Use graphical load-line techniques to solve for v_x and i_x.



S8

The load-line equation is

$$V_s = R_s i_x + v_x$$

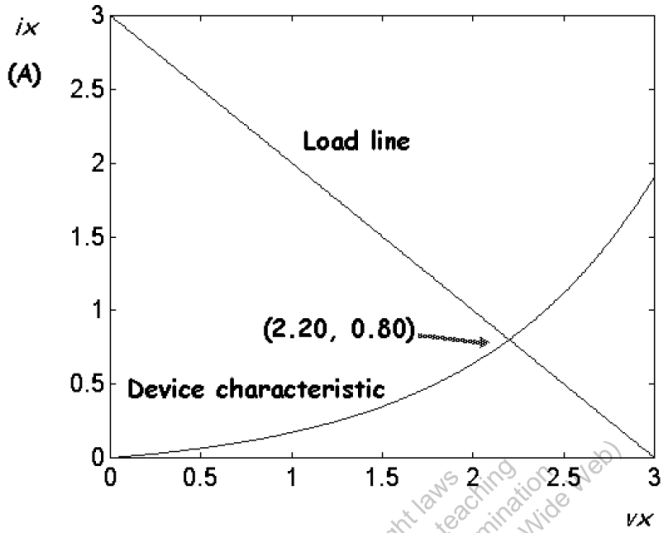
Substituting values, this becomes

$$3 = i_x + v_x$$

Next, we plot the nonlinear device characteristic equation

$$i_x = [\exp(v_x) - 1]/10$$

and the load line on the same set of axes. Finally, the solution is at the intersection of the load line and the characteristic as shown:



Q9 (10 points)

P9.71. Voltage-doubler circuit. Consider the circuit of **Figure P9.71**. The capacitors are very large, so they discharge only a very small amount per cycle. (Thus, no ac voltage appears across the capacitors, and the ac input plus the dc voltage of C1 must appear at point *A*.) Sketch the voltage at point *A* versus time. Find the voltage across the load. Why is this called a voltage doubler? What is the PIV across each diode?

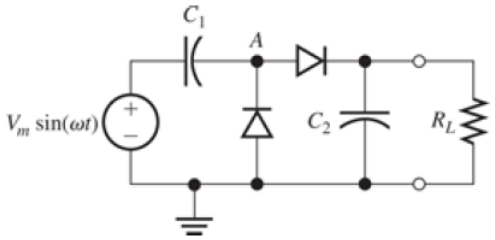
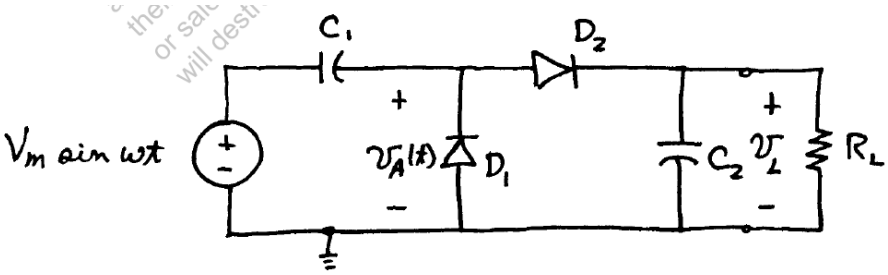
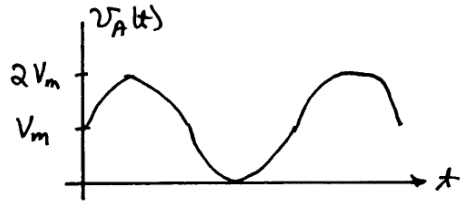


Figure P9.71

S9



The capacitor C_1 and diode D_1 act as a clamp circuit that clamps the negative peak of $v_A(t)$ to zero. Thus, the waveform at point *A* is:



Diode D_2 and capacitor C_2 act as a half-wave peak rectifier. Thus, the voltage across R_L is the peak value of $v_A(t)$. Thus, $v_L(t) \cong 2V_m$. This is called a voltage-doubler circuit because the load voltage is twice the peak value of the ac input. The peak inverse voltage is $2V_m$ for both diodes.

Q10 (10 points)

P9.69. Consider the circuit shown in **Figure P9.69**, in which the *RC* time constant is very long compared with the period of the input and in which the diode is ideal. Sketch vo(t) to scale versus time.

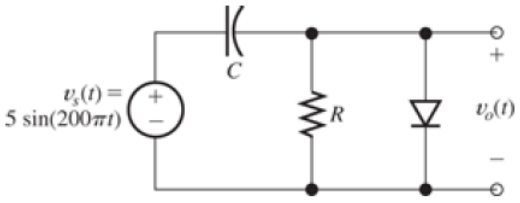
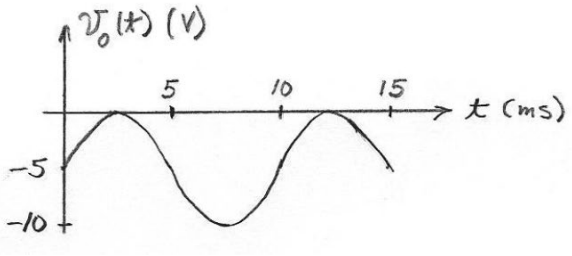


Figure P9.69

S10

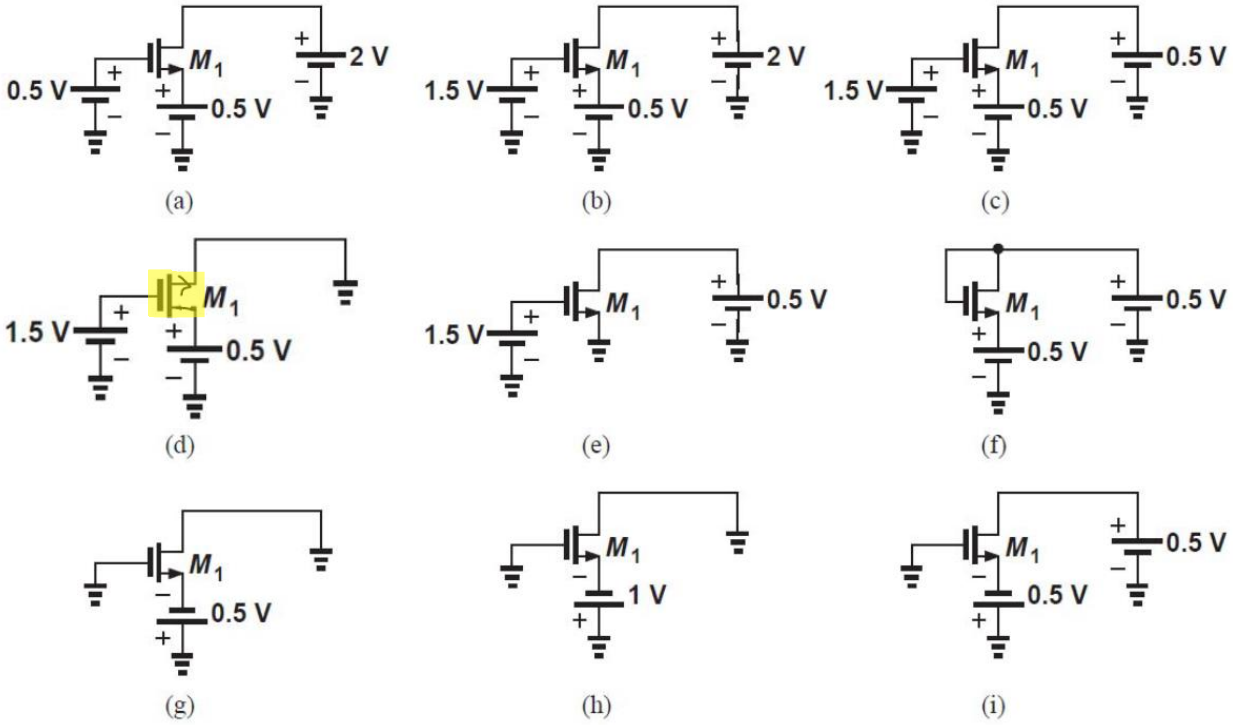
This is a clamp circuit that clamps the positive peaks to zero.



ECE 100, Winter 2022 **Assignment #6**
Electrical and Electronic Circuits Prof. Y. Zhang
University of California, Los Angeles TAs: S. Pei, R. Karmarkar

Due Tuesday, March 8th 2022, by 9 pm to Gradescope.
100 points total.

Q1. (36 marks) **MOSFET as a Resistor**: If the **threshold is equal to 0.7 V**, for each circuit determine whether the device is off or

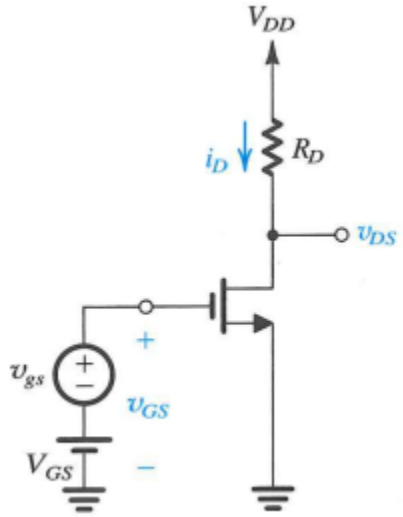


Circuit	Drain voltage (V_D)	Source voltage (V_S)	Gate voltage (V_G)	State of MOSFET (OFF/Res/Sat)
A	2	0.5	0.5	Off
B	2	0.5	1.5	Sat
C	0.5	0.5	1.5	Res
D	0.5	0	1.5	Res
E	0.5	0	1.5	Res
F	0.5	0.5	0.5	Off
G	0	-0.5	0	Off
H	0	-1	0	Sat
I	0.5	-0.5	0	Off

Q2. (10 points)

In the figure alongside: V_{GS} = 5V, V_{DD}= 10V and R_D = 1kΩ, Vth = 0.7V

K=0.24E-3 A/V^2



Draw the small-signal model for the MOSFET and report

a. Transconductance
b. Output resistance
c. Gain
d. Identify the mode operation of the transistor. (CS/CD etc)

(Hint : Refer to Lecture slides)

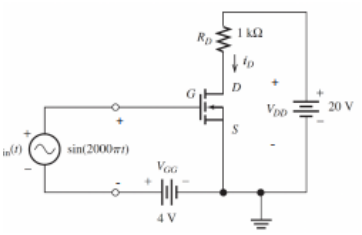
$Id = k\,(Vgs - Vth)^2 = 0.24E-3\;x\;(5-0.7)^2 = 4.4376 - 3\;Amp$

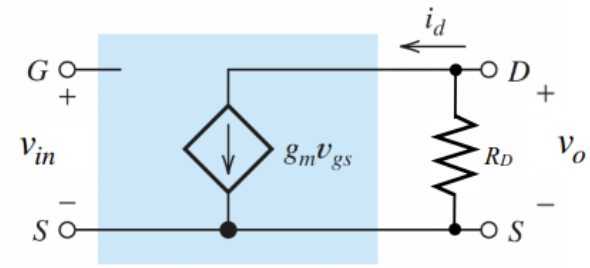
Gm = 2k(Vgs – Vt0) = 2.064E-3 /ohm

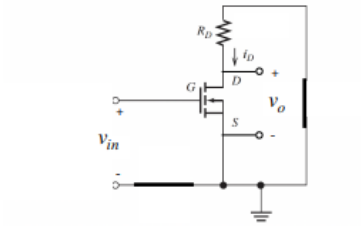
Output resistance = R_D = 1Kohm

Gain = - gm x R_D = - 2.064

MOSFET Common-Source Amplifier







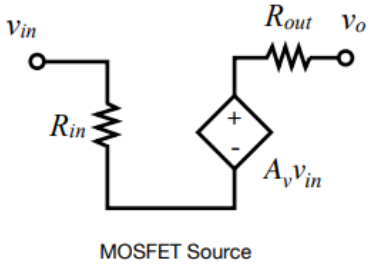
Source terminal is shared by input and output

$v_{gs} = v_{in}$ $\quad v_o = -g_m v_{in} R_D$

Gain: $A_v = \dfrac{v_o}{v_{in}} = -g_m R_D$

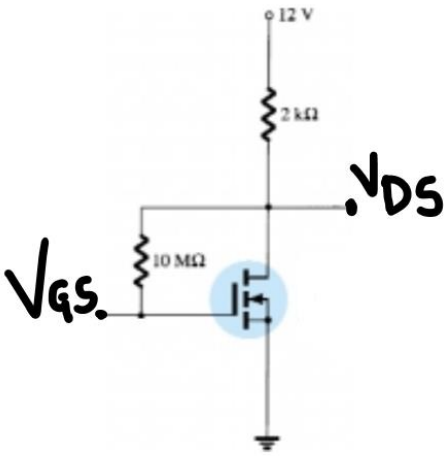
Input Impedance: $R_{in} = \infty$

Output Impedance: $R_{out} = R_D$



MOSFET Source

Q3. (10 points)



Determine I_{DQ} , V_{DSQ} , V_{GSQ} for this MOSFET.

(Hint: Find Q point and assume transistor is in Saturation)

($k = 0.24E\text{-}3\ A/V^2$)

Vth = 3V, $V_{DD} = 12V$, $R_D = 2k\Omega$

Solution :

Here, current through 10Mohm is assumed to be zero, since the input gate current of a MOSFET is very negligible.

Therefore, VGS ≈ VDS and the entire drain current from battery will flow into the MOSFET.

Now its given that the transister is in the saturation.

Hence, $Id = k(V_{GS} - V_{t0})^2 = 0.24E\text{-}3 \times (V_{GS} - 3)^2$

Now, using KCL at the drain of the transistor,

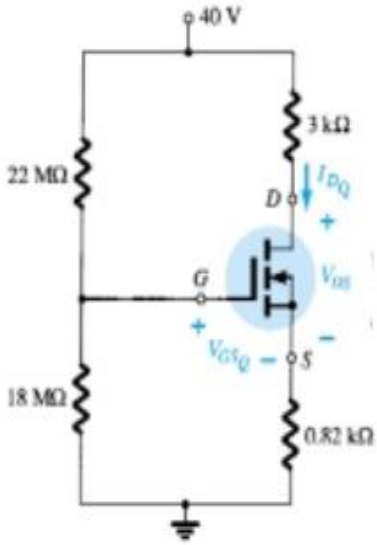
$Id = (12 - V_{DS}) / 2k$

Since VGS ≈ VDS, equating the above two equations, we get :

$0.24E\text{-}3 \times (V_{GS} - 3)^2 = (12 - V_{GS}) / 2k$ → Solving for VGS gives **$V_{GS} = V_{DS} = 6.411V = V_{GSQ} = V_{DSQ}$**

$Id = 0.24E\text{-}3\ (6.411 - 3)^2 =$ 2.79mA

Q4. (15 points)



Determine I_{DQ}, V_{GSQ}, and V_{DSQ}.

Vth = 5V, $K = 0.12E\text{-}3\ A/V^2$

(Hint: Find Q point and assume transistor is in Saturation)

Solution:

By voltage divider: $V_G = 40 \times 18 / (18 + 22) = 18V$

By KVL at input : $V_{GS} = V_G - I_D \times R_S$

Thus, $ID = (V_G - V_{GS}) / Rs = (18 - V_{GS}) / 0.82k$

Given that transistor is in saturation:

$I_D = k (V_{GS} - V_{t0})^2 = 0.12E\text{-}3 (V_{GS} - 5)^2$

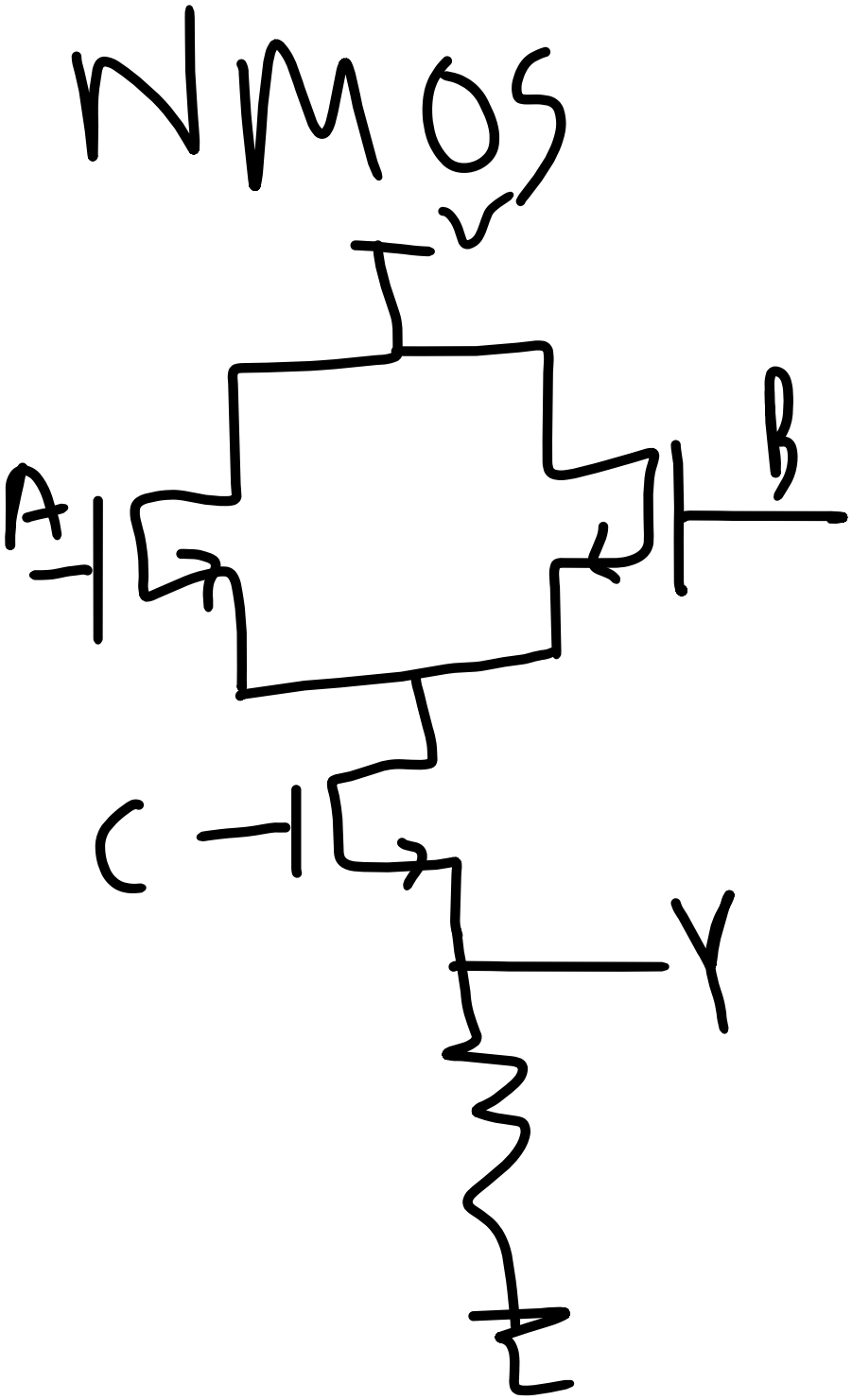
Equating the above two equations of ID and solving for VGS, we get:

$V_{GS} = 12.485V$, and hence $I_D = 6.723mA$ and $V_{DS} = V_{DD} - I_D (R_D + R_S)$

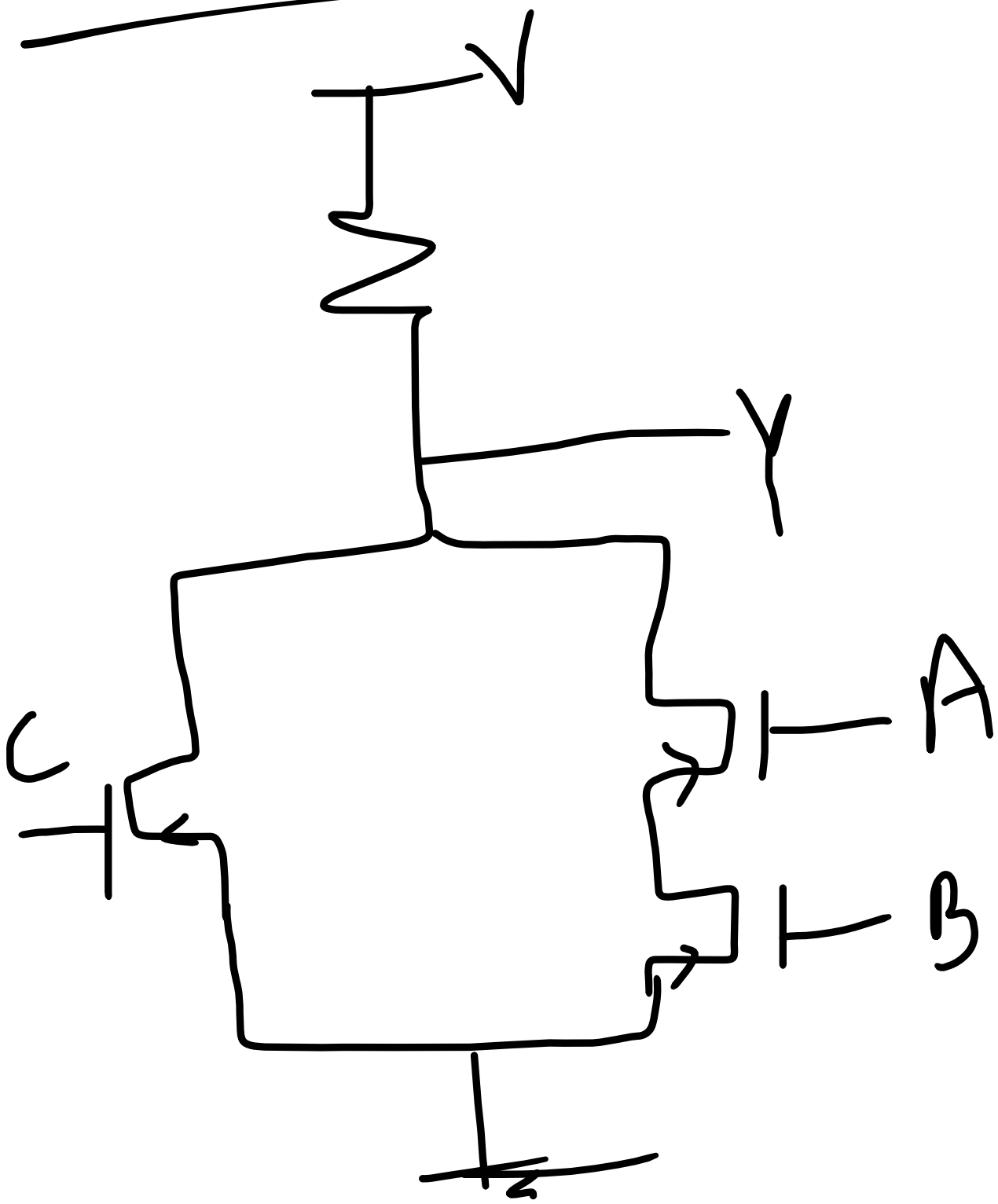
Therefore $V_{DS} = 40 - 6.723E\text{-}3\ (3000+820) = 14.31V$

Q5. (15 points)

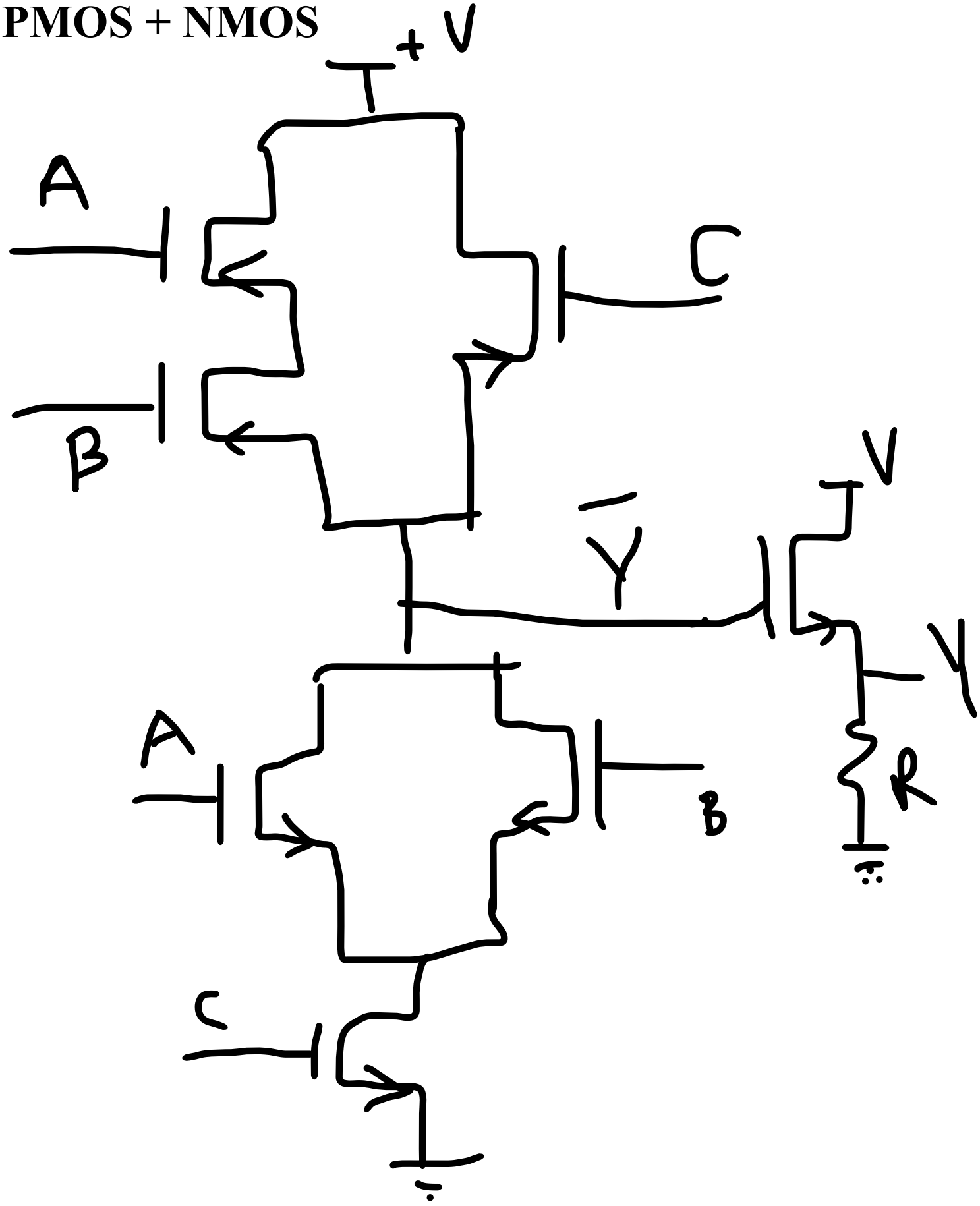
Consider : Y = (A + B) . C where A, B, C are digital inputs [Read this as, Y = (A OR B) AND C]. Implement Y by taking inputs as A, B, C and using NMOS and/or PMOS. You are allowed to use a resistor as well.



PMOS



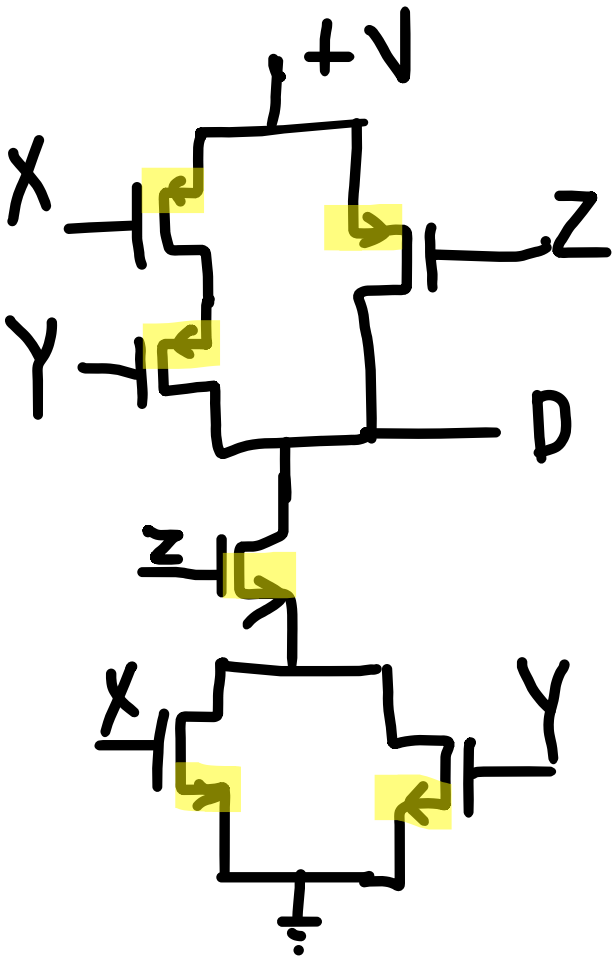
PMOS + NMOS



Q6. (14 points)

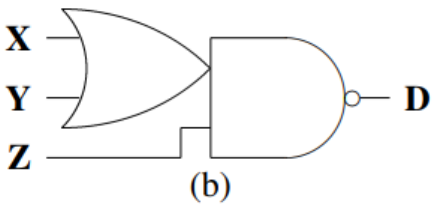
For the circuit shown below, fill in the Truth Table below with 'D' as output and X, Y, Z as input for all possible input combinations. Also, write the Boolean expression for D in terms of X, Y, Z.

Z	Y	X	D

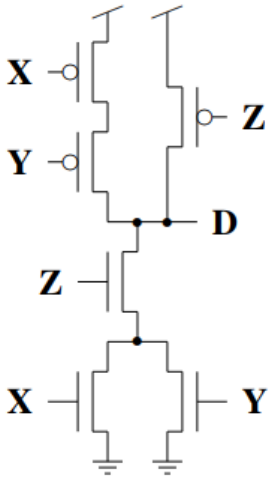


Z	Y	X	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(a)



(b)



(c)

$$D = \overline{(X + Y) \cdot Z}$$

(d)

ECE 100, Winter 2022 **Assignment #7**
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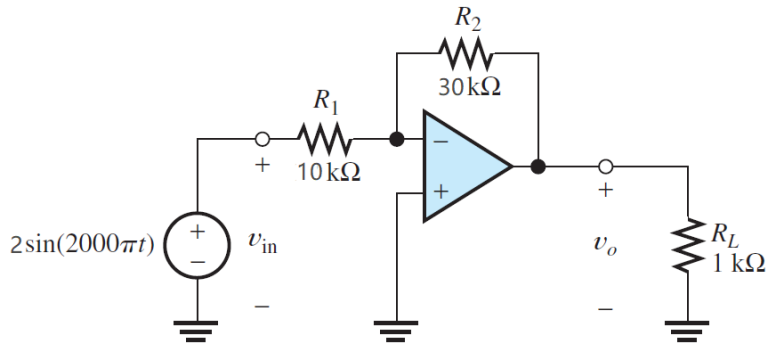
Due **Thursday, March 10th 2022, by 6 pm** to Gradescope.
100 points total.

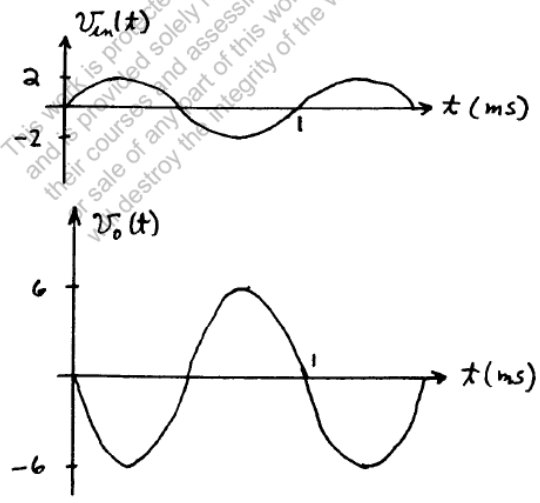
Operational Amplifier – Lecture 15, 16

Q1 (20 points)
Sketch $v_{in}(t)$ and $v_o(t)$ to scale versus time for the circuit shown in Figure. The op amp is ideal.

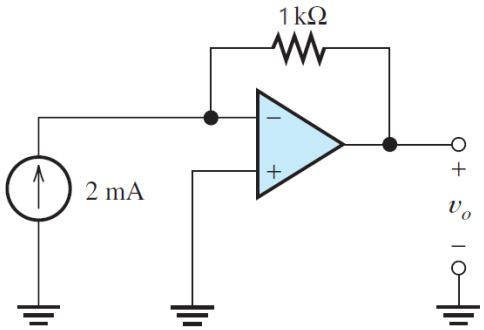


S1

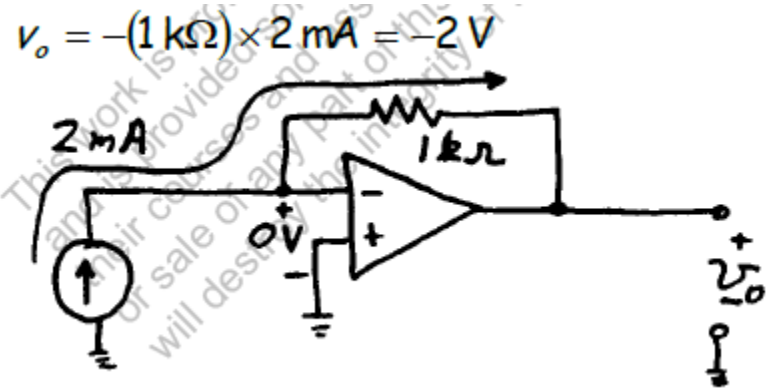
This is an inverting amplifier having a voltage gain given by $A_v = -R_2/R_1 = -3$. Thus, we have $v_o(t) = -3 \times [2\cos(2000\pi t)]$
Sketches of $v_{in}(t)$ and $v_o(t)$ are



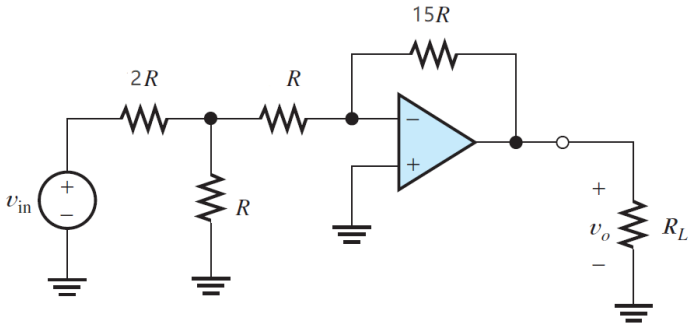
Q2 (20 points)
For each of the circuits shown in Figure, assume that the op amp is ideal and find the value of vo. The circuit has negative feedback, and the summing-point constraint (virtual open-circuit principle) applies.



S2

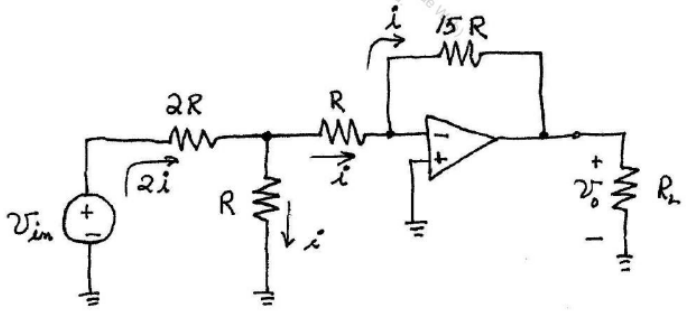


Q3 (20 points)



S3

Because of the summing-point constraint, the voltages across the two resistors of value R are equal. Thus, the currents in the resistors of value R are equal as indicated:

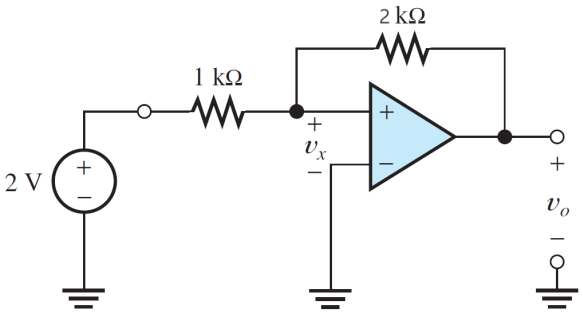


Then applying KVL, we have $v_{in} = 2R(2i) + Ri$ and $v_o = -15Ri$. Solving, we find $A_v = \frac{v_o}{v_{in}} = -3$.

Q4 (20 points)

The op amp shown below is ideal, except that the extreme output voltages that it can produce are ±10 V. Determine two possible values for each of the voltages shown.

[Hint: Notice that this circuit has positive feedback so the summing-point constraint does not apply.]



S4

This circuit has positive feedback and the output can be either +10 V or −10 V. Writing a current equation at the inverting input terminal of the op amp we have

$$\frac{v_x - 2}{1000} + \frac{v_x - v_o}{2000} = 0$$

Solving we find

$$v_x = 1.3333 + 0.3333 v_o$$

For $v_o = 10$ V, we have $v_x = 4.667$ V. On the other hand for $v_o = -10$ V, we have $v_x = -2$ V. Notice that for v_x positive the output remains stuck at its positive extreme and for v_x negative the output remains stuck at its negative extreme.

Q5 (20 points)

P13.33. Derive an expression for the voltage gain of the circuit shown in **FigureP13.33** as a function of T, assuming an ideal op amp. (T varies from 0 to unity, depending on the position of the wiper of the potentiometer.)

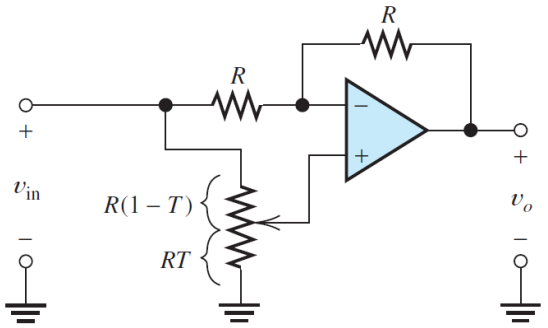
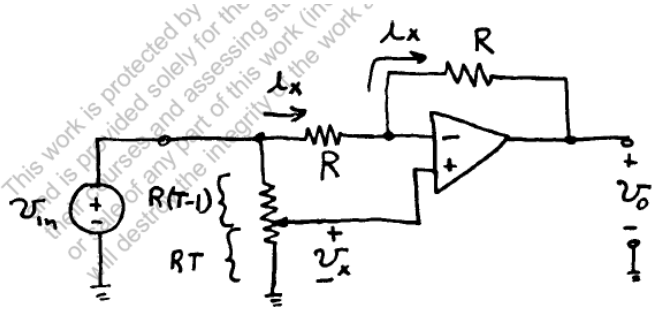


Figure P13.33

S5



By the voltage-division principle, we have

$$v_x = \frac{RT}{RT + (1-T)R} v_{in} = T v_{in}$$

Then, we can write

$$i_x = \frac{v_{in} - v_x}{R} = \frac{v_{in}(1-T)}{R}$$

$$\begin{aligned} v_o &= -Ri_x + v_x \\ &= -v_{in}(1-T) + Tv_{in} \\ &= v_{in}(2T-1) \end{aligned}$$

Thus, as T varies from 0 to unity, the circuit gain varies from -1 through to 0 to +1.