20F-COMSCIM151B-1 Homework 1

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TOTAL POINTS

50 / 50

QUESTION 1

CISC vs. RISC 5 pts

1.1 CISC time 1 / 1

✓ **+ 1 pts** Correct

1.2 RISC time 1 / 1

✓ **+ 1 pts** Correct

+ 0 pts Wrong

1.3 Fastest architecture 1 / 1

✓ **+ 1 pts** Correct

1.4 Target frequency change 2 / 2

✓ **+ 2 pts** Correct

+ 0 pts Wrong

QUESTION 2

Compare implementations 1 17 pts

2.1 Computation time on P1 2 / 2

✓ **+ 2 pts** Correct

+ 0 pts Wrong

2.2 Computation time on P2 2 / 2

✓ **+ 2 pts** Correct

+ 0 pts Wrong

2.3 Change one instruction 3 / 3

✓ **+ 3 pts** Correct instruction

- 1 pts Wrong justification

2.4 CPI of P1 2.5 / 2.5

✓ **+ 2.5 pts** Correct

2.5 CPI of P2 2.5 / 2.5

✓ **+ 2.5 pts** Correct

+ 0 pts Wrong

2.6 New frequency of P1 5 / 5

✓ **+ 5 pts** Correct

+ 0 pts Wrong

- 2.5 pts Missing units

QUESTION 3

Compare implementations 2 10 pts

3.1 Peak performance P1 5 / 5

✓ **+ 5 pts** Correct

+ 0 pts Wrong

3.2 Peak performance P2 5 / 5

✓ **+ 5 pts** Correct

+ 0 pts Wrong

QUESTION 4

Performance/Power tradeoff 18 pts

4.1 Optimum for single core 8 / 8

✓ **+ 8 pts** Correct

+ 0 pts Incorrect

4.2 Number of cores 4 / 4

✓ **+ 4 pts** Correct

+ 0 pts Wrong

4.3 Multi-core frequency & voltage 4 / 4

✓ **+ 4 pts** Correct

+ 0 pts Wrong

4.4 Multi-core time 2 / 2

✓ **+ 2 pts** Correct

+ **0 pts** Wrong

Next time, try to avoid rounding intermediate results.

QUESTION 5

5 Late submission penalty 0 / 0

✓ **+ 0 pts On time**

- 12.5 pts Late submission

Nevin
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Homework Set – I

Session: Fall 2020 Instructor: Prof. P. Gupta

Total Points: 50 **Due Date: 8th Oct (before class starts)**

Instructions

1. **There are two sections in this homework set. The questions under Section – I are for your practice. Solutions to these problems are already provided on the course web page. Students are encouraged to solve the problems before looking at the solution provided.**
2. **Problems under Section – II are to be submitted on to Gradescope.**
3. **Submissions will be auto-graded, so please write your final answer in the boxes provided**

Section – I

1. What binary number does this hexadecimal number represent $(7\text{fff fffa})_{hex}$? What decimal number does it represent?

2. What hexadecimal number does this binary number represent:
$(1100\ 1010\ 1111\ 1110\ 1111\ 1010\ 1100\ 1110)_{two}$?

3. What decimal number does this two's complement binary number represent:
$(0111\ 1111\ 1111\ 1111\ 1111\ 1111\ 1110\ 1111)_{two}$?

4. If x = 0011 0101 0011 and y = 0010 1101 0111, evaluate x * y.

5. Suppose you wish to run a program P with 7.5×10^9 instructions on a 5 GHz machine with a CPI of 0.8.
   a. What is the expected CPU time?
   b. When you run P, it takes 3 seconds of wall clock time to complete. What is the percentage of the CPU time P received?

a. CPU time = $7.5\cdot10^9$ instructions $\cdot \frac{0.8 \text{ cycles}}{1 \text{ instruction}} \cdot \frac{1 \text{ sec}}{5\cdot10^9 \text{ cycles}}$

$= \boxed{1.2 \text{ sec}}$

b. 40%

Section - II

1. In this exercise we will evaluate the performance difference between two CPU architectures: CISC (Complex Instruction Set Computing) and RISC (Reduced Instruction Set Computing). Generally speaking, CISC CPUs have more complex instructions than RISC CPUs and therefore need fewer instructions to perform the same tasks. However, typically one CISC instruction, since it is more complex, takes more time to complete than a RISC instruction. Assume that a certain task needs P CISC instructions and 2P RISC instructions, and that one CISC instruction takes 8T ns to complete, and one RISC instruction take 2T ns.

- Under this assumption, calculate the time that the CISC CPU will take to complete the task? **[1 point]**

CPU time = #instructions · time/instruction

= P · 8T

= 8PT

8PT ns

- Calculate the time that the RISC CPU will take to complete the task? **[1 point]**

2P · 2T

4PT ns

- Which CPU would complete the task faster? **[1 point]**

8PT > 4PT

RISC

- By what percentage should the clock frequency of the slower CPU change to catch up with the faster CPU for this task? **[2 points]**

clock cycle time : seconds/cycle

must 1/2 → freq : ×2

100%

2. Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

	Clock Rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

- Let's assume a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D. Space for solving the problem is provided, however write the final answer in the box. **[7 points]**
  - How many seconds would the program take to execute on P1? **[2 points]**

CPU time = clock cycle time · [CPI · #instruct] = $\frac{1}{1.5\cdot 10^9}$ (CPI · #instruct)

gCPI = $\underline{1}\cdot 10^5 + \underline{2}\cdot 2\cdot 10^5 + \underline{3}\cdot 5\cdot 10^5 + 2\cdot 10^5\cdot \underline{4} = 28\cdot 10^5$ cycles.

CPU time = $\frac{28\cdot 10^5}{1.5\cdot 10^9}$ =

$1.8667\cdot 10^{-3}$ seconds

  - How many seconds would the program take to execute on P2? **[2 points]**

gCPI = $2\cdot 1\cdot 10^5 + 2\cdot 2\cdot 10^5 + 2\cdot 5\cdot 10^5 + 2\cdot 2\cdot 10^5 = 20\cdot 10^5$ cycles.

CPU time = $\frac{20\cdot 10^5}{2\cdot 10^9} = 10\cdot 10^{-4}$ sec

10^{-3} seconds

  - Take P1, and you are allowed to change the implementation of *one instruction* to reduce its CPI by *one cycle*. Which instruction would you choose in order to reduce the overall execution time of the program? **[3 points]**

C: $10^5\cdot 5$ instructions

class C

- What is the global CPI for each implementation? **[2.5 + 2.5 points]**

calculated already !!!

P1: 2.8

P2: 2.0

- What should be the clock rate of P1 such that its performance is at par with P2? **[5 points]**

$$\frac{28 \cdot 10^5}{CR} = 10^{-3}$$

$$CR = 28 \cdot 10^8$$

$$= 2.8 \text{ GHz}$$

2.8 GHz

3. Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions (A, B, C, D, and E) in the instruction set. P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 are as follows:

Class	CPI on P1	CPI on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	3	4

Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence. What are the peak performances of P1 and P2 expressed in instructions per second? **[10 points]**

P_1: inst/sec: $\frac{\text{inst}}{\text{cycle}} \cdot \frac{\text{cycles}}{\text{sec}} = \frac{1}{1} \cdot 4 \cdot 10^9 = 4 \cdot 10^9$ instructions/sec.

P_2: inst/sec: $\frac{\text{inst}}{\text{cycle}} \cdot \frac{\text{cycles}}{\text{sec}} = \frac{1}{2} \cdot 6 \cdot 10^9 = 3 \cdot 10^9$ instructions/sec

P1: $4 \cdot 10^9$ instructions/sec

P2: $3 \cdot 10^9$ instructions/sec.

4. You are tasked with designing a multi-core chip (only cores) for a perfectly parallel application i.e., the runtime of the application reduces by a factor of N when N CPU cores are available. The application runtime on a single core is 32 billion cycles. Assume that you have one pre-designed core available which has the following specifications:
    - Nominal Frequency: 1GHz
    - Nominal Voltage: 1V
    - Power @1GHz/1V: 50W
    - Area: 20mm^2
    - Also assume that frequency of the core scales linearly with voltage.
    - Minimum Voltage of Operation: 0.4V, Maximum: 1.5V

    - The chip you need to design has a thermal limit of 75W and an area budget of 20mm^2. At what voltage and frequency should the chip be run to get the maximum performance under the thermal and area budgets? **[8 points]**

power: $\propto V^2 \cdot f$

@ power 50W $\rightarrow$ V = 1V, f = 1GHz

@ V = k Volts

$P = 50 \cdot k^2 \cdot k = 50k^3 \leq 75\,W$

$k^3 \leq 1.5$

$k \leq 1.145$

$V = 1.145\,V$

Frequency: 1.145 GHz

Voltage: 1.145 V

- Assume you have a total of 100 mm^2 and a thermal limit of 100W. How many cores will you to put in the chip and what voltage-frequency point will each core run at (all cores run at same voltage-frequency point)? The goal is to get the best performance possible. How many milli-seconds would the application need to complete. **[10 points]**

Assume 5 cores:

each core @ voltage V, and f V GHz

each power: $50 \cdot V^3$

total power: $5 \cdot 50 \cdot V^3 = 250 \cdot V^3$ watts

$$250 \cdot V^3 \leq 100$$

$$V^3 \leq 2/5 \Rightarrow V \leq 0.737 \text{ V}$$

$$f = 0.737 \text{ GHz}$$

$$\frac{32 \cdot 10^9 \text{ cycles}}{5 \cdot 0.737 \cdot 10^9 \text{ cycles/sec}} = 8.684 \text{ sec.}$$

If 4 cores, $4 \cdot 50 \cdot V^3 = 200 \cdot V^3$ watts $\leq 100 \rightarrow V \leq 0.794 V$

$f = 0.794$ GHz

$$\frac{32 \cdot 10^9}{4 \cdot 0.794 \cdot 10^9} = 10.076 > 8.684 \text{ so slower}$$

Number of cores:	5
Frequency:	0.737 GHz
Voltage:	0.737 V
Time (ms):	8684 ms