Q1
4 Points

For a cache with 4 total blocks and block size of 4 bytes, following memory reference sequence is given: 00000 00100 01001 11000 11110 01100 11100. Assume LRU replacement strategy, 5 bit memory addresses and byte addressable memory.

Q1.1
2 Points

What are possible associativities for this cache ? Check all correct answers.

- [ ] 8
- [x] 2
- [x] 4
- [ ] 0
- [x] 1

Q1.2
2 Points

If the last access is a miss, what is the associativity of the cache ?

1

Q2
3 Points

In a two level cache (L1, L2, memory), L1 miss rate is 5% and L2 miss rate is 1%. Access time for L1 is 1 cycle. Access time for L2 is 10 cycles including any time required to handle the L1 miss. Main memory access time is 100 cycles including any time required for handling L2 miss.

Q2.1
3 Points

What is the average memory access time ?

1.495

Q3
3 Points

Consider a L1+main memory system with L1 hit time of 1 cycle and main memory access time of 100 cycles. For the questions below, only report the time spent in doing the memory access.

Q3.1
1 Point

If the cache is write-through with no write buffer, how many cycles would it take to process a store hit ? ONLY write a number in the space below.

101

Q3.2
1 Point

If the cache is write-back, how many cycles would it take to process a store hit ? ONLY write number in the space below.

1

Q3.3
1 Point

If the cache is write-around, how much time would it take to process a store miss ?

100

Quiz 4

GRADED

STUDENT
LIANG, NEVIN

TOTAL POINTS
10 / 10 pts

QUESTION 1

(no title) **4** / 4 pts

1.1 (no title) **2** / 2 pts

1.2 (no title) **2** / 2 pts

QUESTION 2

(no title) **3** / 3 pts

2.1 (no title) **3** / 3 pts

QUESTION 3

(no title) **3** / 3 pts

3.1 (no title) **1** / 1 pt

3.2 (no title) **1** / 1 pt

3.3 (no title) **1** / 1 pt