Q1 ISA

5 Points

Q1.1 Organization Style

3 Points

I want to implement the following operation:
A = $XY + XZ$
How will you implement it in accumulator, register-memory and load-store architecture ? Assume ISA has ADD, MULT operations available in addition to any LOAD, STORE needed. A, X, Y, Z are all in memory.

Accumulator:

```
Load X
Mult Y
Store A
Load X
Mult Z
Add A
Store A
```

Register-memory

```
MULT Y, X, Y
MULT Z, X, Z
ADD A, Y, Z
```

Load-Store

```
LOAD R1, X
LOAD R2, Y
LOAD R3, Z
MULT Y, X, Y
MULT Z, X, Z
ADD R4, Y, Z
STORE A, R4
```

Q1.2 Need more registers

2 Points

MIPS was invented in 1985 with 32 integer registers. According to Moore's Law, named after Intel founder Gordon Moore, the number of transistors per microprocessor doubles every 1.5 years. Thus, microprocessors could have 1000 times the number of transistors in 2000 as they could in 1985. It would seem that we could easily build microprocessors with, say, 256 registers. Select all the reasons why MIPS has not increased the number of integer registers from 32 to 256.

- [ ] There is no need for more than 32 registers, as compilers have difficulty using the 32 registers in the MIPS architecture now.
- [x] Due to the importance of binary compatibility, new MIPS processors must be able to execute old MIPS instructions, and it would be very hard to find room for 256 registers in the original MIPS instruction format.
- [x] 32 registers are much smaller than 256 registers, and since smaller is faster, the 32 registers makes it easier to build fast microprocessors than if there were 256 registers.
- [ ] Moore's Law applies to Intel microprocessors, not MIPS microprocessors, hence the hypothesis is false. The MIPS chip would be too expensive if it had 256 registers.

Q2 Measuring Performance

5 Points

You are running a benchmark on your company's processor, Mbase, which runs at 400 MHz and has the following characteristics:

Instruction	Frequency	#Cycles
A	40%	2
B	30%	3

C	20%	3
D	10%	5

You ask the hardware team if they can improve the processor design. They tell you that they could make this processor run at 500 MHz, however they would have to increase the number of cycles for instruction type B to 4. (All the other instruction types still take the same number of cycles). Call this machine Mopt.

How much percent faster is Mopt than Mbase (to one decimal place)?

11.4

Show your work here:

Let there be 100 instructions:
For MBASE:
40 A's, 30 B's, 20 C's, 10 D's
Total Cycles = 40 * 2 + 30 * 3 + 20 * 3 + 10 * 5 = 280 cycles
At 400 MHz, or 400e9 cycles/second, this will take 280/400e9 seconds

For MOPT:
40 A's, 30 B's, 20 C's, 10 D's
Total Cycles = 40 * 2 + 30 * (4) + 20 * 3 + 10 * 5 = 310 cycles
At 500 MHz, or 500e9 cycles/second, this will take 310/500e9 seconds

Now, to calculate how much FASTER Mopt is compared to Mbase, given th e same number of instructions, we use the formula |T2 - T1| / T1 * 100% whic h comes out to

|310/500e9 - 280/400e9| / (280/400e9) * 100% = 11.4%

Quiz 1

GRADED

STUDENT

LIANG, NEVIN

TOTAL POINTS

9 / 10 pts

QUESTION 1

ISA — **4** / 5 pts

1.1 Organization Style — **2** / 3 pts

1.2 Need more registers — **2** / 2 pts

QUESTION 2

Measuring Performance — **5** / 5 pts