Q1

6 Points

The page size of a RISC5 computer is 16 Kbytes; the cache block size is 32 words and the machine is byte-addressable (each word is 4 bytes). The cache size is 4 Kbyte, and it is 4-way set associative. The virtual addresses are 42 bits and physical addresses are 36 bits long. The cache is physically addressed. Calculate the sizes (number of bits) of the following fields:

Q1.1

1 Point

Block offset

7

Q1.2

1 Point

Set index

3

Q1.3

1 Point

Tag

26

Q1.4

1 Point

Page offset

14

Q1.5
1 Point

Virtual page number

28

Q1.6
1 Point

Physical page number

22

Q2
2 Points

A processor has a 8 entry TLB and 4KB pages. What is the maximum memory a program should access to maximize its performance ? Write the answer in KB below. Only enter a number below.

32

Q3
2 Points

You are debating whether to have your L1 cache physically addressed or virtually addressed in your processor. Assume that entire cache has to correspond to one program at a time for security reasons. Check *all* that are correct:

- [x] Choose virtually addressed if the system is single programmed.
- [x] Physically addressed is likely better for a multi-programmed system with a TLB which context switches a lot.
- [ ] Virtually addressed is likely better better if cache size is large

Quiz 5

GRADED

STUDENT
LIANG, NEVIN

TOTAL POINTS
10 / 10 pts

QUESTION 1

(no title) **6** / 6 pts

1.1	(no title)	**1** / 1 pt
1.2	(no title)	**1** / 1 pt
1.3	(no title)	**1** / 1 pt
1.4	(no title)	**1** / 1 pt
1.5	(no title)	**1** / 1 pt
1.6	(no title)	**1** / 1 pt

QUESTION 2

(no title) **2** / 2 pts

QUESTION 3

(no title) **2** / 2 pts