Logic Design Autumn 2018

M1522.000700(001) CSE (Jihong Kim)

# **Assignment 5**

**Total: 60 points**

**Received: 2018/11/21**

**Due: 3:00 p.m., 2018/11/30**

1. **Notes on Assignment 5:**

In this assignment, you will design a simple finite state machine using Xilinx ISE. You must use Verilog to design your finite state machine.

1. **What to Submit:**

Submit both your design document and design files. Your design document must include at least the following information:

1. Explanations on how you approached the given design problem including a state diagram description of your finite state machine.
2. Printouts of output waveforms for the required test inputs, Test Numbers 1, 2, 3 and 4.

Submit your design document and your Verilog source files to **ETL before the deadline**. **We plan to test your design using other test inputs as well**, so please make sure your design works for all possible input combinations.

**\* Problem: Pattern Counter**

Design a sequential logic subsystem with three inputs, clk, X, TYPE, and four outputs, Y3, Y2, Y1, Y0, that behaves as follows. The outputs Y3Y2Y1Y0 indicate the number of occurrences of a specific bit pattern in the input sequence fed into the subsystem. (Y3 is the highest-order bit and Y0 is the lowest-order bit.) A bit pattern of interest is determined by the value of the input TYPE. If TYPE is zero, a bit pattern of 101 is used, and if TYPE is one, a bit pattern of 0101 is used.

Use following **PatternRecognizer** interface for the Verilog implementation. A bit pattern is represented by the input signal **X**. The module reads input **X** at the negative edge of the **clk** signal, and updates its internal state to generate the total number **Y** of pattern occurrence so far. The pattern is defined by the **TYPE** input.

**module** **PatternRecognizer**(

**input** clk,

**input** X,

**input** TYPE,

**output** [3:0] Y);

As an example, when **TYPE** is set to 1, if the input sequence 010101 is fed into the pattern counter, Y3Y2Y1Y0 will output 0001 when first four inputs are read. Then after the remaining two inputs are read, the output will change to 0010.

Test your design using the following input cases:

|  |  |  |
| --- | --- | --- |
| Test Number | TYPE value | Input Sequence |
| 1 | 0 | 0101101011010101011010110101 |
| 2 | 1 | 0100100100101010110101101001 |
| 3 | 0 | 0101110010010100110010110101 |
| 4 | 1 | 1010101001010101011001000101 |

If the problem is not clearly defined, you may make your own assumptions. If you do, make sure that you state your assumptions in your design document.