

# ChipWhisperer CW310 "Bergen Board" - Xilinx Kintex 7 Target Board

NewAE Technology Inc.

## Suggested Layer Stack



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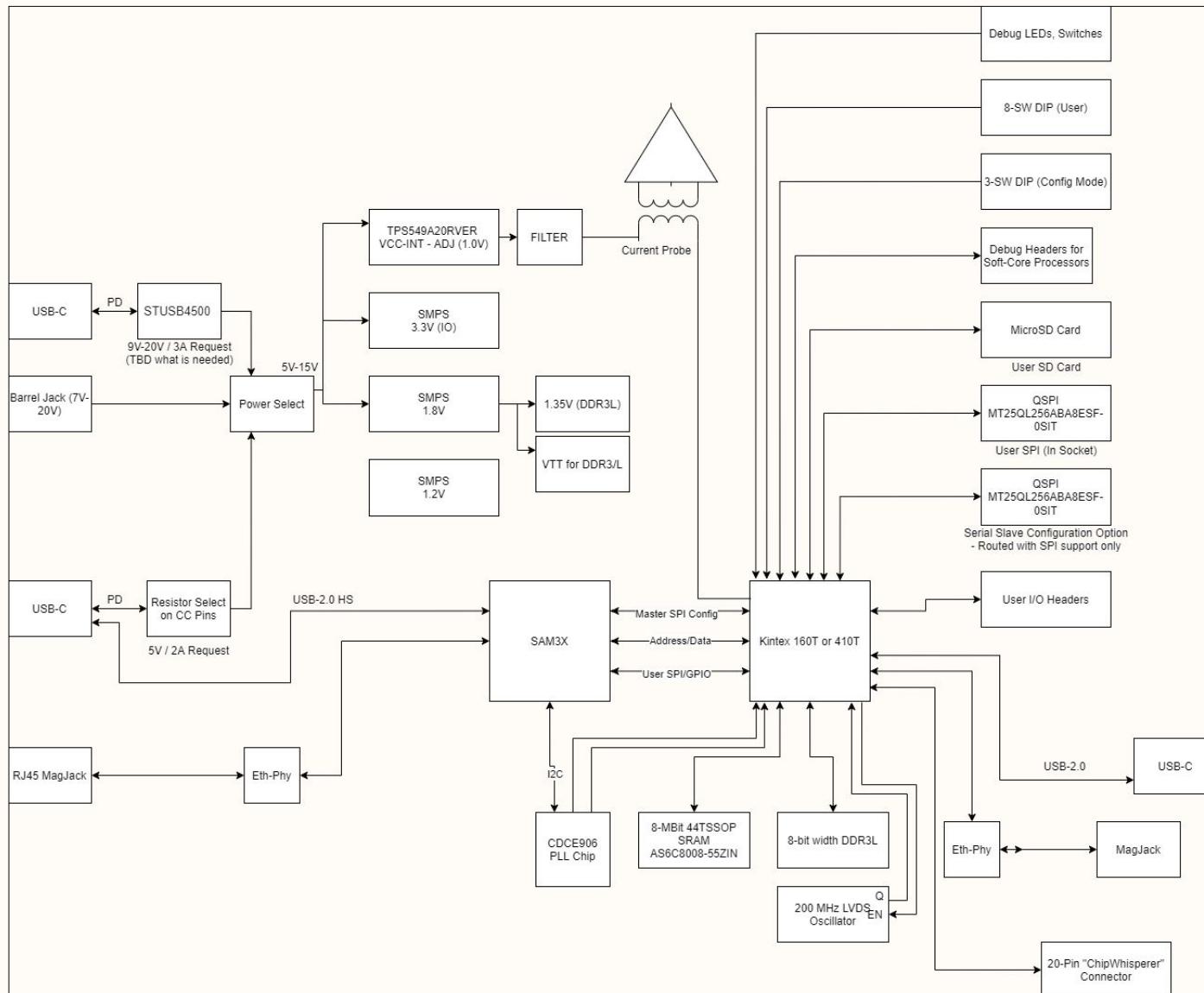
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## Revision Summary

- 00: Ultra-alpha.
- 01: Super-alpha.
- 02: March 10/2021 Feature complete.
- 03: March 13/2021 Internal release.
- 04: March 15/2021 Add brown-out on 5V, silkscreen updates
- 05: March 22/2021 Change FPGA routing for HP/HR banks.
- 06: March 30/2021 Mark DNP parts, fix a few missing resistors.

Title: Bergen Board - The Cover Sheet		Approved: Yes	
Rev: 06	Project: BERGENBOARD	License: NewAE	
Date: 2021-03-30	Time: 5:33:43 PM	Sheet 1 of 31	Copyright © NewAE Technology Inc.   NewAE.com
File: CW310_Cover_Page.SchDoc			

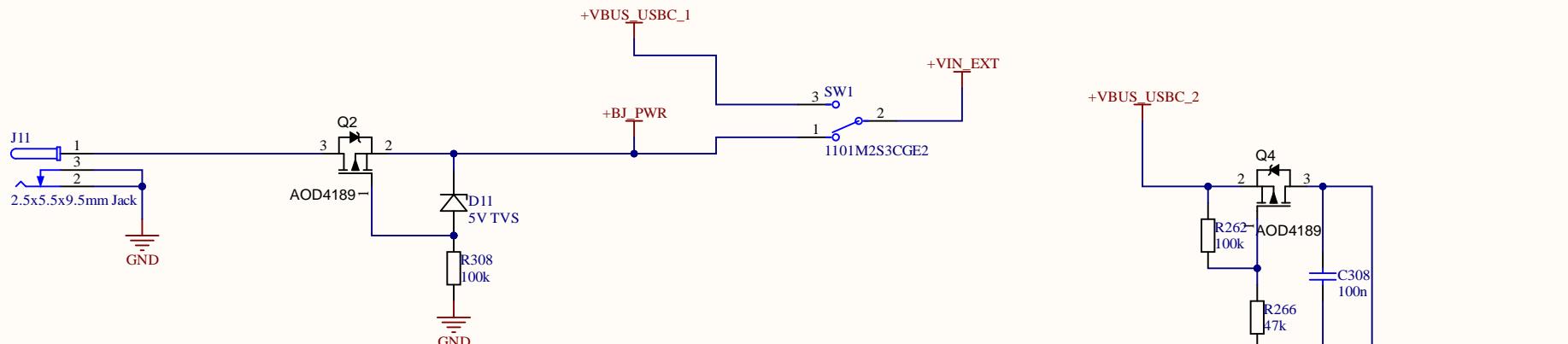
# Block Diagram



Title: <b>Block Diagram</b>		Approved:	NewAE
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Date: 2021-03-30	Time: 5:33:43 PM	Sheet 2 of 31	Copyright © NewAE Technology Inc.   NewAE.com
File: CW310_Block_Diagram.SchDoc			

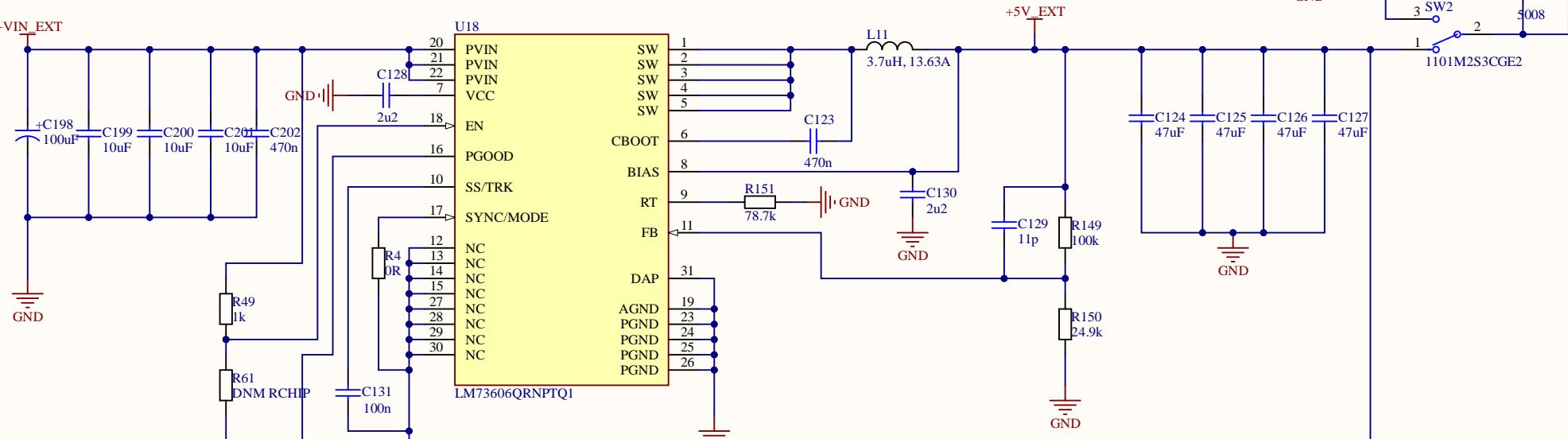
# INPUT POWER

A



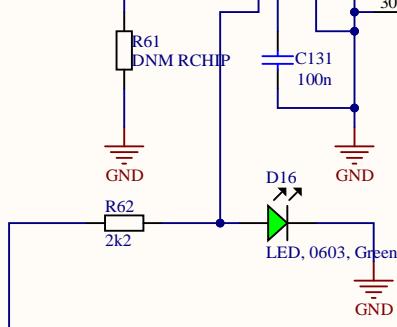
A

B



B

C



C

Based on design from  
<https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=9C49F428E2C4FF82>

Title: **5V Regulator**

Approved: Yes



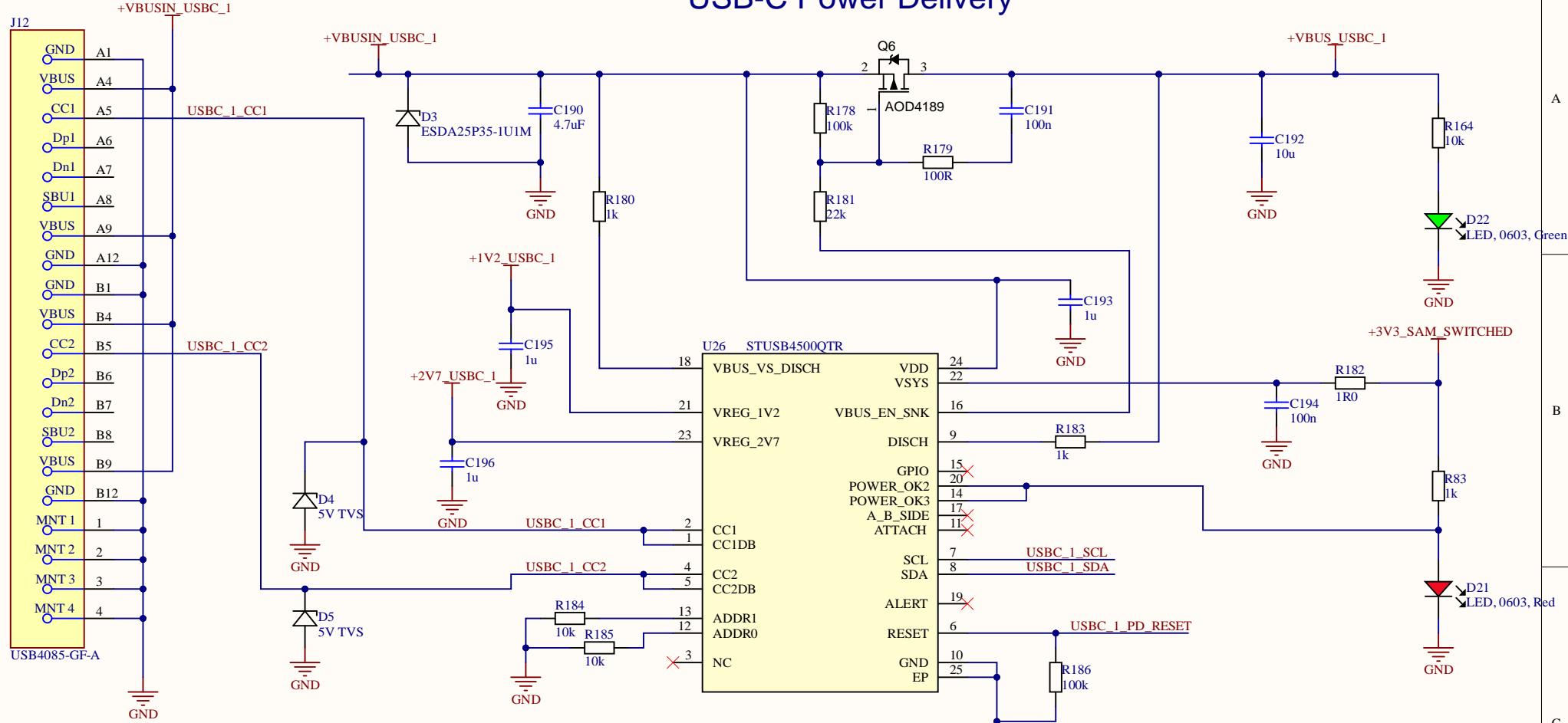
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File: CW310\_INPUT\_POWER.SchDoc

# USB-C Power Delivery



Title: **USB-C PD Controller**

Approved: Yes



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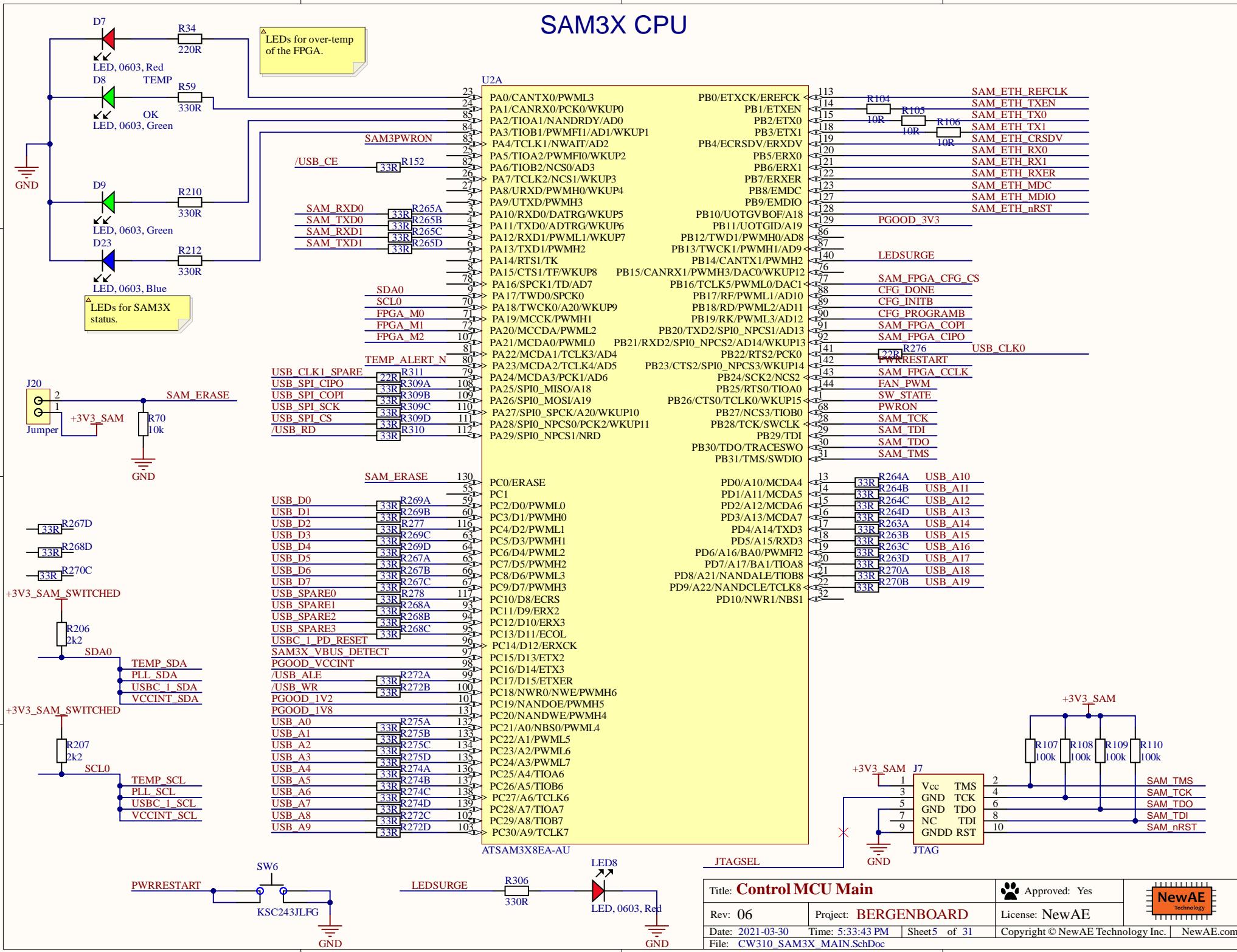
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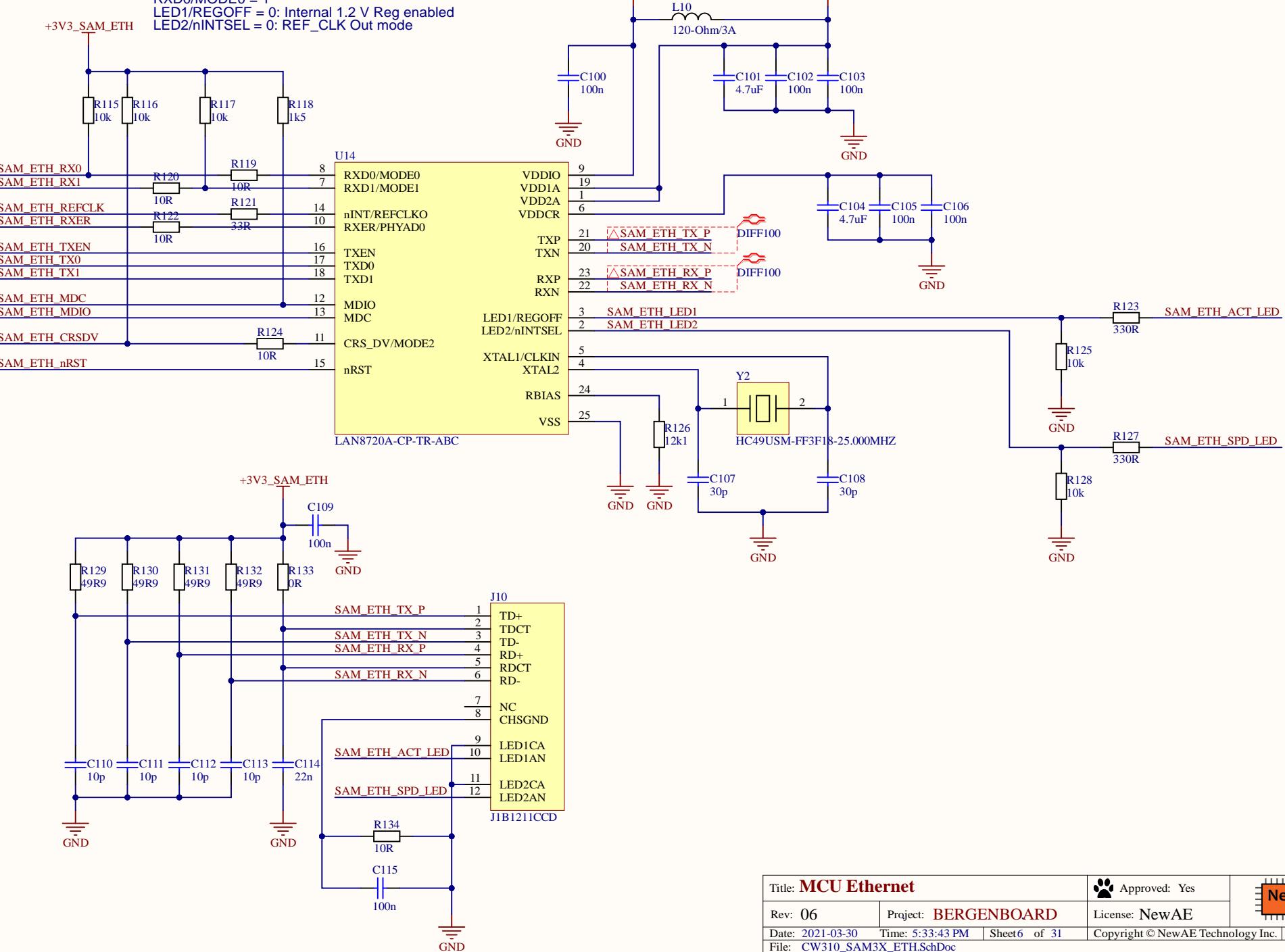
File: CW310\_USB\_POWER.SchDoc

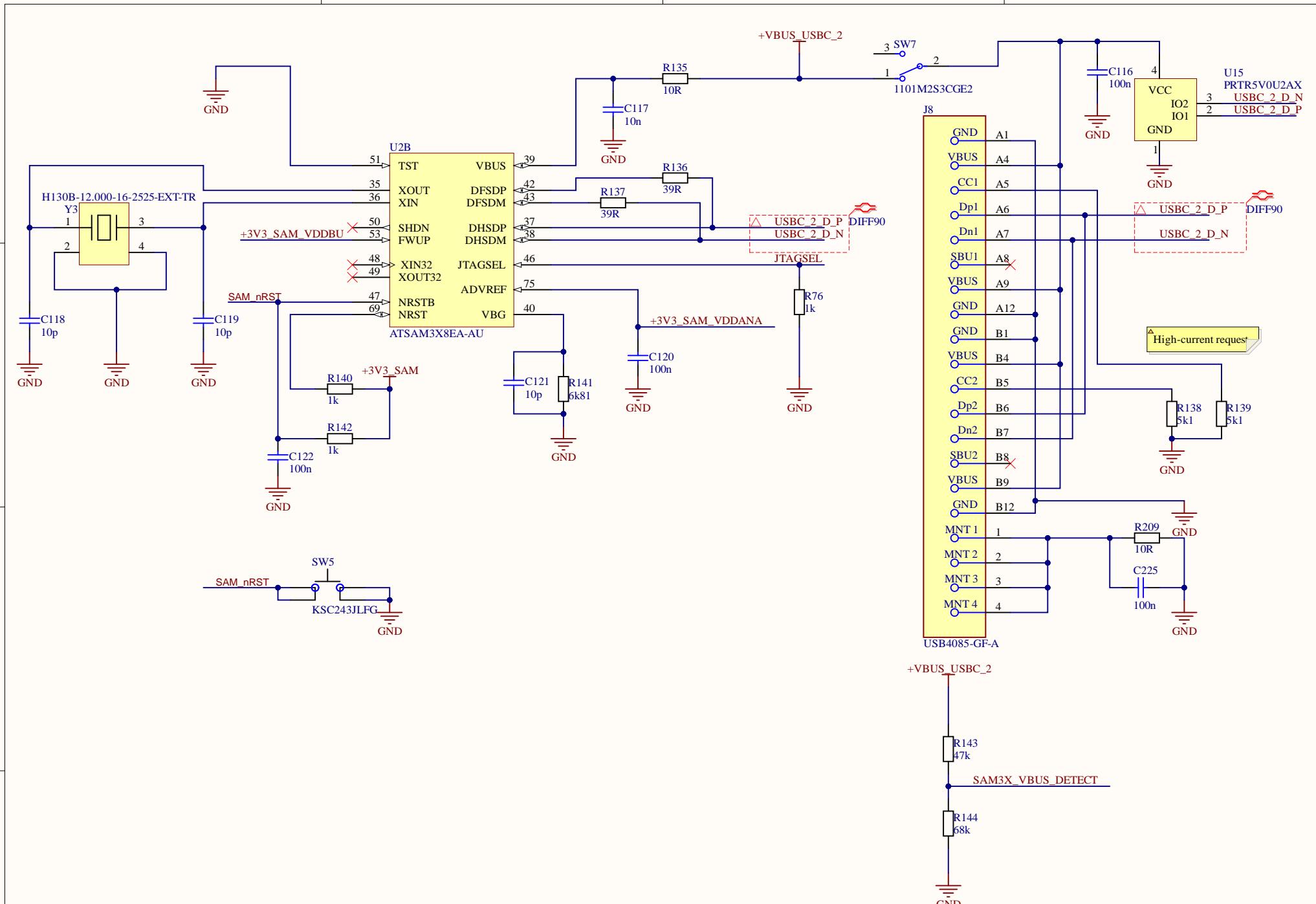
# SAM3X CPU



# SAM3X Ethernet

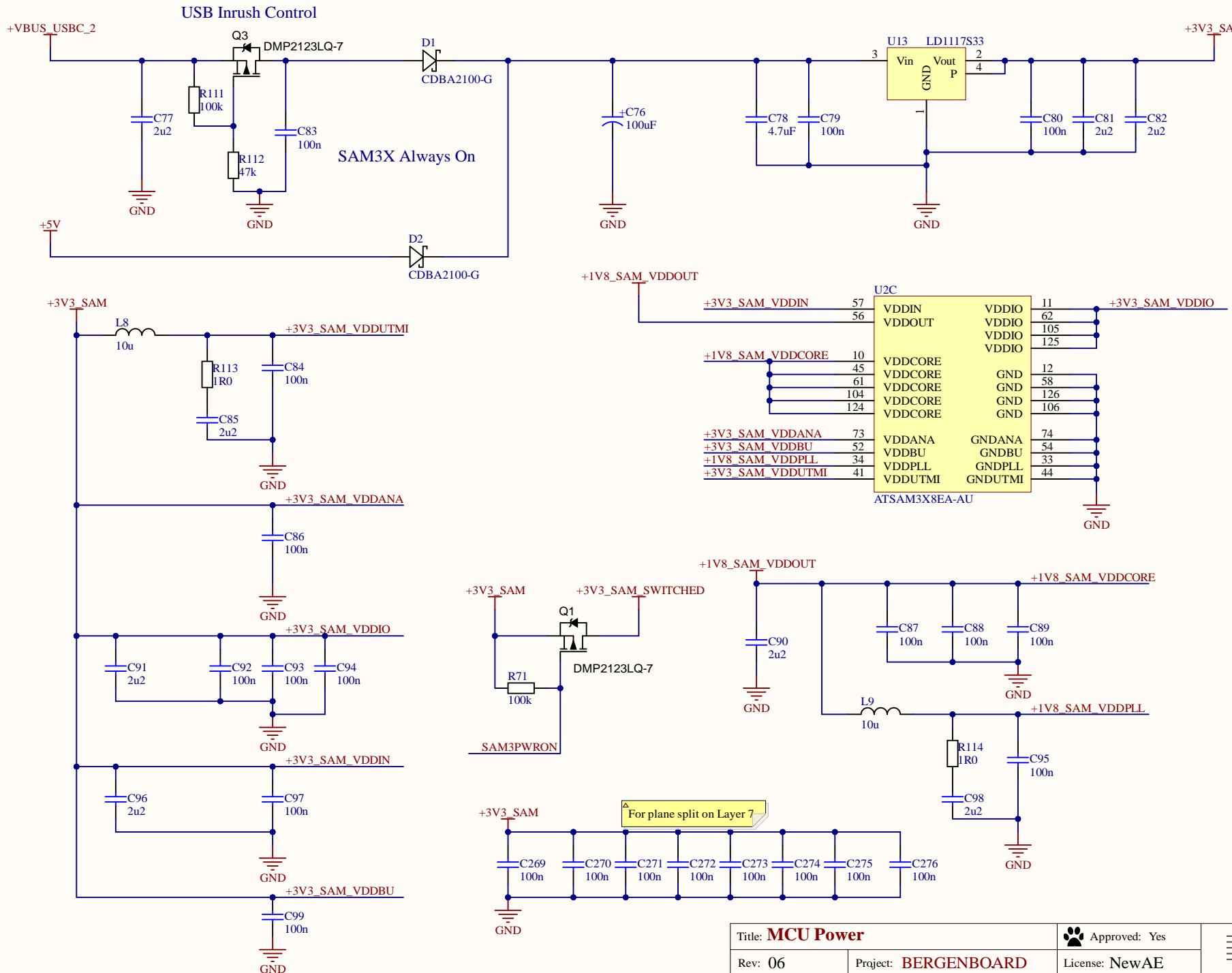
**LAN8720 PHY Configuration**  
PHYAD0 = 0: Phy Address 0  
CRS\_DV/MODE2 = 1: All modes, autonegotiation enabled  
RXD1/MODE1 = 1  
RXD0/MODE0 = 1  
LED1/REGOFF = 0: Internal 1.2 V Reg enabled  
LED2/nINTSEL = 0: REF\_CLK Out mode

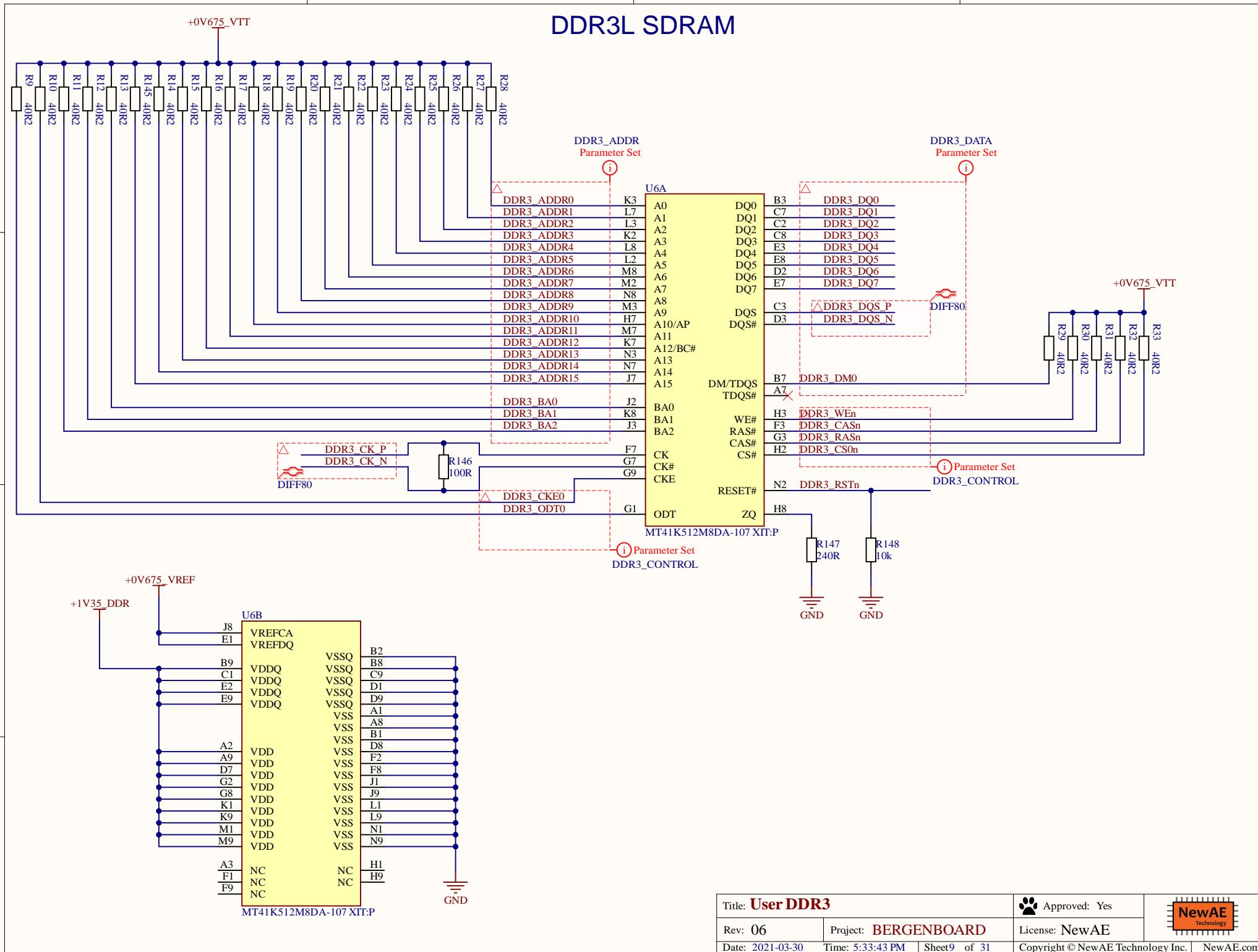




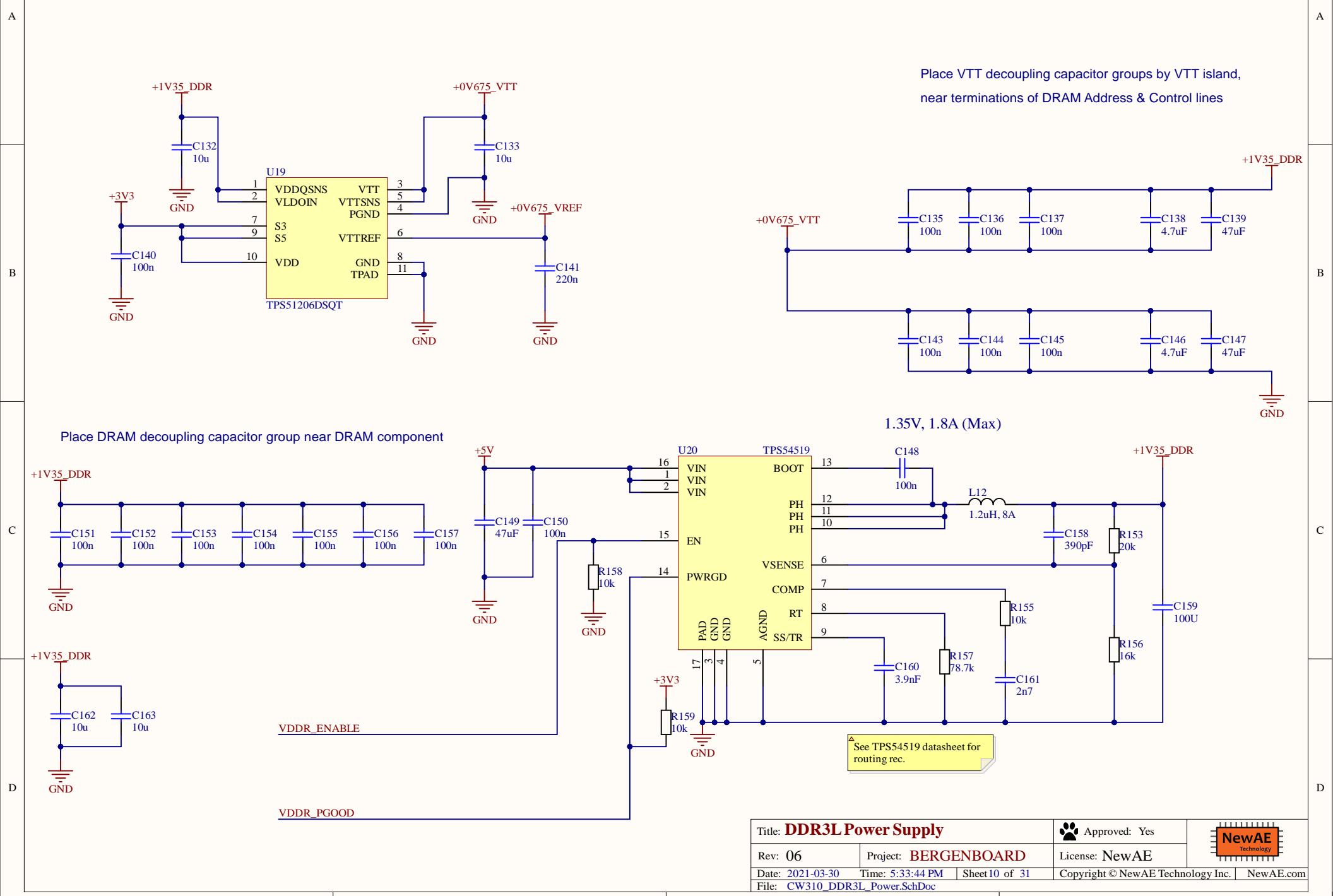
Title: <b>MCU USB</b>		 Approved: Yes	
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File: CW310 SAM3X USB.SchDoc			

# SAM3X Power



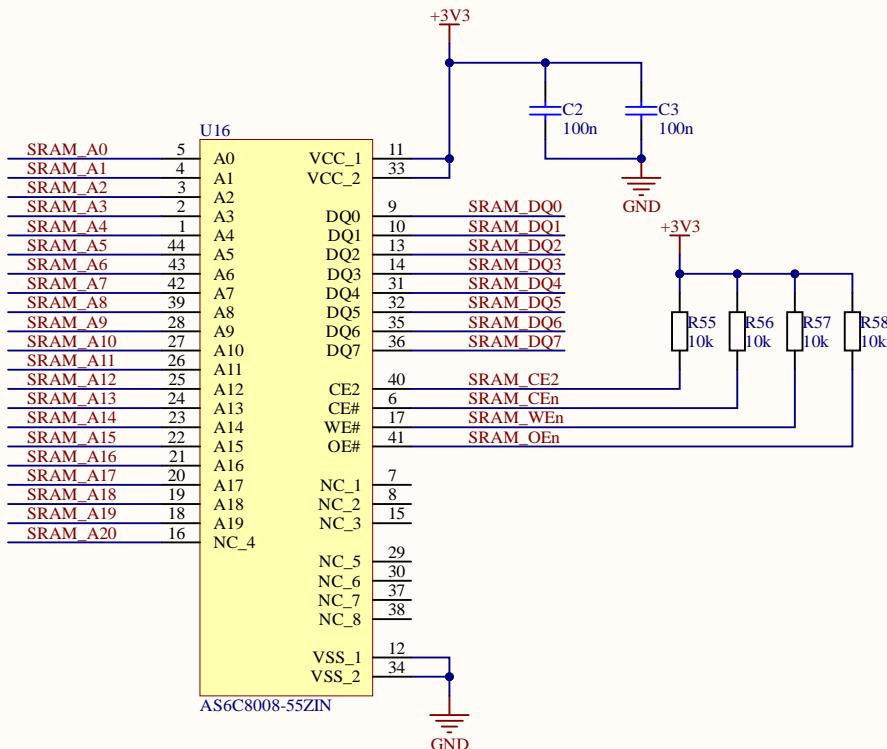


# DDR3L VTT & DECOUPLING



## SRAM

▲ SRAM should be footprint compatible with:  
AS6C8008-55ZIN  
CY62158EV30LL-45ZSXIT  
IS62WV10248DBLL-55TLI



Title: **User SRAM** Approved: Yes   
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 File: [CW310\\_SRAM.SchDoc](#)

FPGA Bank: 3.3V  
U1A

## BANK 12

IO_L21N_T3_DQS_12	AE26 USB A3
IO_L23P_T3_12	AD25 USB A2
IO_L21P_T3_DQS_12	AD26 USB A1
IO_L24 USB A6	AD24 USB A6
IO_L16N_T2_12	AB24 USB A4
IO_L11N_T1_SRCC_12	Y25 /USB_ALE
IO_L10P_T1_12	AB26 CWIO_MOSI
IO_L9P_T1_DQS_12	AC24 USB A5
IO_L14N_T2_SRCC_12	U24 USB A13
IO_L22P_T0_12	AB21 CWIO_HS1
IO_L18P_T2_12	U22 USB A14
IO_L11P_T0_12	AD23 USB A7
IO_L16P_T2_12	AC22
IO_L17N_T2_12	AB25 USB A9
IO_L7N_T1_12	U26 USB D1
IO_L4P_T0_12	U25 USB D0
IO_L2N_T0_12	W20 USB A19
IO_L15P_T2_DQS_12	W23 USB A10
IO_L8P_T1_12	V23 USB A11
IO_L3P_T0_DQS_12	V22 USB A15
IO_L1N_T0_12	U21 USB A16
IO_L6P_T0_12	IO_0_12
IO_L22P_T0_12	V21 USB A17
IO_L11P_T1_SRCC_12	AA23 /USB_CE
IO_L19N_T3_VREF_12	AE21 CWIO_MISO
IO_L6N_T0_VREF_12	W21 USB A18
IO_L14P_T2_SRCC_12	AC23 /USB_RD
IO_L5N_T0_12	W26 USB D5
IO_L15N_T2_DQS_12	Y21 USB A12
IO_L5P_T0_12	W25 USB D6
IO_L10N_T1_12	Y26 USB D7
IO_L9N_T1_DQS_12	AC26 USB A0
IO_L18N_T2_12	AC21 USB D2
IO_L7P_T2_12	AB22 SAM_RXD0
IO_L12N_T1_MRCC_12	AA24 SAM_TXD0
IO_L13N_T2_MRCC_12	AA22 SAM_RXD1
IO_L8N_T1_12	W24 SAM_RXD1
IO_L20P_T3_12	AF24 CWIO_I04
IO_L7P_T1_12	AA25 /USB_WR
IO_L3N_T0_DQS_12	Y24 USB D3
IO_L4N_T0_12	Y26 USB D4
IO_L23N_T3_12	AE25 CWIO_I01
IO_L20N_T3_12	AF25 CWIO_I02
IO_L22N_T3_12	AF23 CWIO_I03
IO_L12P_T1_MRCC_12	Y23 USB CLK0
IO_L24P_T3_12	AE22 CWIO_TSCK
IO_L19P_T3_12	AD21 CWIO_TPDIC
IO_L22P_T3_12	AE23 CWIO_TPDID
IO_L13P_T2_MRCC_12	Y22 CWIO_HS2
IO_L25_12	Y20 CWIO_RST

XC7K160T-1FBG676C

FPGA Bank: 3.3V  
U1B

## BANK 13

IO_L19N_T3_VREF_13	IO_25_13	U16	USR_DBG_VCCDETECT
IO_L17N_T2_13	T19	PMOD1_I08	
IO_L24P_T0_13	T23	PMOD1_I06	
IO_L20N_T3_13	P24	PMOD1_I01	
IO_L2P_T0_13	N17	PMOD1_I02	
IO_L20N_T3_13	R26	PMOD1_I02	
IO_L2P_T0_13	R23	PMOD1_I03	
IO_L14N_T2_SRCC_13	T22	PMOD1_I04	
IO_L17P_T2_13	R25	PMOD1_I05	
IO_L6P_T0_13	P23	PMOD1_I07	
IO_L11P_T1_SRCC_13	M22	PMOD2_I01	
IO_L10N_T1_13	M21	PMOD2_I02	
IO_L10P_T1_13	N19	PMOD2_I03	
IO_L7P_T1_13	K25	USRLED7	
IO_L1P_T0_13	L24	USRLED6	
IO_L8N_T1_13	K26	USRLED5	
IO_L1N_T0_13	L25	USRLED4	
IO_L3N_T0_DQS_13	M19	USRLED3	
IO_L22N_T3_13	M24	USRLED2	
IO_L8P_T1_13	M25	USRLED1	
IO_L3P_T0_DQS_13	M26	USRLED0	
IO_L5N_T0_13	T24		
IO_L15P_T2_DQS_13	P26	PMOD2_I04	
IO_L2N_T0_13	N21	PLL_CLK2	
IO_L12P_T1_MRCC_13	N23	PMOD2_I05	
IO_L11N_T1_SRCC_13	N26	PMOD2_I06	
IO_L5P_T0_13	M20	PMOD2_I07	
IO_L7N_T1_13	R22	PLL_CLK1	
IO_L14P_T2_SRCC_13	T25	USB_SPARE0	
IO_L15N_T2_DQS_13	N22		
IO_L12N_T1_MRCC_13	N16	USR_DBG_TMS	
IO_0_13	P20		
IO_L9N_T1_DQS_13	P19	USRUSB_PWREN	
IO_L9P_T1_DQS_13	P25	PMOD2_I08	
IO_L6N_T0_VREF_13	U17		
IO_L23P_T3_13	U19	USR_DBG_TDAT1	
IO_L18P_T2_13	U20	USR_DBG_TDAT2	
IO_L18N_T2_13	T20	USR_DBG_TDAT3	
IO_L16P_T2_13	R20	USR_DBG_NCO	
IO_L16N_T2_13	P21	USR_DBG_TDATO	
IO_L13N_T2_MRCC_13	T18		
IO_L19P_T3_13	R21	USR_DBG_TRACECLK	
IO_L13P_T2_MRCC_13	N18	USR_DBG_TCK	
IO_L22P_T3_13	P16	USR_DBG_TDO	
IO_L20P_T3_13	R16	USR_DBG_TDI	
IO_L21P_T3_DQS_13	T17	USR_DBG_nRST	
IO_L23N_T3_13	N24	VDDR_ENABLE	
IO_L4N_T0_13	R18	VDDR_PGOOD	
IO_L24P_T3_13	P18	USRUSB_VBUS_DETECT	
IO_L24N_T3_13	R17		

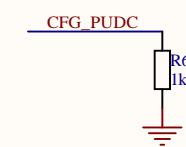
XC7K160T-1FBG676C

FPGA Bank: 3.3V, Configuration, SRAM  
U1C

## BANK 14

IO_L1P_T0_D00_MOSI_14	K21	CFG_SPI_MOSI
IO_L1N_T0_D01_DIN_14	B24	CFG_SER_DIN
IO_L2P_T0_D02_14	A25	USB_CLK1_SPARE
IO_L2N_T0_D03_14	B22	USB_SPI_CPO
IO_L3P_T0_DQS_PUDC_B_14	B25	CFG_PUDC
IO_L3N_T0_DQS_EMCCLK_14	B26	CFG_EMCCLK
IO_L4P_T0_D04_14	A23	USB_SPARE3
IO_L4N_T0_D05_14	A24	USB_SPI_COPI
IO_L5P_T0_D06_14	C26	USB_SPI_SCK
IO_L5N_T0_D07_14	C23	CFG_SPI_CS
IO_L6P_T0_FCS_B_14	H21	SRAM_A12
IO_L19P_T3_A10_D26_14	E23	SRAM_A13
IO_L12N_T1_MRCC_14	H22	SRAM_A14
IO_L9N_T1_DQS_D13_14	E22	SRAM_A15
IO_L20P_T3_A08_D24_14	H23	SRAM_A16
IO_L20N_T3_A07_D23_14	H24	SRAM_A17
IO_L18P_T2_A12_D28_14	H26	SRAM_A18
IO_L18N_T2_A11_D27_14	L23	SRAM_A20
IO_25_14	J24	SRAM_DQ0
IO_L22P_T3_A05_D21_14	E26	SRAM_DQ1
IO_L17N_T2_A13_D29_14	K23	SRAM_DQ2
IO_L24P_T3_A01_D17_14	D21	SRAM_DQ3
IO_L7P_T1_D09_14	C24	SRAM_DQ4
IO_L6N_T0_D08_VREF_14	D24	SRAM_DQ5
IO_L11N_T1_SRCC_14	D23	SRAM_DQ6
IO_L11P_T1_SRCC_14	C22	SRAM_DQ7
IO_L7N_T1_D10_14	F25	USB_SPARE2
IO_L15P_T2_DQS_RDWR_B_14	D25	CFG_SER_DOUT
IO_L15N_T2_DQS_DOUT_CSO_B_14	G25	USB_SPARE1
IO_L16P_T2_CSI_B_14	F23	SRAM_A0
IO_L13N_T2_MRCC_14	F25	SRAM_A1
IO_L12P_T2_A14_D30_14	G24	SRAM_A2
IO_L14P_T2_SRCC_14	F22	SRAM_A3
IO_L12P_T1_MRCC_14	G21	SRAM_A4
IO_L19N_T3_A09_D25_VREF_14	B20	SRAM_A5
IO_L8P_T1_D11_14	A20	SRAM_A6
IO_L8N_T1_D12_14	K22	SRAM_A7
IO_L23N_T3_A02_D18_14	B21	SRAM_A8
IO_L10N_T1_D15_14	E21	SRAM_A9
IO_L9P_T1_DQS_14	G22	SRAM_A10
IO_L13P_T2_MRCC_14	F24	SRAM_A11
IO_L14N_T2_SRCC_14	J25	
IO_L22N_T3_A04_D20_14	J22	
IO_L23P_T3_A03_D19_14	J21	SRAM_CE2
IO_L16N_T2_A15_D31_14	G26	SRAM_CE
IO_L24N_T3_A00_D16_14	J23	SRAM_WE
IO_L10P_T1_D14_14	C21	SRAM_OEn

XC7K160T-1FBG676C



Title: Kintex IO Banks

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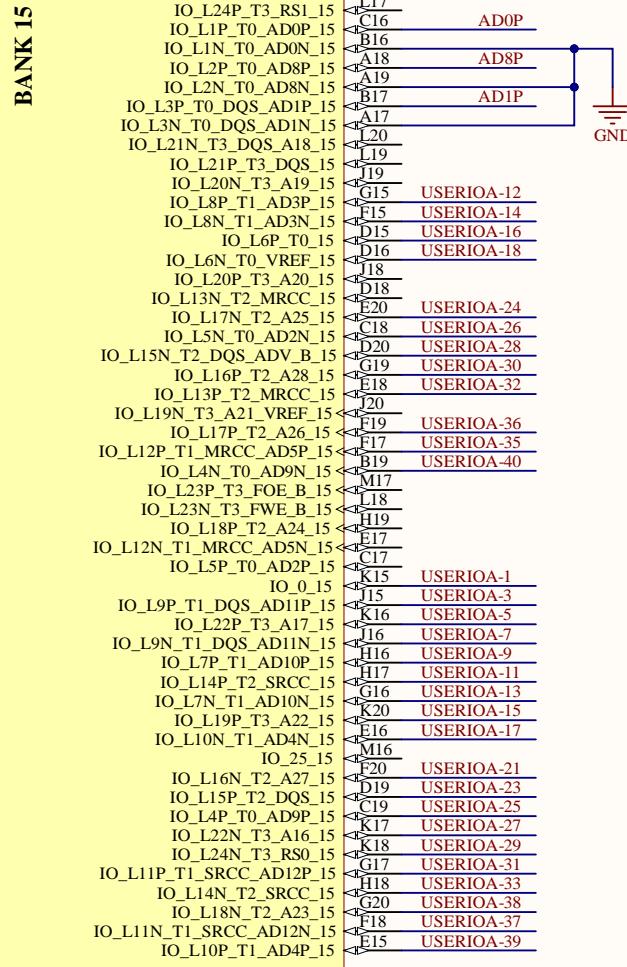
File: CW310\_FPGAIO\_1.SchDoc

Approved: Yes

NewAE  
Technology

## FPGA Bank: VCCIOA

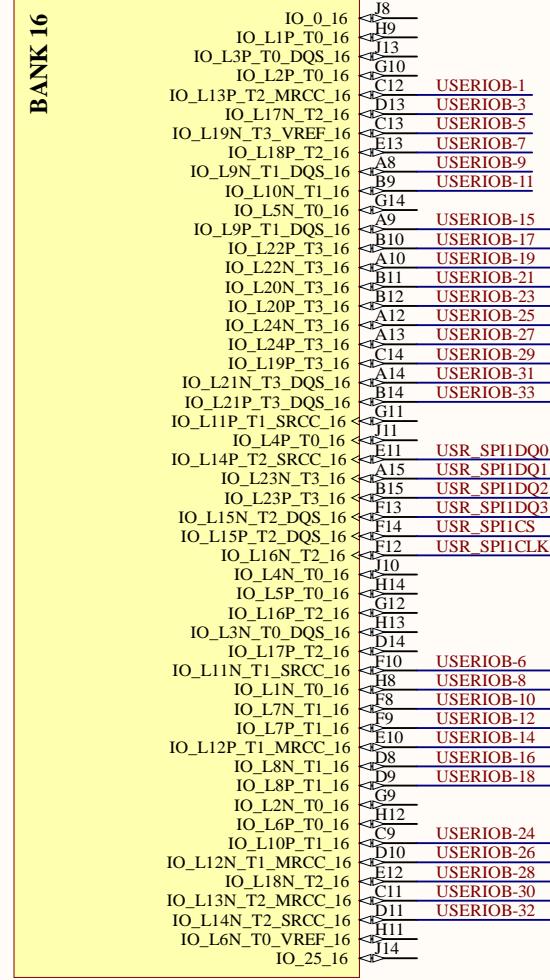
U1D



XC7K160T-1FBG676C

## FPGA Bank: VCCIOB

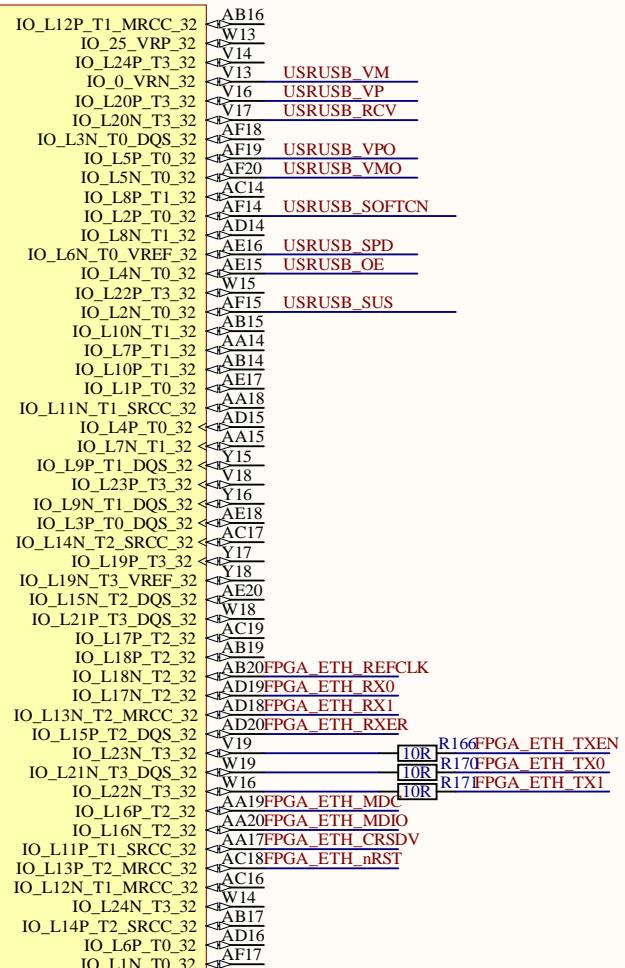
U1E



XC7K160T-1FBG676C

## FPGA Bank: 1.8V (HP Bank)

U1F



XC7K160T-1FBG676C

A

A

B

B

C

C

D

D

BANK 15

BANK 16

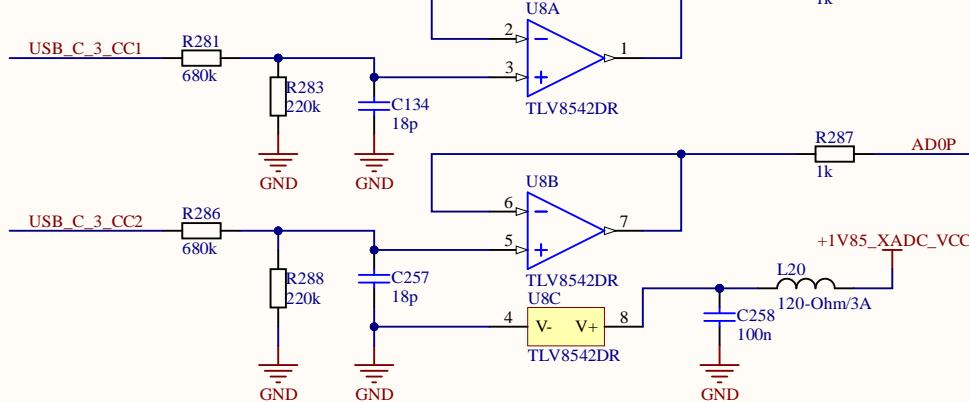
BANK 32

1

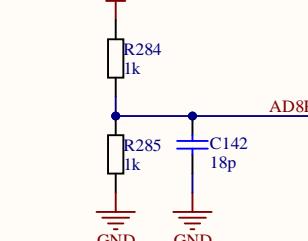
2

3

4



+1V0\_VCCINT\_SHUNTLLOW



Title: Kintex IO Banks

Approved: Yes



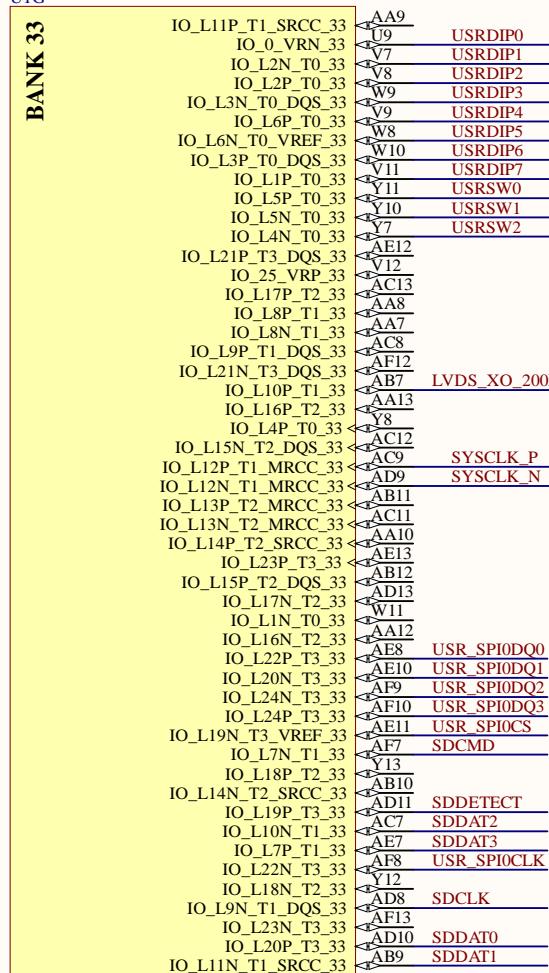
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FPGA Bank: 1.8V (HP Bank)

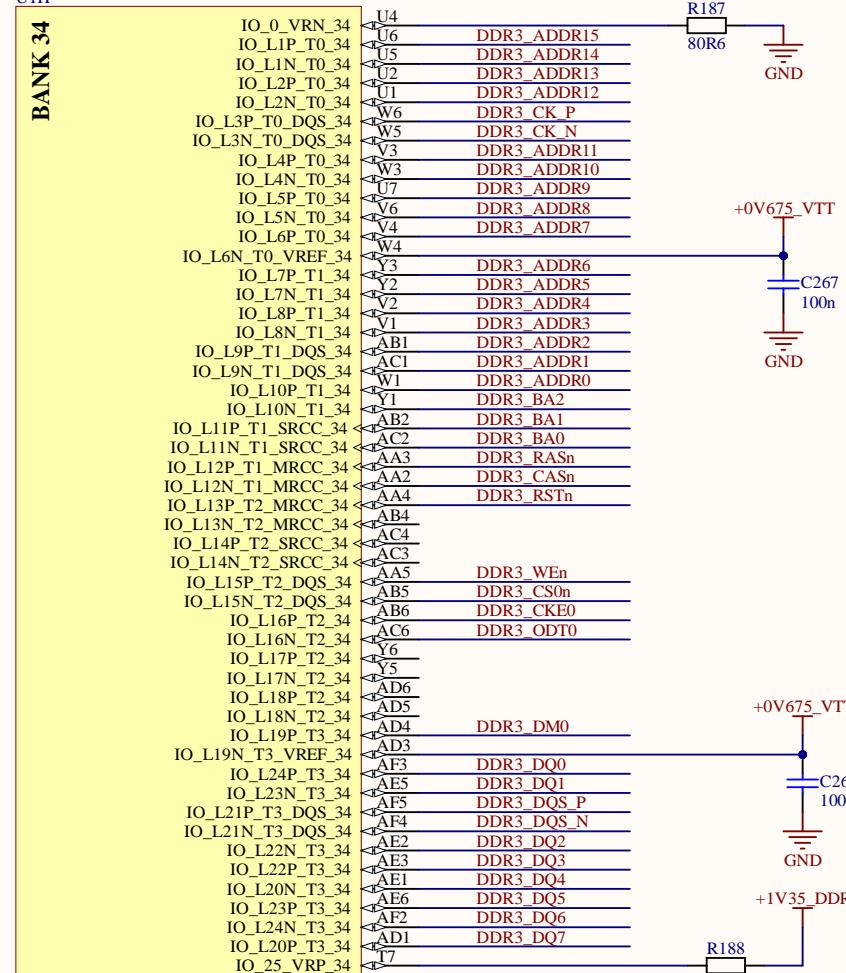
U1G



XC7K160T-1FBG676C

FPGA Bank: DDR3, 1.35V (HP Bank)

U1H



XC7K160T-1FBG676C

Title: Kintex IO Banks

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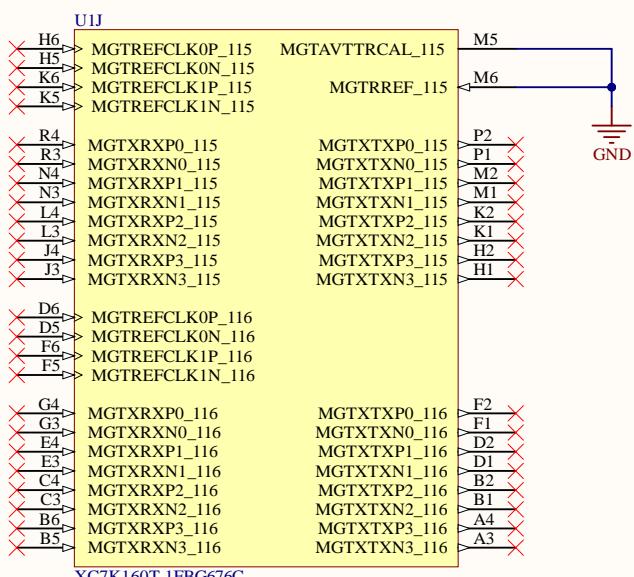
File: CW310\_FPGAIO\_3.SchDoc

Approved: Yes



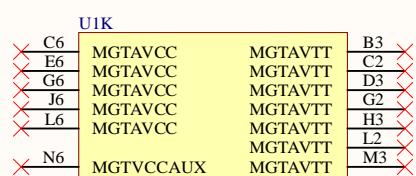
# FPGA MGT Interface

A



B

A



C

B

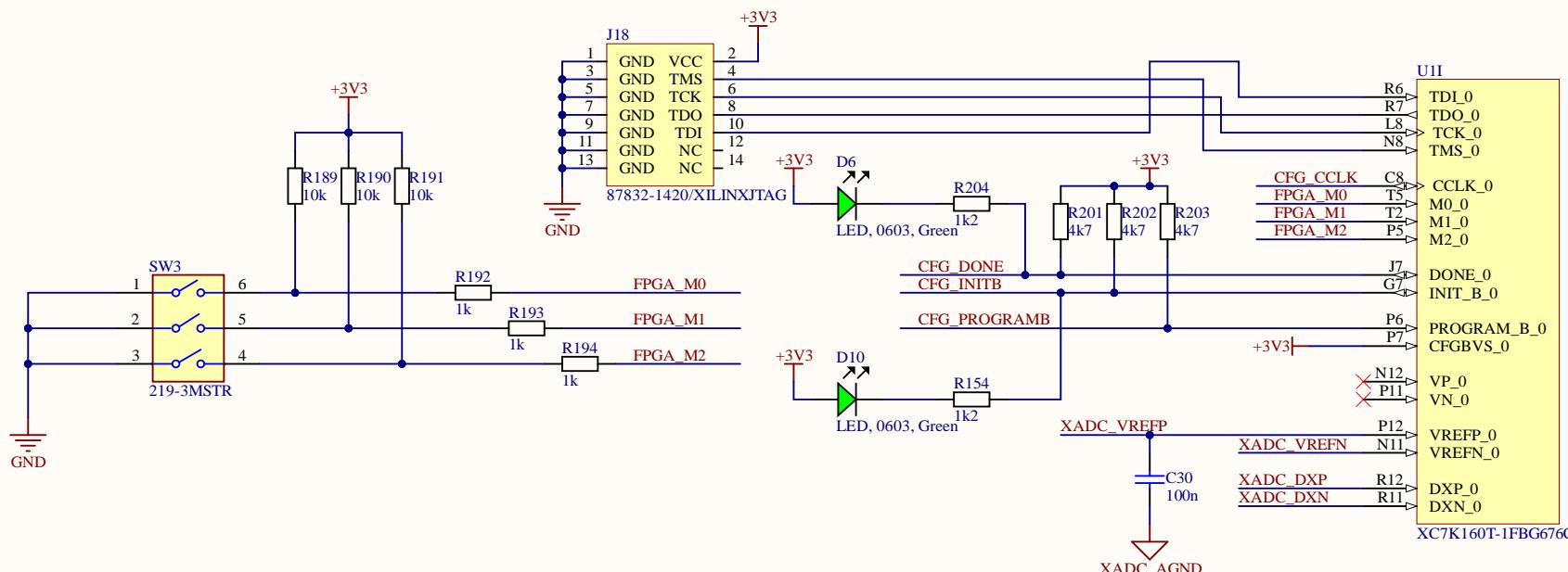
D

C

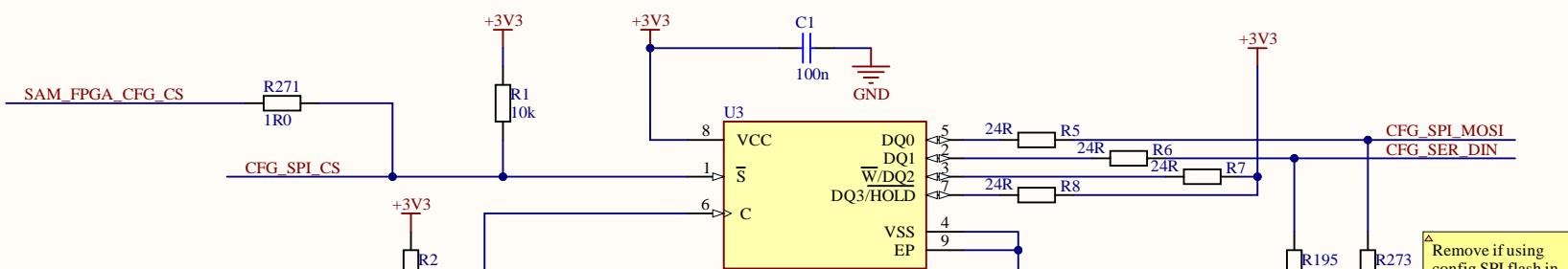
D

Title: <b>Kintex MGT Tiles</b>		Approved: Yes	NewAE Technology
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A

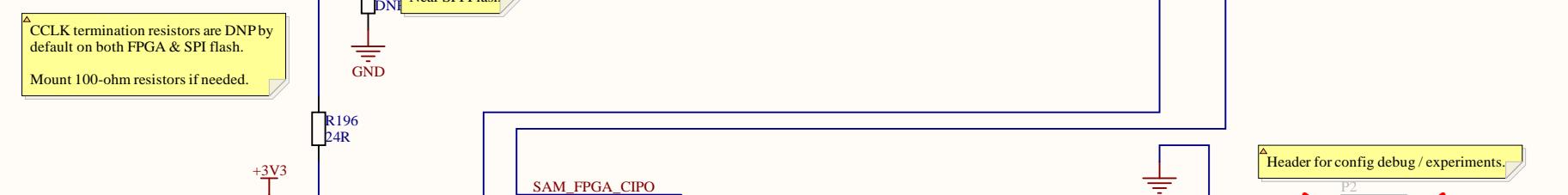


B



C

△ CCLK termination resistors are DNP by default on both FPGA & SPI flash.  
Mount 100-ohm resistors if needed.



D



### Title: Kintex Configuration

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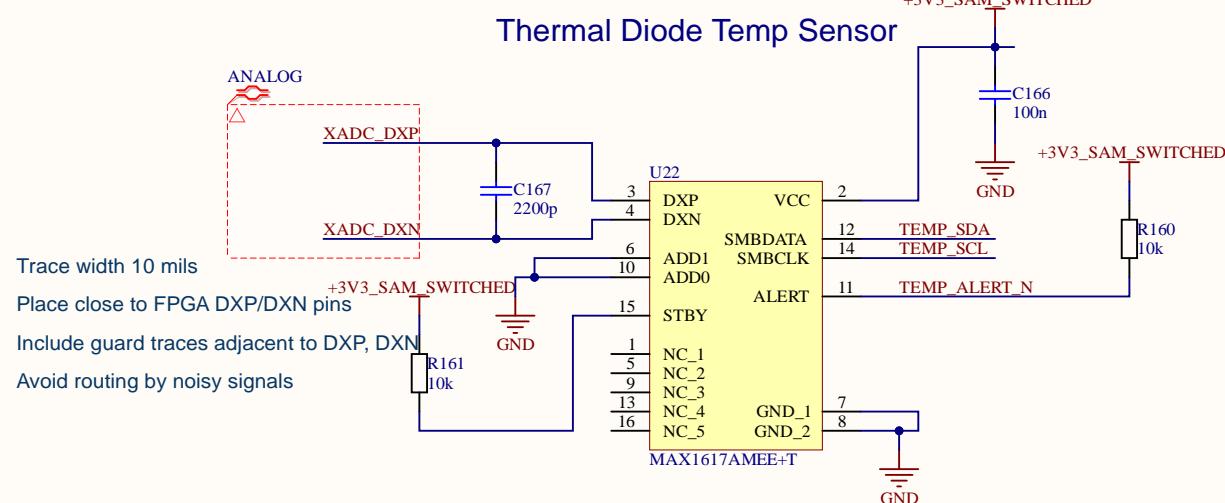
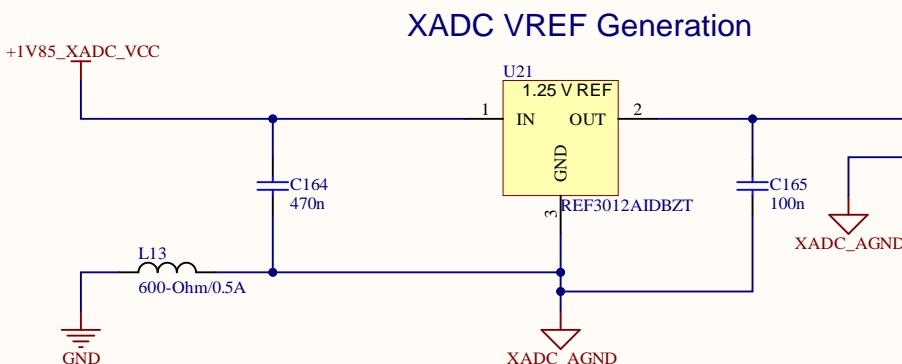
File: CW310\_FPGA\_CFG.SchDoc

Approved: YES



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# FPGA XADC POWER

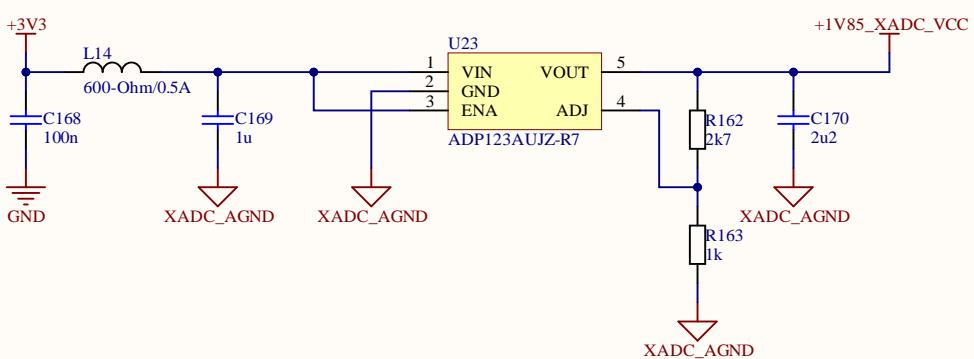


I2C Address = 0x18

Temperature diode ideality factor = 1.010

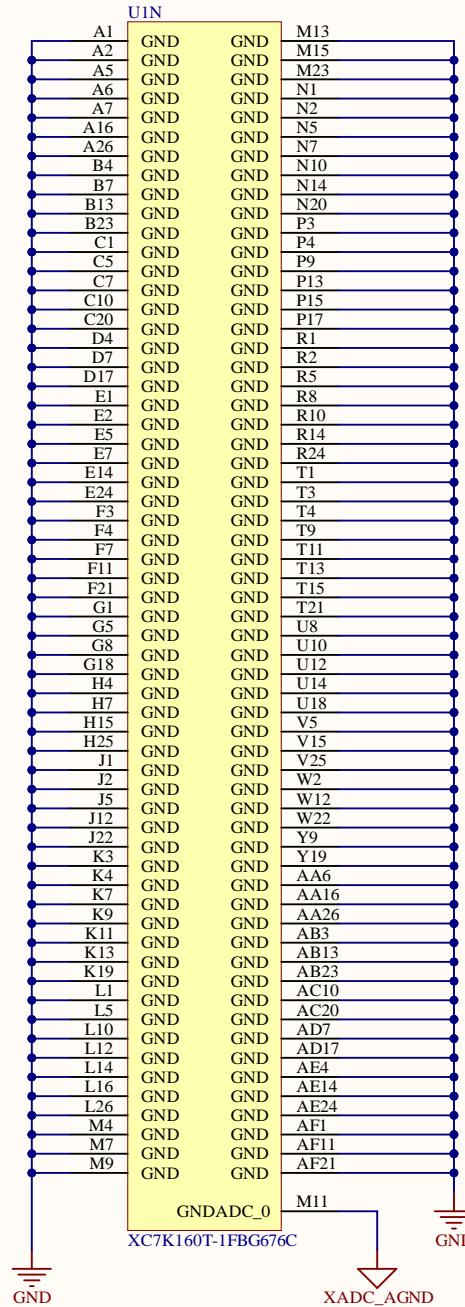
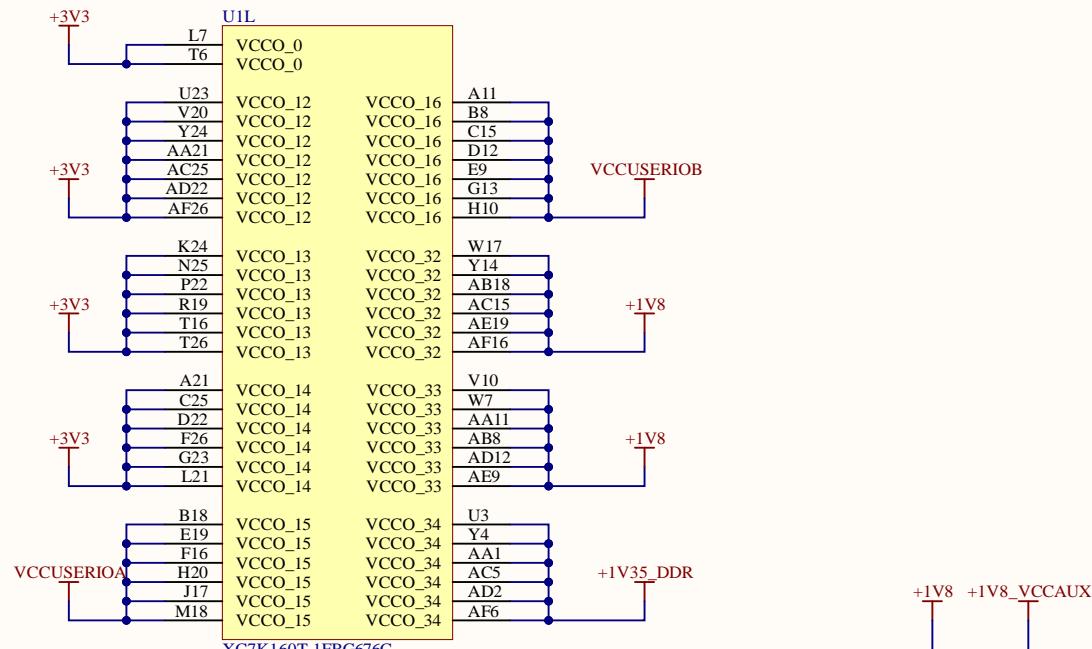
Temperature diode series resistance = 2

## XADC VCC Generation



Title: <b>FPGA - Thermal + XADC</b>		Approved: Yes	NewAE Technology
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# FPGA POWER



Title: **Kintex Power Connections** Approved: YES

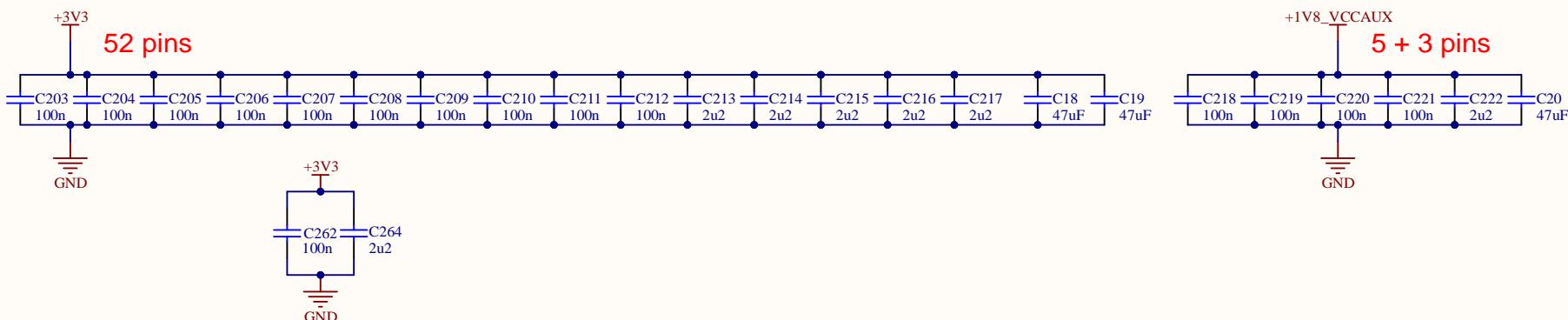
Rev: 06 Project: **BERGENBOARD** License: NewAE

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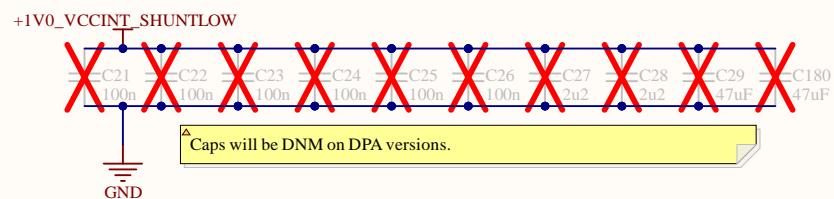
File: CW310\_FPGA\_PWR.SchDoc

# FPGA Decoupling

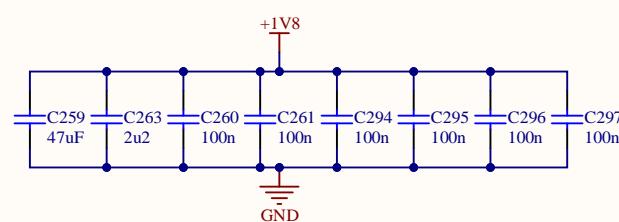
A



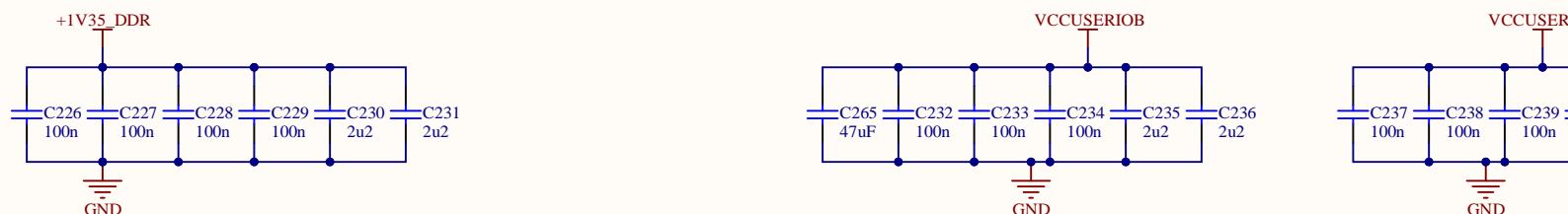
A



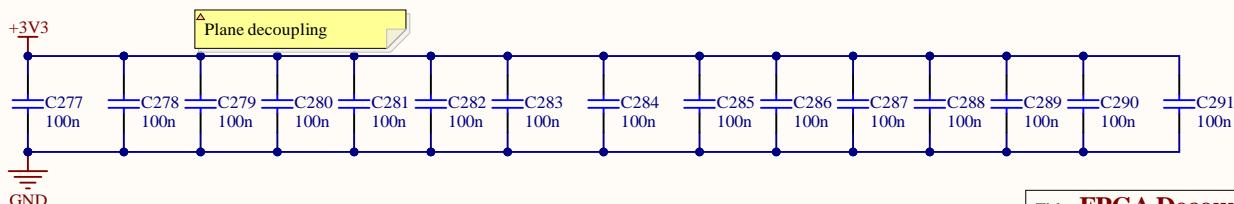
B



C



C



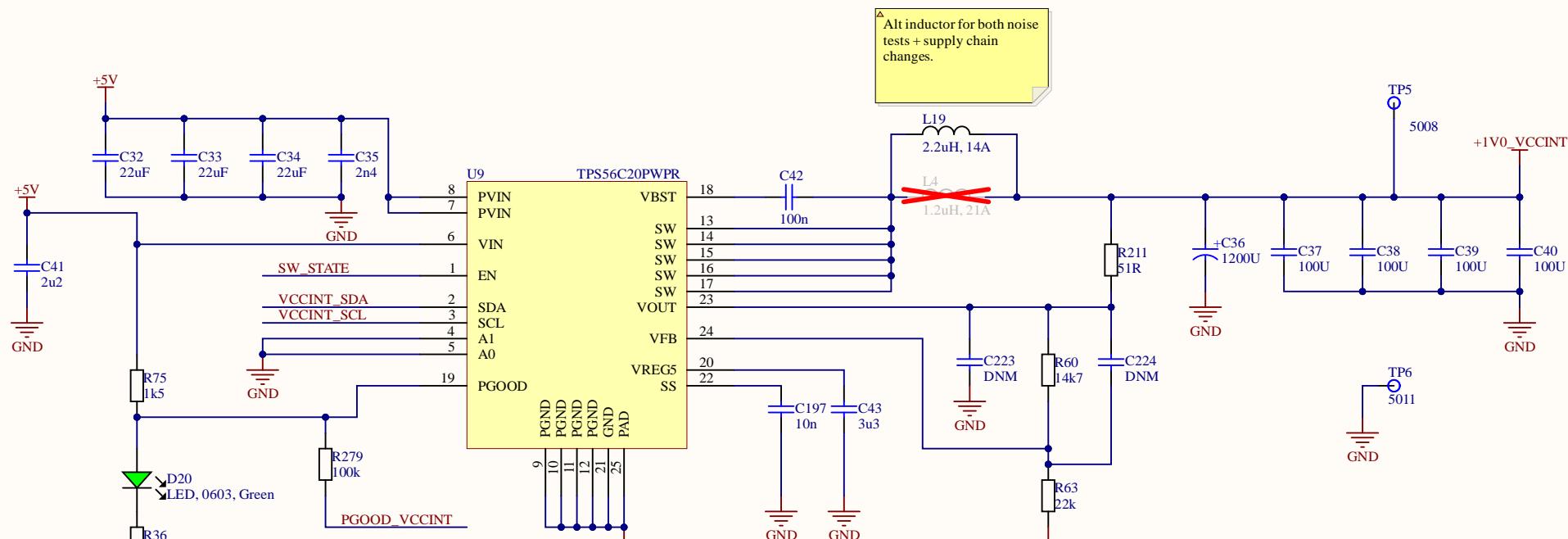
D

Title: <b>FPGA Decoupling</b>		Approved: Yes	
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File: CW310_FPGA_DECOUP.SchDoc			

# FPGA VCCINT Power Generation / Control

A

A



B

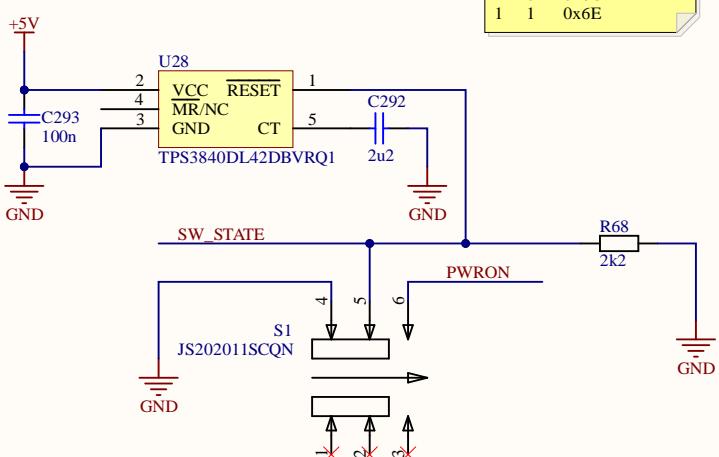
B

C

C

D

D



Title: <b>VCCINT Variable PSU</b>		Approved: YES	NewAE Technology
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Date: 2021-03-30	Time: 5:33:45 PM	Sheet 20 of 31	Copyright © NewAE Technology Inc.   NewAE.com
File: CW310_PSU_VCCINT.SchDoc			

A

A

B

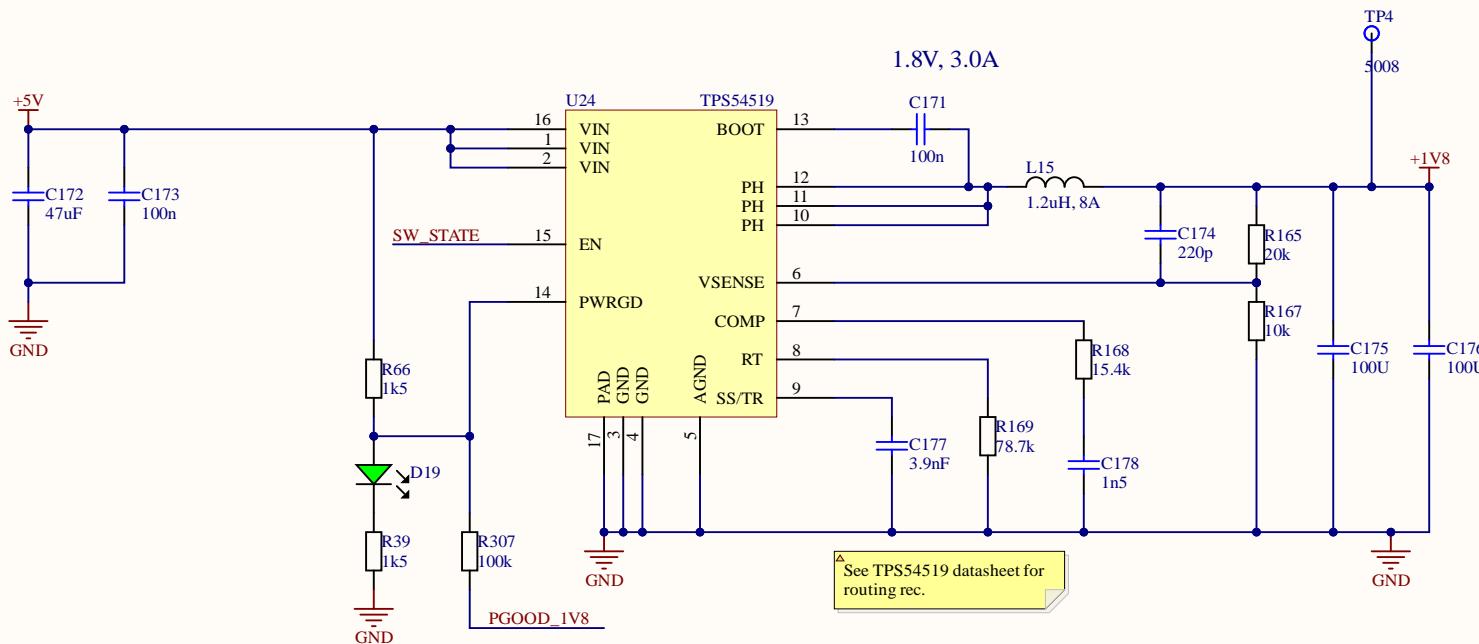
B

C

C

D

D



Title: VCC-AUX SMPS

Approved: YES

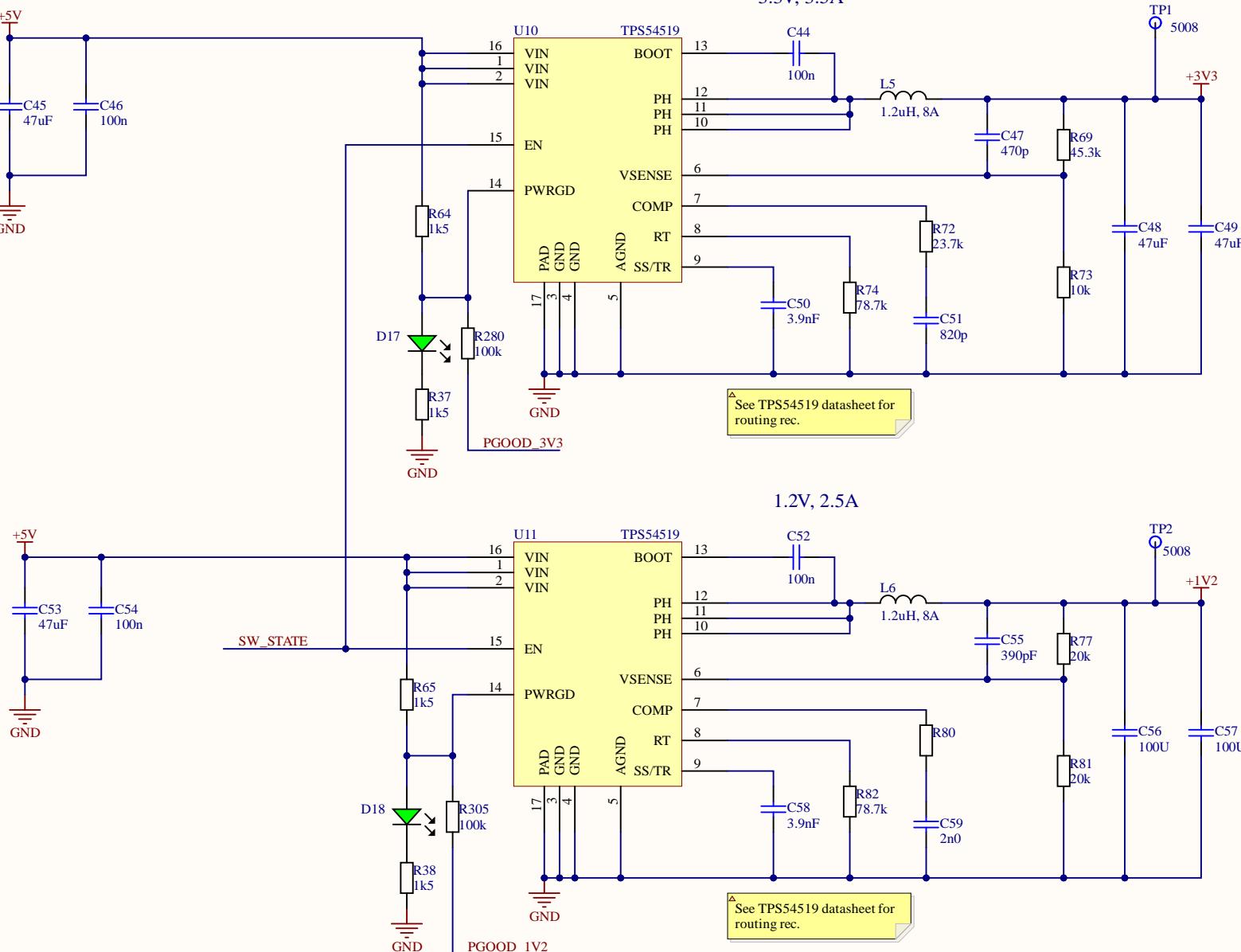


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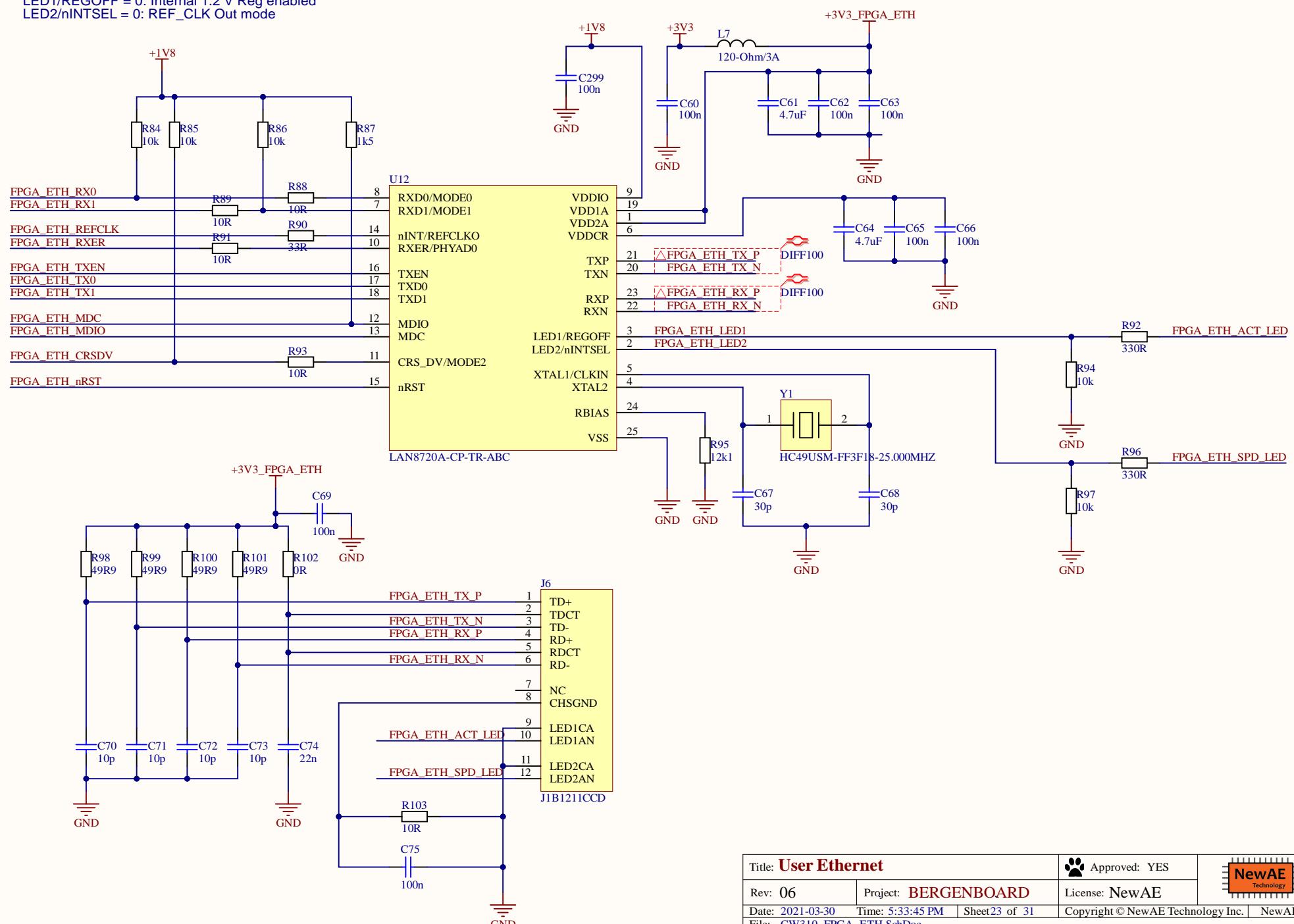
File: CW310\_PSU\_VCCAUX.SchDoc



# FPGA Ethernet

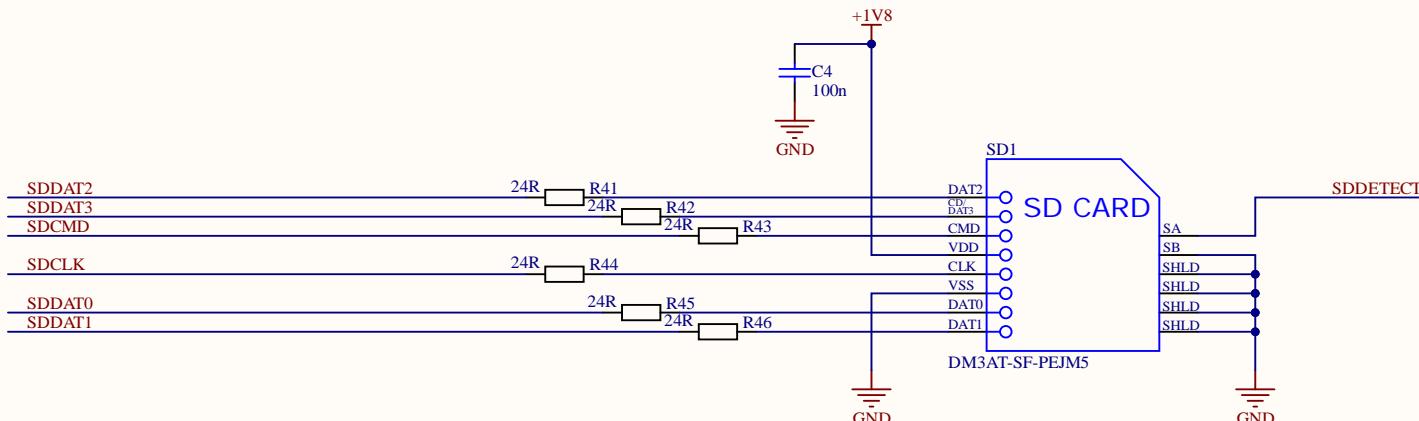
## LAN8720 PHY Configuration

PHYAD0 = 0: Phy Address 0  
 CRS\_DV/MODE2 = 1: All modes, autonegotiation enabled  
 RXD1/MODE1 = 1  
 RXD0/MODE0 = 1  
 LED1/REGOFF = 0: Internal 1.2 V Reg enabled  
 LED2/nINTSEL = 0: REF\_CLK Out mode



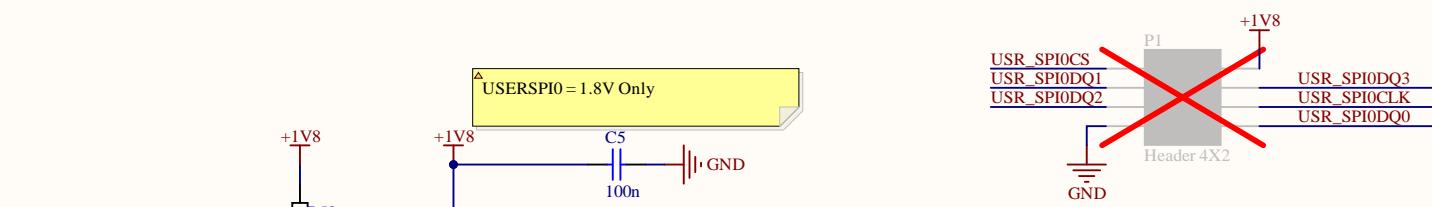
Title: User Ethernet		Approved: YES	NewAE Technology
Rev: 06	Project: BERGENBOARD	License: NewAE	
Date: 2021-03-30	Time: 5:33:45 PM	Sheet 23 of 31	Copyright © NewAE Technology Inc.   NewAE.com
File: CW310_FPGA_ETH.SchDoc			

A



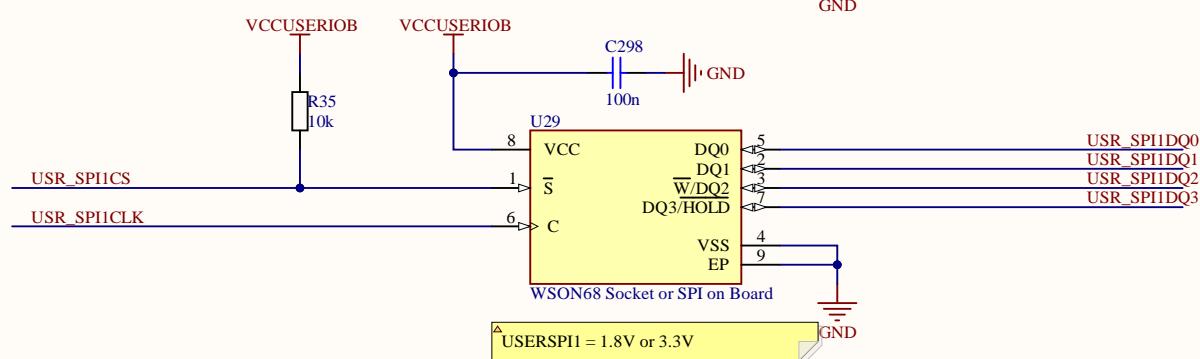
A

B



B

C



C

D

Title: User SPI Flash + SD Card

Approved: Yes



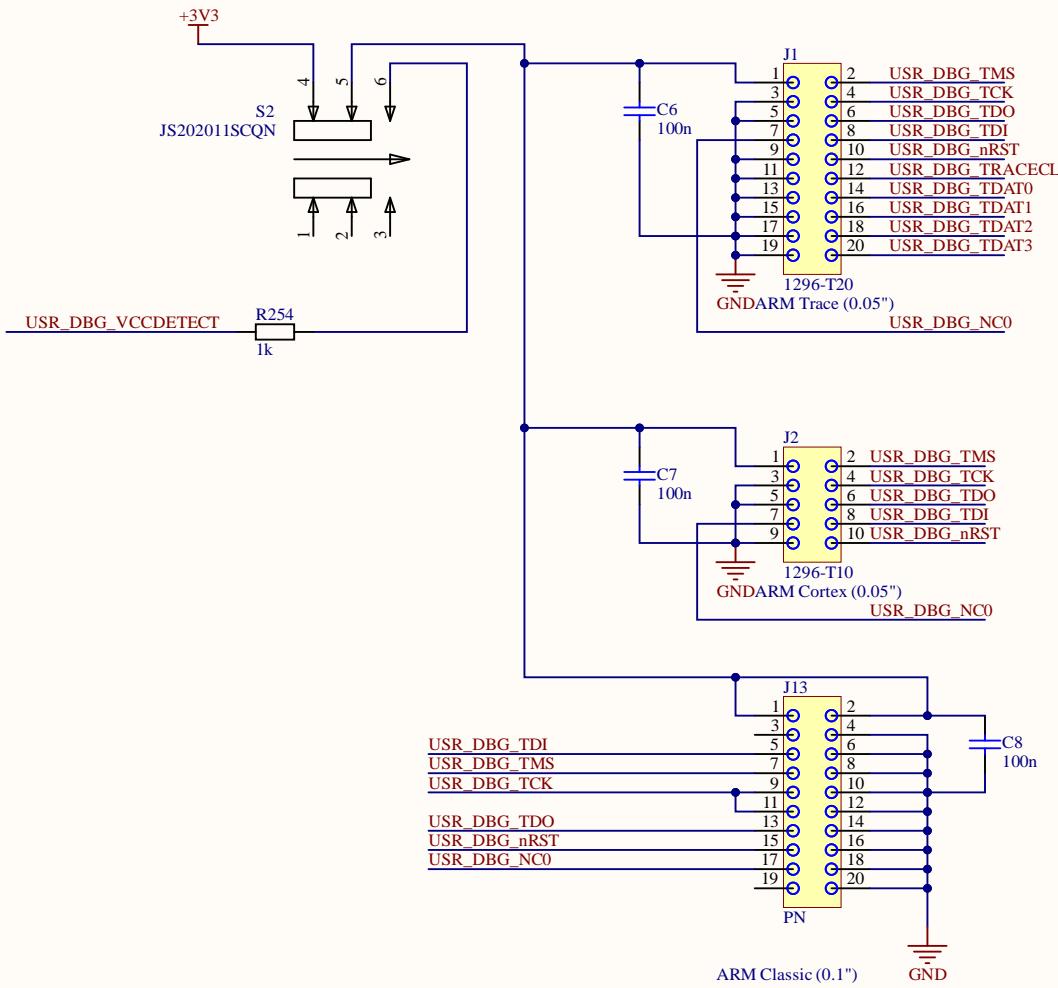
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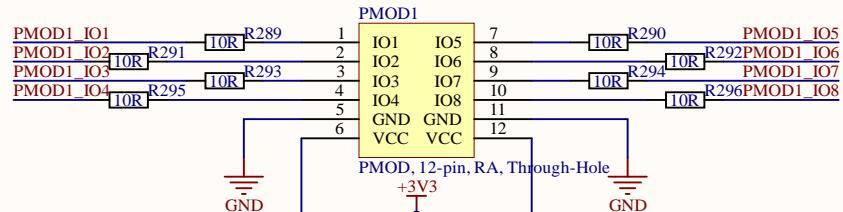
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File: CW310\_SPI\_flashes.SchDoc

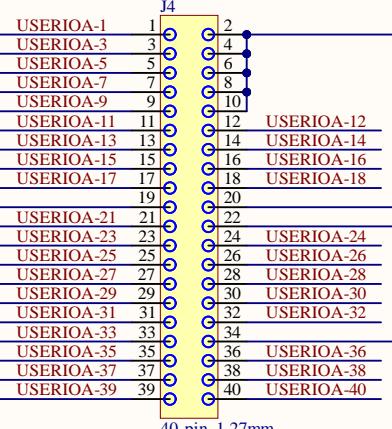


Title: <b>User Debug Headers</b>		Approved: Yes	NewAE Technology
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File: CW310_USERIO_debug.SchDoc			

A



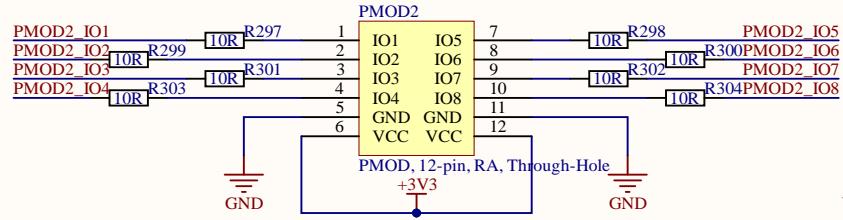
VCCUSERIOA



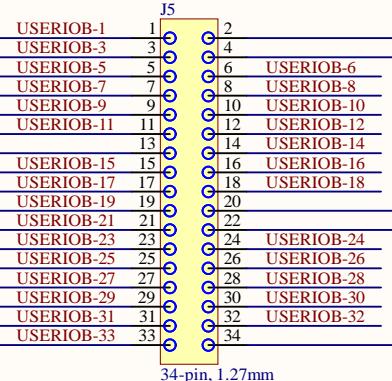
+3V3

GND

B



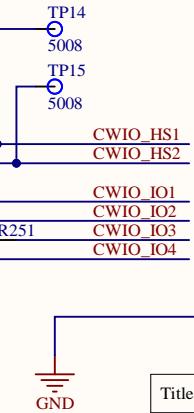
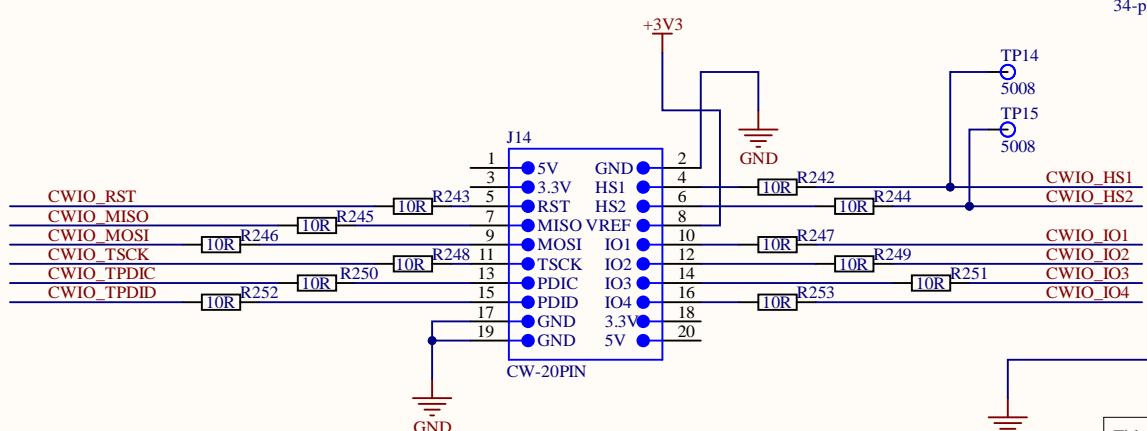
VCCUSERIOB



+3V3

GND

C



VCCUSERIOB

Header 3X2

**Title: User GPIO Headers**

Approved: Yes



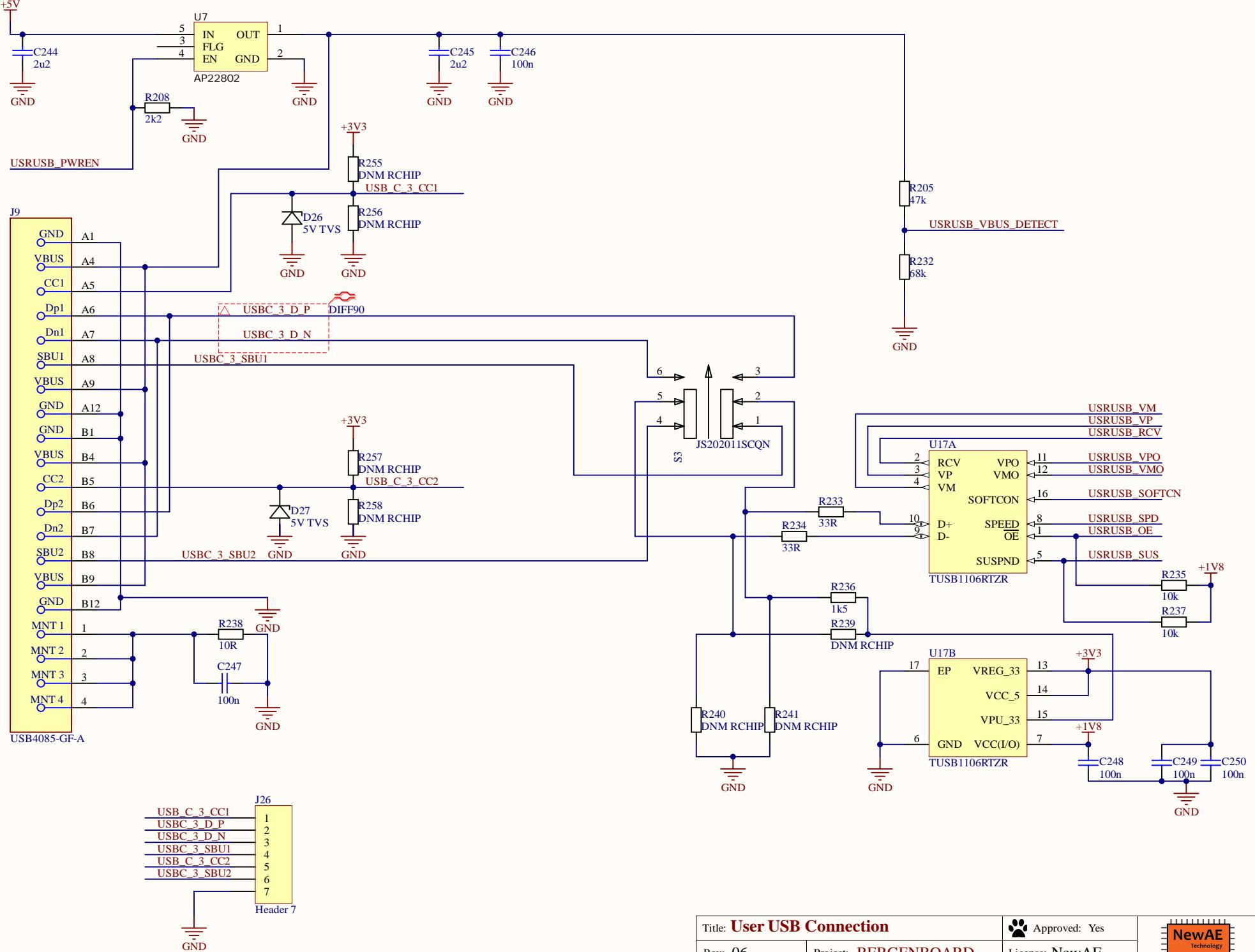
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File: CW310\_USERIO\_Header.SchDoc



Title: **User USB Connection**

Approved: Yes



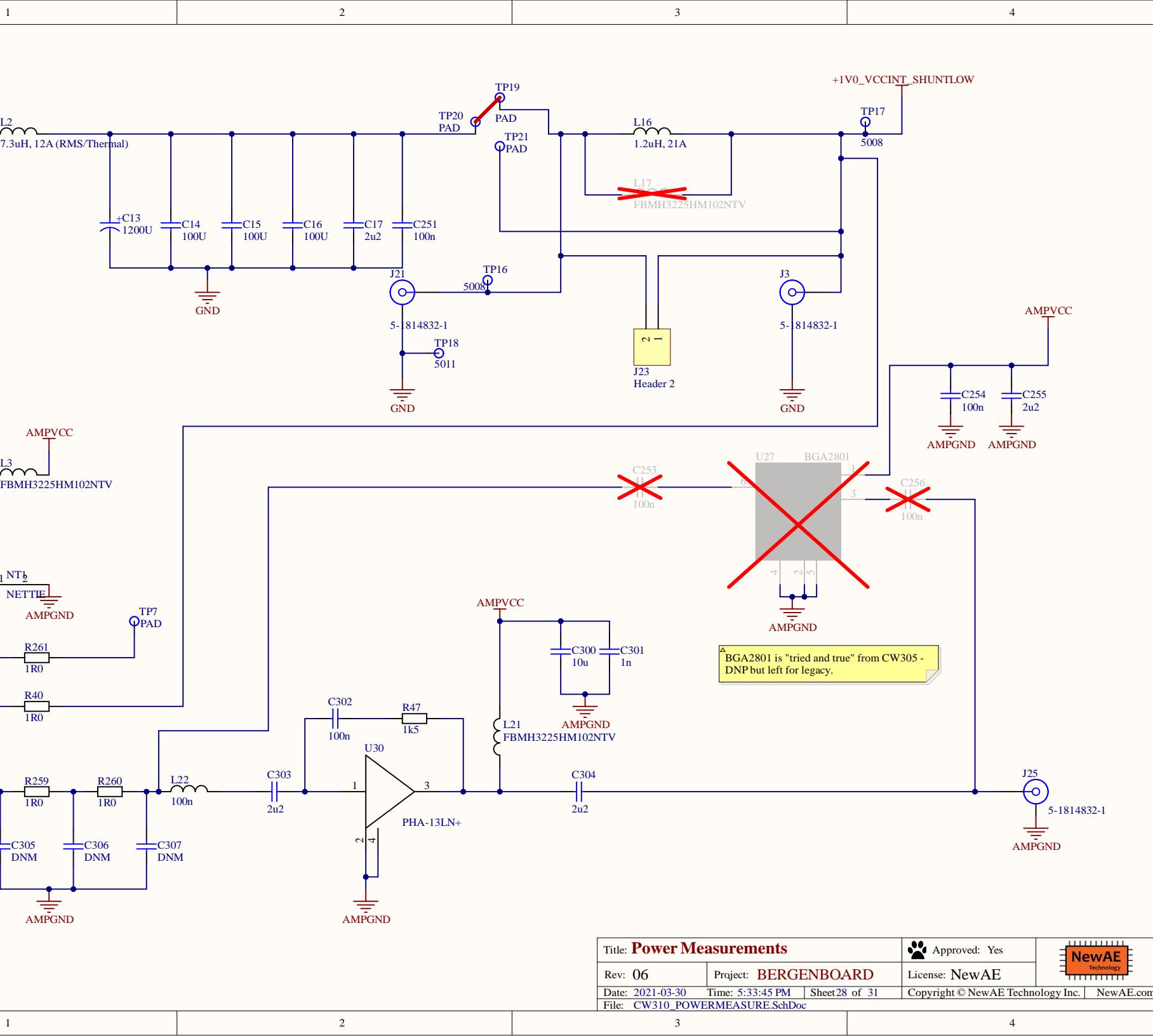
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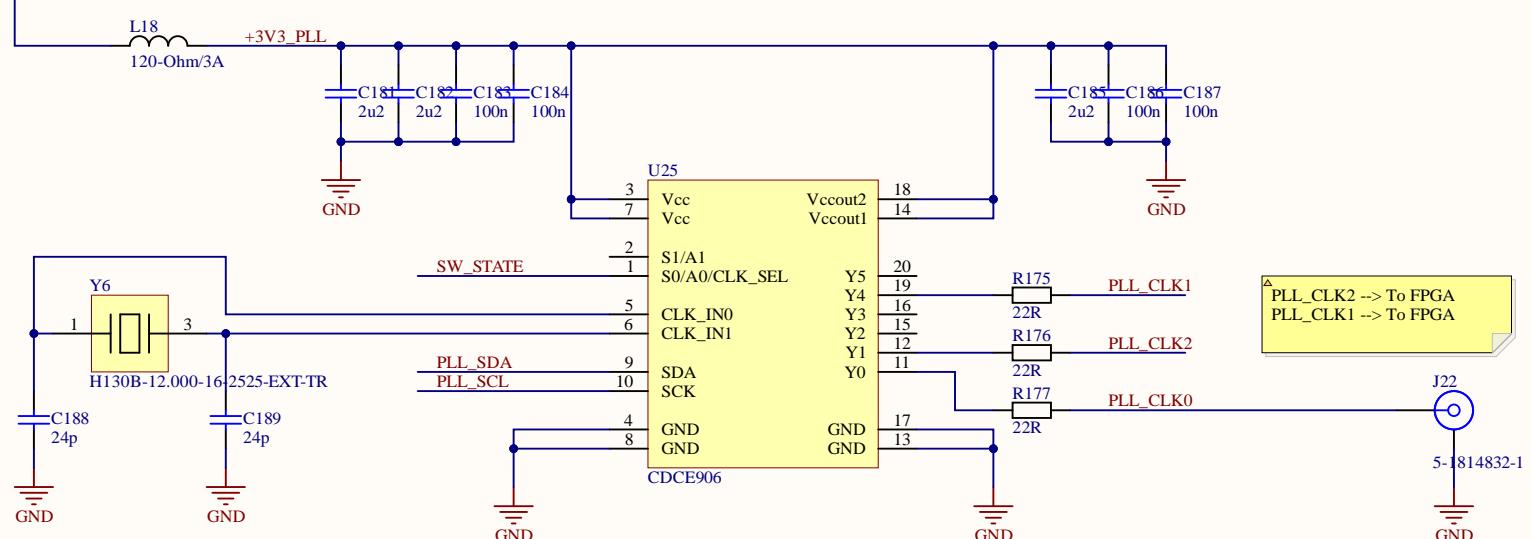
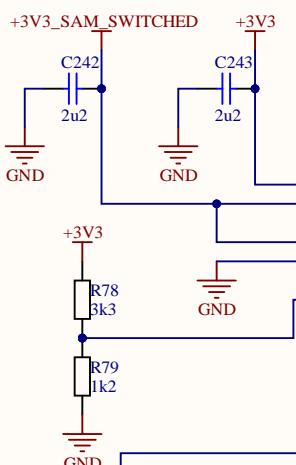
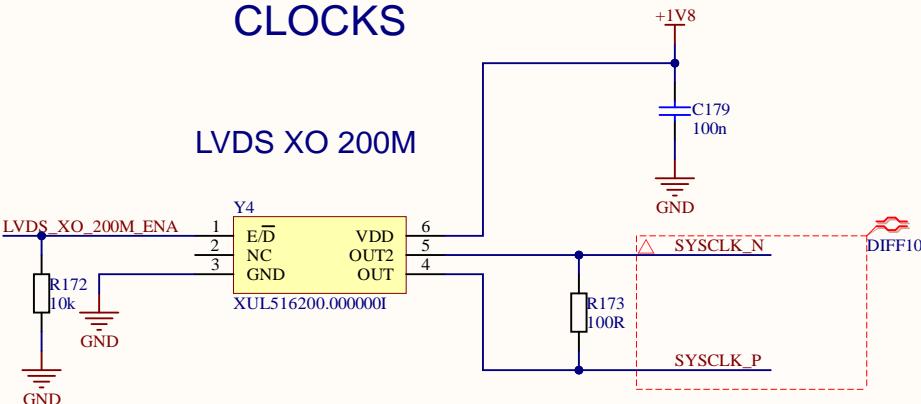
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File: CW310\_USERIO\_USB.SchDoc



# CLOCKS

## LVDS XO 200M



Title: PLL, Clocks for FPGA

Approved: Yes



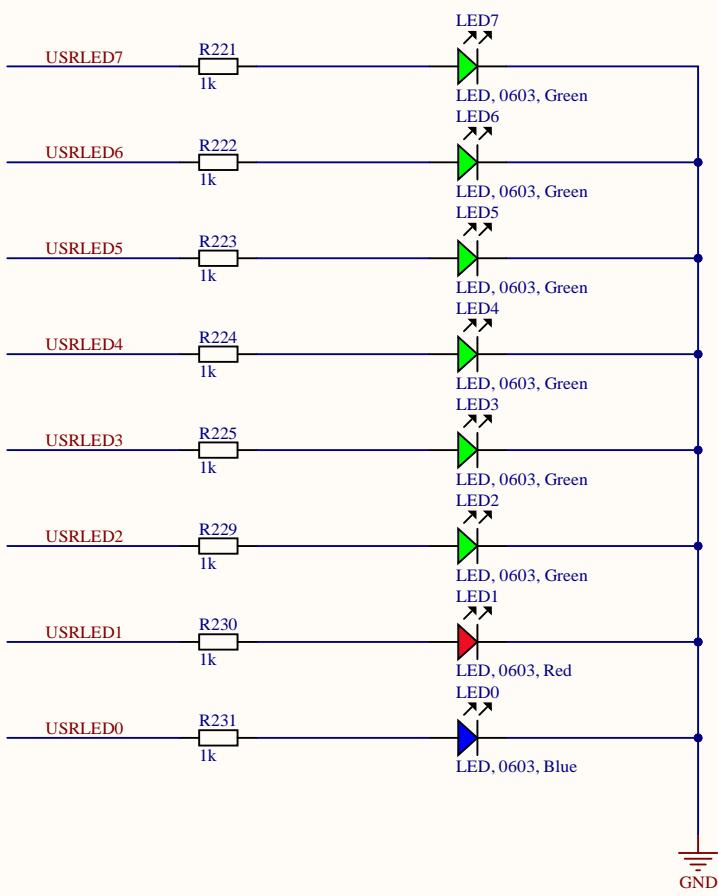
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File: CW310\_Clocks.SchDoc

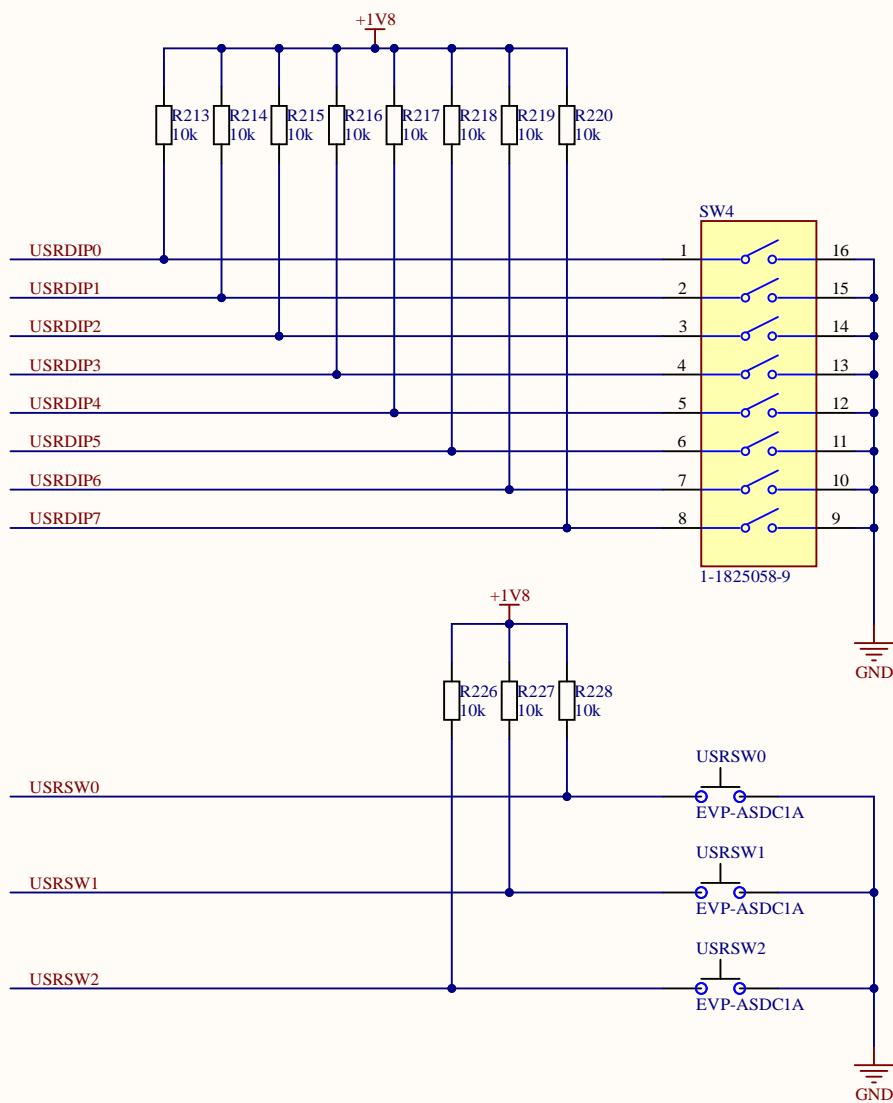
A



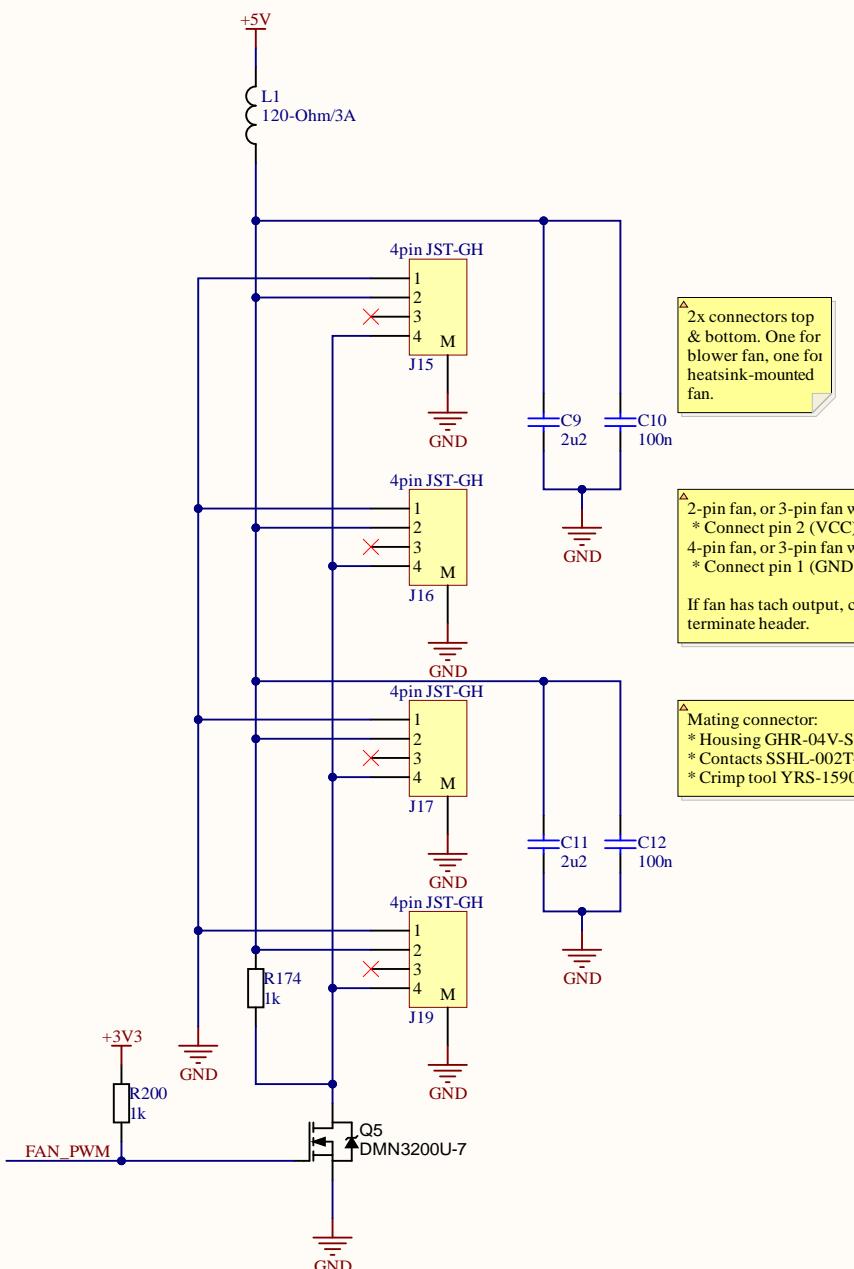
B

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D

D



△ Fan mounted top or bottom side of board. Blower style to pass over "open die top".

Blower Fan, 5V, 35x35mm

△ Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.



Title: <b>FAN Headers</b>		Approved: Yes	NewAE Technology
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File: CW310_HEATSINK_FAN.SchDoc			