

ChipWhisperer CW310 "Bergen Board" - Xilinx Kintex 7 Target Board

NewAE Technology Inc.

Suggested Layer Stack



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Change/add page numbers here,
when finished rename .SchDoc files
in form "[pg #] CW310_Group_Function"

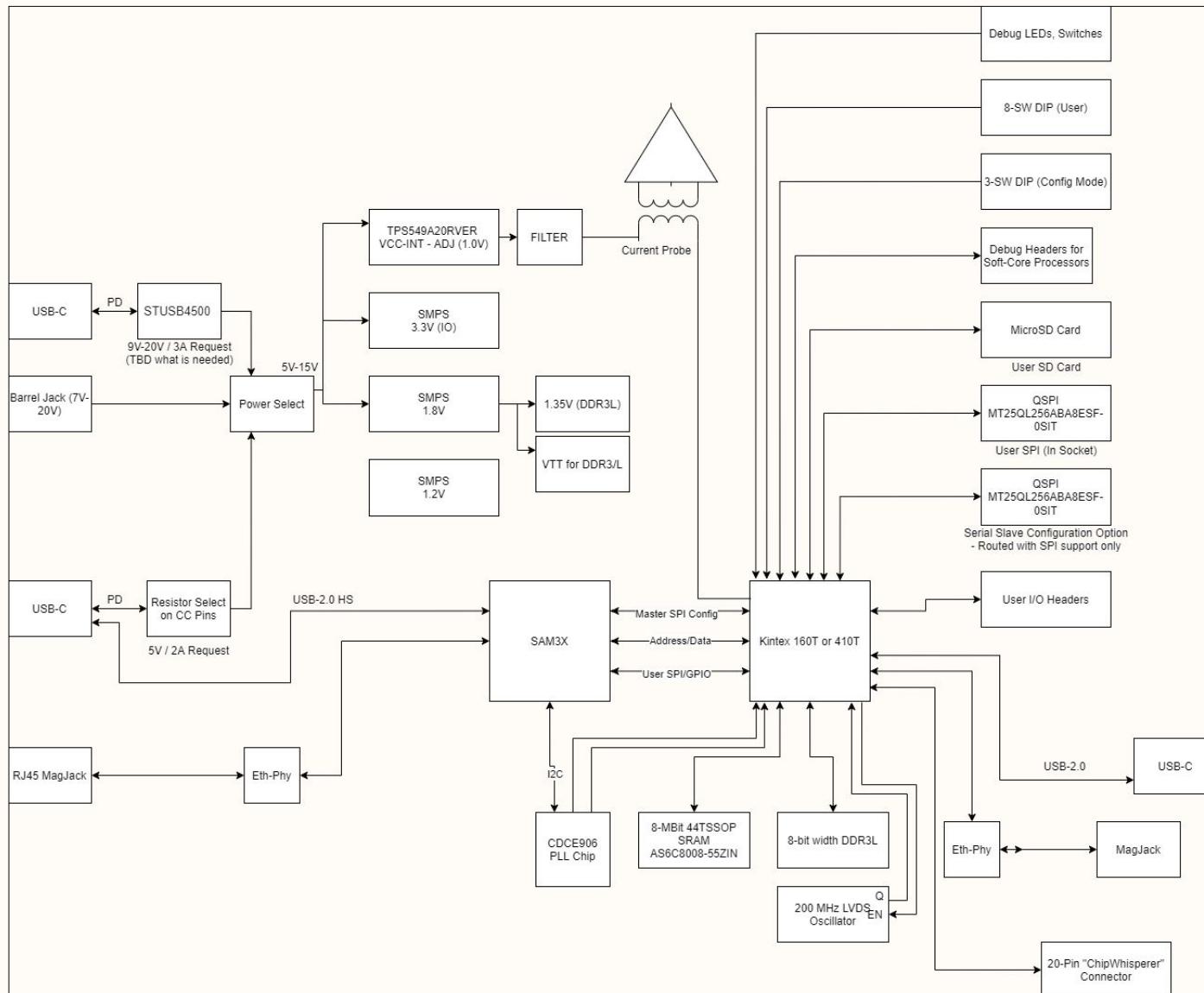
Status: Draft

Revision Summary

- 00: Ultra-alpha.
- 01: Super-alpha.
- 02: March 10/2021 Feature complete.
- 03: March 13/2021 Internal release.
- 04: March 15/2021 Add brown-out on 5V, silkscreen updates

Title: Bergen Board - The Cover Sheet		Approved:	
Rev: 04	Project: BERGENBOARD	License: TBD	
Date: 2021-03-15	Time: 10:18:15 AM	Sheet 1 of 27	Copyright © NewAE Technology Inc. NewAE.com
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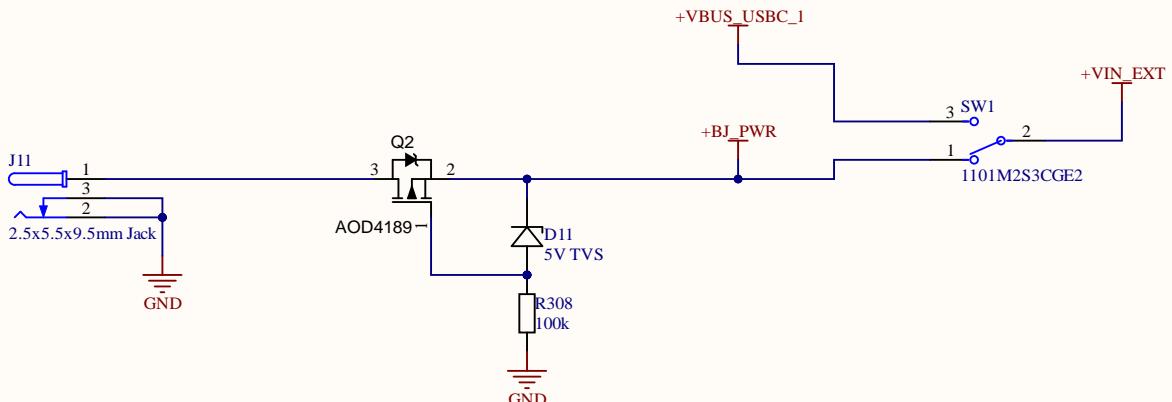
Block Diagram



INPUT POWER

A

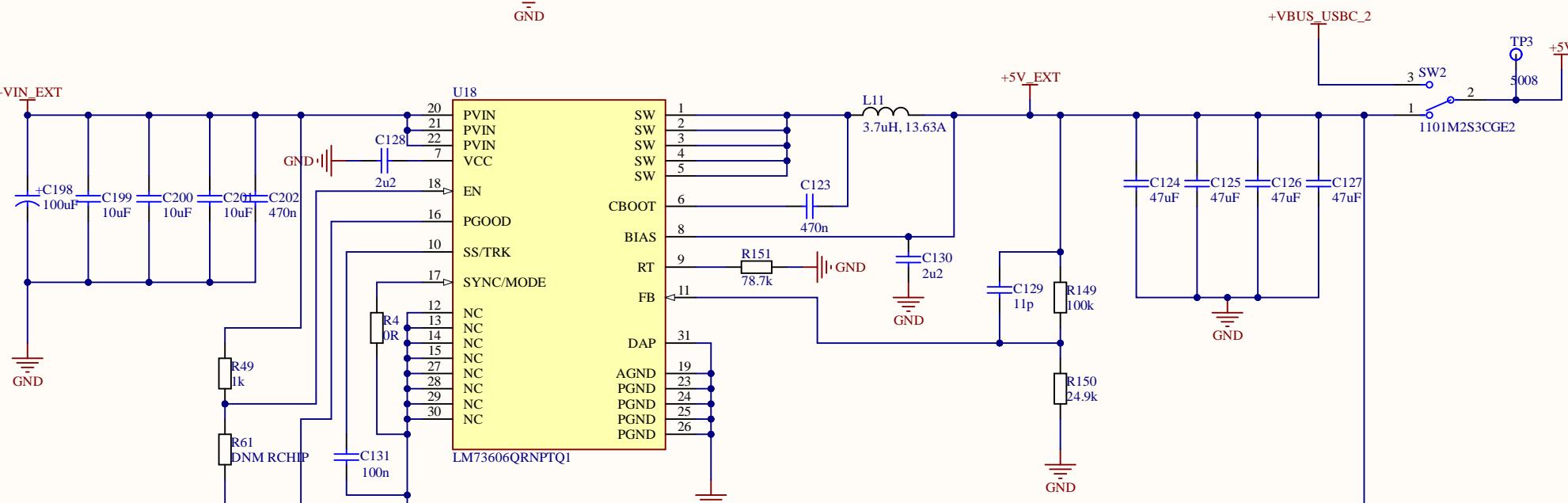
A



[△] To check:
 * VBUS_USBC_2 should be inrush controlled & switched from SAM3X probably.
 * Auto-switch 5V source - is that useful or keep with manual?

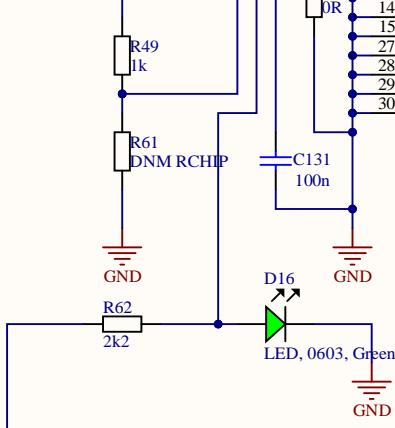
B

B



C

C



[△] Based on design from
<https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=9C49F428E2C4FF82>

D

D

Title: **5V Regulator**

Approved: NO



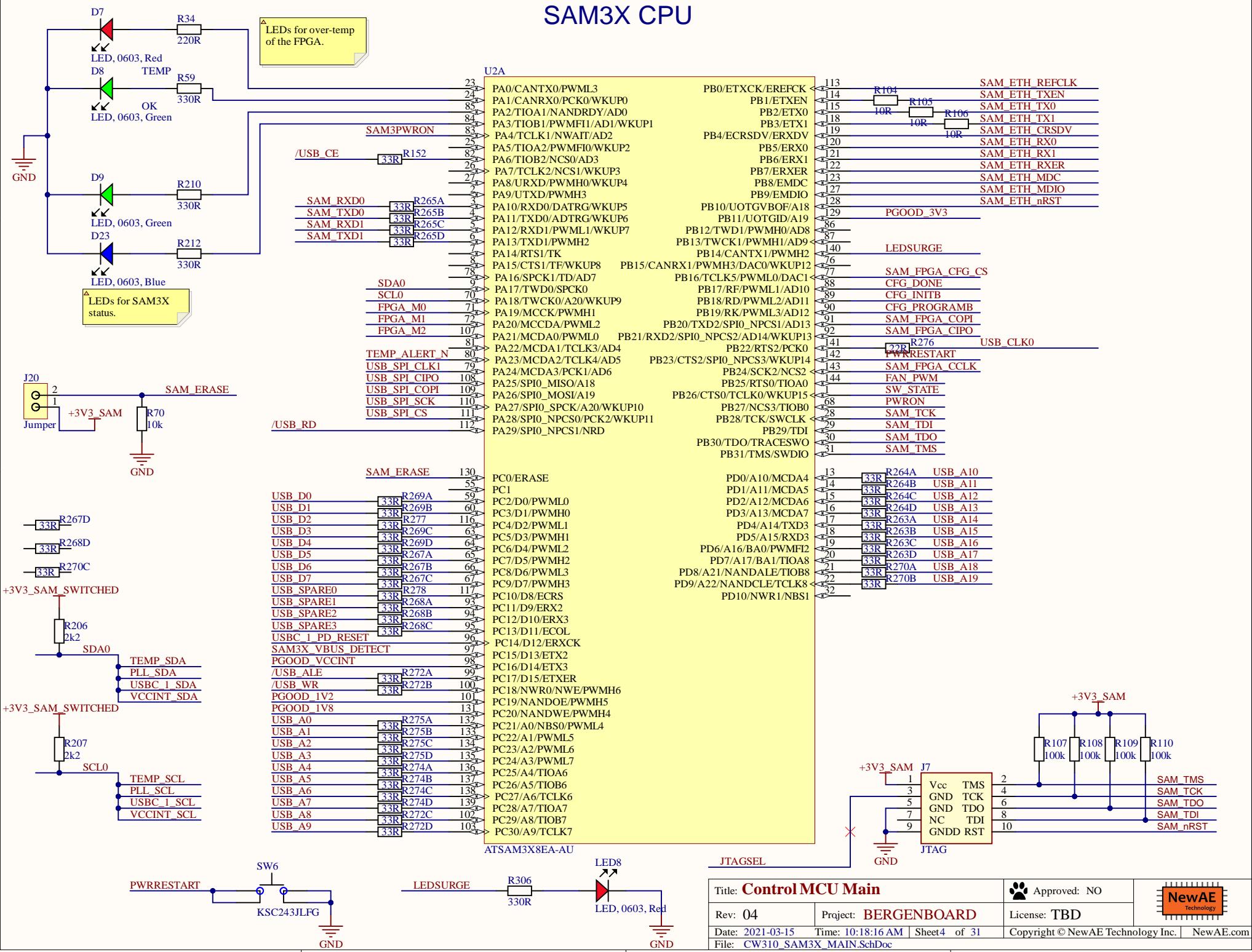
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File: CW310_INPUT_POWER.SchDoc

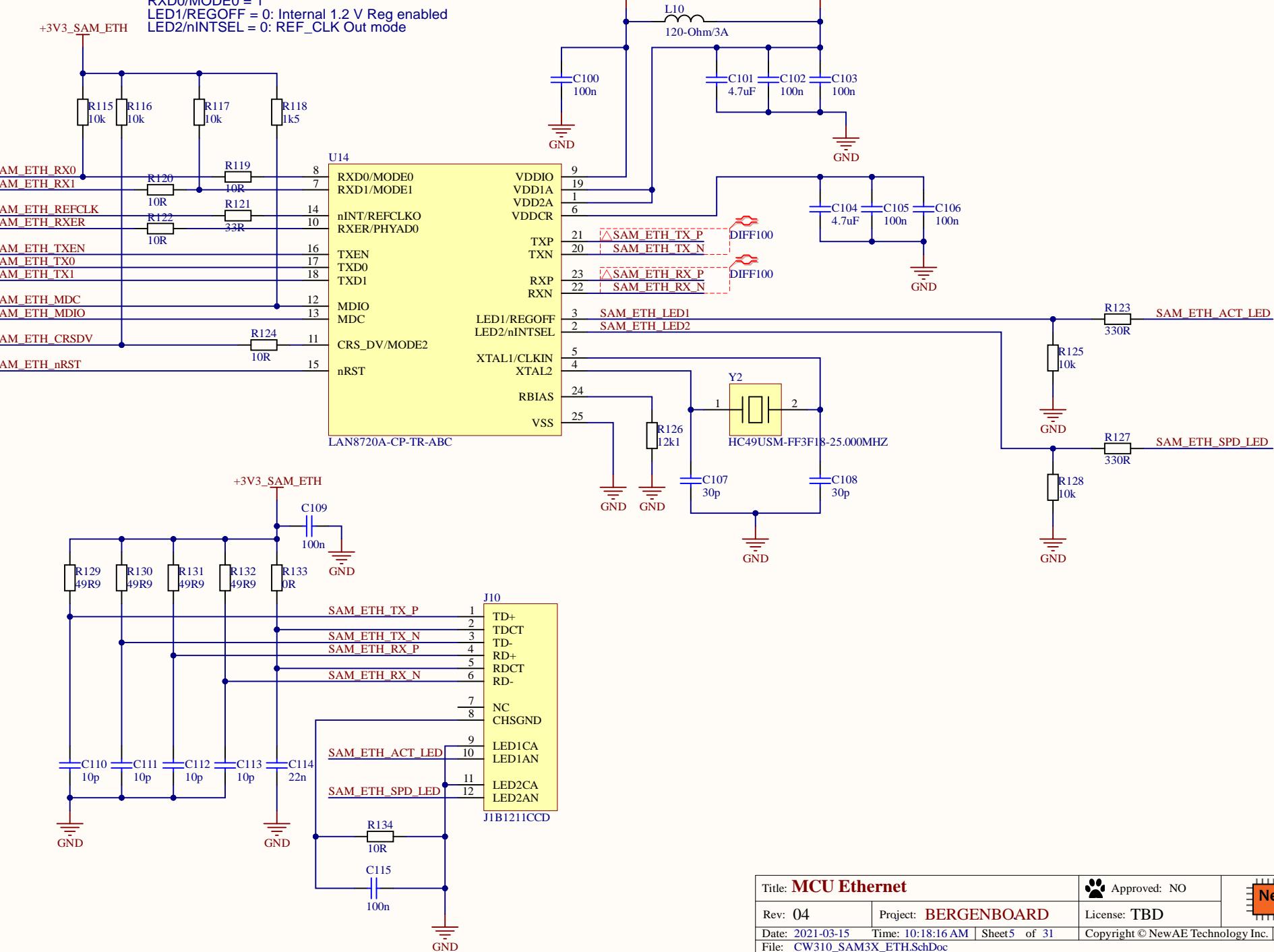
SAM3X CPU



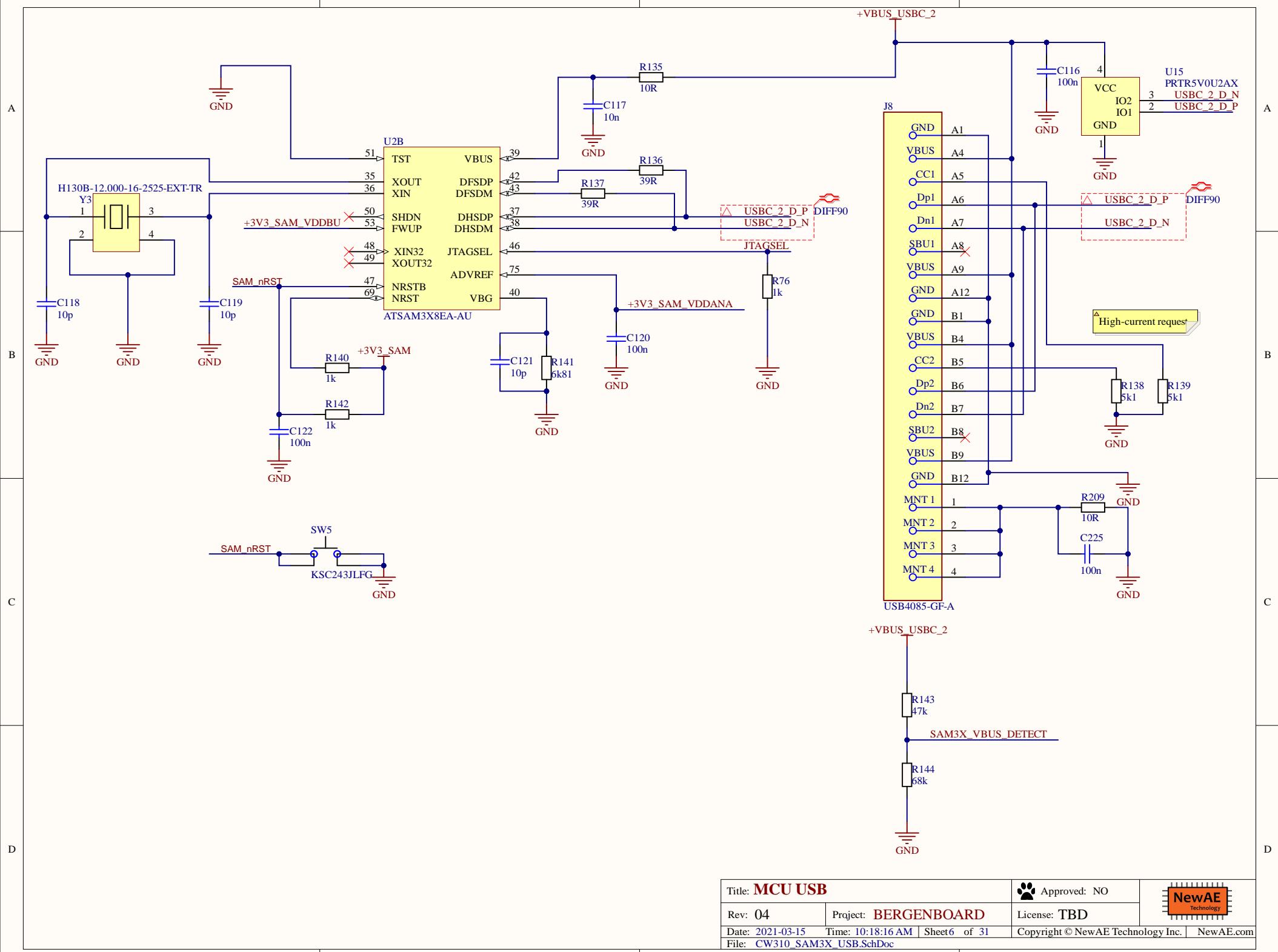
SAM3X Ethernet

LAN8720 PHY Configuration

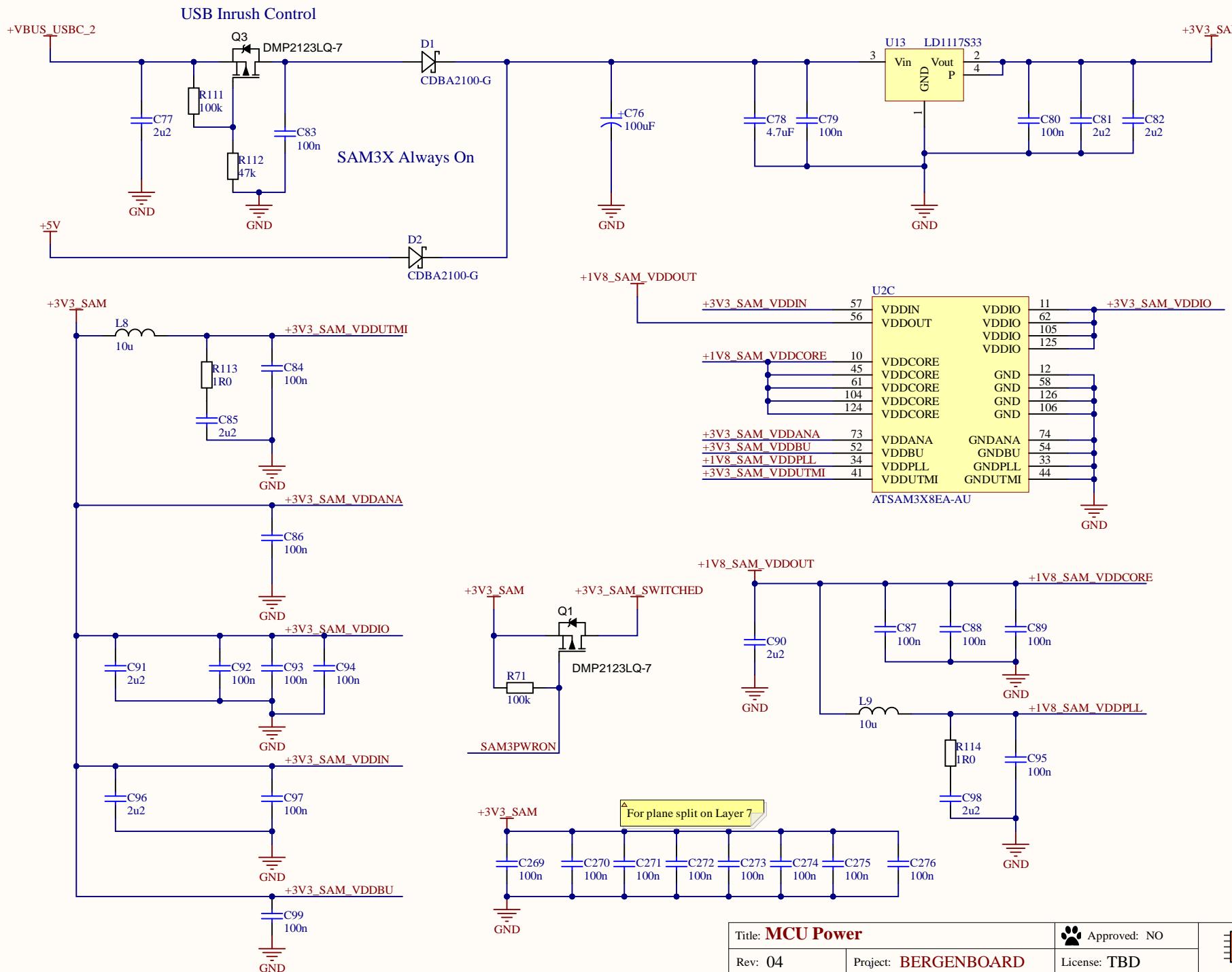
PHYAD0 = 0: Phy Address 0
 CRS_DV/MODE2 = 1: All modes, autonegotiation enabled
 RXD1/MODE1 = 1
 RXD0/MODE0 = 1
 LED1/REGOFF = 0: Internal 1.2 V Reg enabled
 LED2/nINTSEL = 0: REF_CLK Out mode



Title: MCU Ethernet		
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SAM3X Power

Title: **MCU Power**

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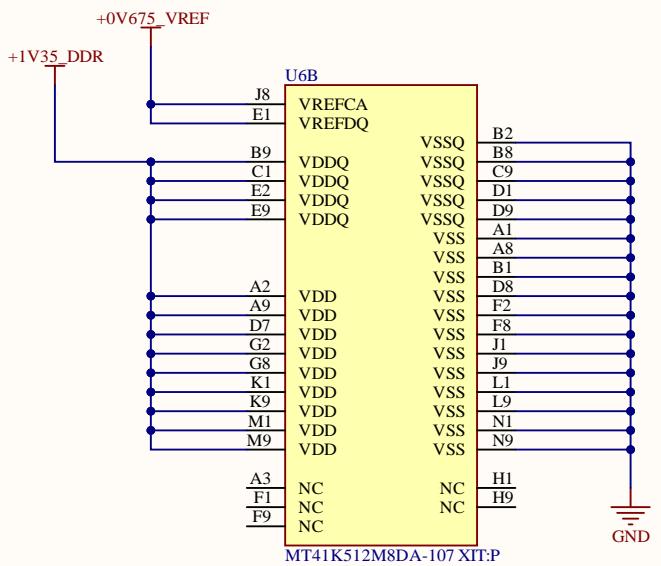
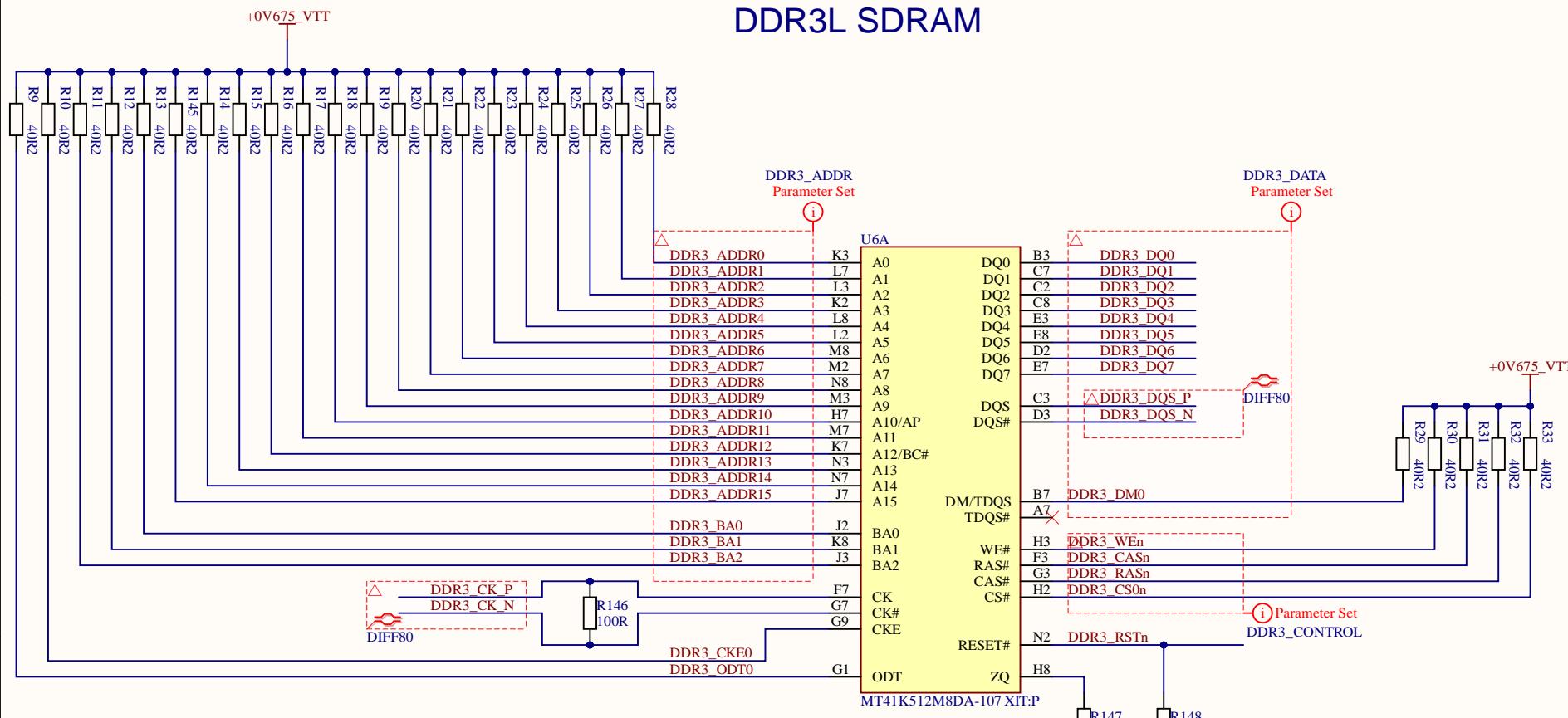
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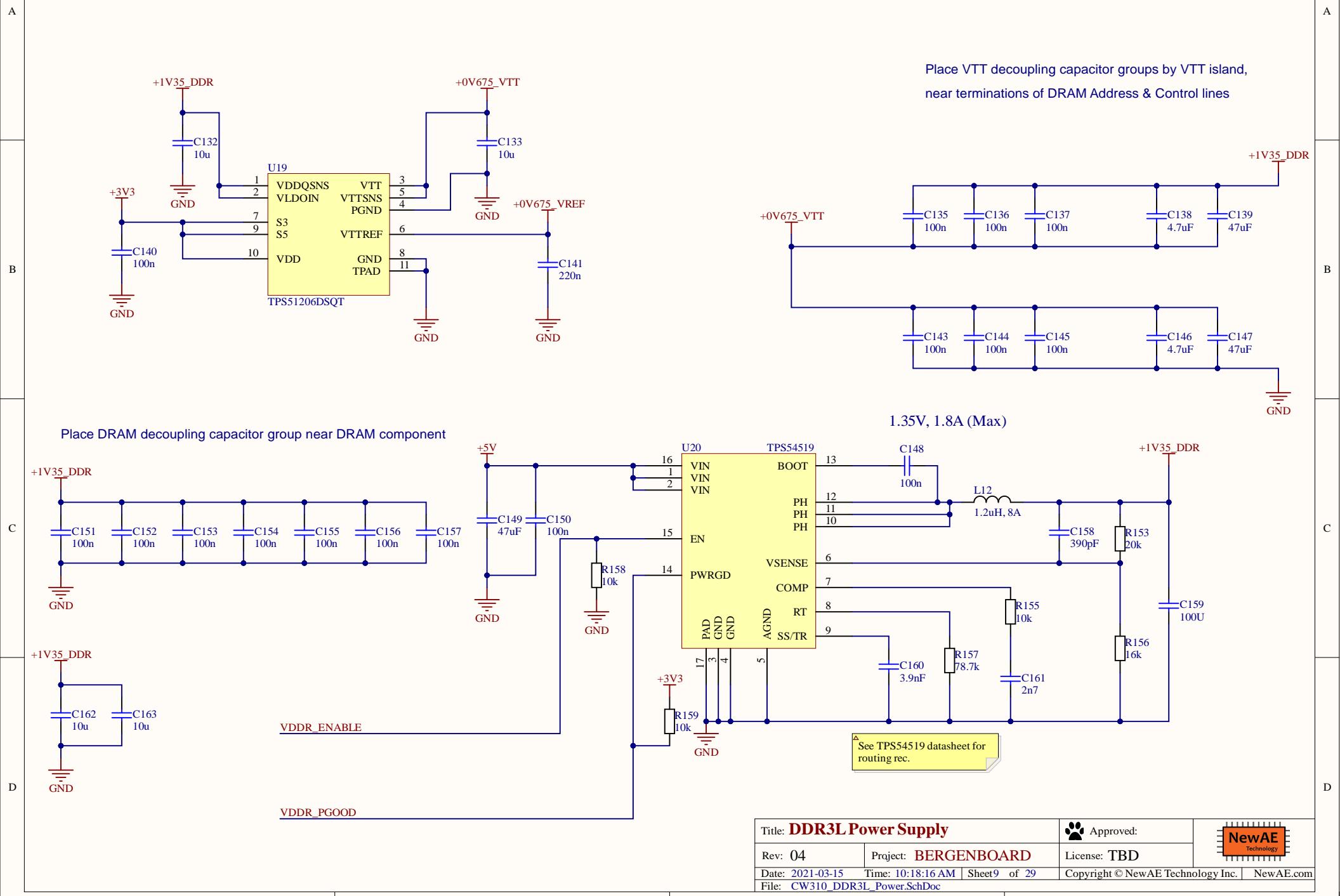
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DDR3L SDRAM



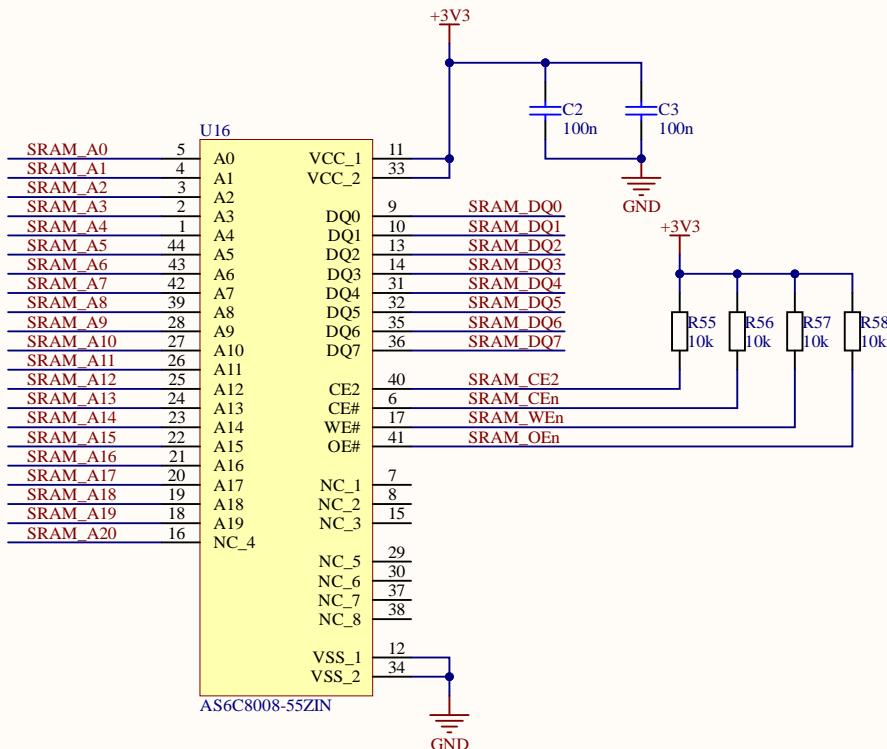
Title: User DDR3		 Approved: NO	
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File: CW310_DDR3L.SchDoc			

DDR3L VTT & DECOUPLING



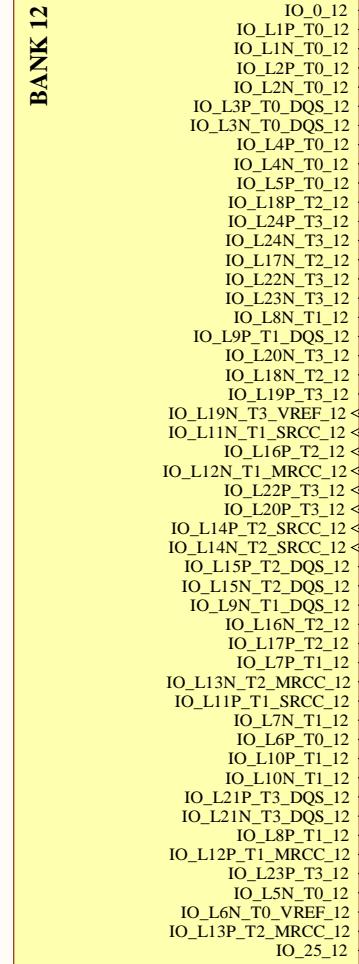
SRAM

[△] SRAM should be footprint compatible with:
 AS6C8008-55ZIN
 CY62158EV30LL-45ZSXIT
 IS62WV10248DBLL-55TLI

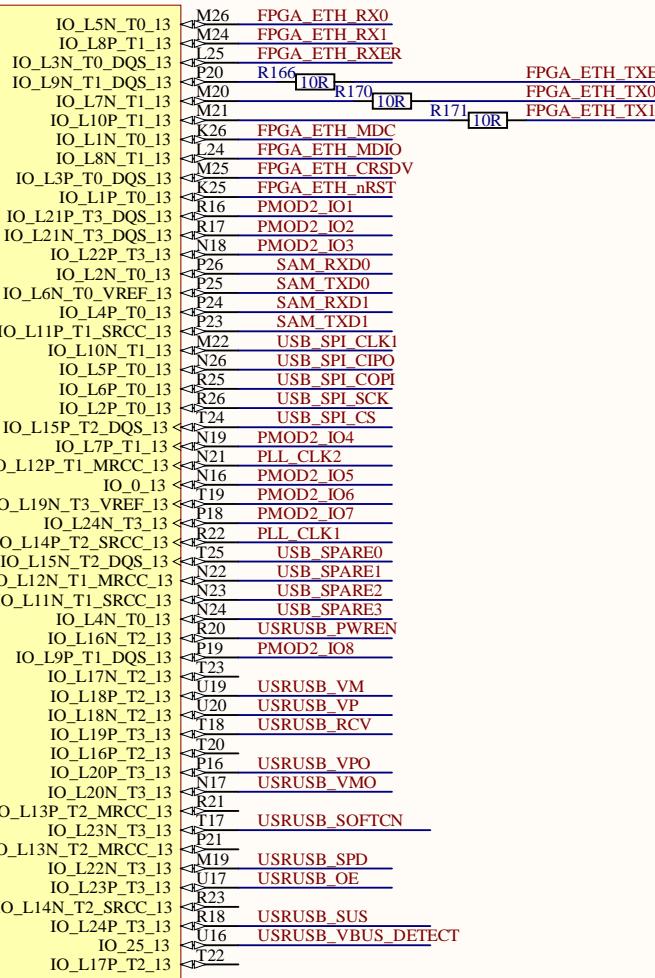


Title: User SRAM		Approved: NO	
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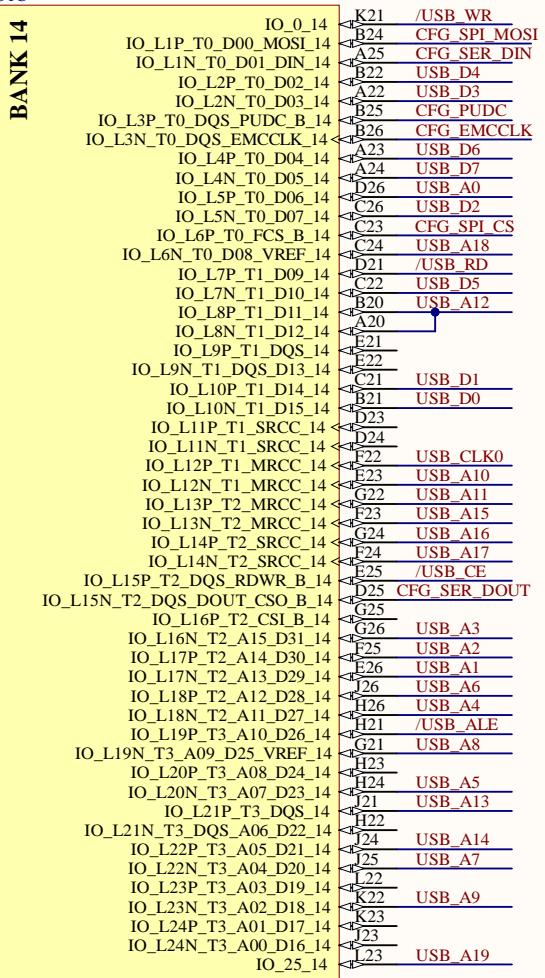
U1A



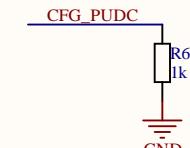
XC7K160T-1FBG676C

FPGA Bank: 3.3V, SAM3X Other GPIO, LEDs
U1B**BANK 13**

XC7K160T-1FBG676C

FPGA Bank: 3.3V, SAM3X A/D Bus, Configuration
U1C**BANK 14**

XC7K160T-1FBG676C



Title: Kintex IO Banks

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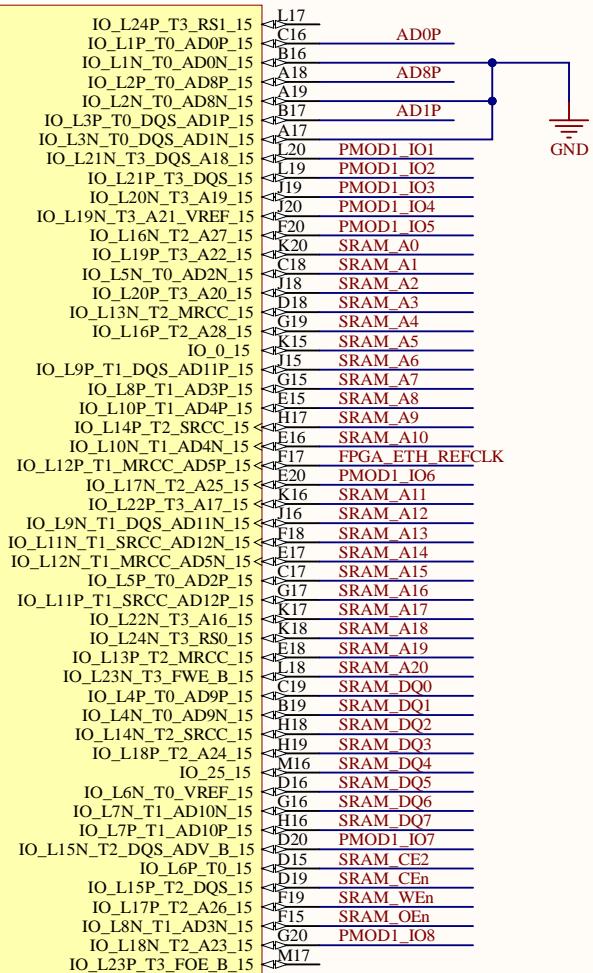
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FPGA Bank: 3.3V, SRAM Chip, Eth
U1D

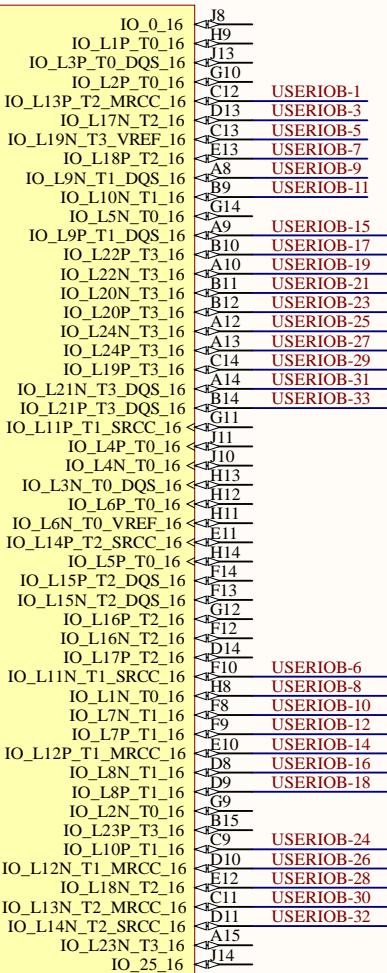
BANK 15



XC7K160T-1FBG676C

FPGA Bank: VCCIOB
UIE

BANK 16



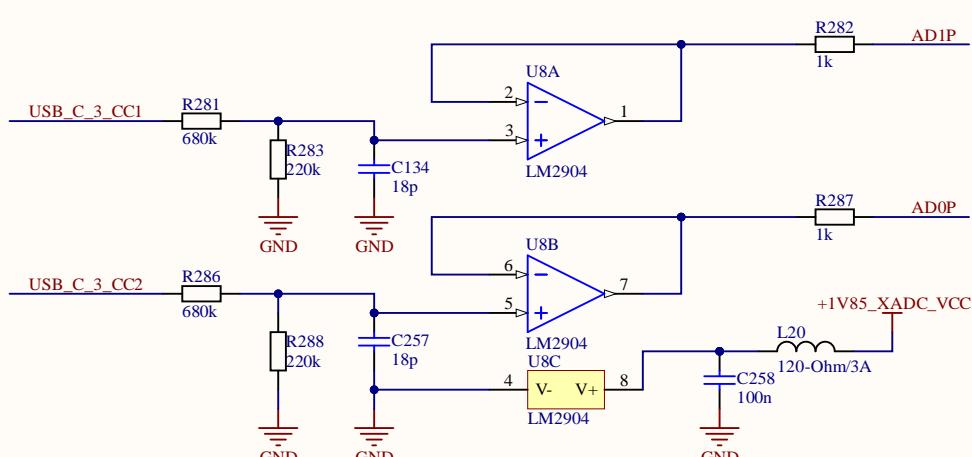
XC7K160T-1FBG676C

FPGA Bank: VCCIOA
UIF

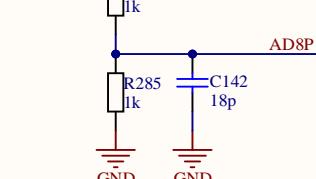
BANK 32



XC7K160T-1FBG676C



+1V0_VCCINT_SHUNTLLOW



Title: Kintex IO Banks

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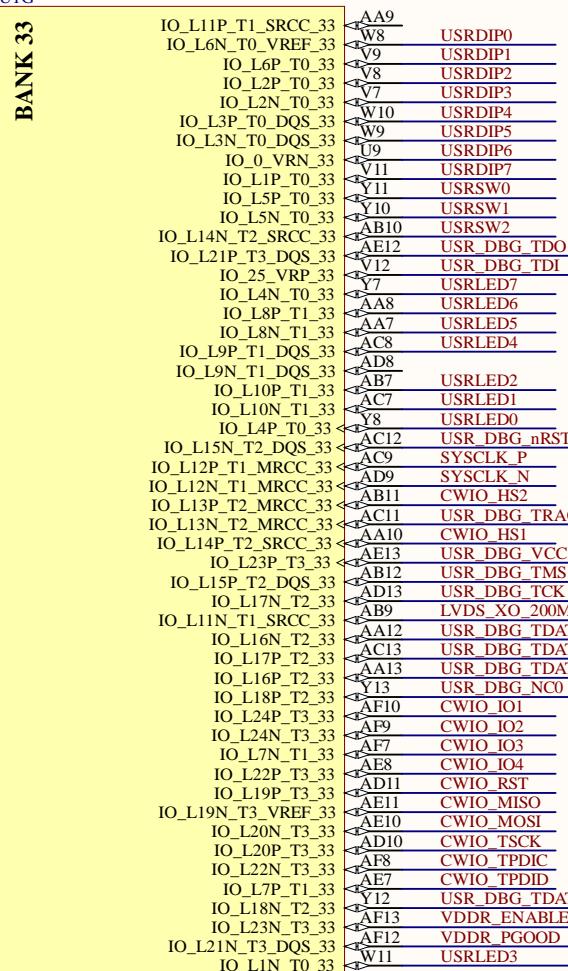
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Technology

FPGA Bank: 3.3V, CLKIN, USERLEDS, USERSW, USERIO

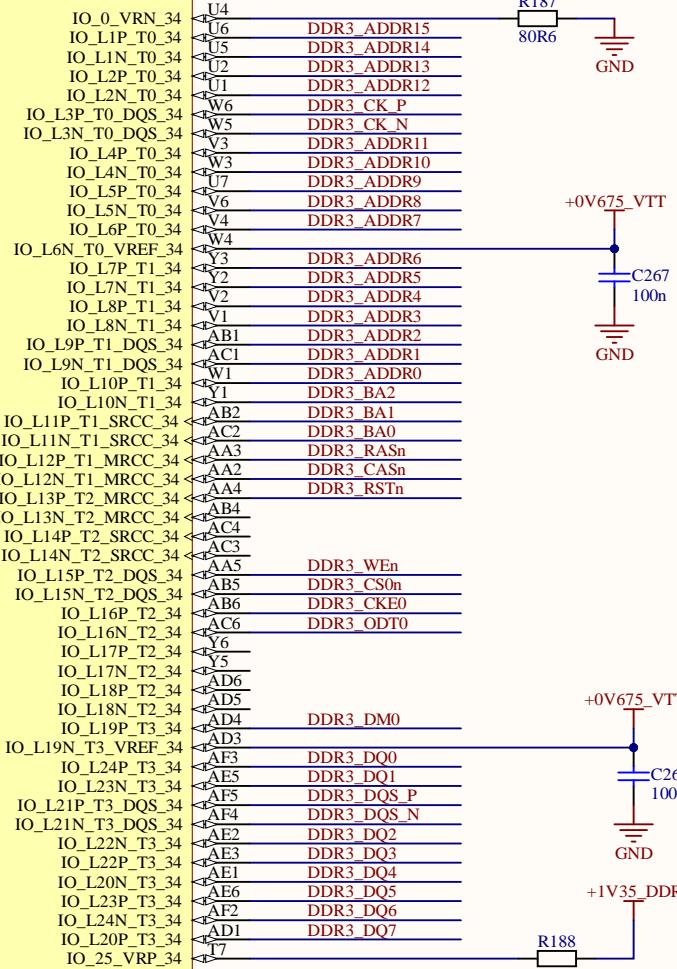
U1G



XC7K160T-1FBG676C

U1H Text

BANK 34



XC7K160T-1FBG676C

Title: **Kintex IO Banks**

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File: CW310_FPGAIO_3.SchDoc

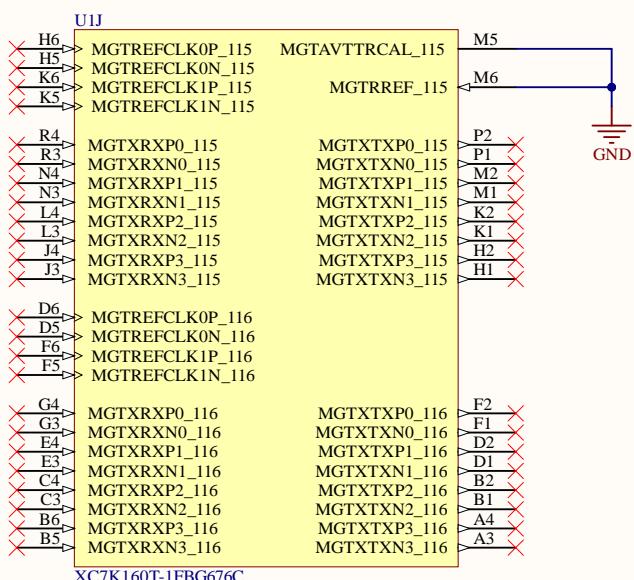
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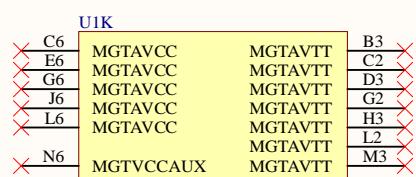
FPGA MGT Interface

A



B

A



B

C

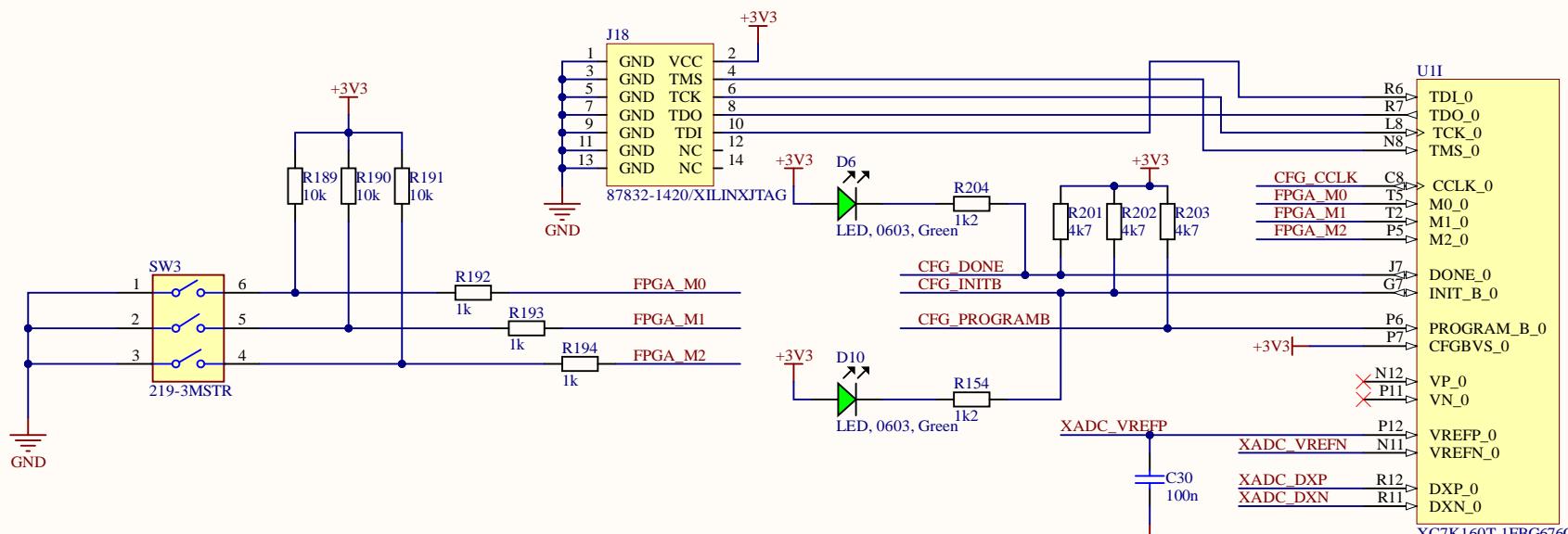
C

D

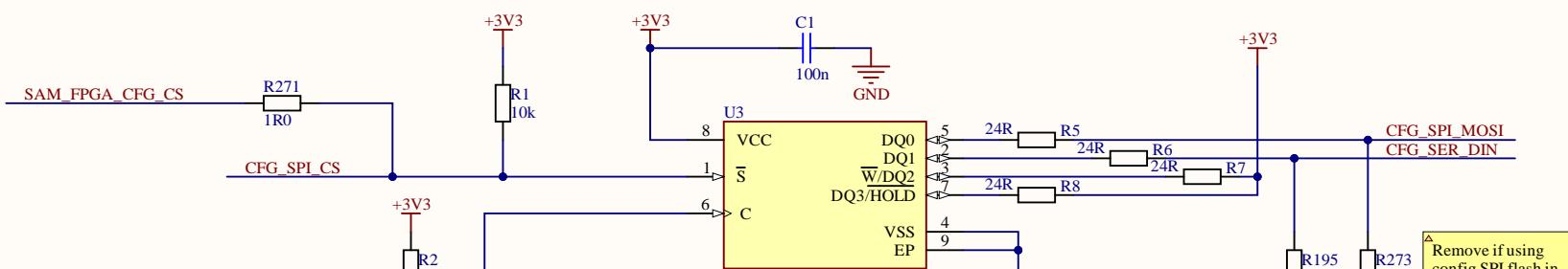
D

Title: Kintex MGT Tiles		Approved: NO	
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File: CW310_FPGA_MGT.SchDoc			

A



B

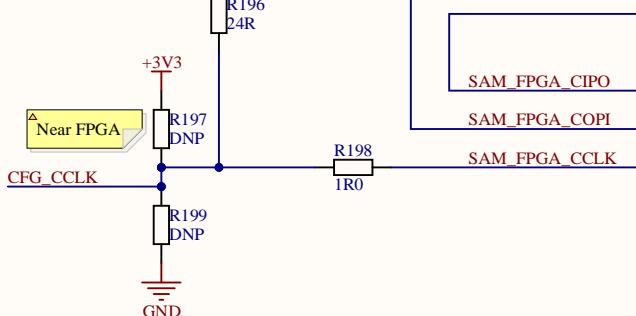


C

▲ CCLK termination resistors are DNP by default on both FPGA & SPI flash.
Mount 100-ohm resistors if needed.

▲ Near SPI Flash

▲ Near FPGA



D

Title: Kintex Configuration

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File: CW310_FPGA_CFG.SchDoc

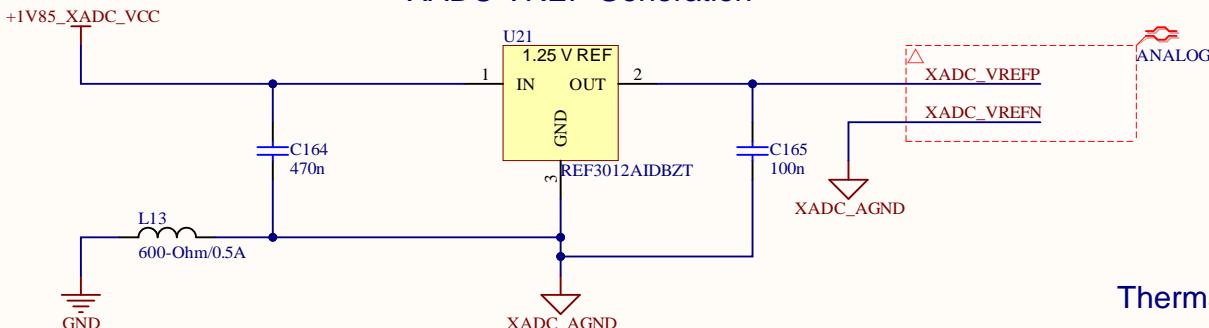
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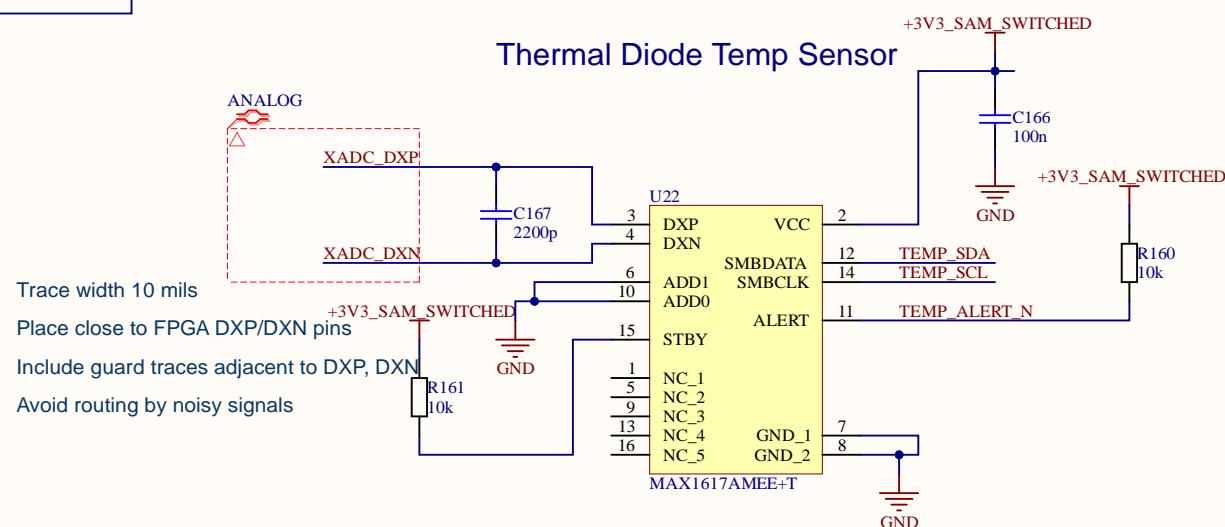
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FPGA XADC POWER

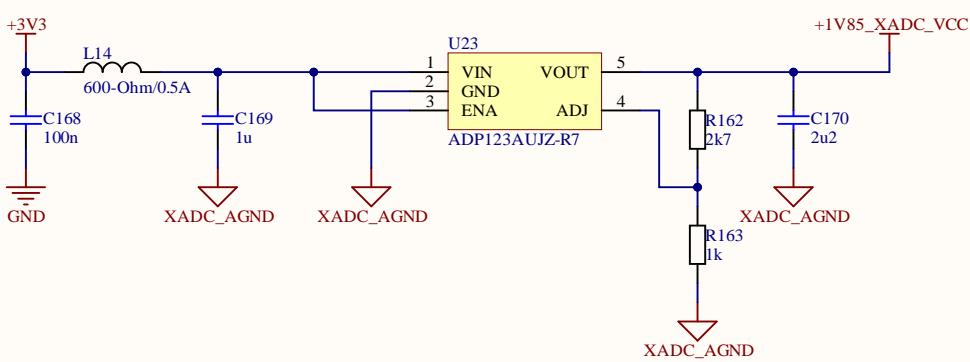
XADC VREF Generation



Thermal Diode Temp Sensor

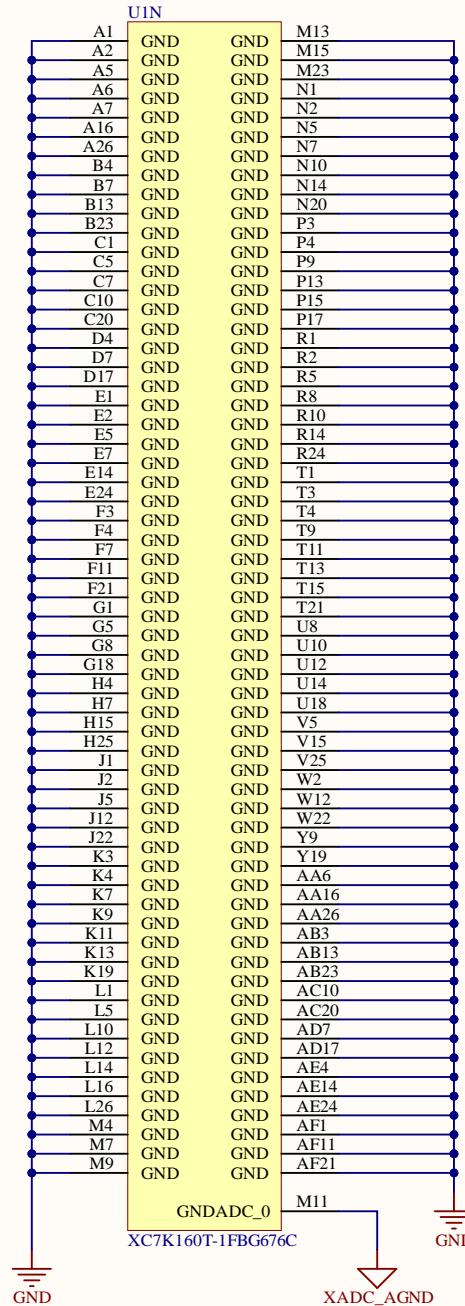
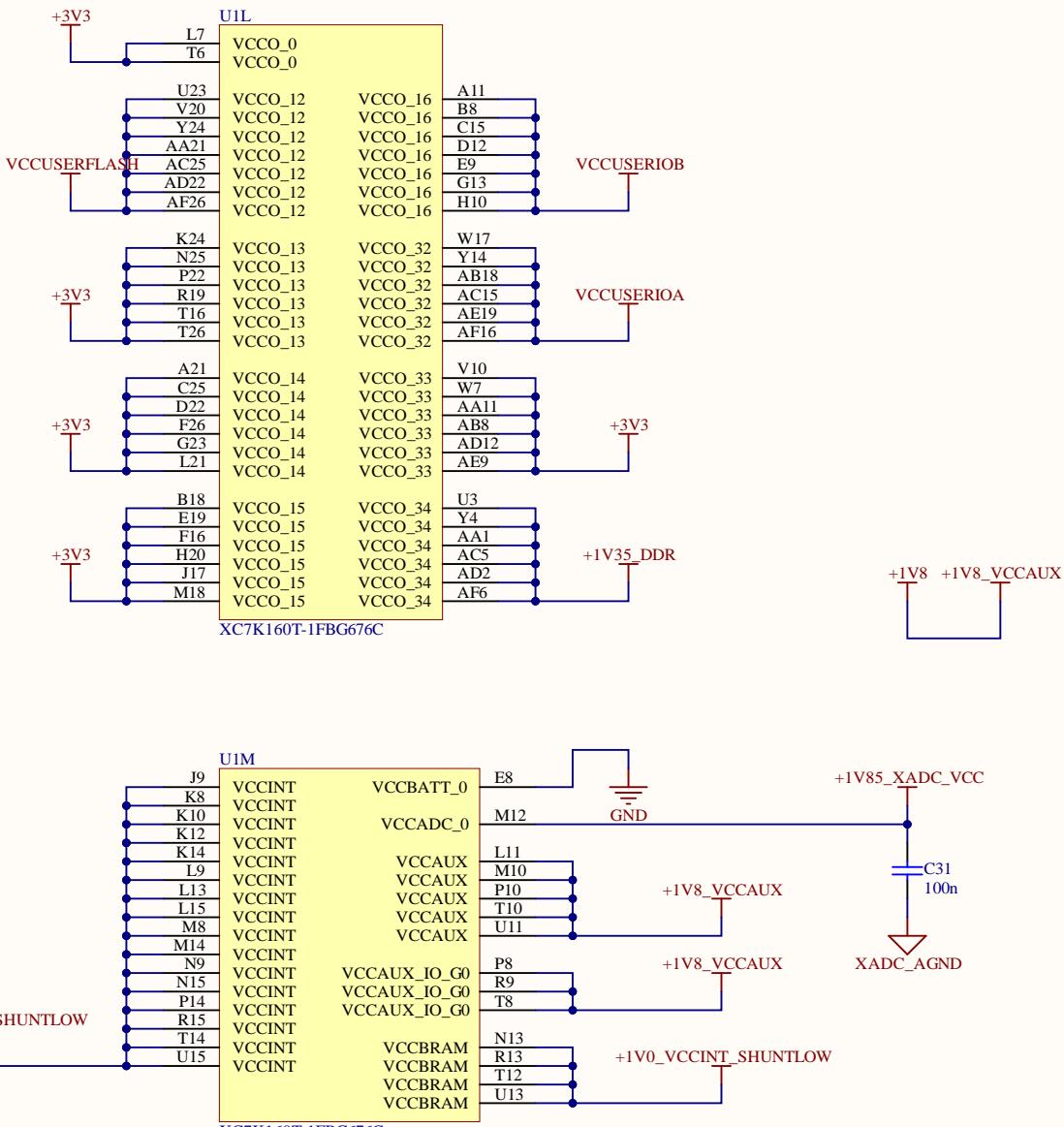


XADC VCC Generation



Title: FPGA - Thermal + XADC		Approved:	
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FPGA POWER



Title: **Kintex Power Connections**

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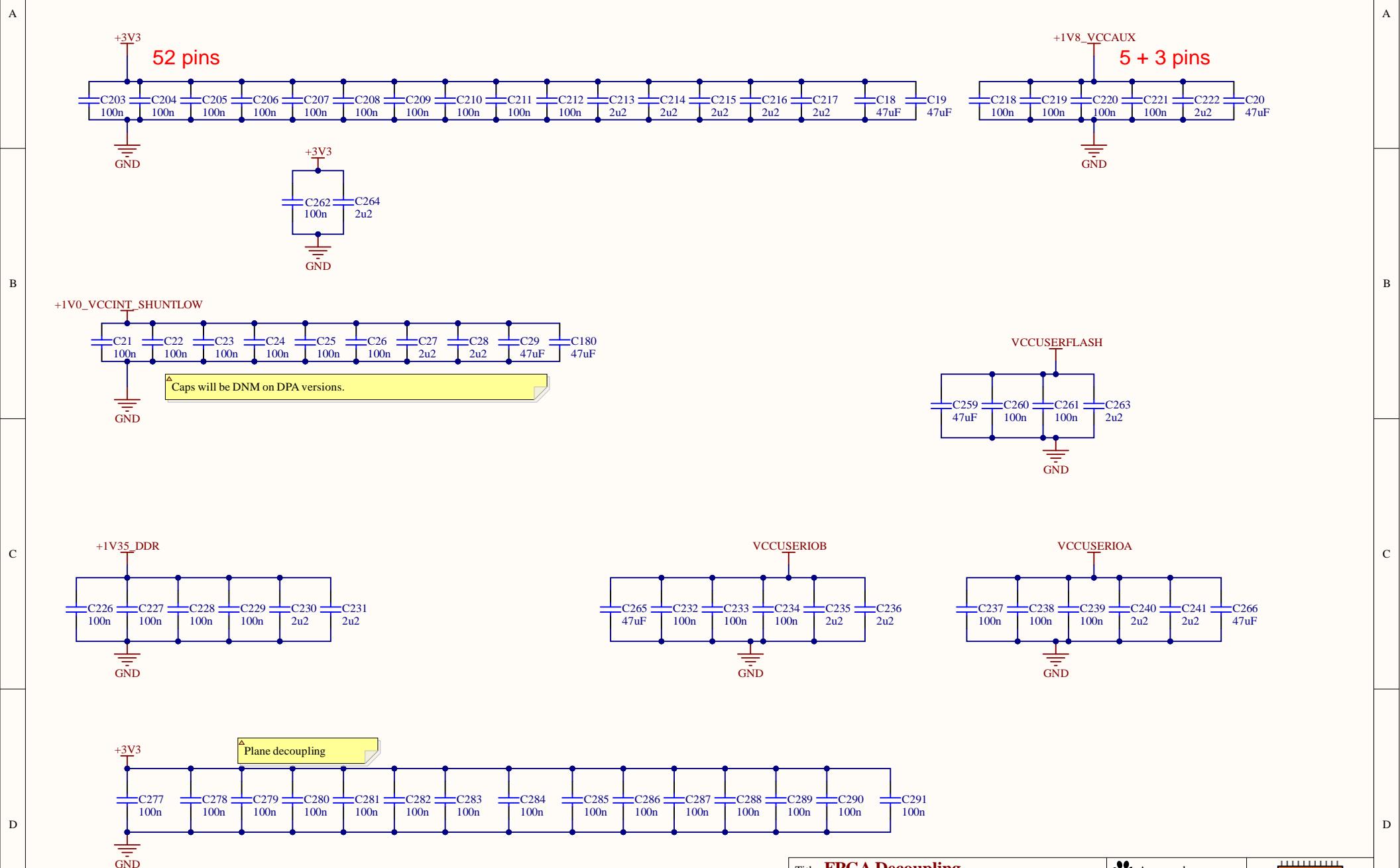
1

2

2

1

FPGA Decoupling



Title: **FPGA Decoupling**

Approved:



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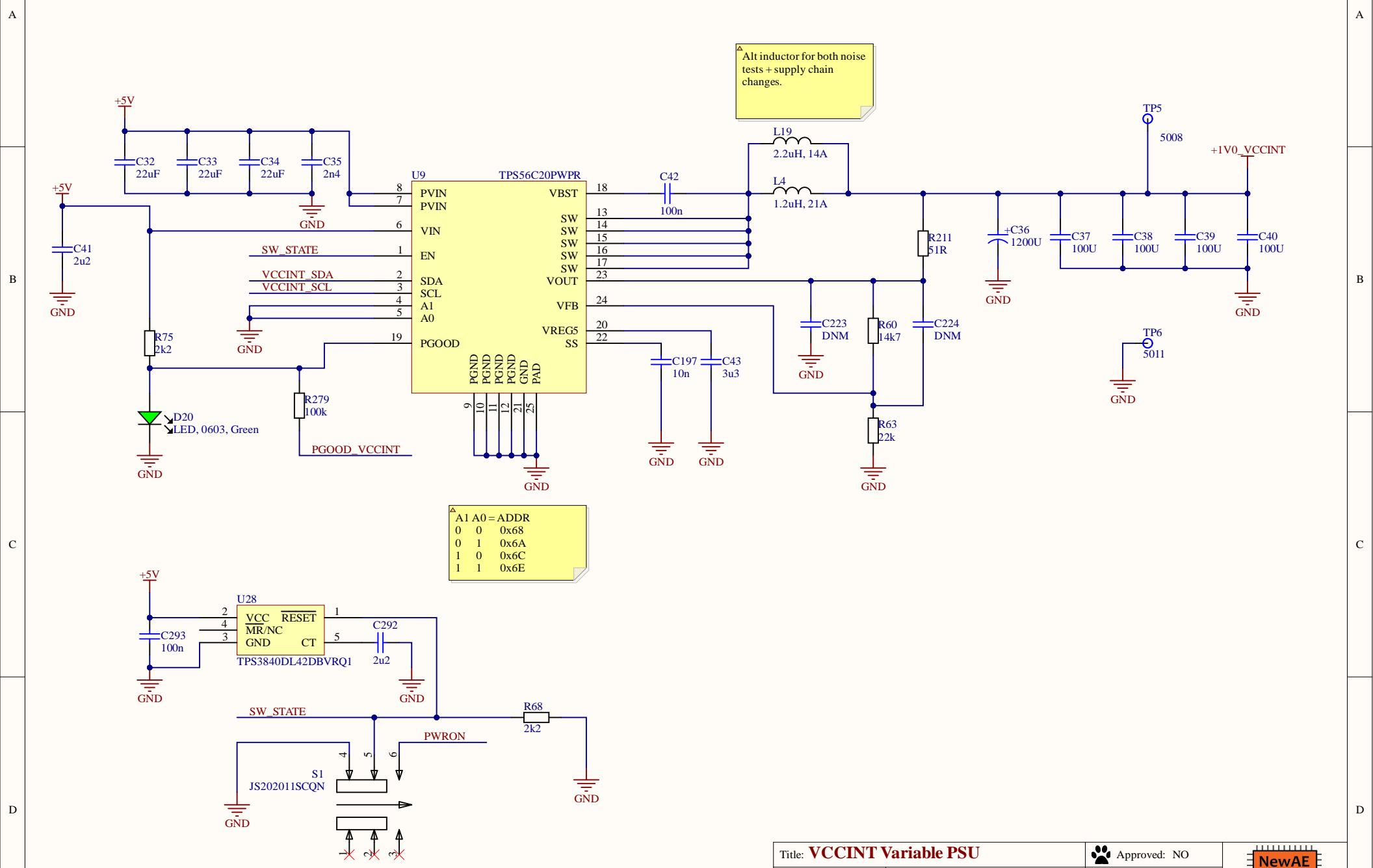
Date: 2021-03-15

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File: CW310_FPGA_DECOUPLING.SchDoc

FPGA VCCINT Power Generation / Control



Title: VCCINT Variable PSU		Approved: NO	NewAE Technology
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File: CW310_PSU_VCCINT.SchDoc			

A

A

B

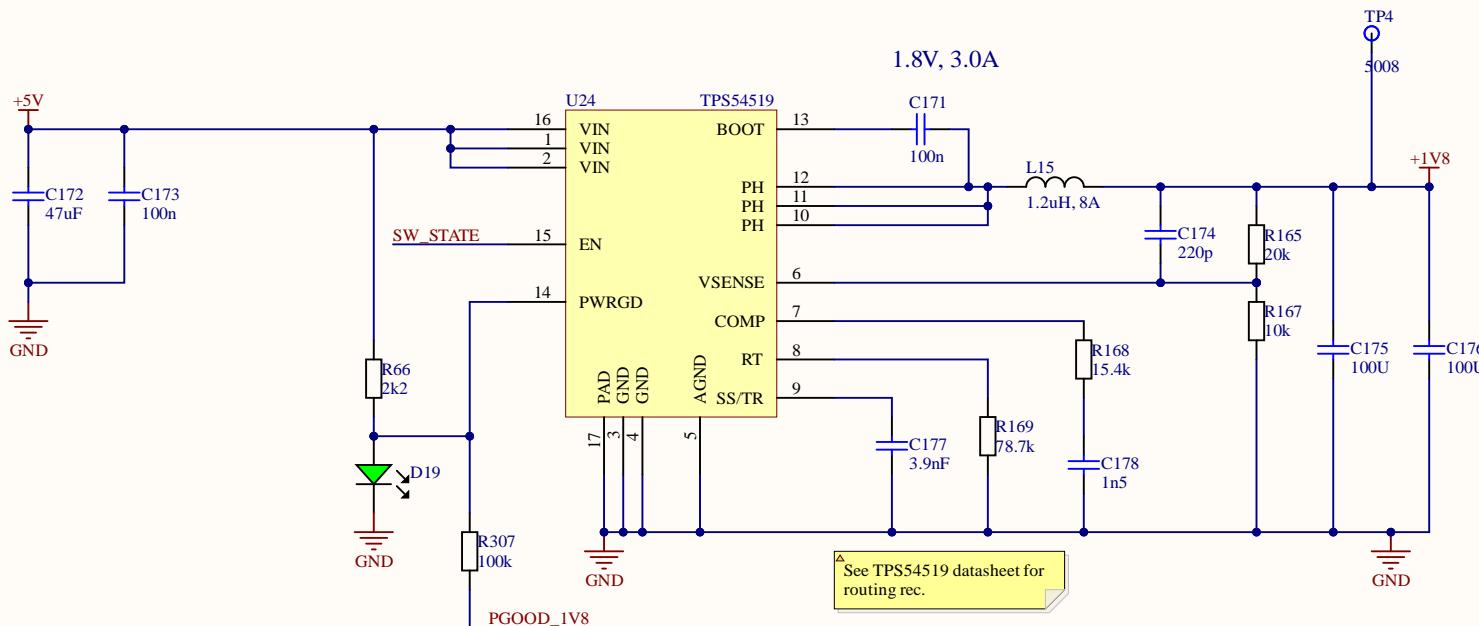
B

C

C

D

D



Title: VCC-AUX SMPS

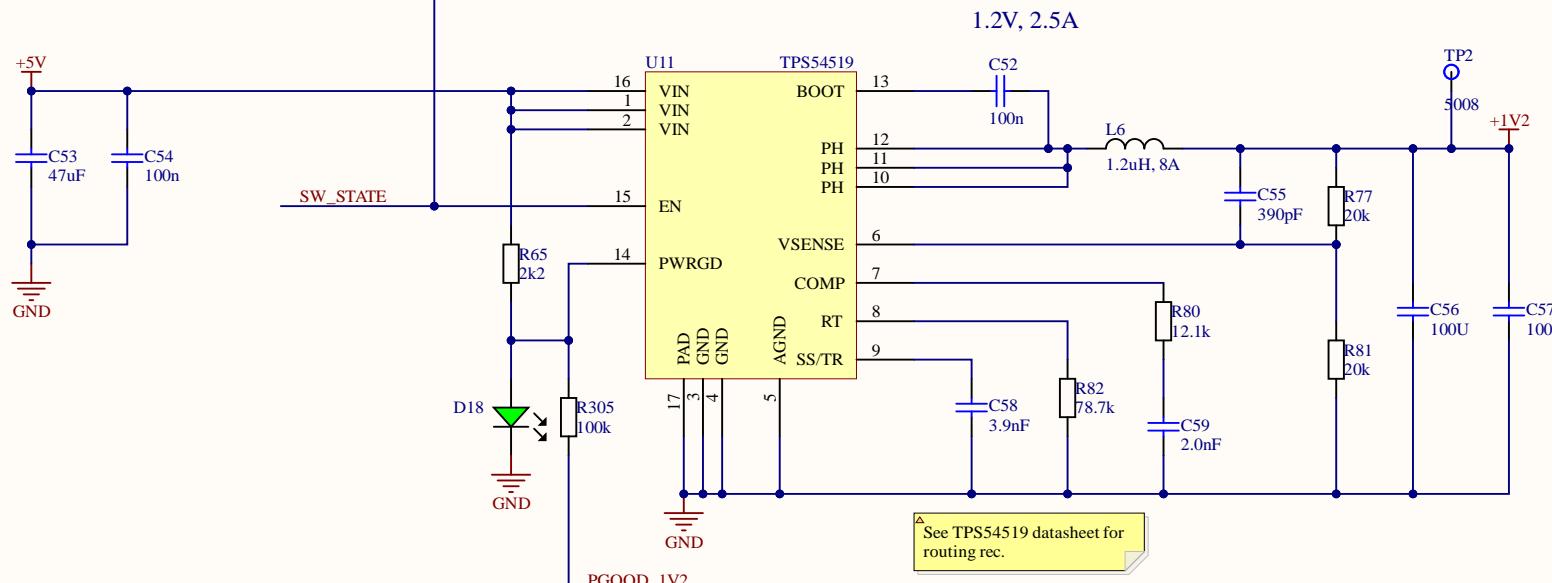
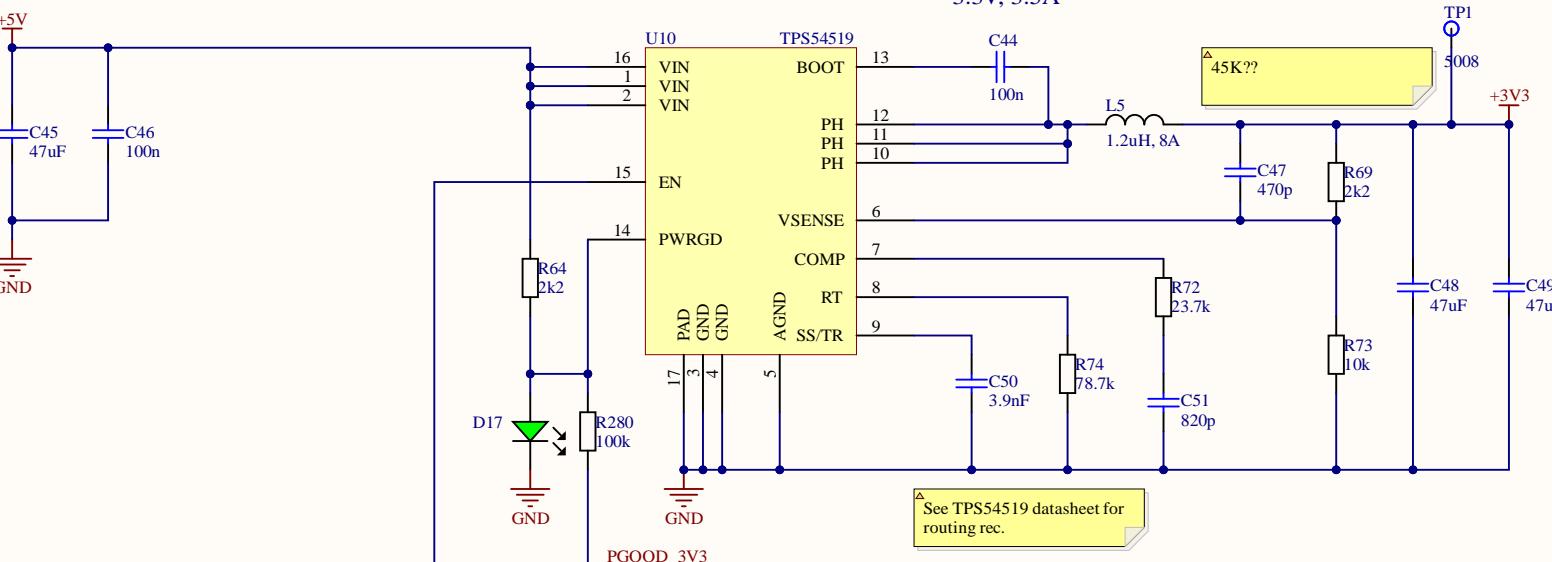
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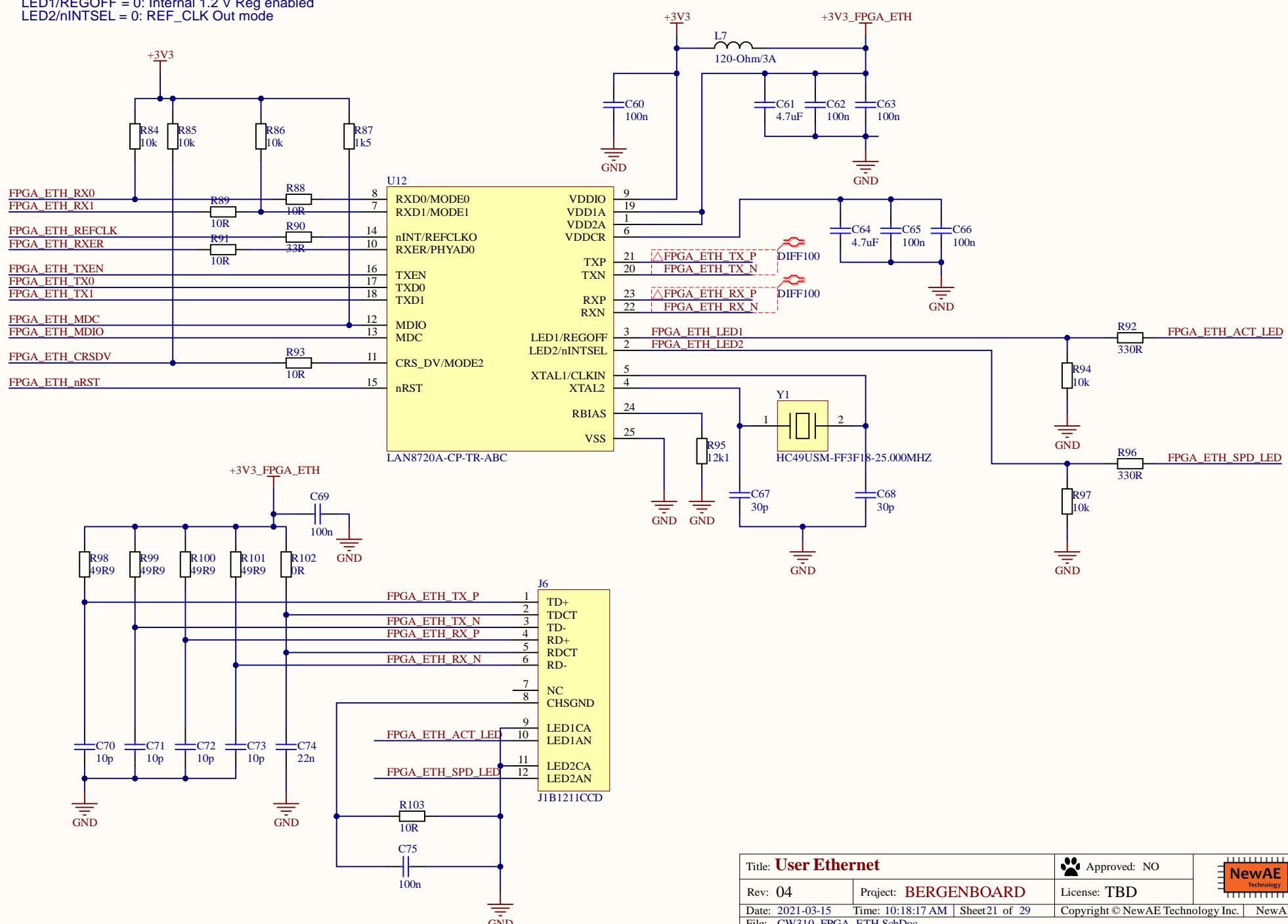
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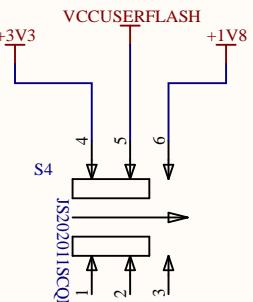
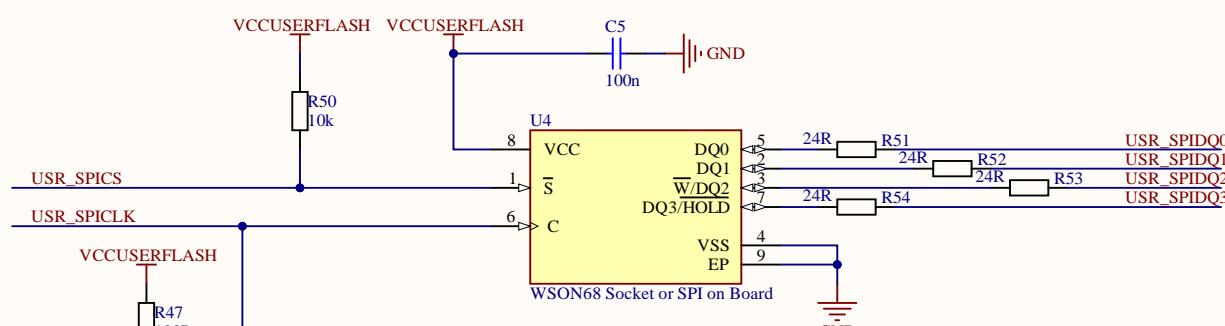
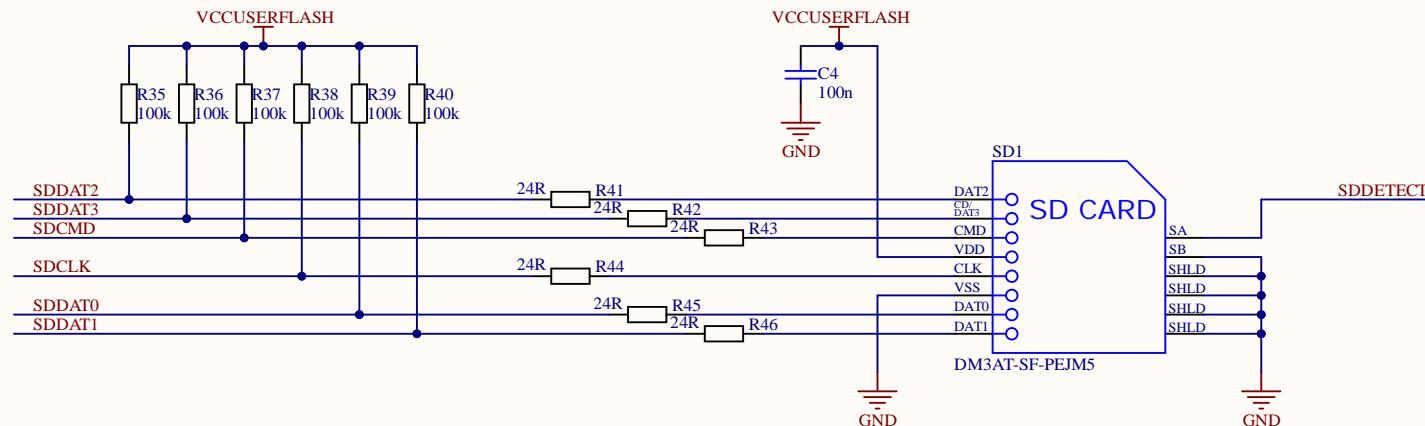
FPGA Ethernet

LAN8720 PHY Configuration

PHYAD0 = 0: Phy Address 0
 CRS_DV/MODE2 = 1: All modes, autonegotiation enabled
 RXD1/MODE1 = 1
 RXD0/MODE0 = 1
 LED1/REGOFF = 0: Internal 1.2 V Reg enabled
 LED2/nINTSEL = 0: REF_CLK Out mode



Title: User Ethernet		Approved: NO	NewAE Technology
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Title: **User SPI Flash + SD Card**

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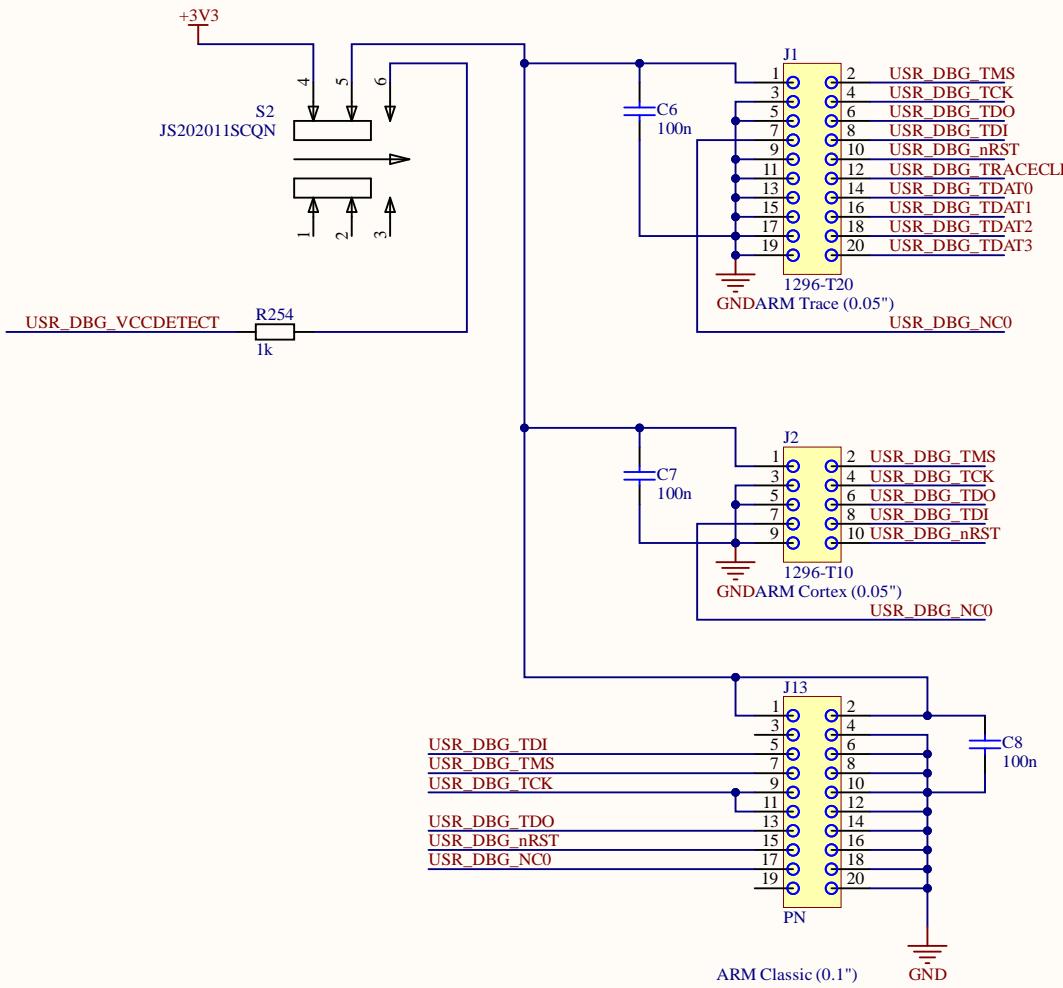
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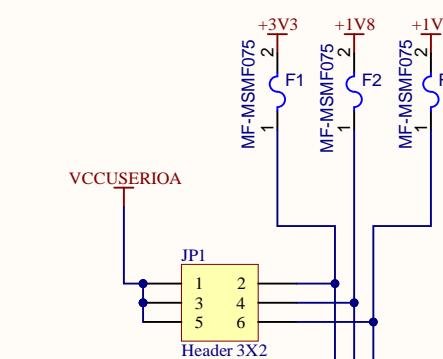
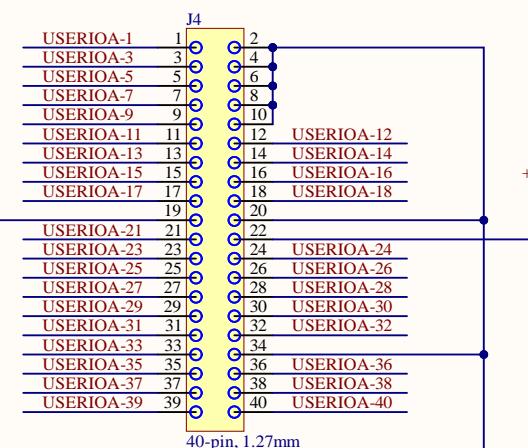
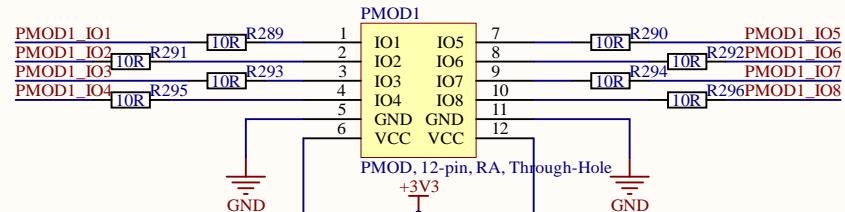
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File: CW310_SPI_flashes.SchDoc

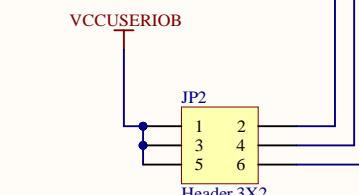
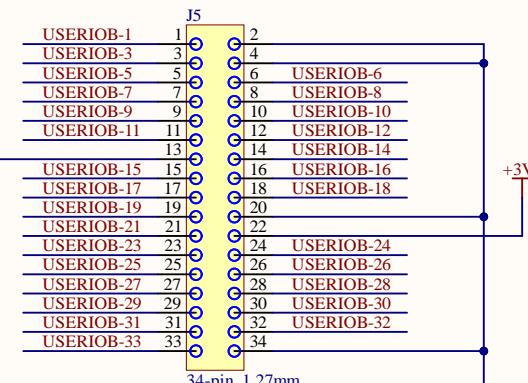
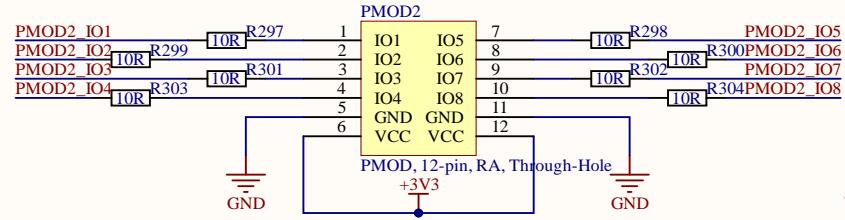


Title: User Debug Headers		Approved: NO	NewAE Technology
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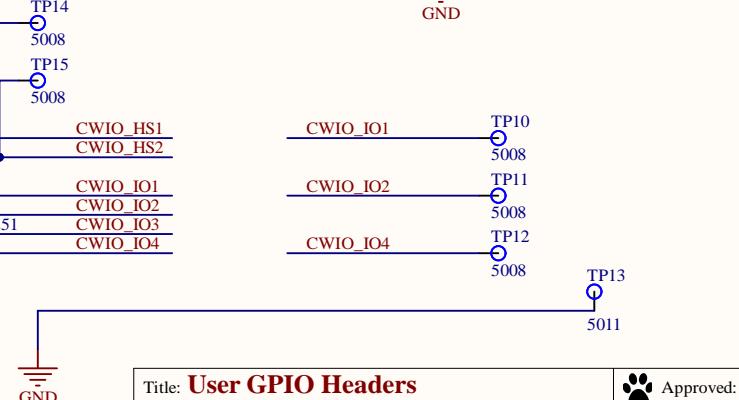
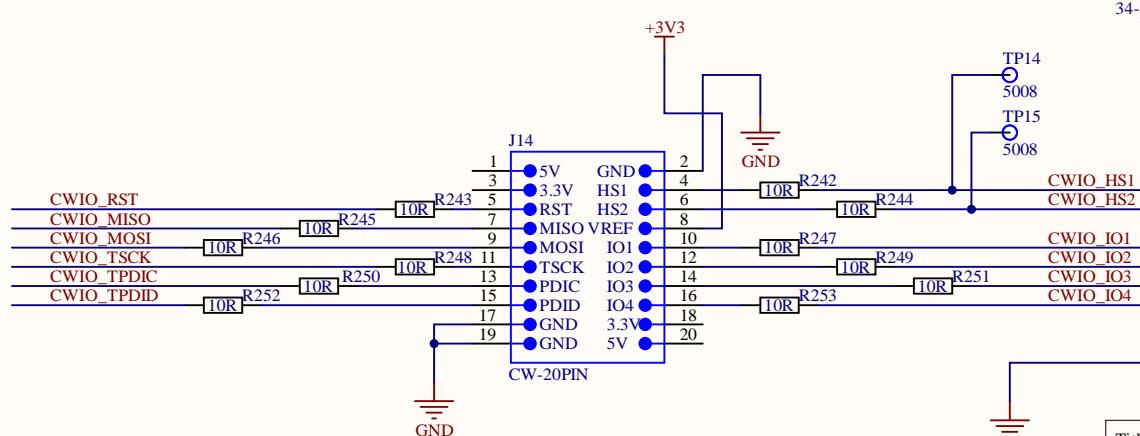
A



B



C

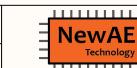
**Title: User GPIO Headers**

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Date: 2021-03-15 Time: 10:18:17 AM Sheet 24 of 29

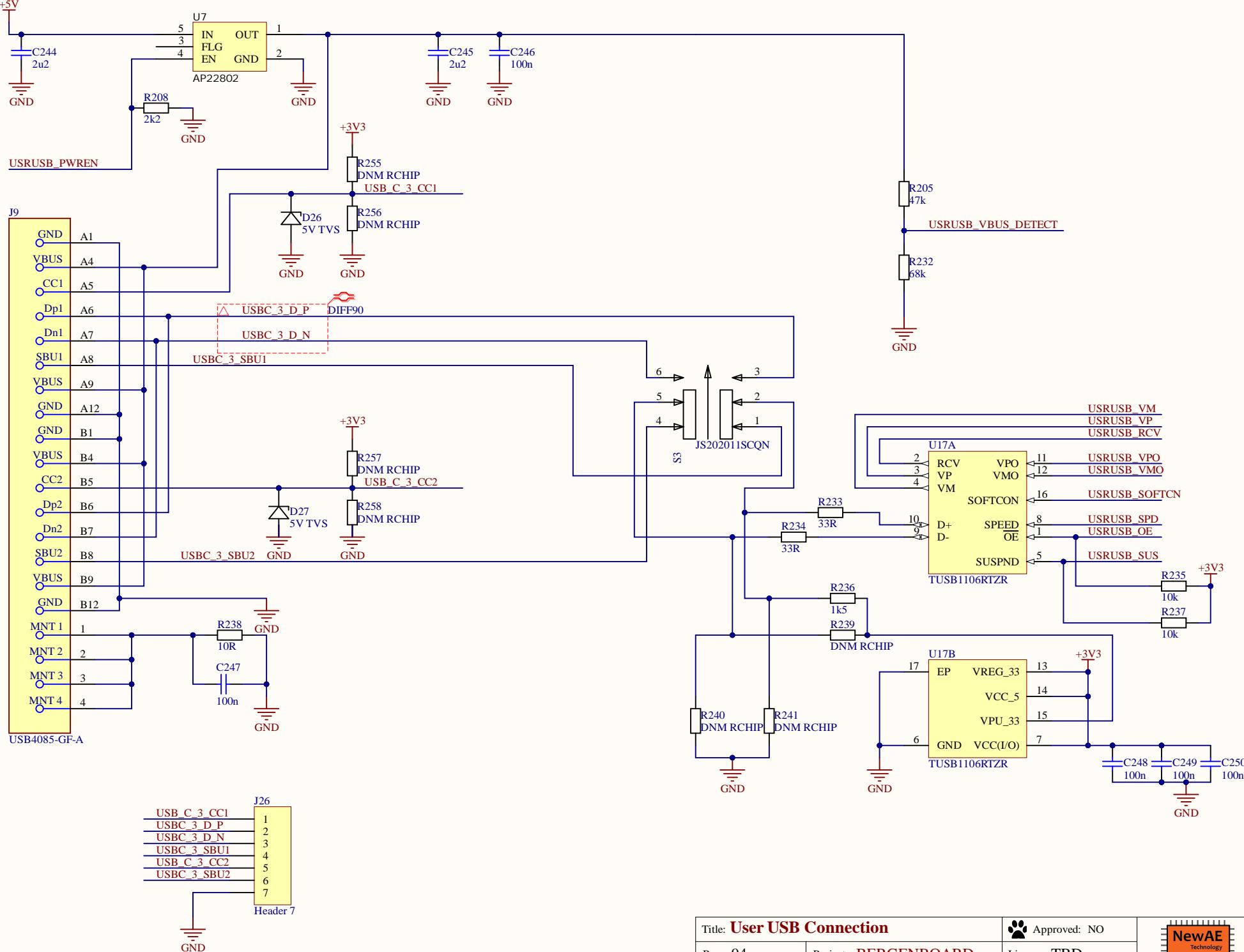
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Title: **User USB Connection**

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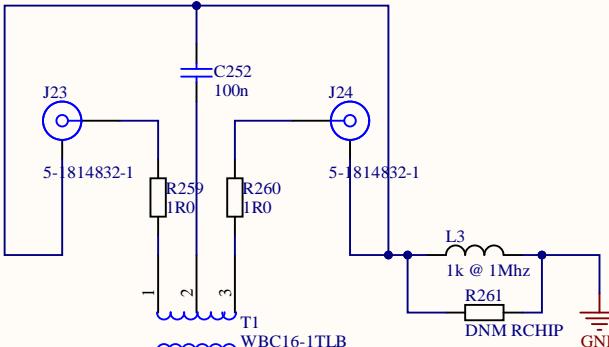
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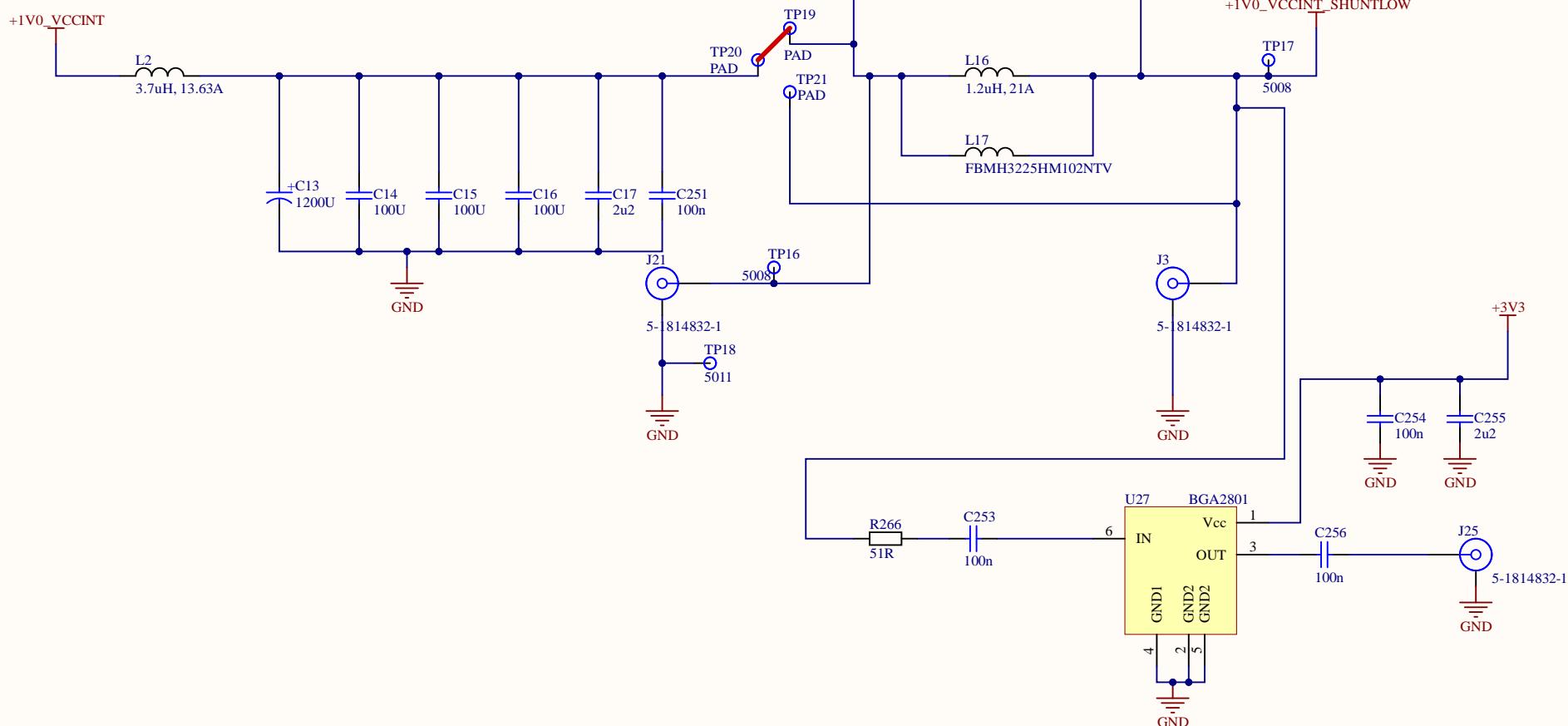
Approved: NO



A



B



Title: Power Measurements

Approved: NO



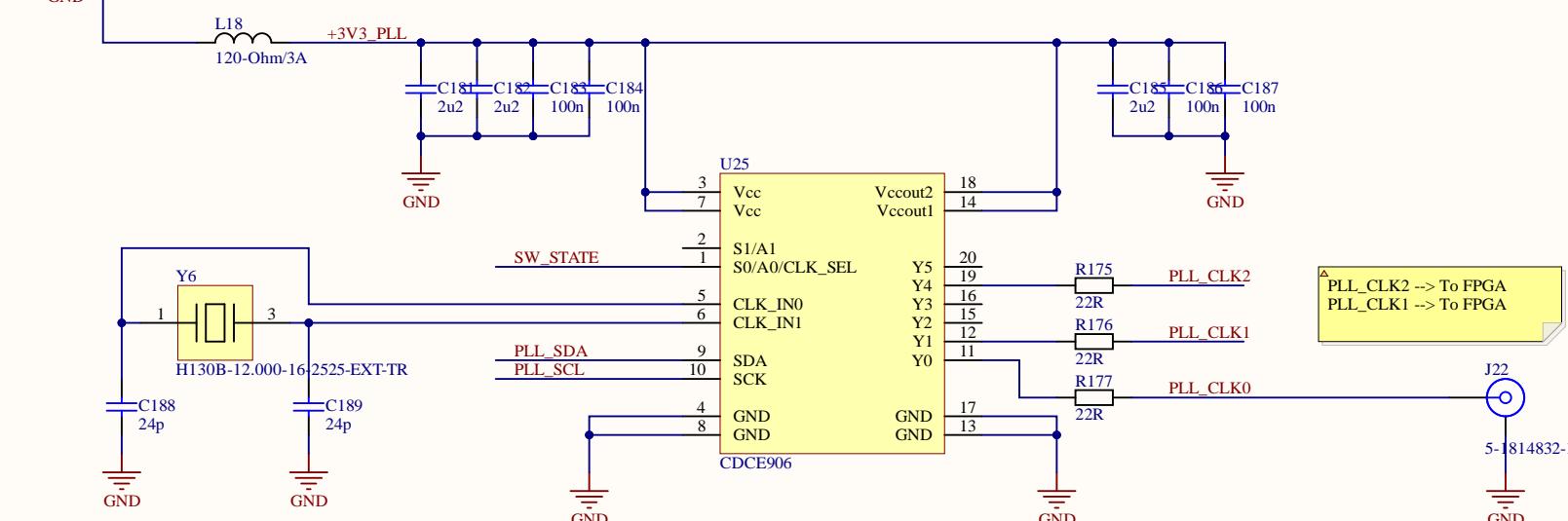
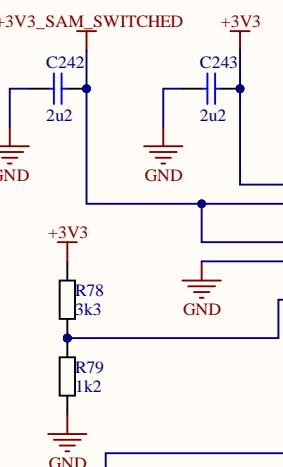
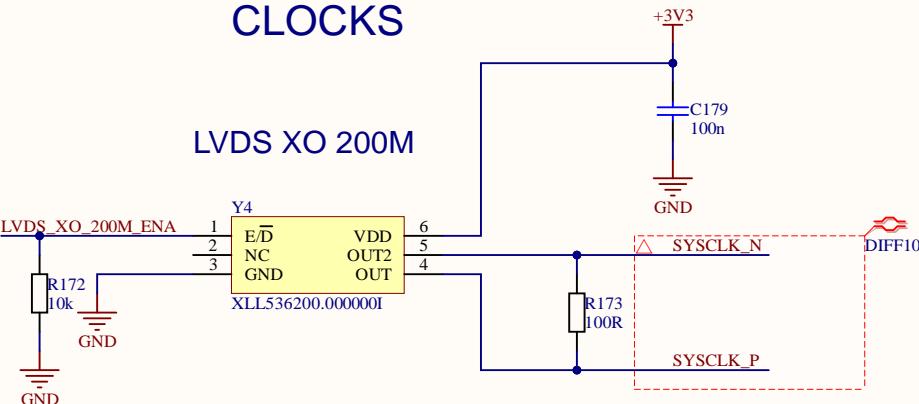
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CLOCKS

LVDS XO 200M



Title: PLL, Clocks for FPGA

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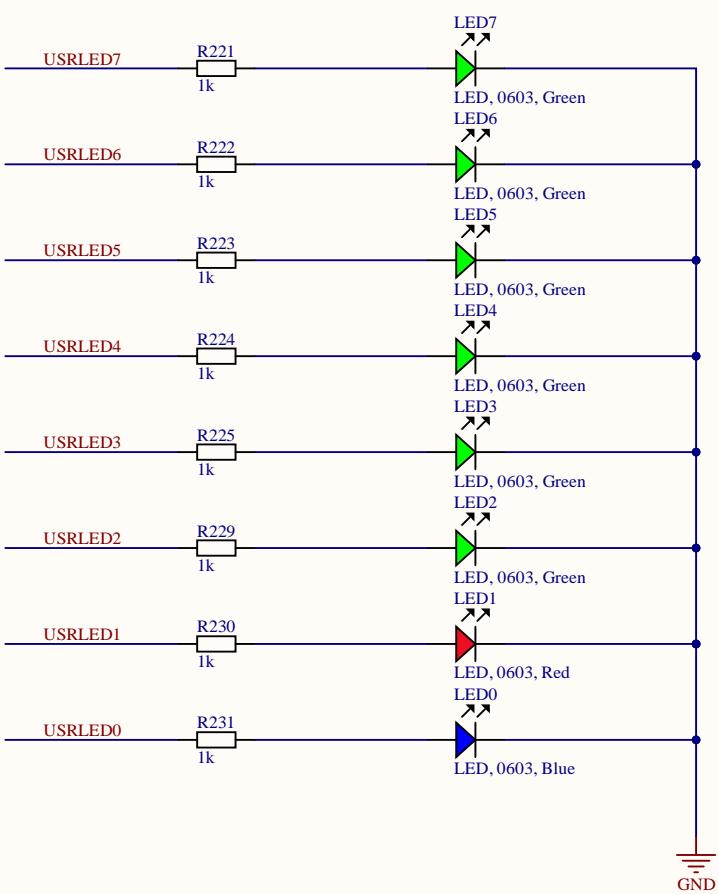
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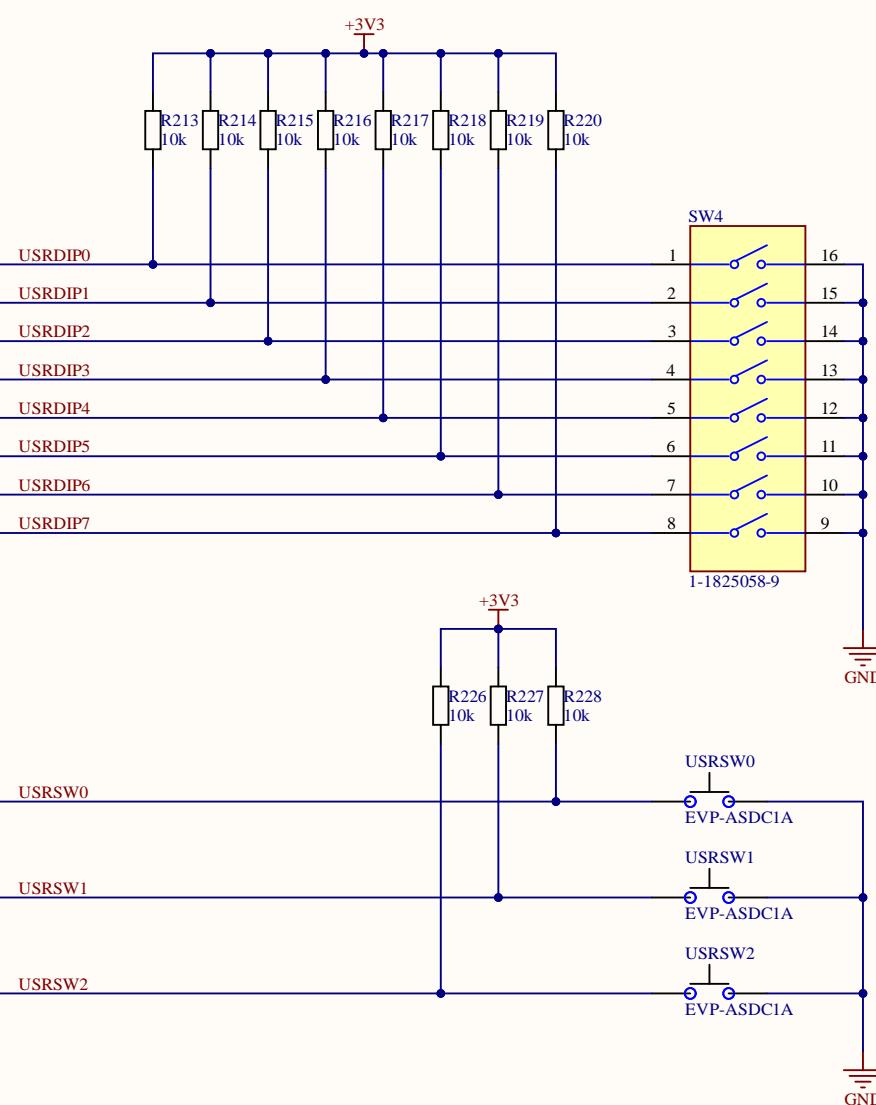
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File: CW310_Clocks.SchDoc

A

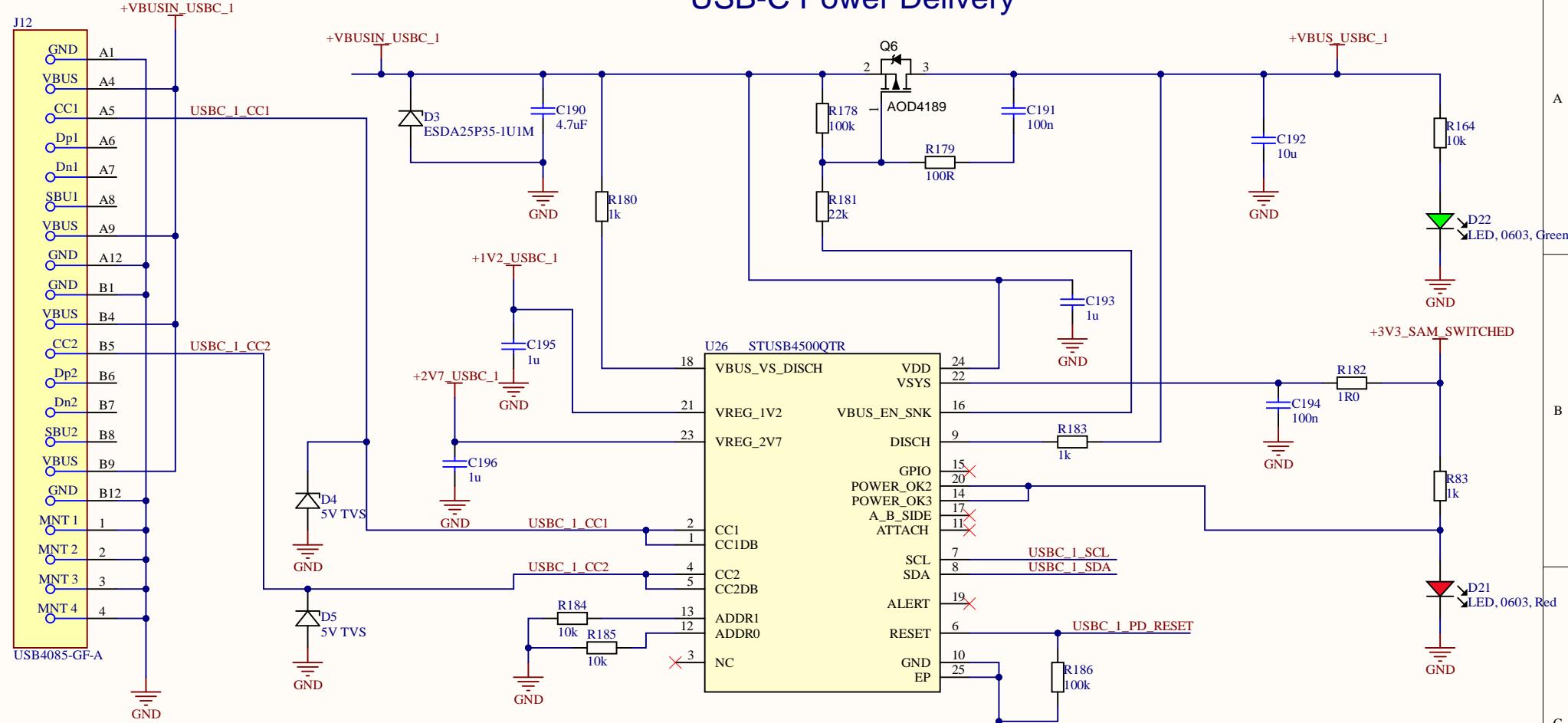


B



C

USB-C Power Delivery



Title: **USB-C PD Controller**

Approved:



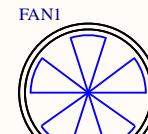
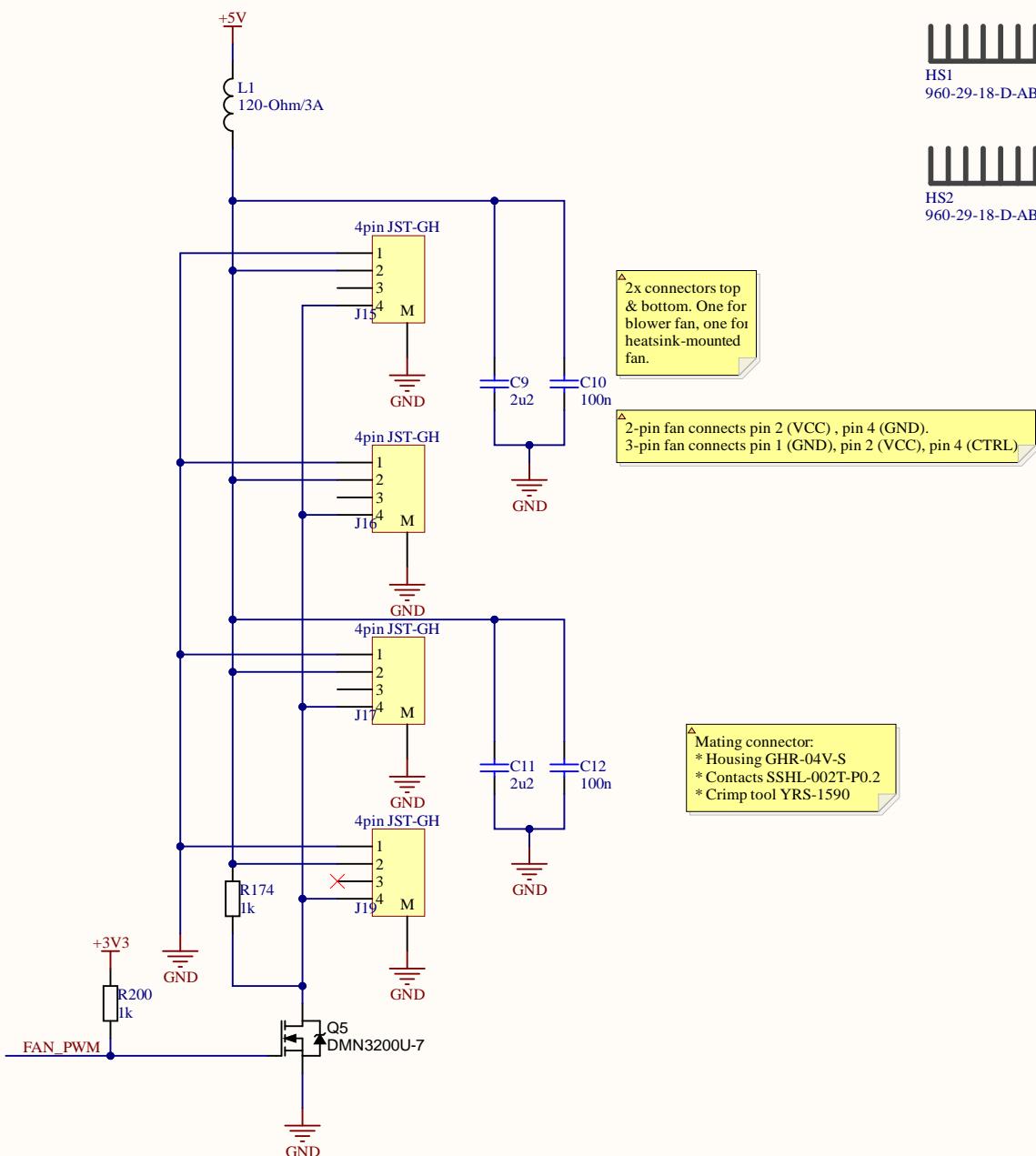
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File: CW310_USB_POWER.SchDoc



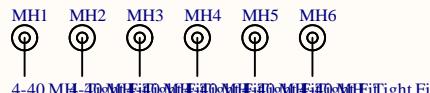
HS1
960-29-18-D-AB-0



HS2
960-29-18-D-AB-0

 Fan mounted top or bottom side of board. Blower style to pass over "open die top".

▲ Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.



Title: FAN Headers		 Approved: NO	
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