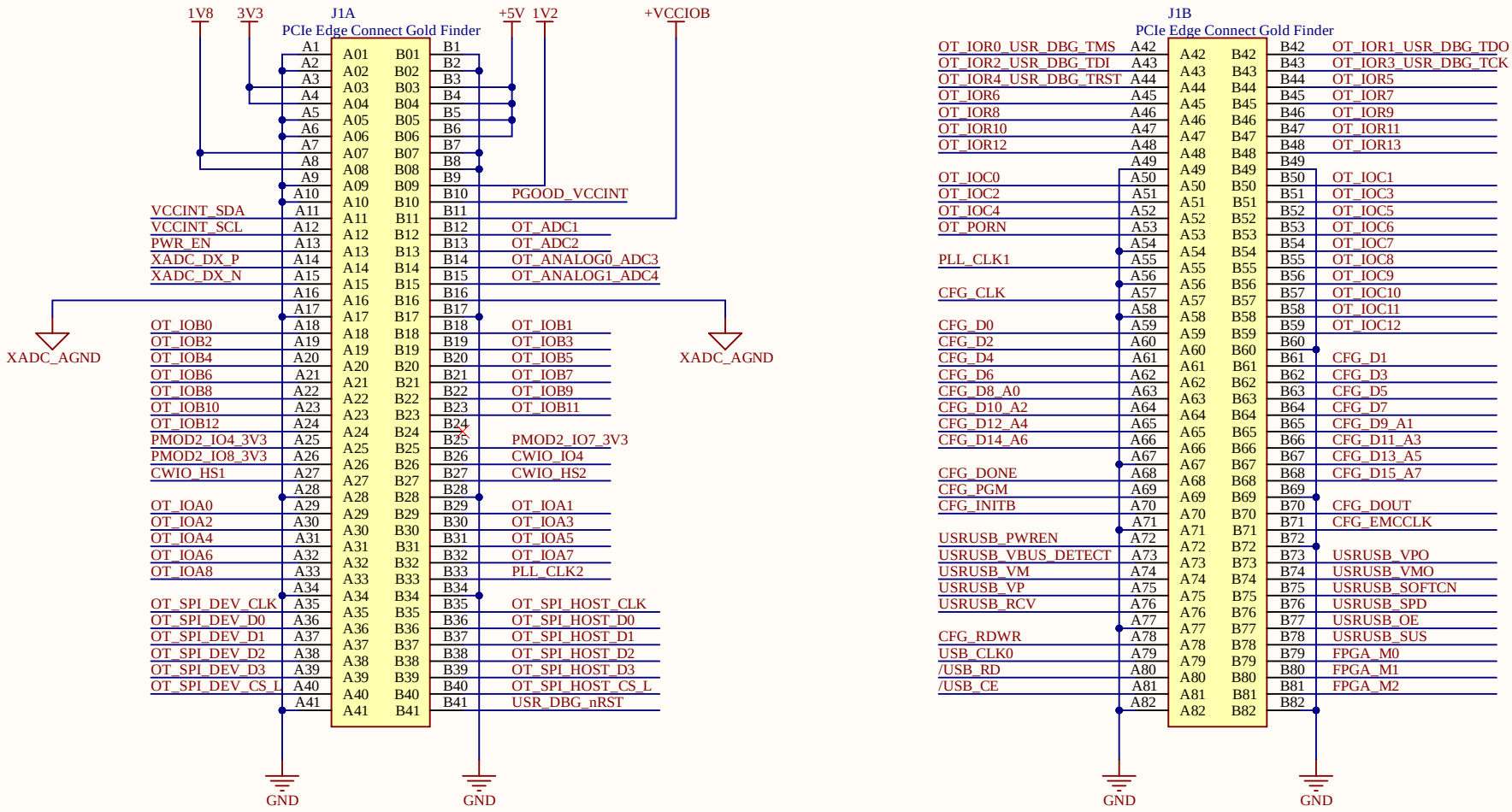

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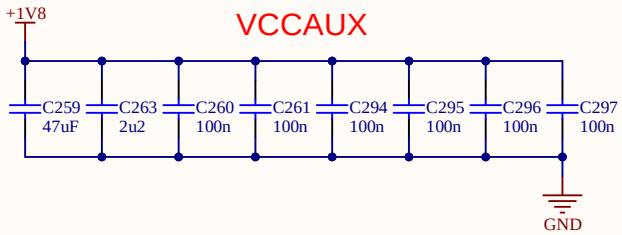
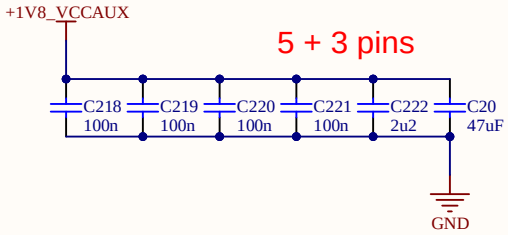
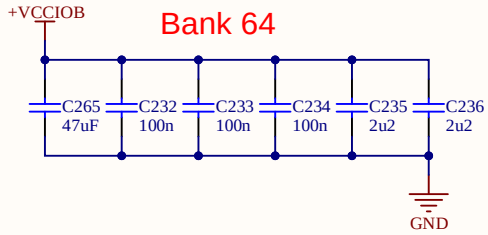
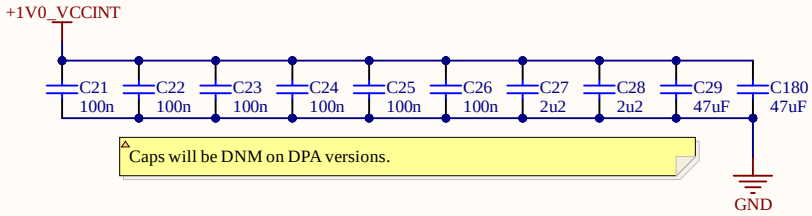
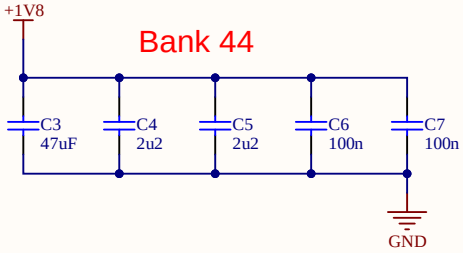
FPGA Decoupling

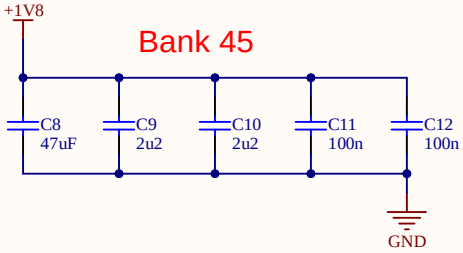


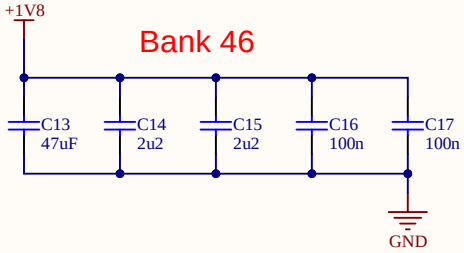


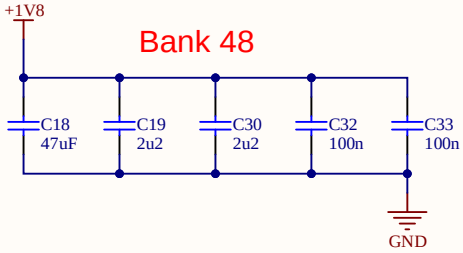


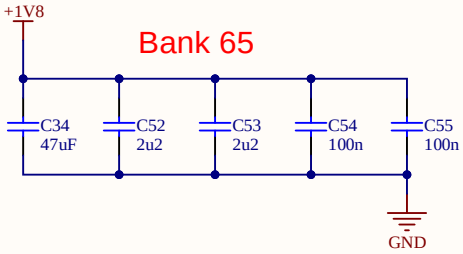


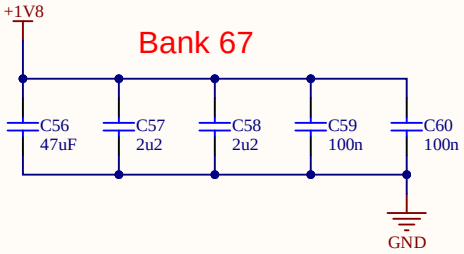


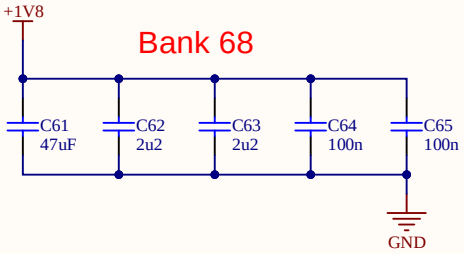












Title: **FPGA Decoupling**		Approved: No	NewAE Technology
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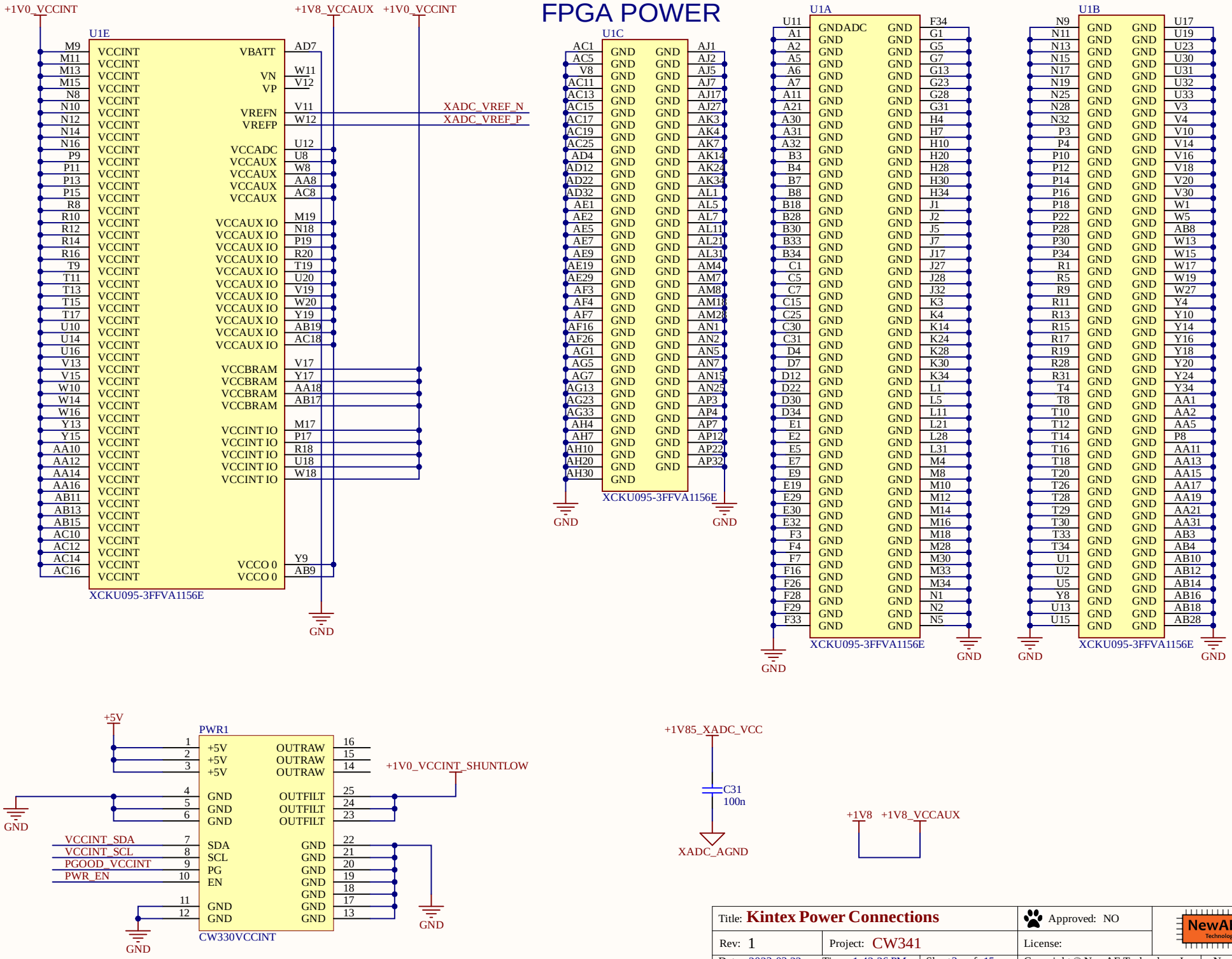
FPGA POWER



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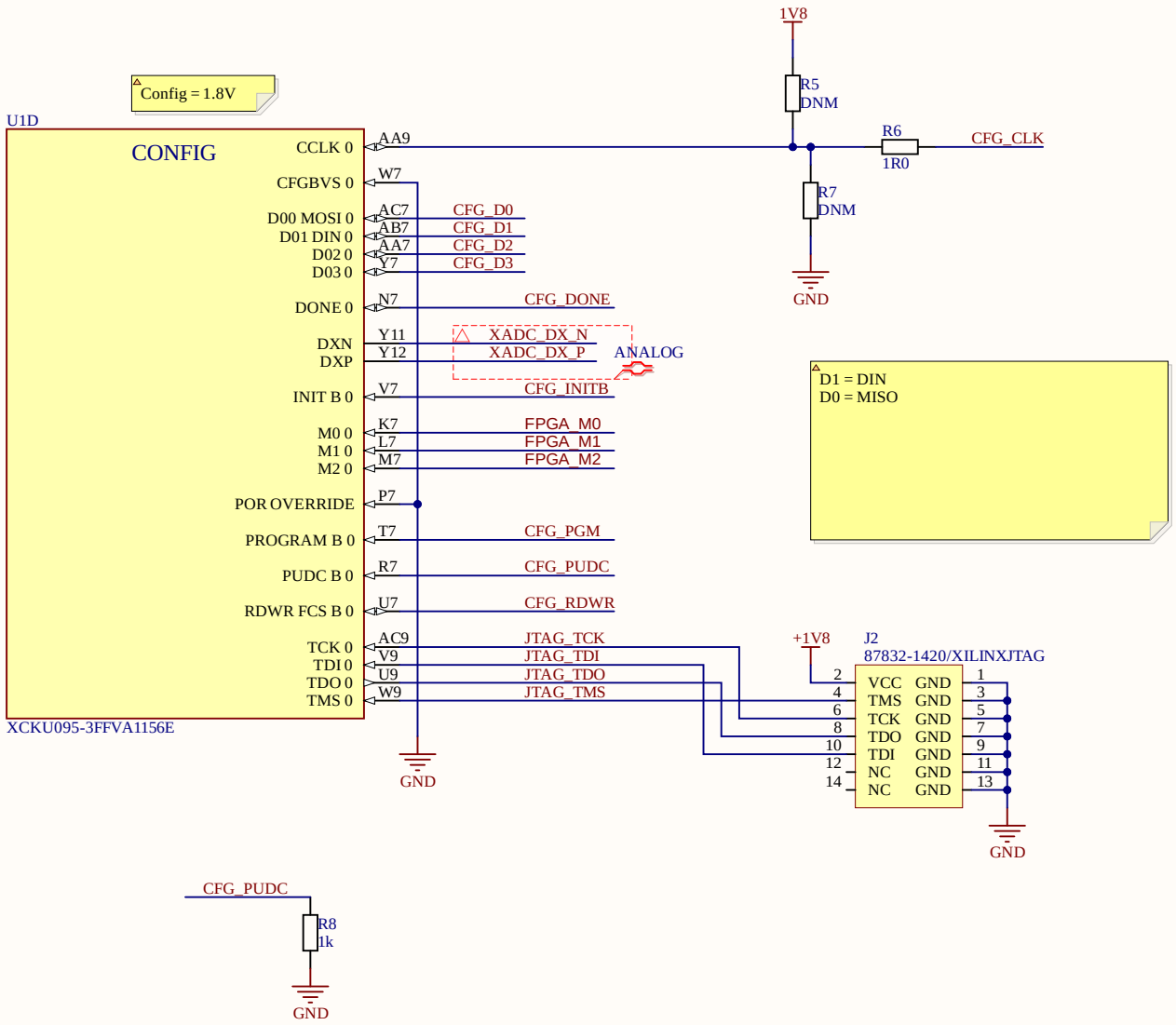

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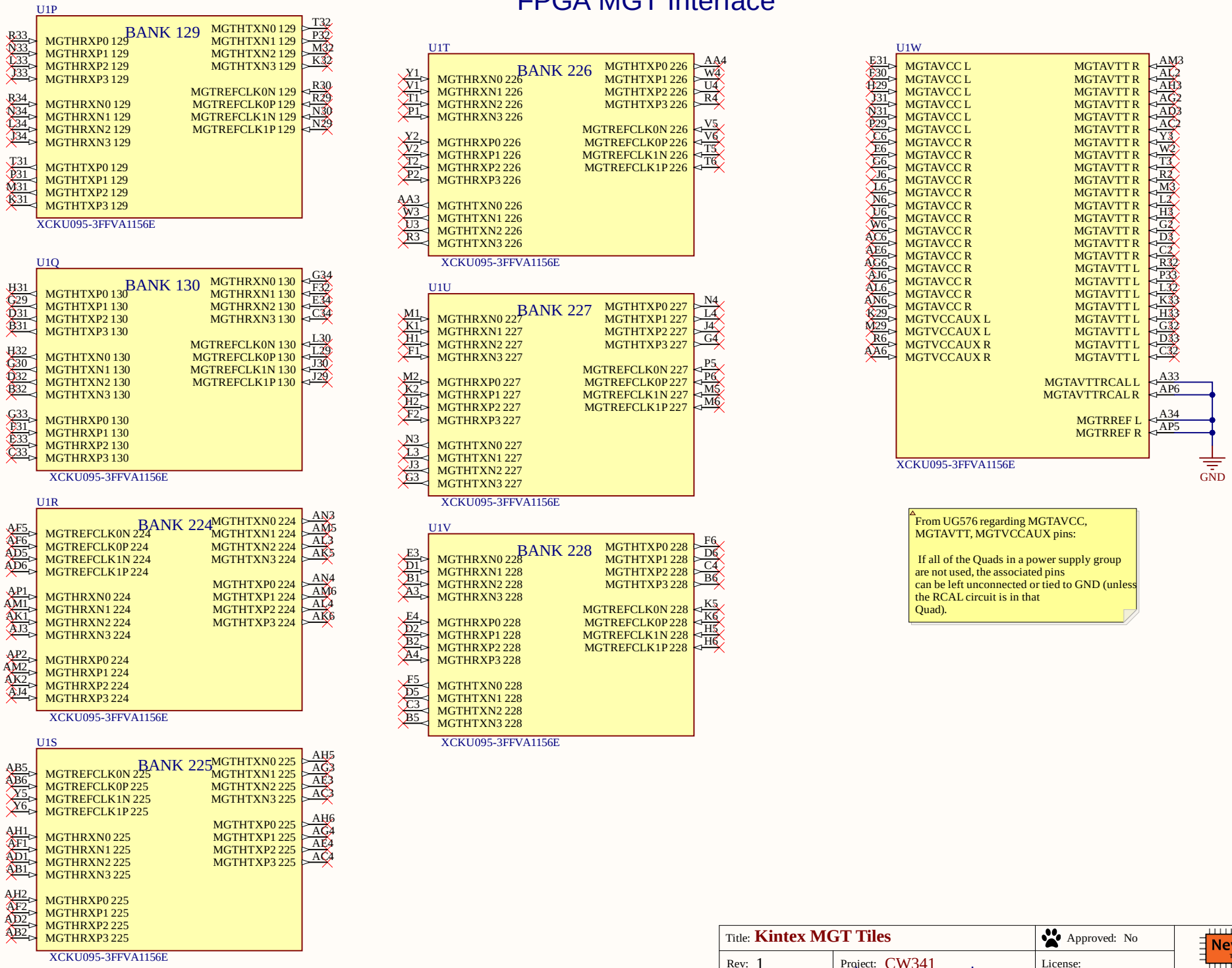
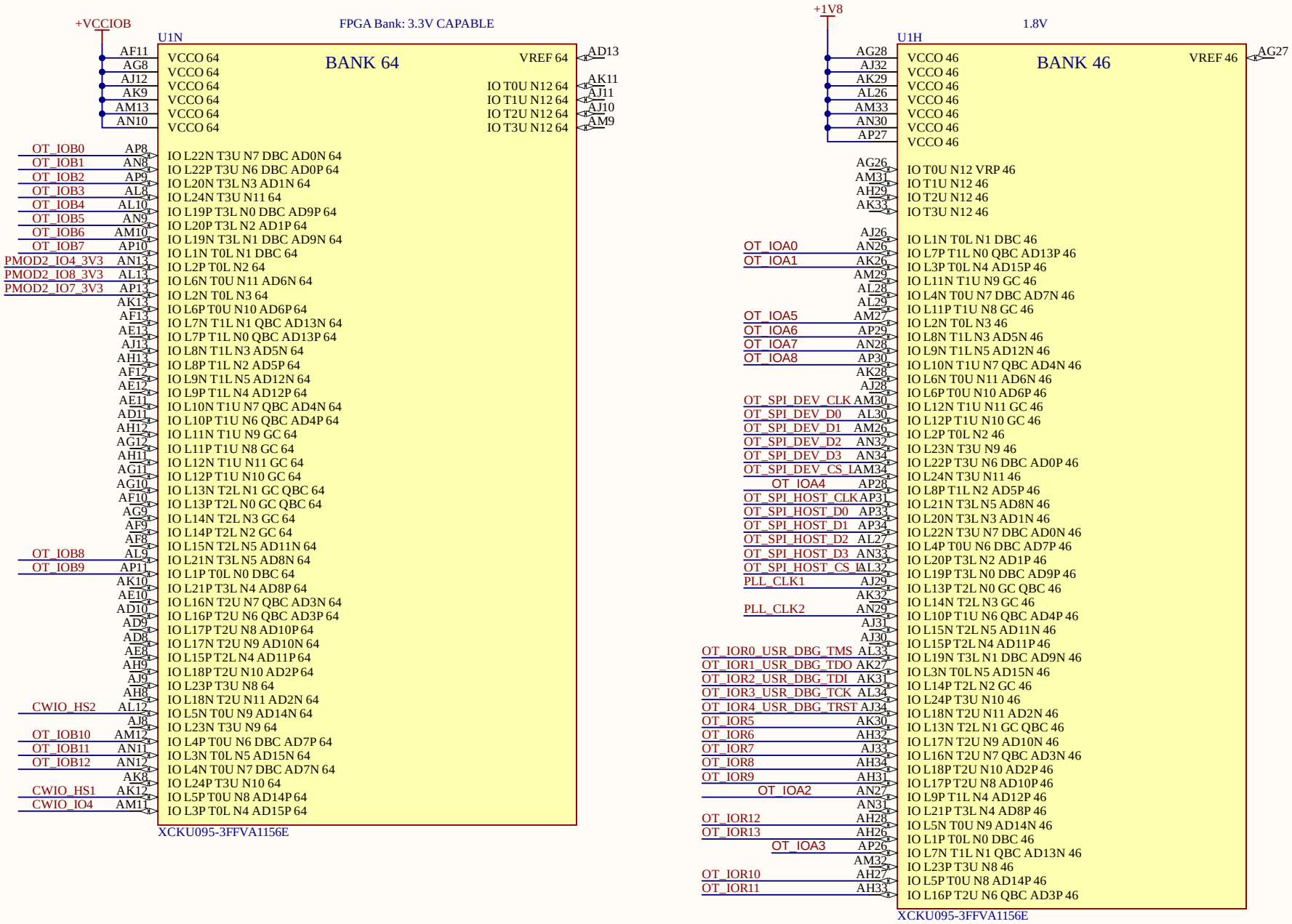
FPGA MGT Interface




+VCCIOB
FPGA Bank: 3.3V CAPABLE
U1N
BANK 64
VREF 64
AD13
VCCO 64
AF11
VCCO 64
AG8
VCCO 64
AJ12
VCCO 64
AK9
VCCO 64
AM13
VCCO 64
AN10
IO T0U N12 64
AK11
IO T1U N12 64
AJ11
IO T2U N12 64
AJ10
IO T3U N12 64
AM9
OT_IOB0 AP8 IO L22N T3U N7 DBC AD0N 64
OT_IOB1 AN8 IO L22P T3U N6 DBC AD0P 64
OT_IOB2 AP9 IO L20N T3L N3 AD1N 64
OT_IOB3 AL8 IO L24N T3U N11 64
OT_IOB4 AL10 IO L19P T3L N0 DBC AD9P 64
OT_IOB5 AN9 IO L20P T3L N2 AD1P 64
OT_IOB6 AM10 IO L19N T3L N1 DBC AD9N 64
OT_IOB7 AP10 IO L1N T0L N1 DBC 64
PMOD2_IO4_3V3 AN13 IO L2P T0L N2 64
PMOD2_IO8_3V3 AL13 IO L6N T0U N11 AD6N 64
PMOD2_IO7_3V3 AP13 IO L2N T0L N3 64
AK13 IO L6P T0U N10 AD6P 64
AF13 IO L7N T1L N1 QBC AD13N 64
AE13 IO L7P T1L N0 QBC AD13P 64
AJ13 IO L8N T1L N3 AD5N 64
AH13 IO L8P T1L N2 AD5P 64
AF12 IO L9N T1L N5 AD12N 64
AE12 IO L9P T1L N4 AD12P 64
AE11 IO L10N T1U N7 QBC AD4N 64
AD11 IO L10P T1U N6 QBC AD4P 64
AH12 IO L11N T1U N9 GC 64
AG12 IO L11P T1U N8 GC 64
AH11 IO L12N T1U N11 GC 64
AG11 IO L12P T1U N10 GC 64
AG10 IO L13N T2L N1 GC QBC 64
AF10 IO L13P T2L N0 GC QBC 64
AG9 IO L14N T2L N3 GC 64
AF9 IO L14P T2L N2 GC 64
AF8 IO L15N T2L N5 AD11N 64
OT_IOB8 AL9 IO L21N T3L N5 AD8N 64
OT_IOB9 AP11 IO L1P T0L N0 DBC 64
AK10 IO L21P T3L N4 AD8P 64
AE10 IO L16N T2U N7 QBC AD3N 64
AD10 IO L16P T2U N6 QBC AD3P 64
AD9 IO L17P T2U N8 AD10P 64
AD8 IO L17N T2U N9 AD10N 64
AE8 IO L15P T2L N4 AD11P 64
AH9 IO L18P T2U N10 AD2P 64
AJ9 IO L23P T3U N8 64
AH8 IO L18N T2U N11 AD2N 64
CWIO_HS2 AL12 IO L5N T0U N9 AD14N 64
AJ8 IO L23N T3U N9 64
OT_IOB10 AM12 IO L4P T0U N6 DBC AD7P 64
OT_IOB11 AN11 IO L3N T0L N5 AD15N 64
OT_IOB12 AN12 IO L4N T0U N7 DBC AD7N 64
AK8 IO L24P T3U N10 64
CWIO_HS1 AK12 IO L5P T0U N8 AD14P 64
CWIO_IO4 AM11 IO L3P T0L N4 AD15P 64
XCKU095-3FFVA1156E
+1V8
1.8V
U1H
BANK 46
VREF 46
AG27
VCCO 46
AG28
VCCO 46
AJ32
VCCO 46
AK29
VCCO 46
AL26
VCCO 46
AM33
VCCO 46
AN30
VCCO 46
AP27
VCCO 46
IO T0U N12 VRP 46
AG26
IO T1U N12 46
AM31
IO T2U N12 46
AH29
IO T3U N12 46
AK33
AJ26
OT_IOA0 AN26 IO L1N T0L N1 DBC 46
OT_IOA1 AK26 IO L7P T1L N0 QBC AD13P 46
AM29 IO L3P T0L N4 AD15P 46
AL28 IO L11N T1U N9 GC 46
AL29 IO L4N T0U N7 DBC AD7N 46
OT_IOA5 AM27 IO L11P T1U N8 GC 46
OT_IOA6 AP29 IO L2N T0L N3 46
OT_IOA7 AN28 IO L8N T1L N3 AD5N 46
OT_IOA8 AP30 IO L9N T1L N5 AD12N 46
AK28 IO L10N T1U N7 QBC AD4N 46
AJ28 IO L6N T0U N11 AD6N 46
OT_SPI_DEV_CLK AM30 IO L6P T0U N10 AD6P 46
OT_SPI_DEV_D0 AL30 IO L12N T1U N11 GC 46
OT_SPI_DEV_D1 AM26 IO L12P T1U N10 GC 46
OT_SPI_DEV_D2 AN32 IO L2P T0L N2 46
OT_SPI_DEV_D3 AN34 IO L23N T3U N9 46
OT_SPI_DEV_CS_I AM34 IO L22P T3U N6 DBC AD0P 46
OT_IOA4 AP28 IO L24N T3U N11 46
OT_SPI_HOST_CLK AP31 IO L8P T1L N2 AD5P 46
OT_SPI_HOST_D0 AP33 IO L21N T3L N5 AD8N 46
OT_SPI_HOST_D1 AP34 IO L20N T3L N3 AD1N 46
OT_SPI_HOST_D2 AL27 IO L22N T3U N7 DBC AD0N 46
OT_SPI_HOST_D3 AN33 IO L4P T0U N6 DBC AD7P 46
OT_SPI_HOST_CS_I AL32 IO L20P T3L N2 AD1P 46
PLL_CLK1 AJ29 IO L19P T3L N0 DBC AD9P 46
AK32 IO L13P T2L N0 GC QBC 46
PLL_CLK2 AN29 IO L14N T2L N3 GC 46
AJ31 IO L10P T1U N6 QBC AD4P 46
AJ30 IO L15N T2L N5 AD11N 46
OT_IOR0_USR_DBG_TMS AL33 IO L15P T2L N4 AD11P 46
OT_IOR1_USR_DBG_TDO AK27 IO L19N T3L N1 DBC AD9N 46
OT_IOR2_USR_DBG_TDI AK31 IO L3N T0L N5 AD15N 46
OT_IOR3_USR_DBG_TCK AL34 IO L14P T2L N2 GC 46
OT_IOR4_USR_DBG_TRST AJ34 IO L24P T3U N10 46
OT_IOR5 AK30 IO L18N T2U N11 AD2N 46
OT_IOR6 AH32 IO L13N T2L N1 GC QBC 46
OT_IOR7 AJ33 IO L17N T2U N9 AD10N 46
OT_IOR8 AH34 IO L16N T2U N7 QBC AD3N 46
OT_IOR9 AH31 IO L18P T2U N10 AD2P 46
OT_IOA2 AN27 IO L17P T2U N8 AD10P 46
AN31 IO L9P T1L N4 AD12P 46
OT_IOR12 AH28 IO L21P T3L N4 AD8P 46
OT_IOR13 AH26 IO L5N T0U N9 AD14N 46
OT_IOA3 AP26 IO L1P T0L N0 DBC 46
AM32 IO L7N T1L N1 QBC AD13N 46
OT_IOR10 AH27 IO L23P T3U N8 46
OT_IOR11 AH33 IO L5P T0U N8 AD14P 46
IO L16P T2U N6 QBC AD3P 46
XCKU095-3FFVA1156E
Title: Kintex IO Banks
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Rev: 1
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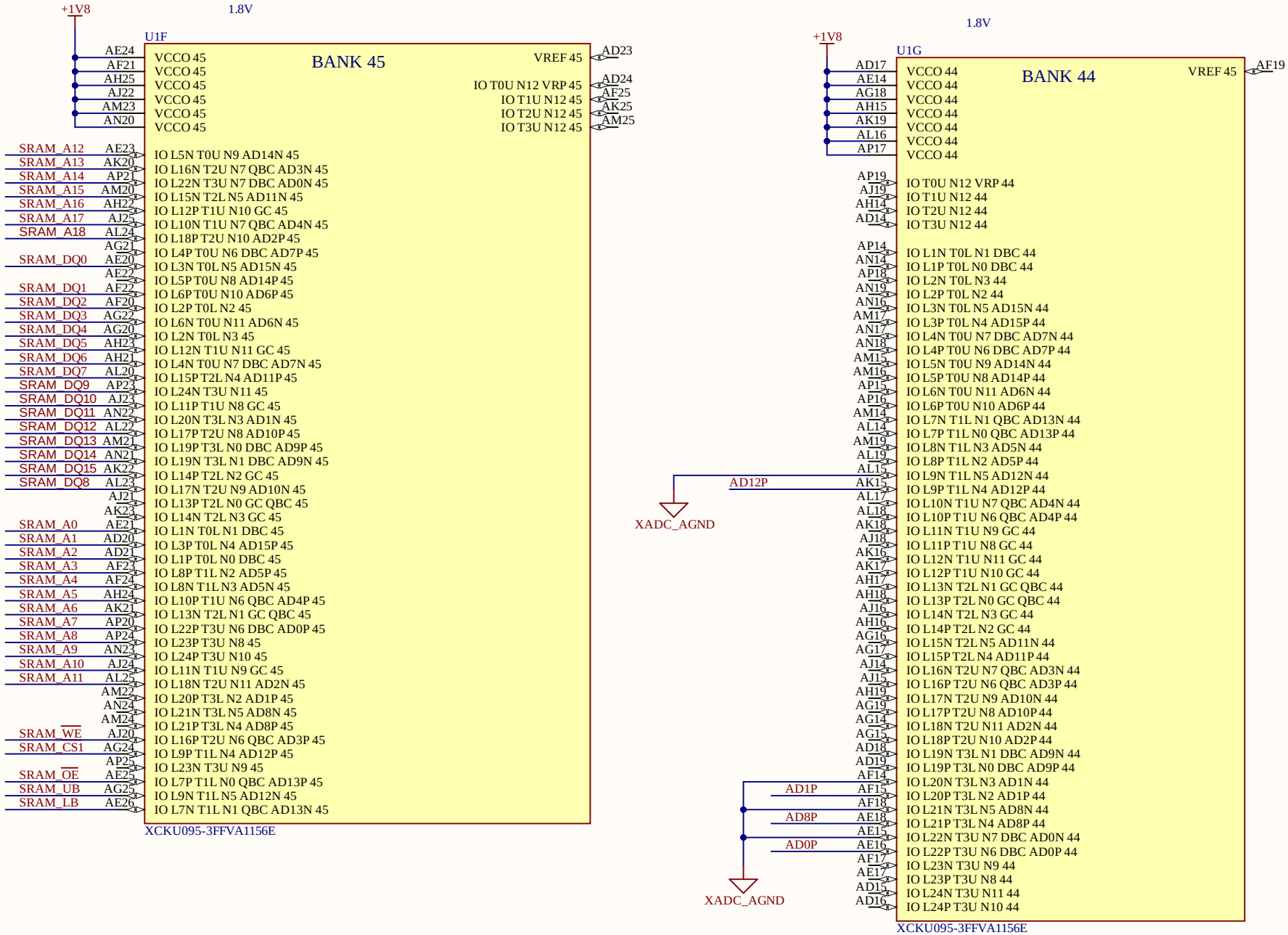
FPGA Bank: VCCIOA



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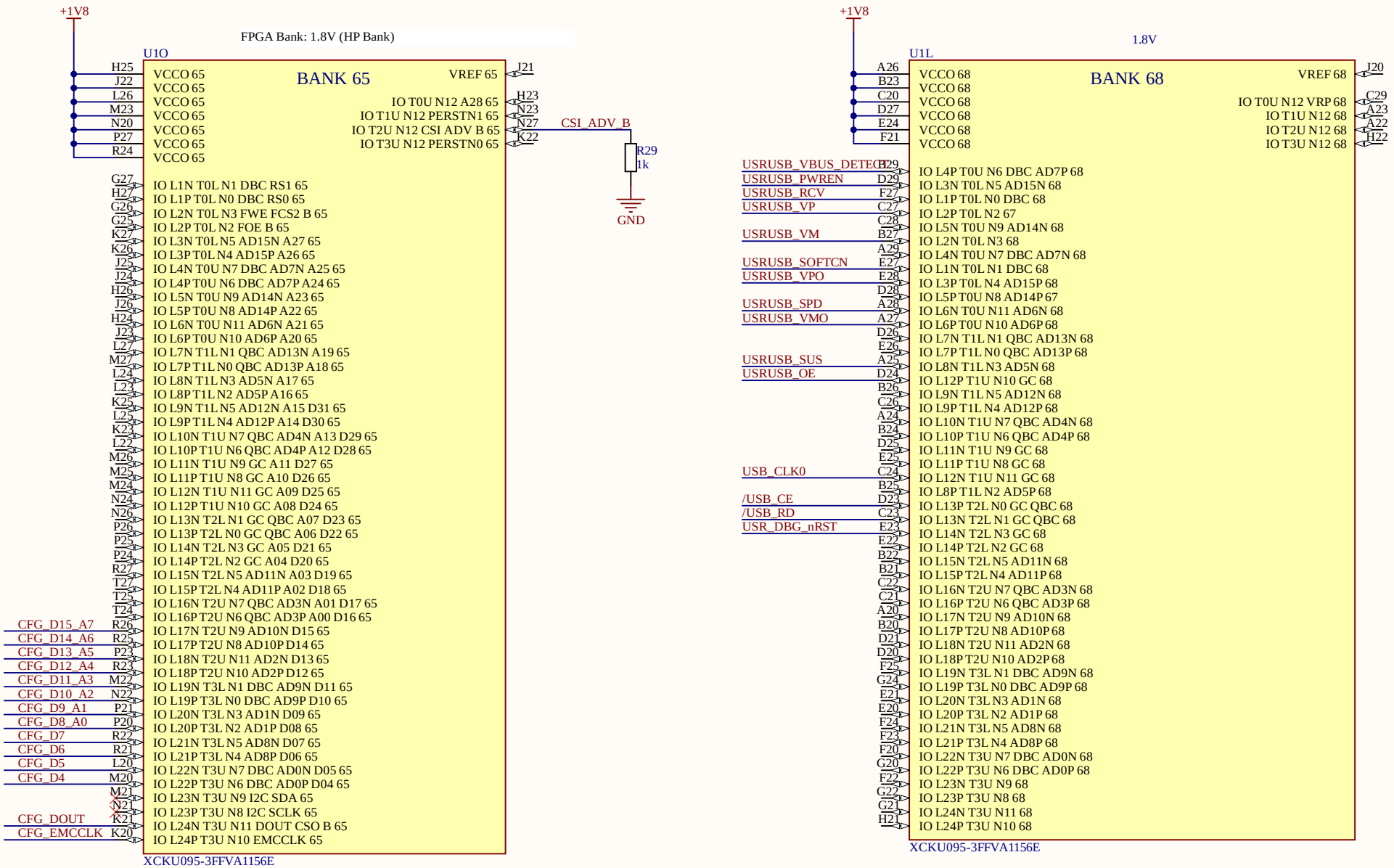

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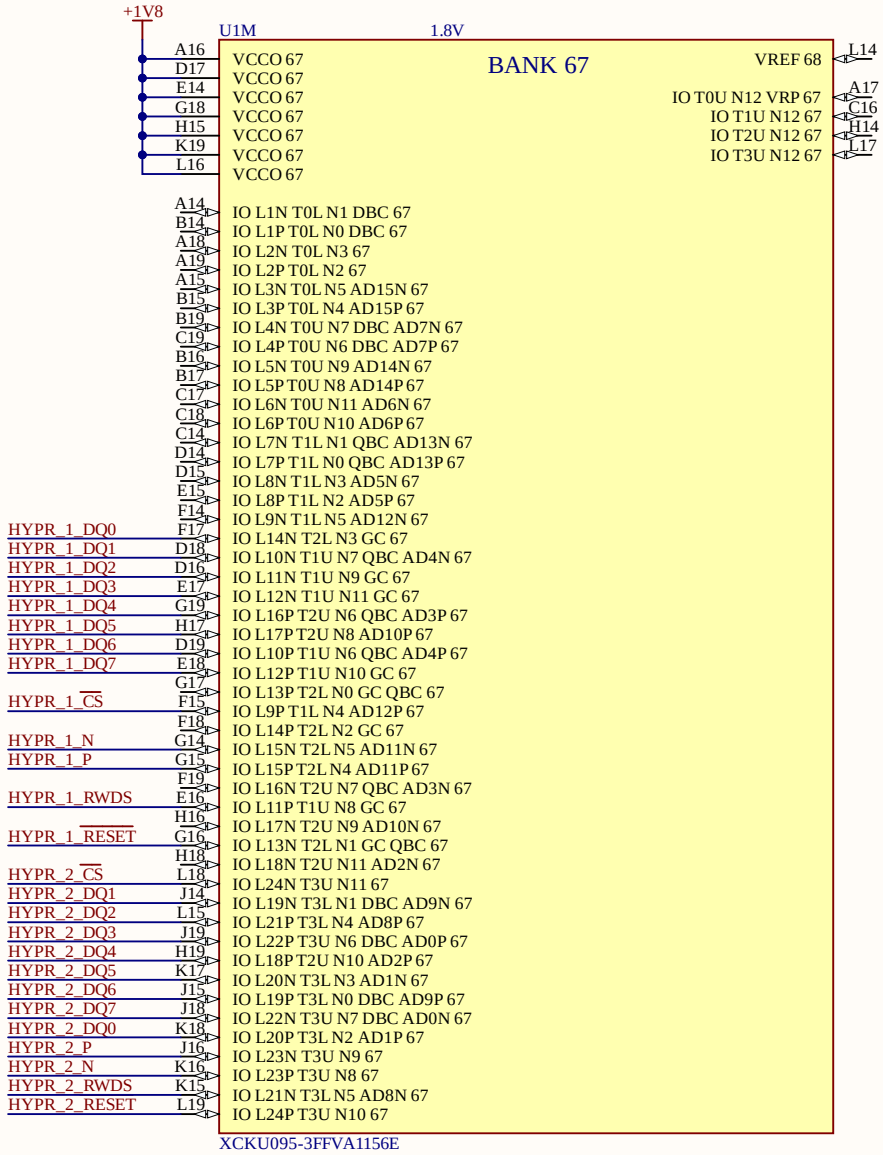

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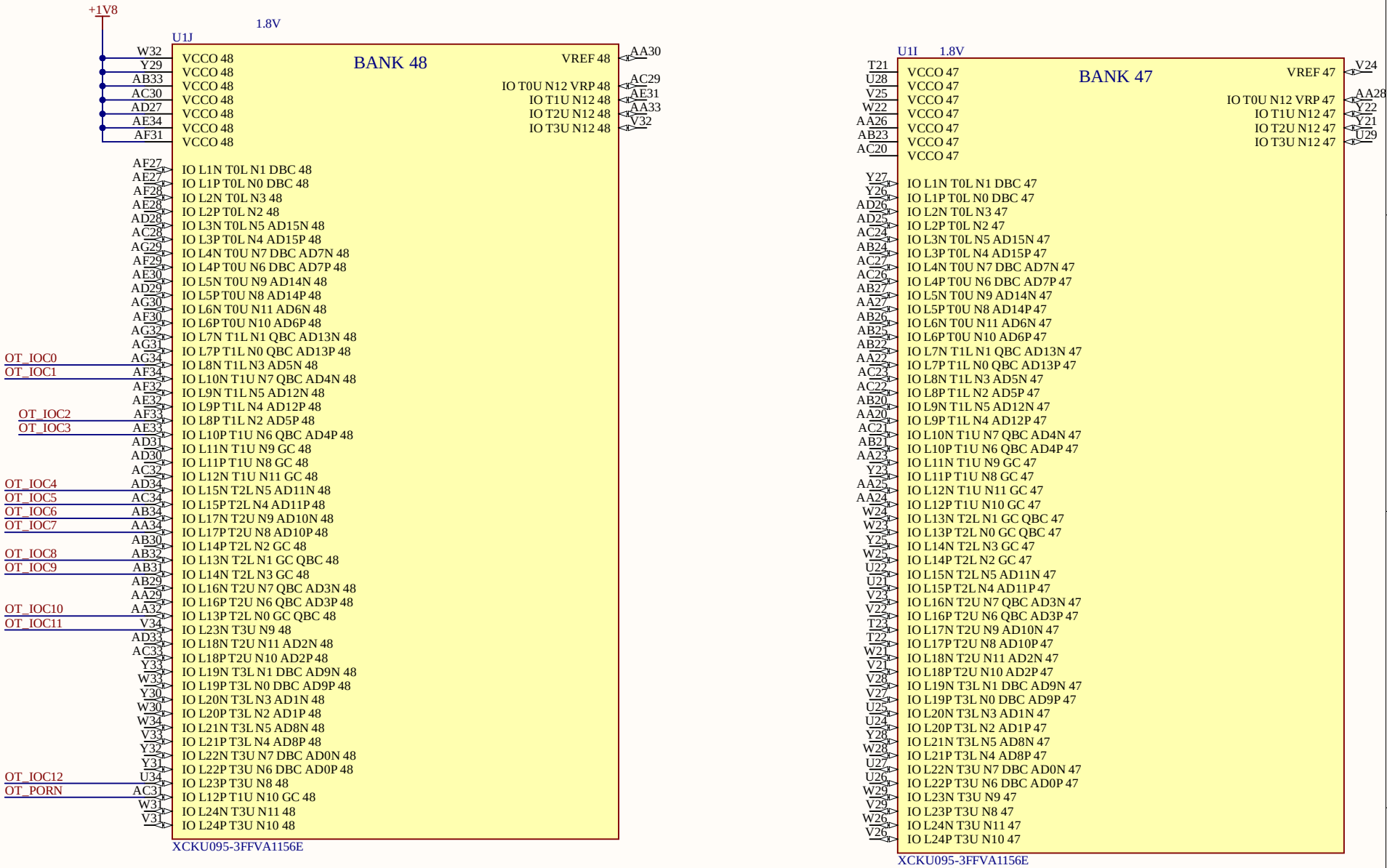

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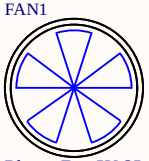
FAN1



Blower Fan, 5V, 35x35mm

Fan mounted top or bottom side of board. Blower style to pass over "open die top".

Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.

Title: **Heatsink and Fan**		Approved: NO	NewAE Technology
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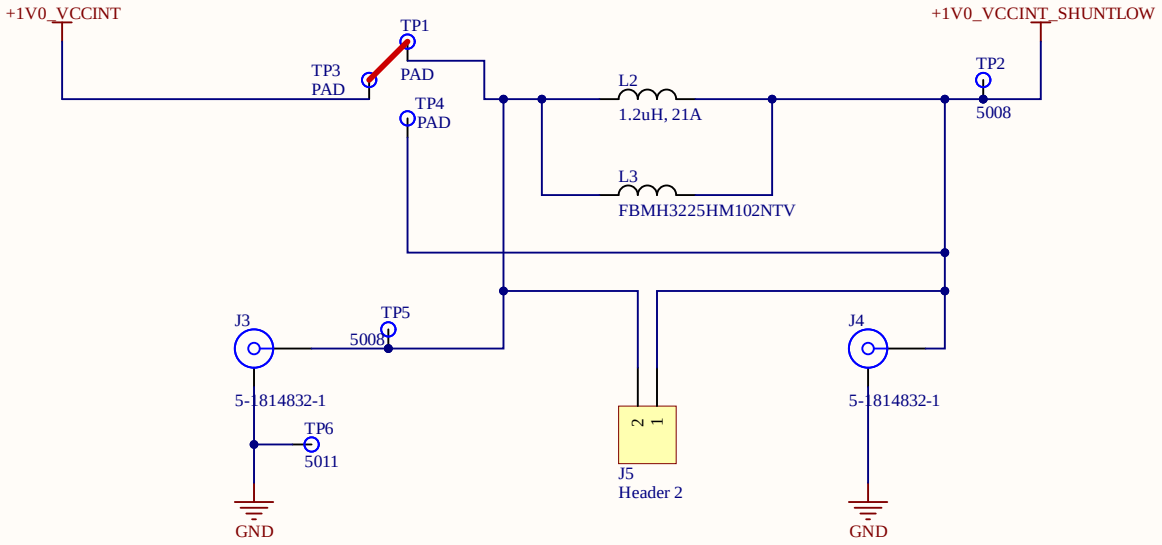
File: CW341_HeatsinkFan.SchDoc			



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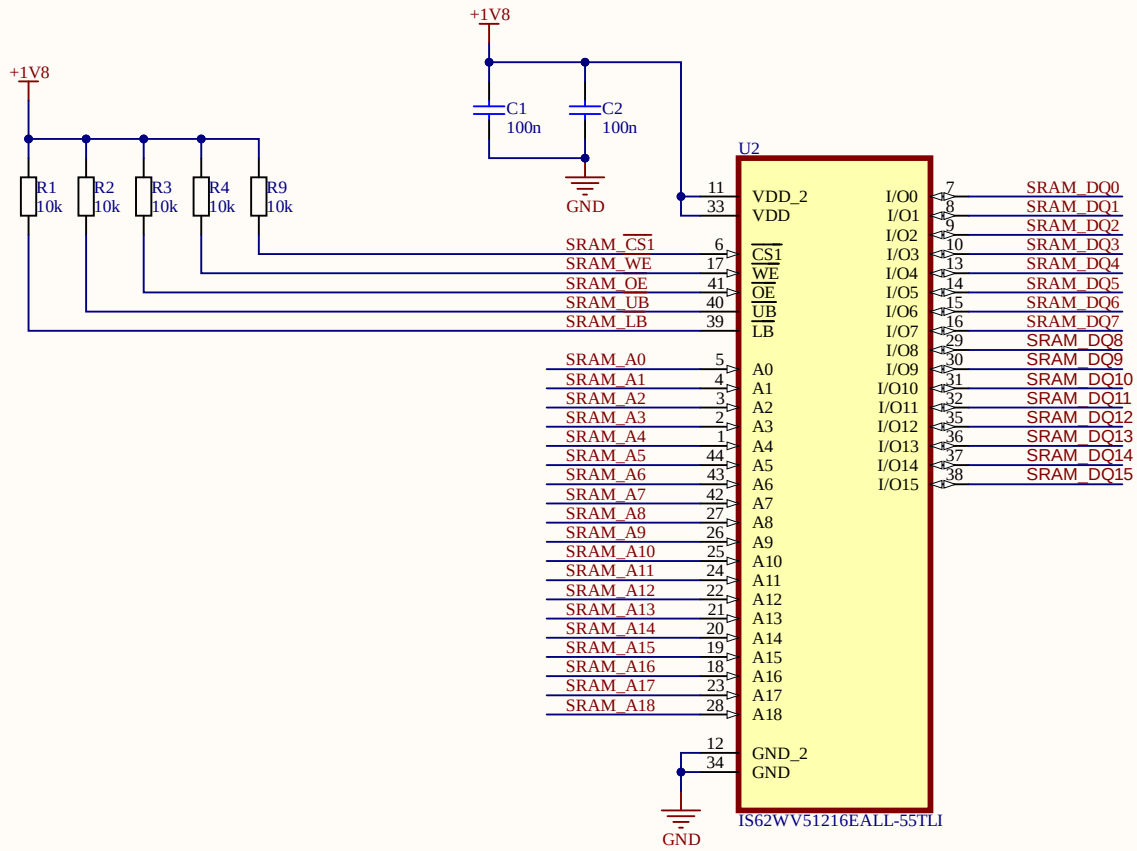

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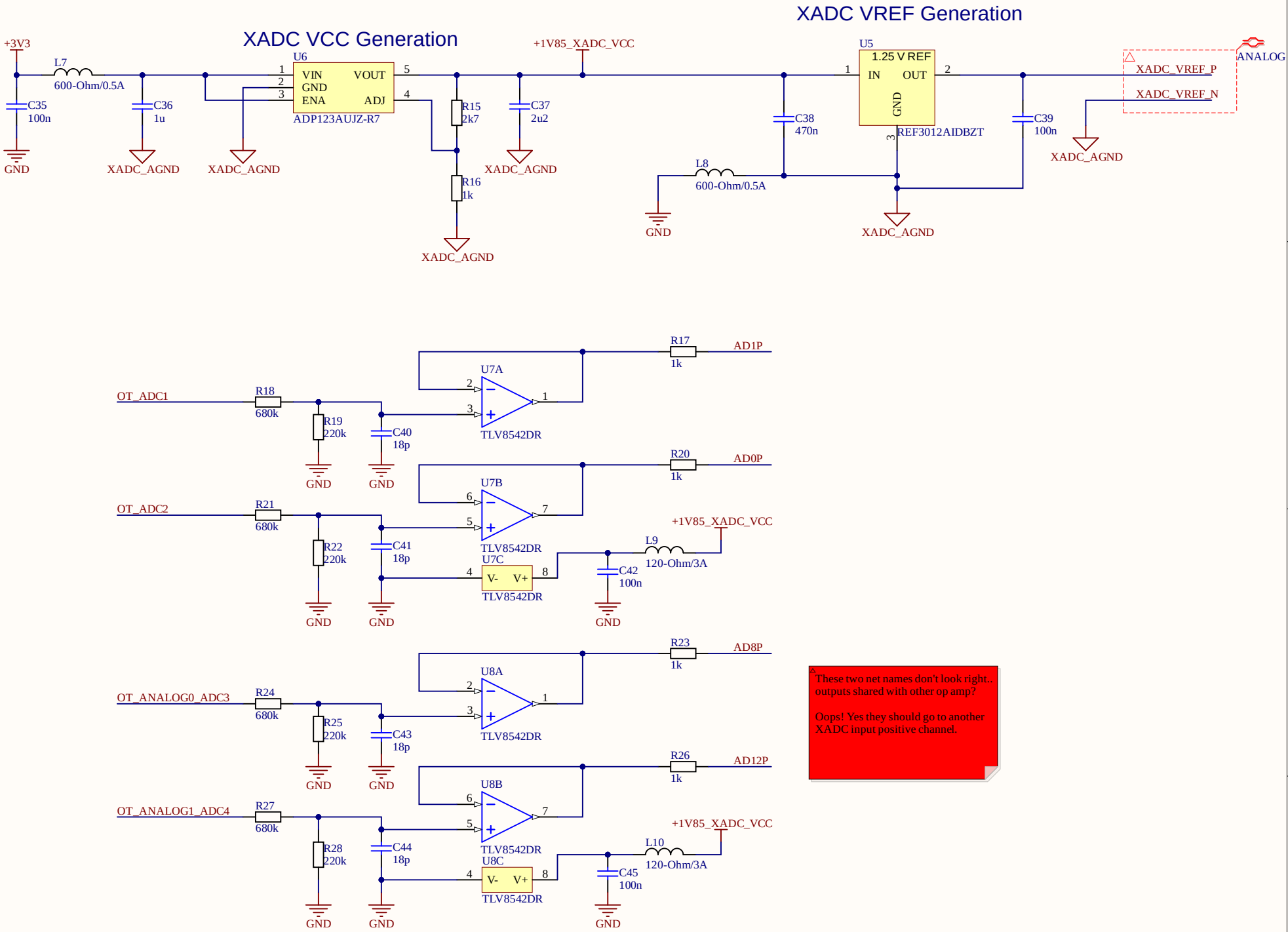
File: CW341_SRAM.SchDoc			


XADC VCC Generation
XADC VREF Generation
+3V3
L7
600-Ohm/0.5A
C35
100n
C36
1u
GND
XADC_AGND
U6
VIN
VOUT
GND
ENA
ADJ
ADP123AUJZ-R7
R15
2k7
R16
1k
C37
2u2
+1V85_XADC_VCC
U5
1.25 V REF
IN
OUT
GND
REF3012AIDBZT
C38
470n
L8
600-Ohm/0.5A
C39
100n
ANALOG
XADC_VREF_P
XADC_VREF_N
OT_ADC1
R18
680k
R19
220k
C40
18p
U7A
TLV8542DR
R17
1k
AD1P
OT_ADC2
R21
680k
R22
220k
C41
18p
U7B
U7C
V-
V+
R20
AD0P
L9
120-Ohm/3A
C42
100n
OT_ANALOG0_ADC3
R24
680k
R25
220k
C43
18p
U8A
R23
AD8P
OT_ANALOG1_ADC4
R27
680k
R28
220k
C44
18p
U8B
U8C
R26
AD12P
L10
120-Ohm/3A
C45
100n
These two net names don't look right.. outputs shared with other op amp?
Oops! Yes they should go to another XADC input positive channel.
Title: CW341 XADC
Approved: NO
Rev: 1
Project: CW341
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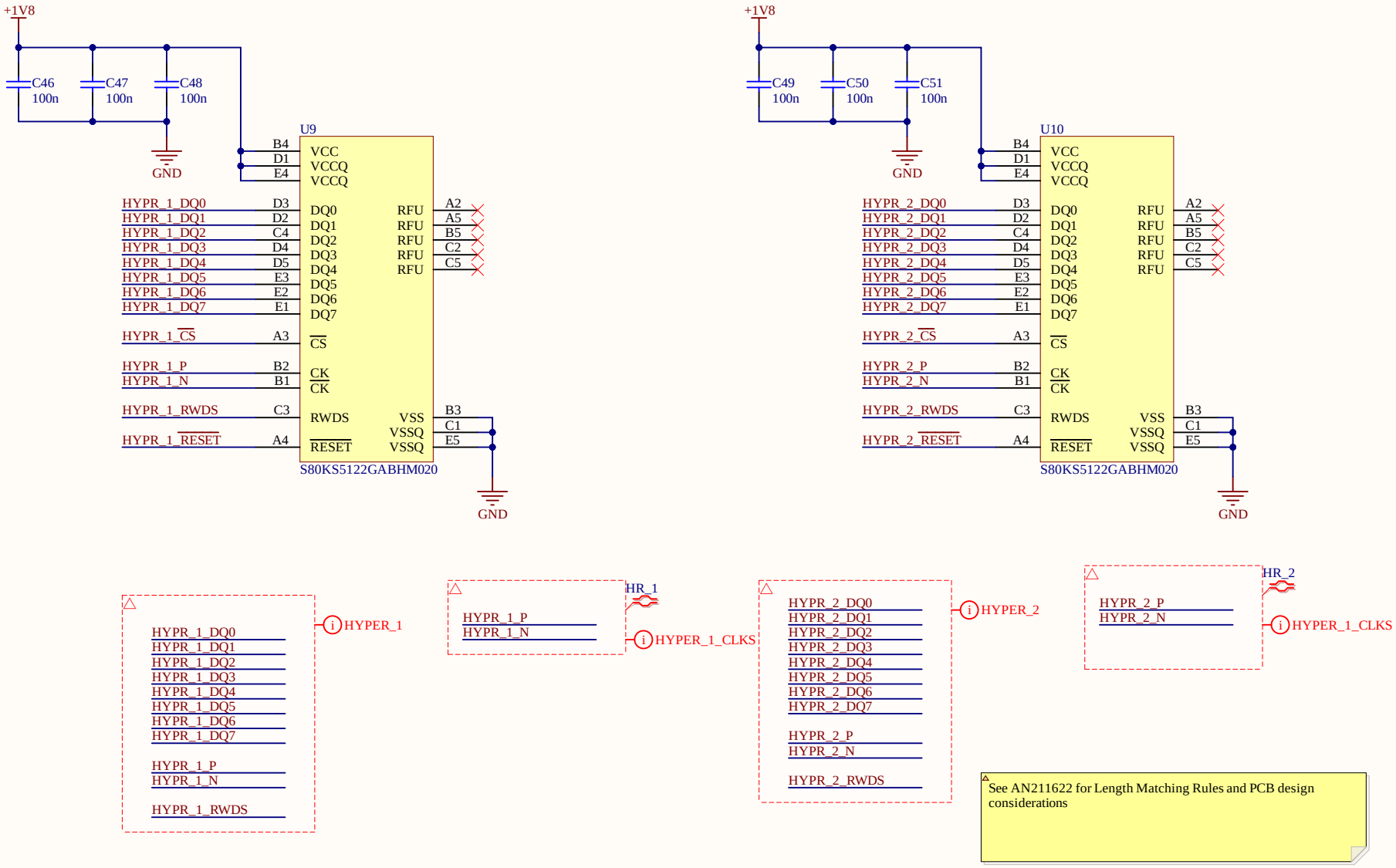

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