

ChipWhisperer CW340 "Luna Board" - Xilinx Kintex Ultrascale Target Board

NewAE Technology Inc.

Table of Contents

Revision Summary

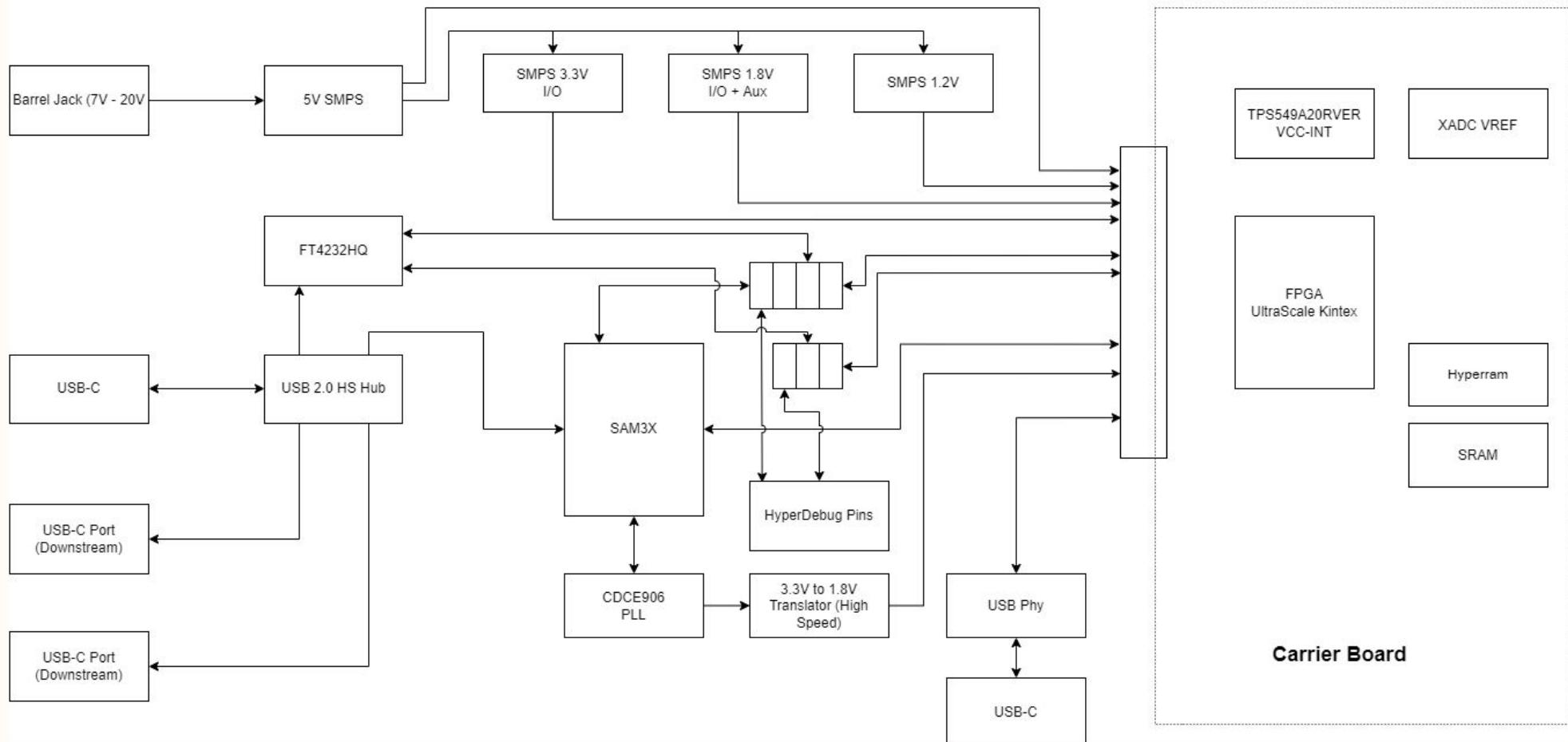
- 00: Ultra-alpha.
- 02: Test version.
- 03: First Beta

Title: Bergen Board - The Cover Sheet		Approved: Yes	
Rev: 03	Project: CW340 .	License: TBD	
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File: CW340_Cover_Page.SchDoc			

A

A

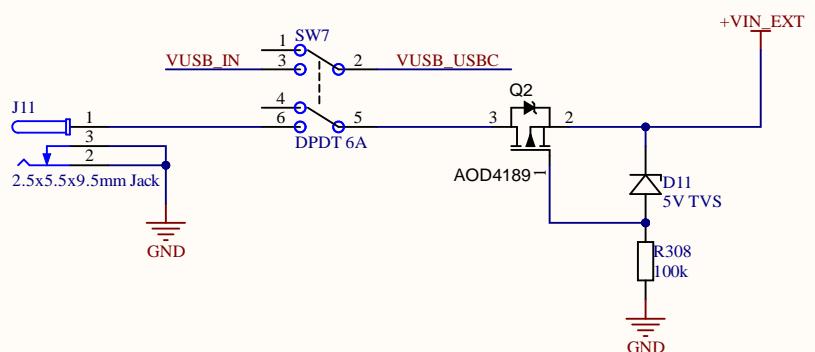
Block Diagram


Carrier Board

Title: Block Diagram		Approved: *	
Rev: 03	Project: CW340 *	License: TBD	
Date: 2023-03-21	Time: 12:08:01 PM	Sheet 2 of 31	Copyright © NewAE Technology Inc. NewAE.com
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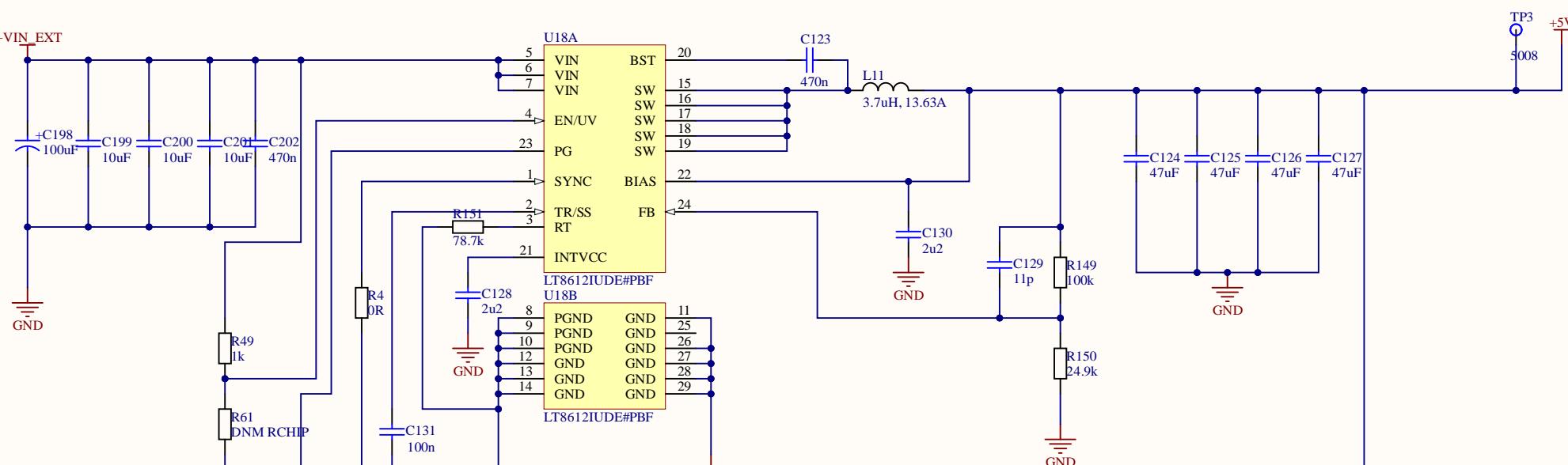
INPUT POWER

A



A

B



B

C

△ Check R149/R150!

△ Based on design from
<https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=9C49F428E2C4FF82>

Title: **5V Regulator**

Approved: Yes

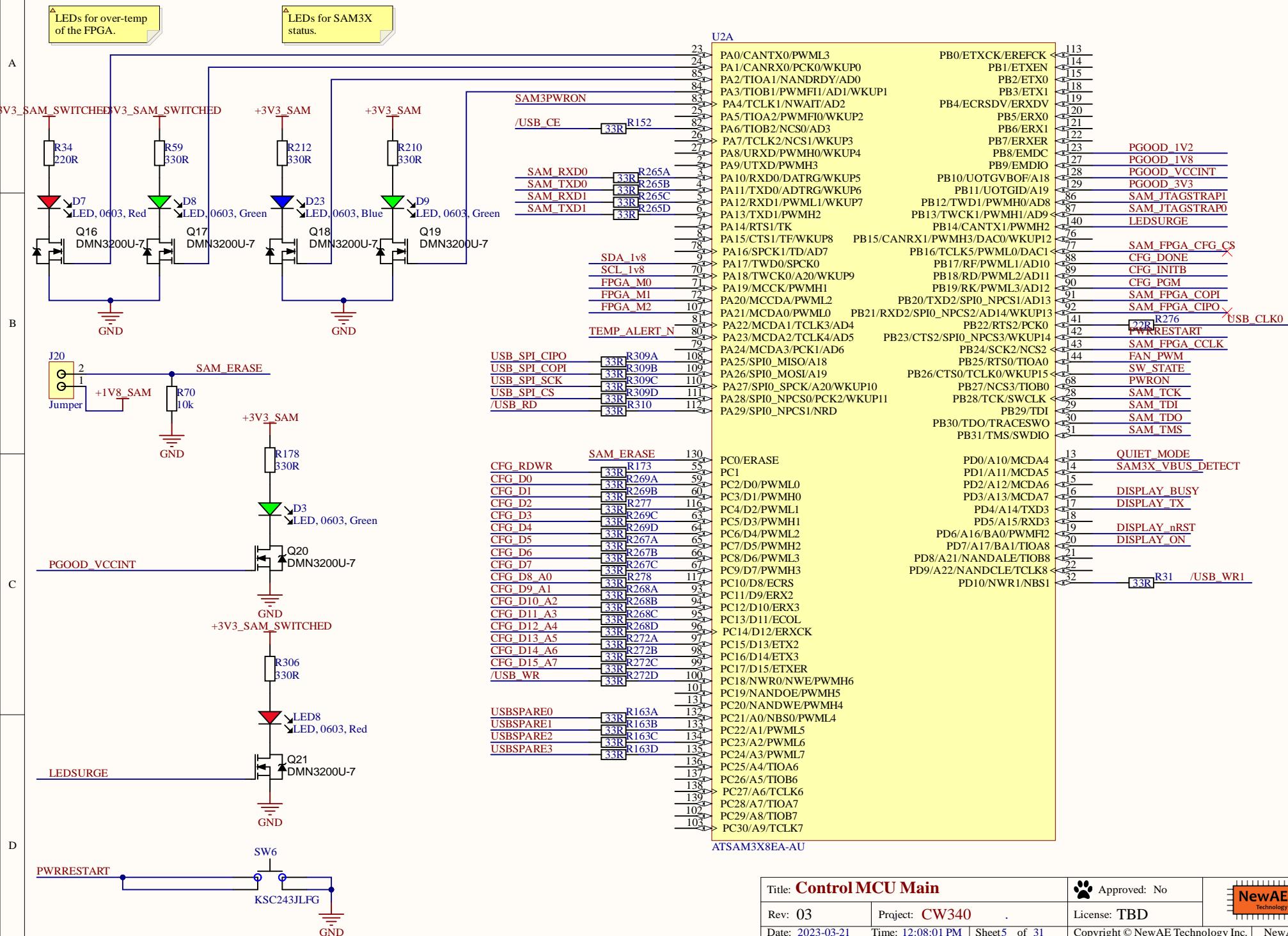


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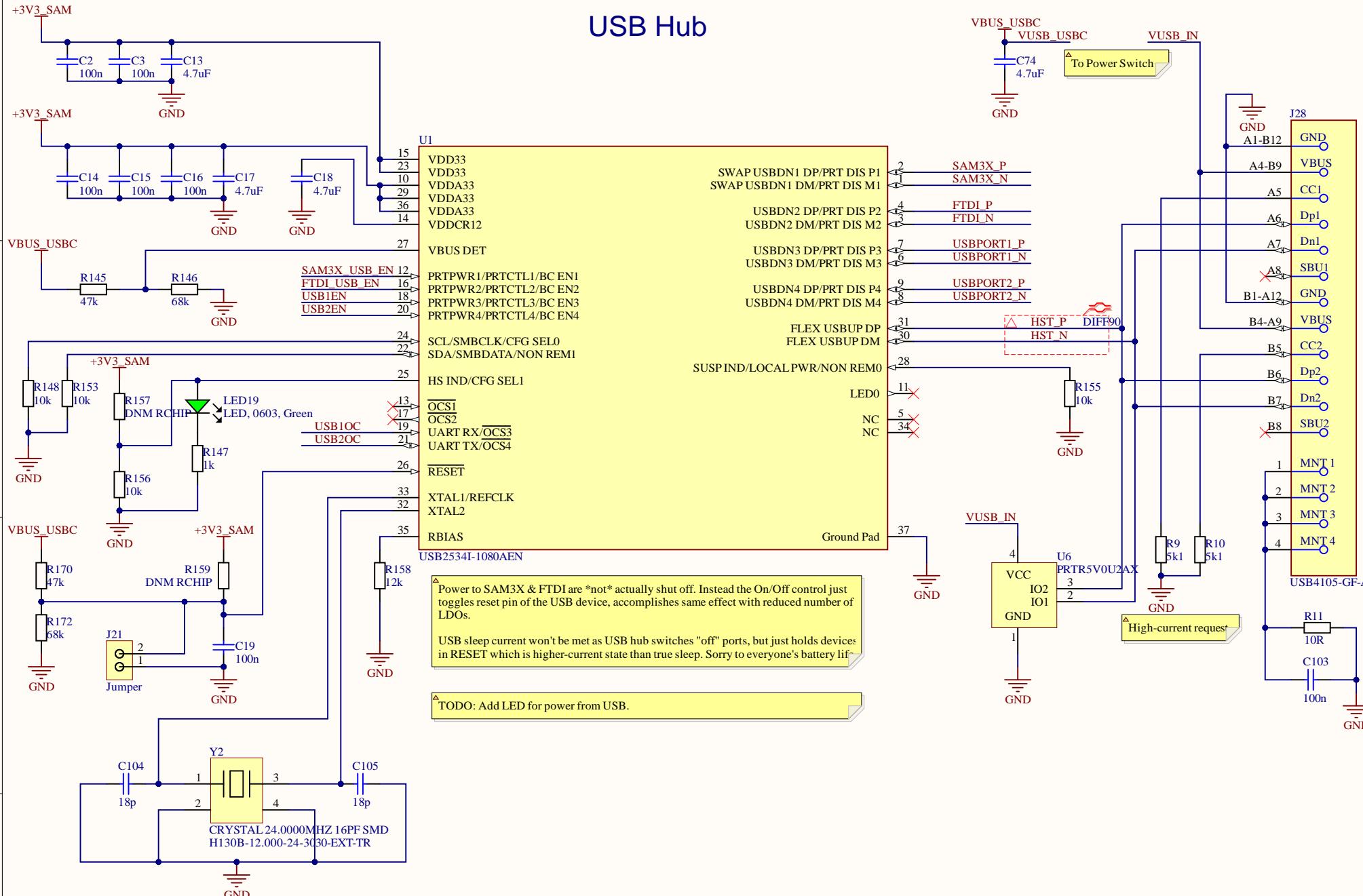
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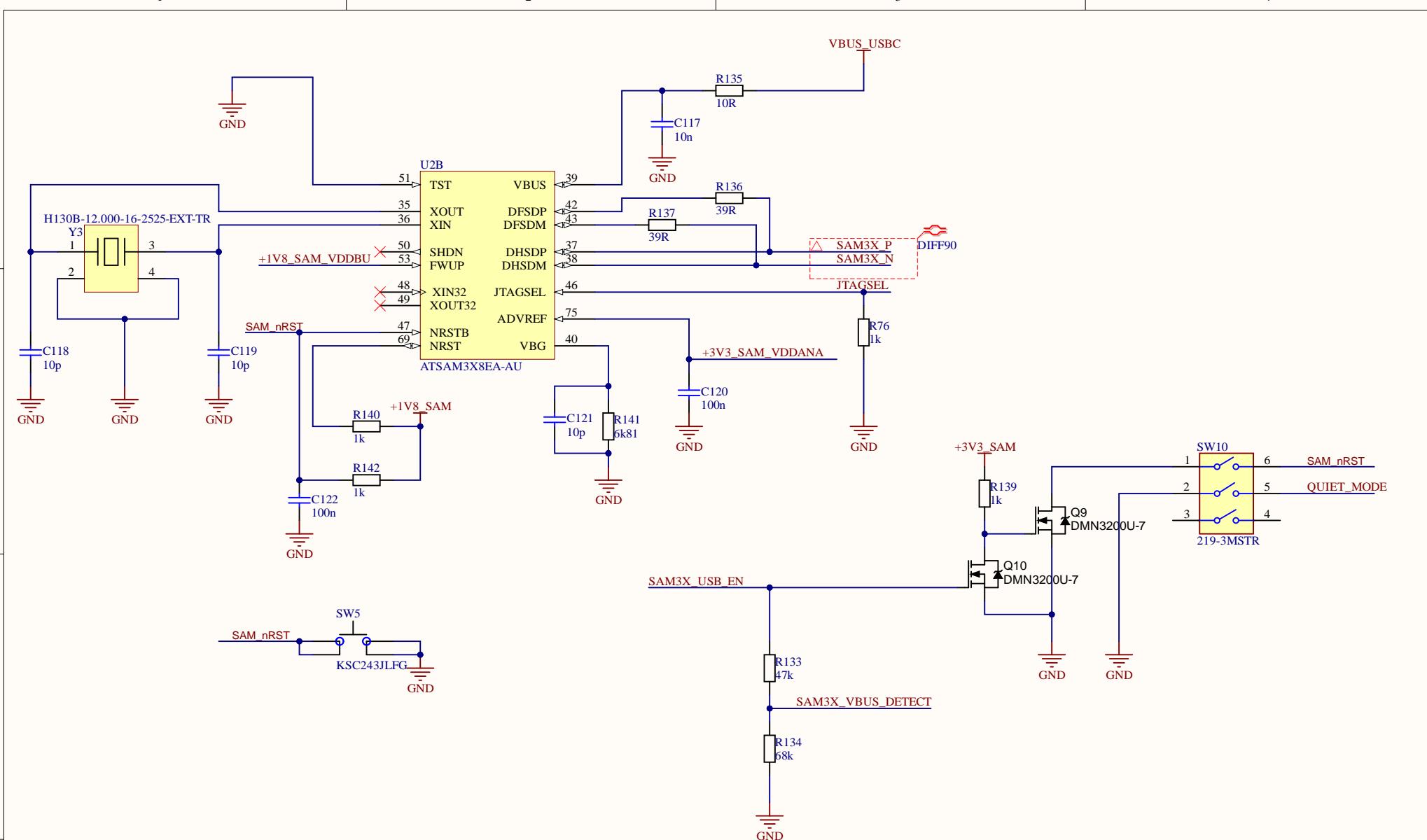
SAM3X CPU

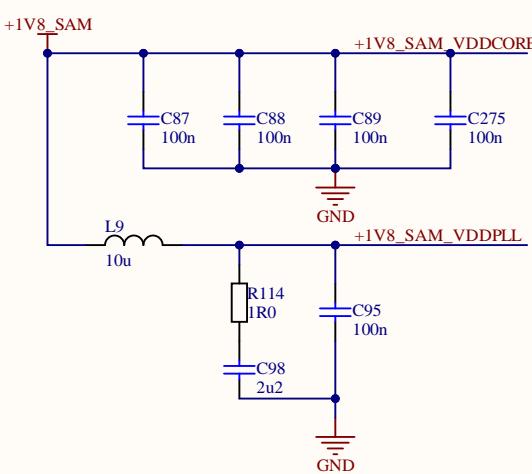
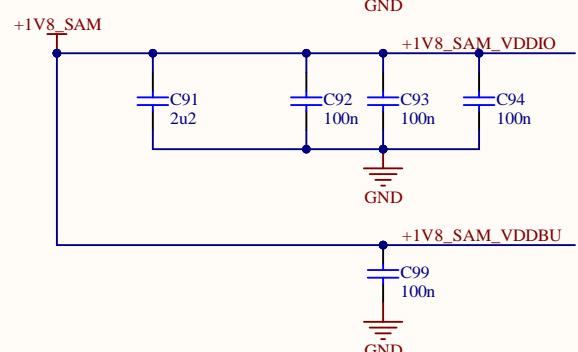
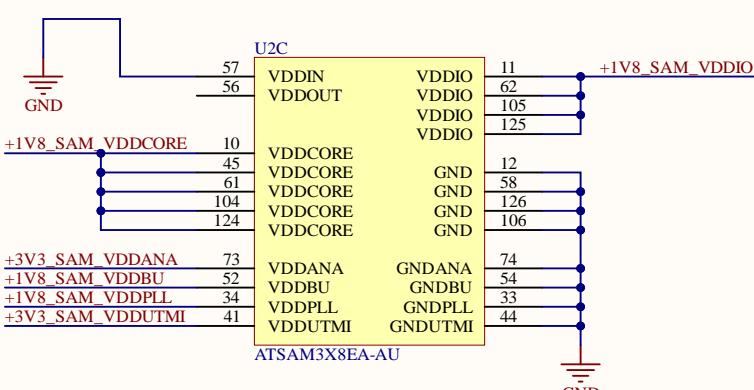
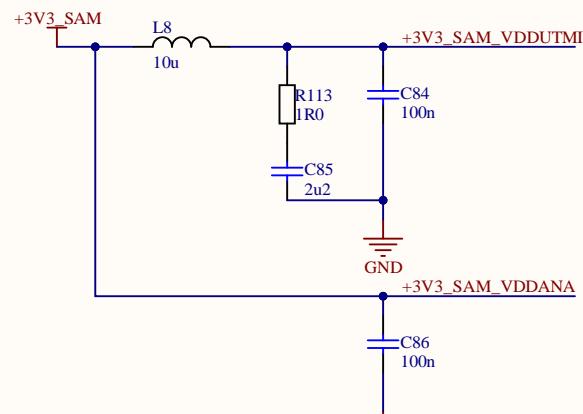
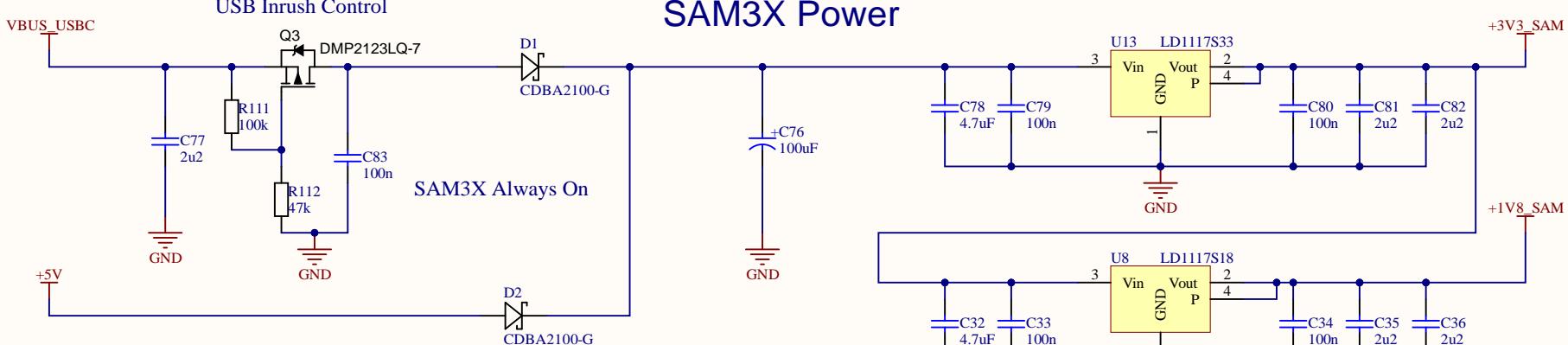


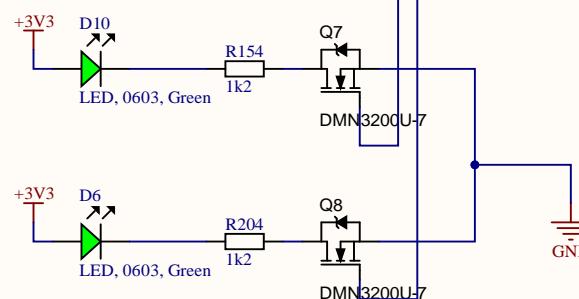
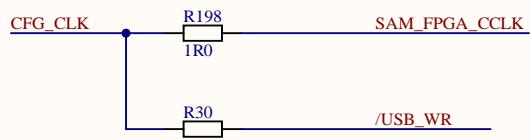
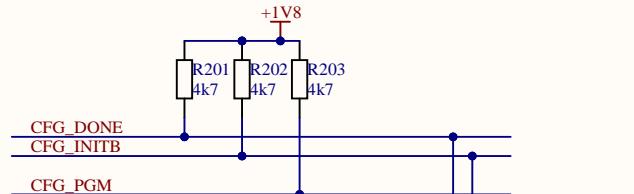
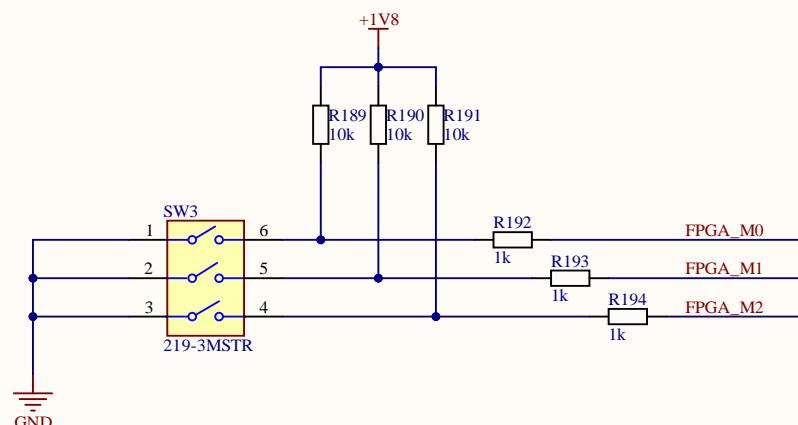
USB Hub



Title: USB Hub		Approved: YES	NewAE Technology
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D

Title: Configuration Routing		Approved: NO	NewAE Technology
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A

A

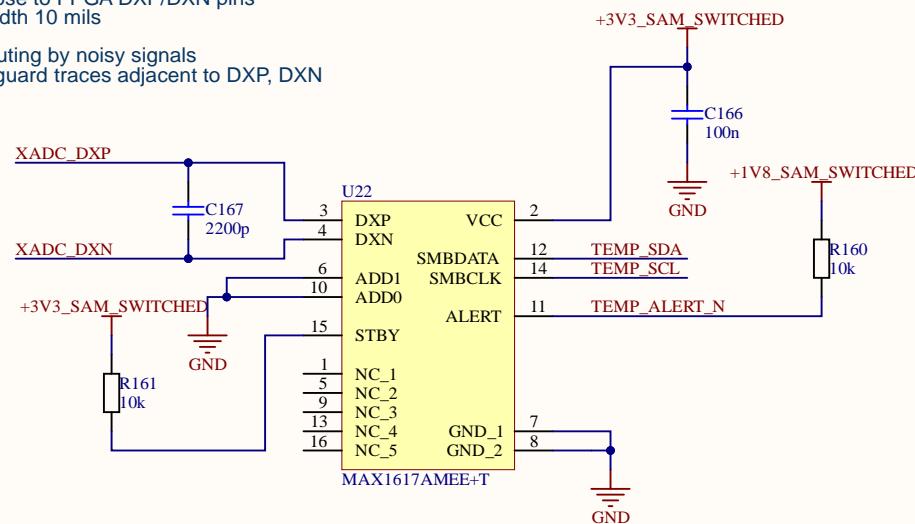
Thermal Diode Temp Sensor

B

B

Place close to FPGA DXP/DXN pins
Trace width 10 mils

Avoid routing by noisy signals
Include guard traces adjacent to DXP, DXN



C

C

I₂C Address = 0x18

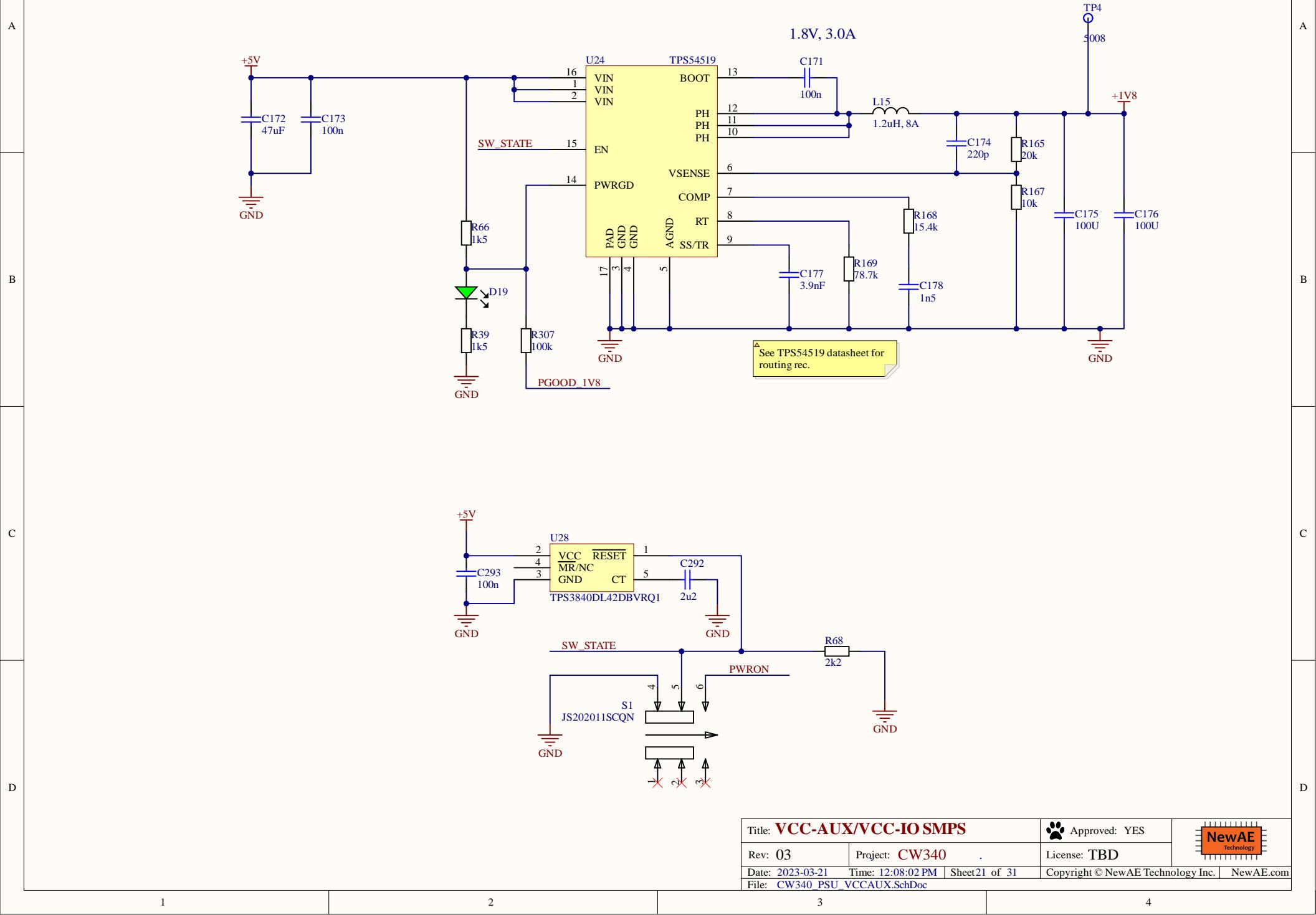
Temperature diode ideality factor = 1.010

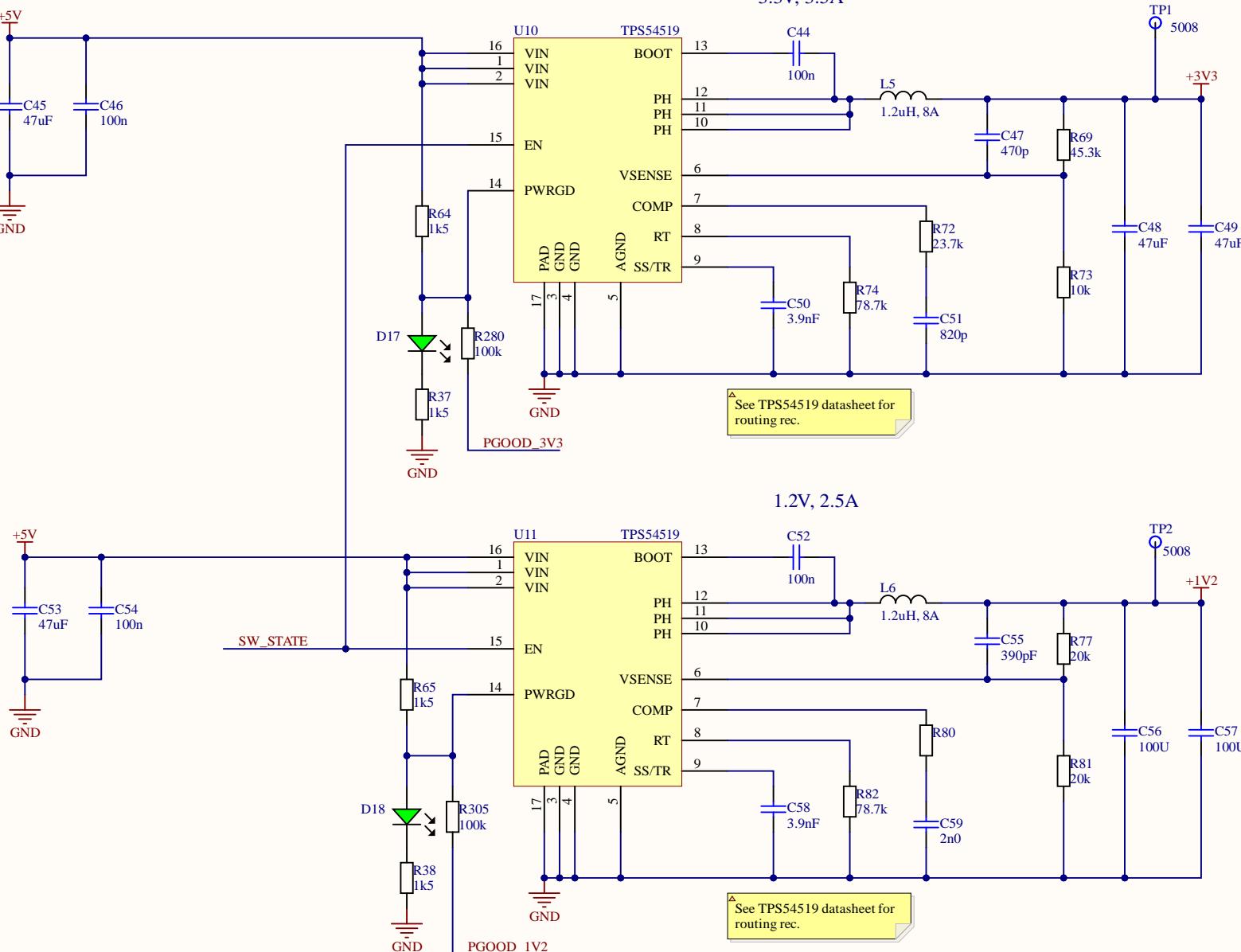
Temperature diode series resistance = 2

D

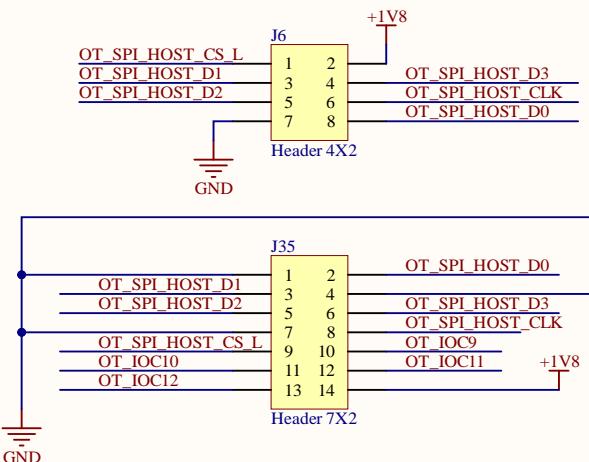
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Title: FPGA - Thermal + XADC		Approved: Yes	
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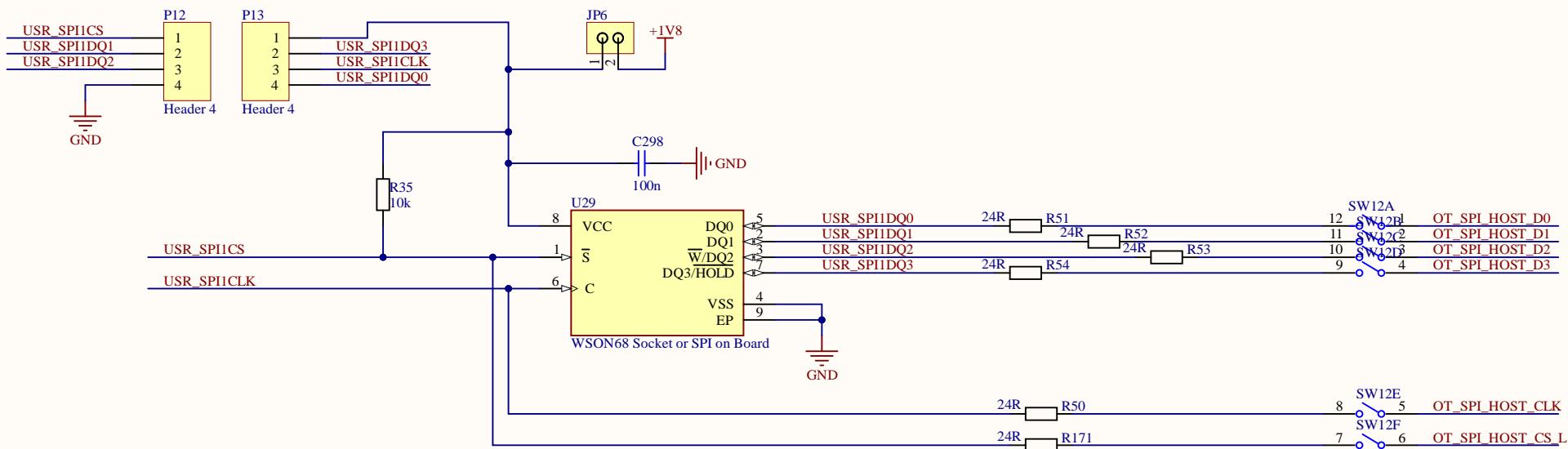




A



B



C

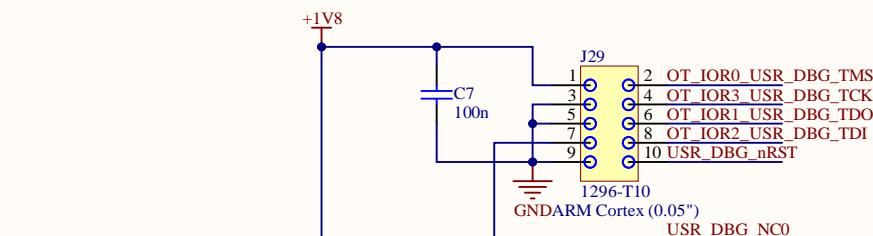
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Title: SPI Flash & Breakout		Approved: NO	NewAE Technology
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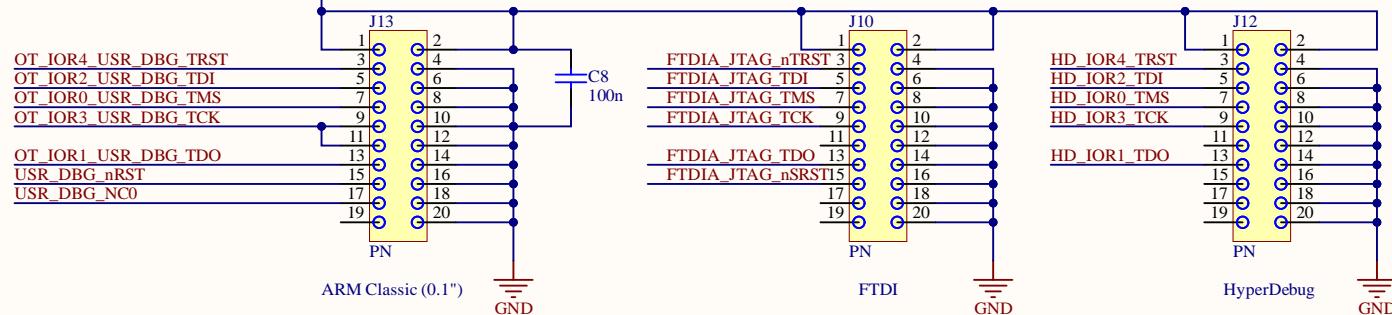
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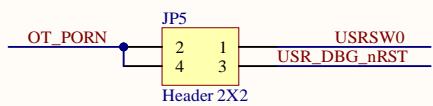
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C

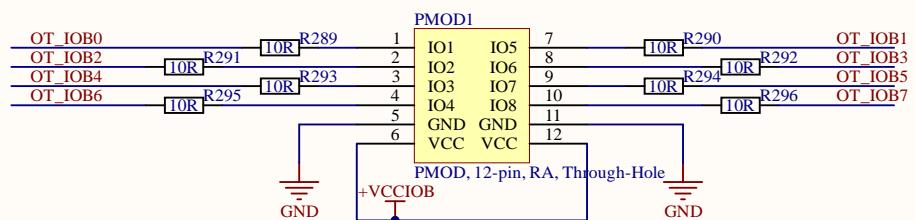


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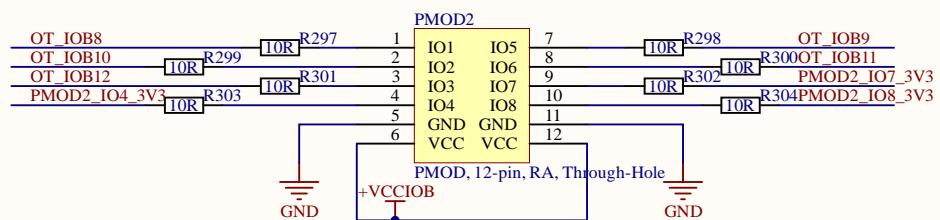


Title: User Debug Headers		Approved: Yes	NewAE Technology
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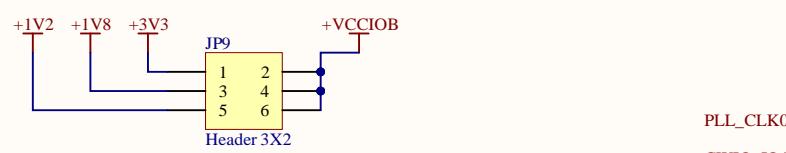
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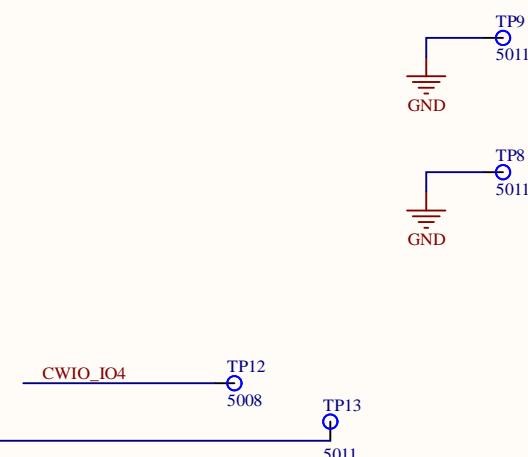
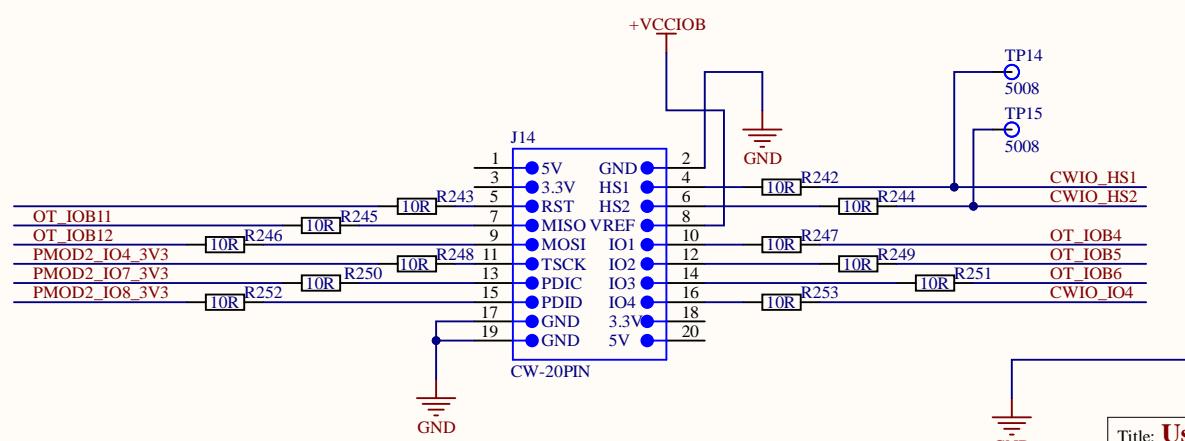
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C



D



Title: User GPIO Headers

Rev: 03 Project: CW340

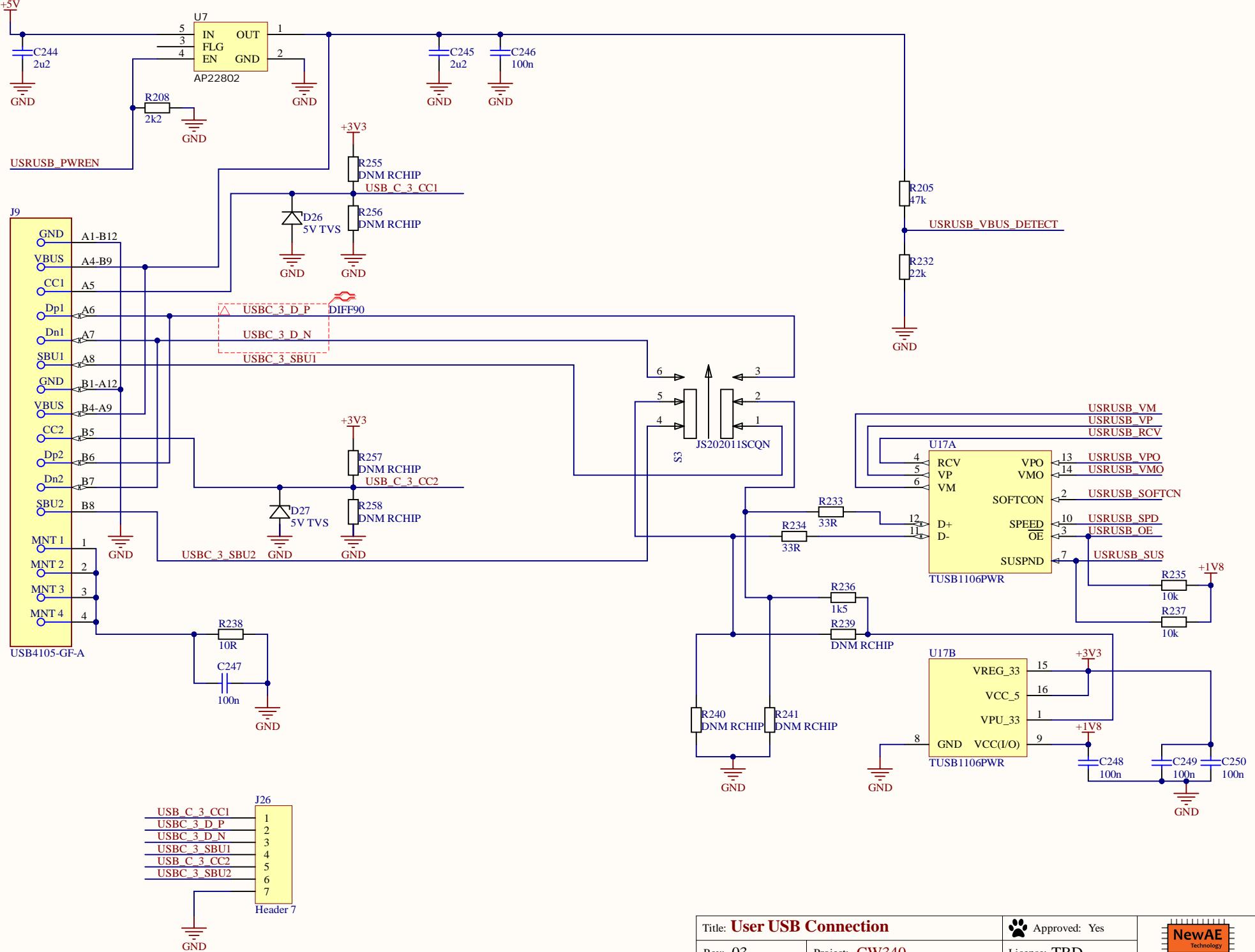
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File: CW340_USERIO_Header.SchDoc

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Title: **User USB Connection**

Approved: Yes



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Project: **CW340**

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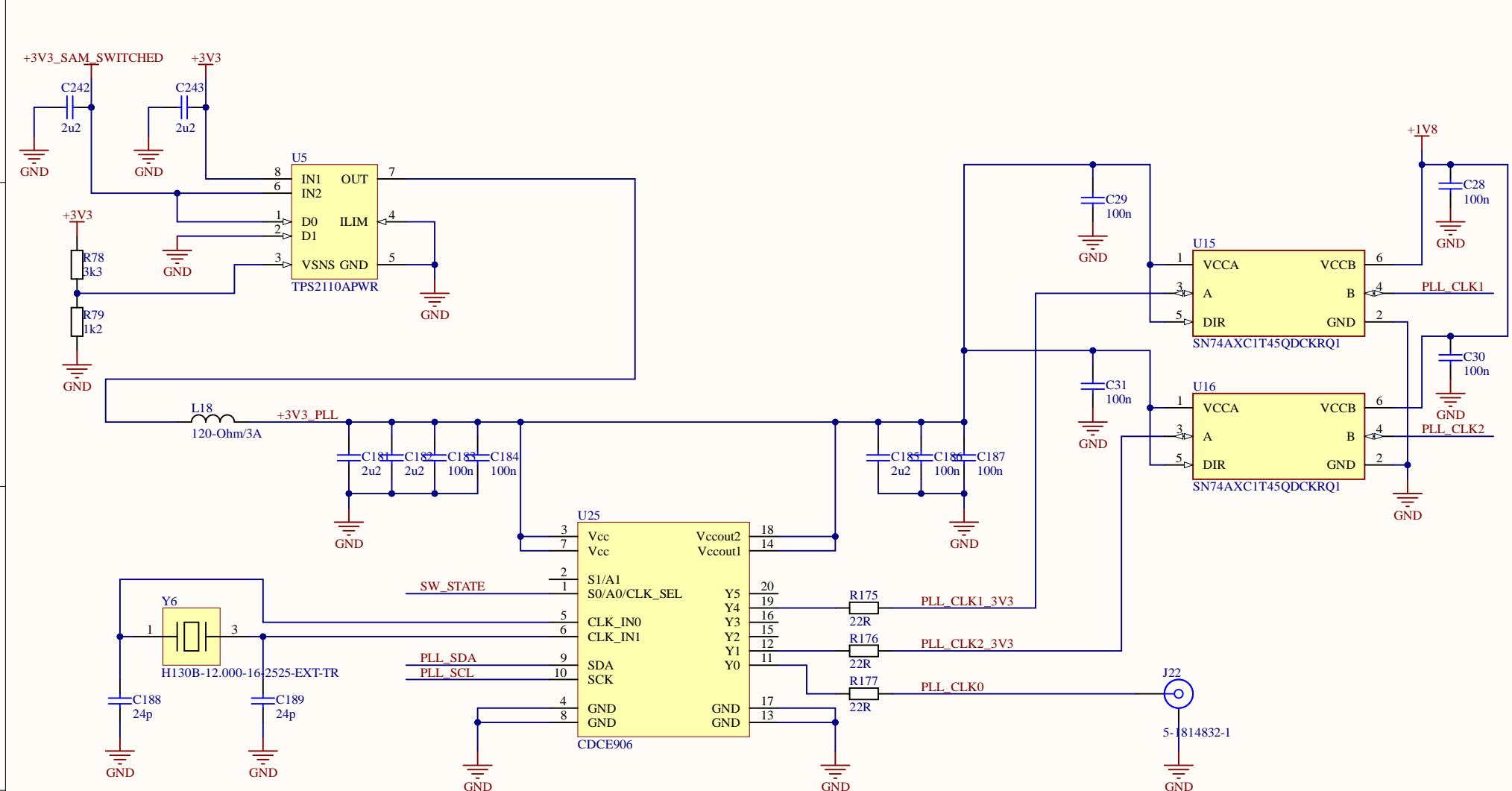
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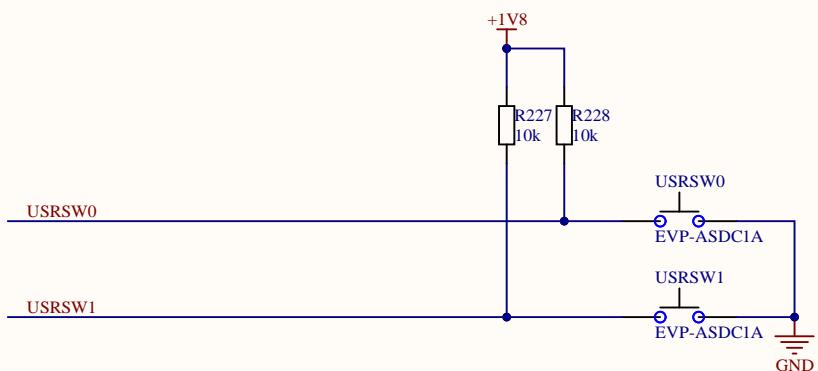
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CLOCKS



Title: PLL, Clocks for FPGA		Approved: NO	NewAE Technology
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A DIP0-6 connected to 1.8V/3.3V bank.
DIP7 is connected to 1.8V bank.

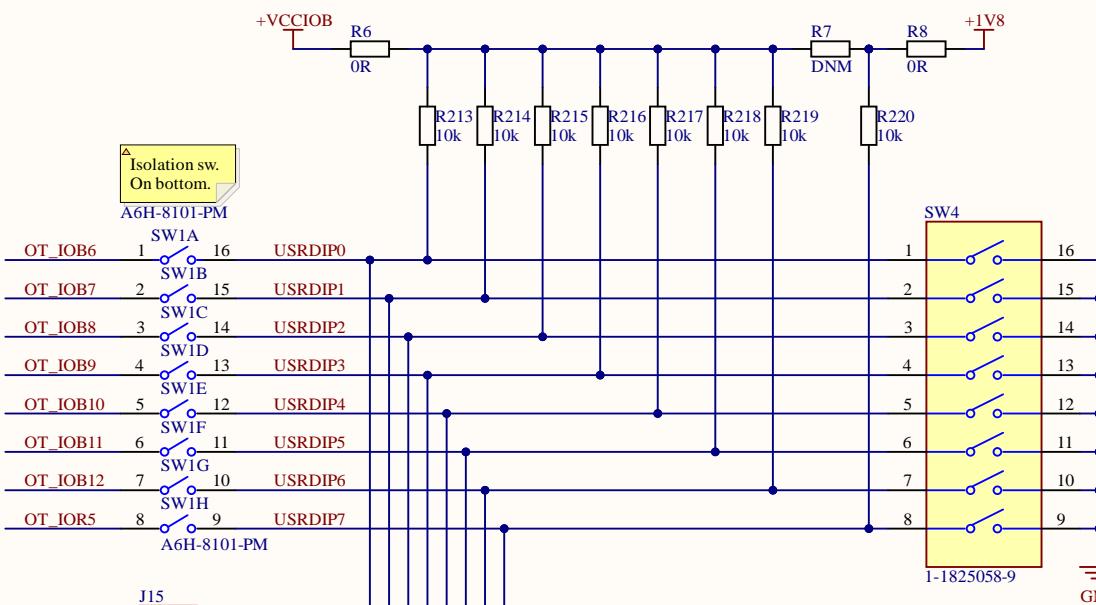
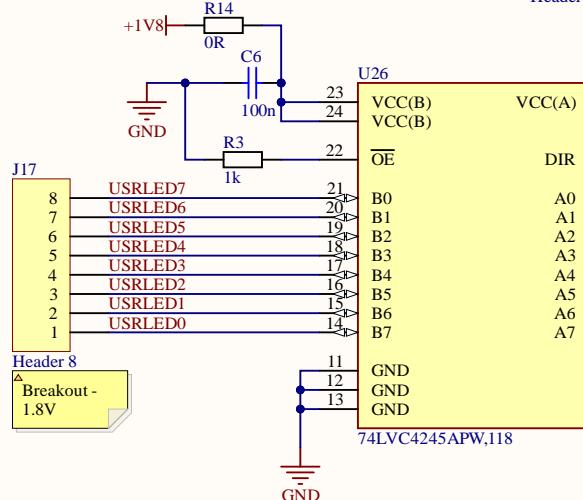


Section C:

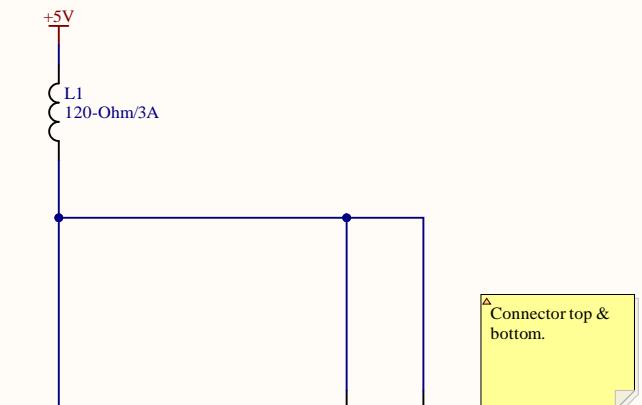
Isolation sw. On bottom. A6H-8101-PM

OT_IOR13	8	9	USRLED7
OT_IOR12	7	10	USRLED6
OT_IOR11	6	11	USRLED5
OT_IOR10	5	12	USRLED4
OT_IOR9	4	13	USRLED3
OT_IOR8	3	14	USRLED2
OT_IOR7	2	15	USRLED1
OT_IOR6	1	16	USRLED0

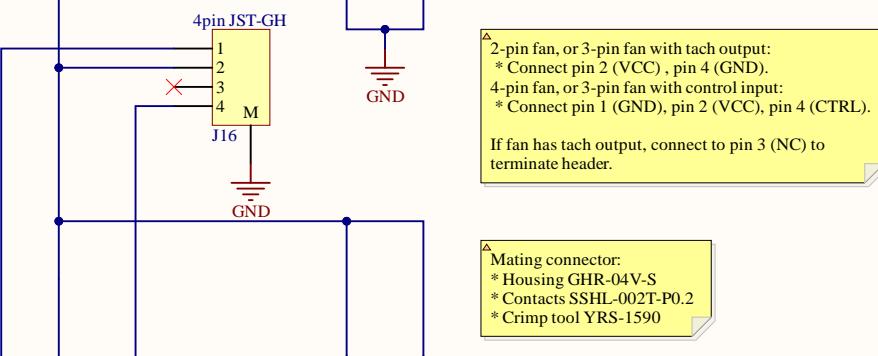
Isolation sw. On bottom. A6H-8101-PM



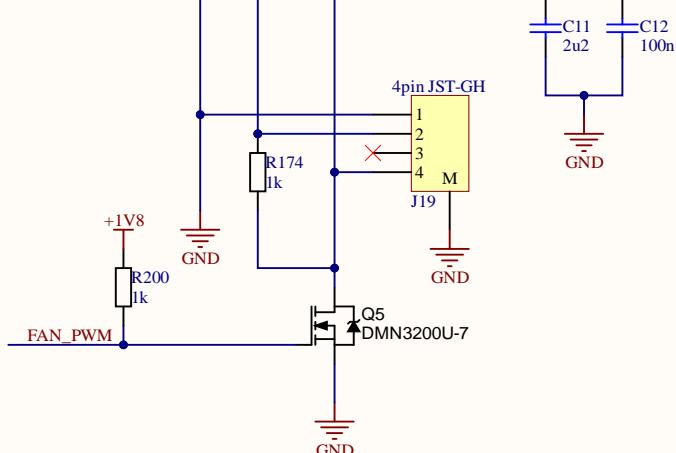
A



B



C



Title: FAN Headers

Approved: Yes

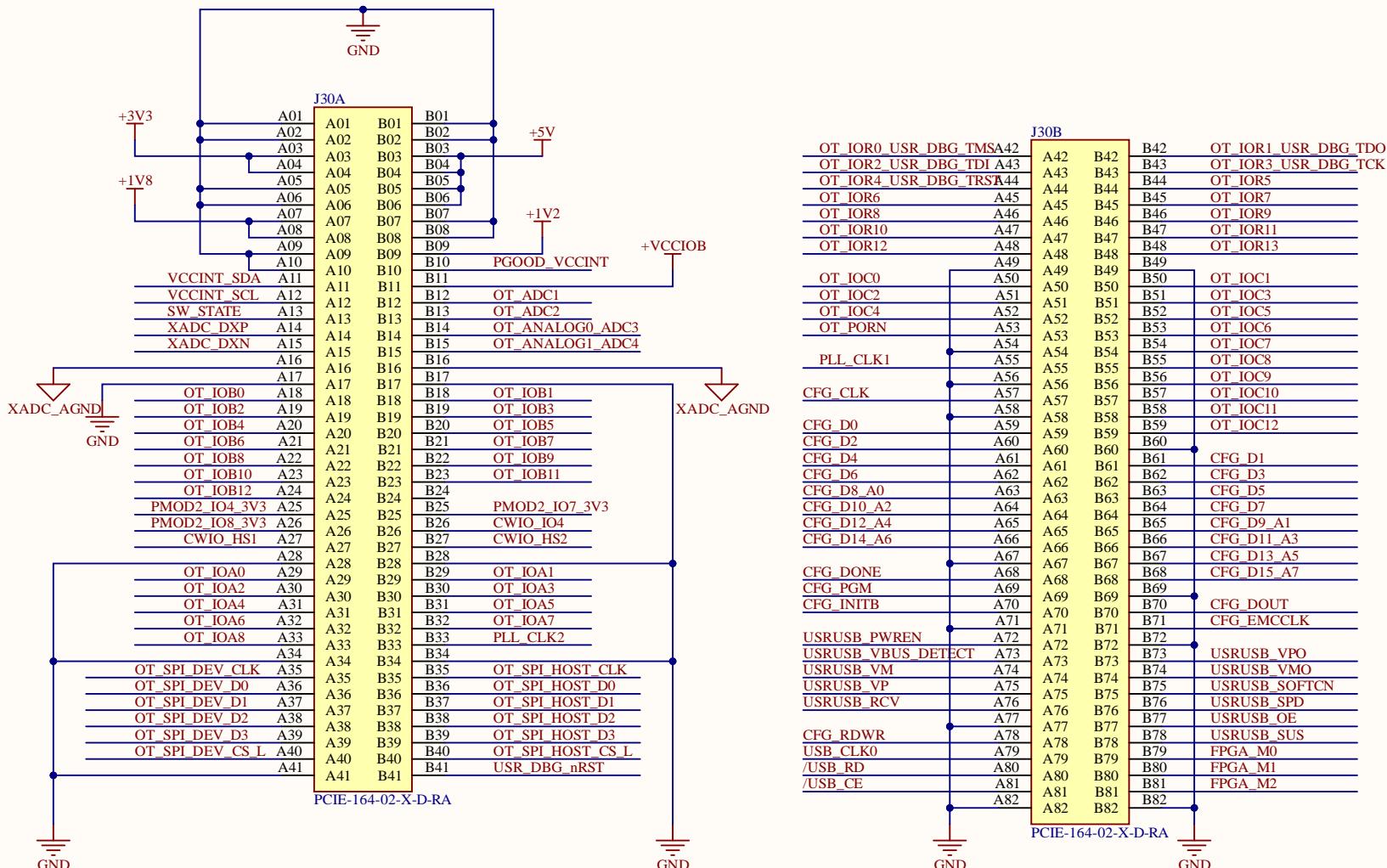


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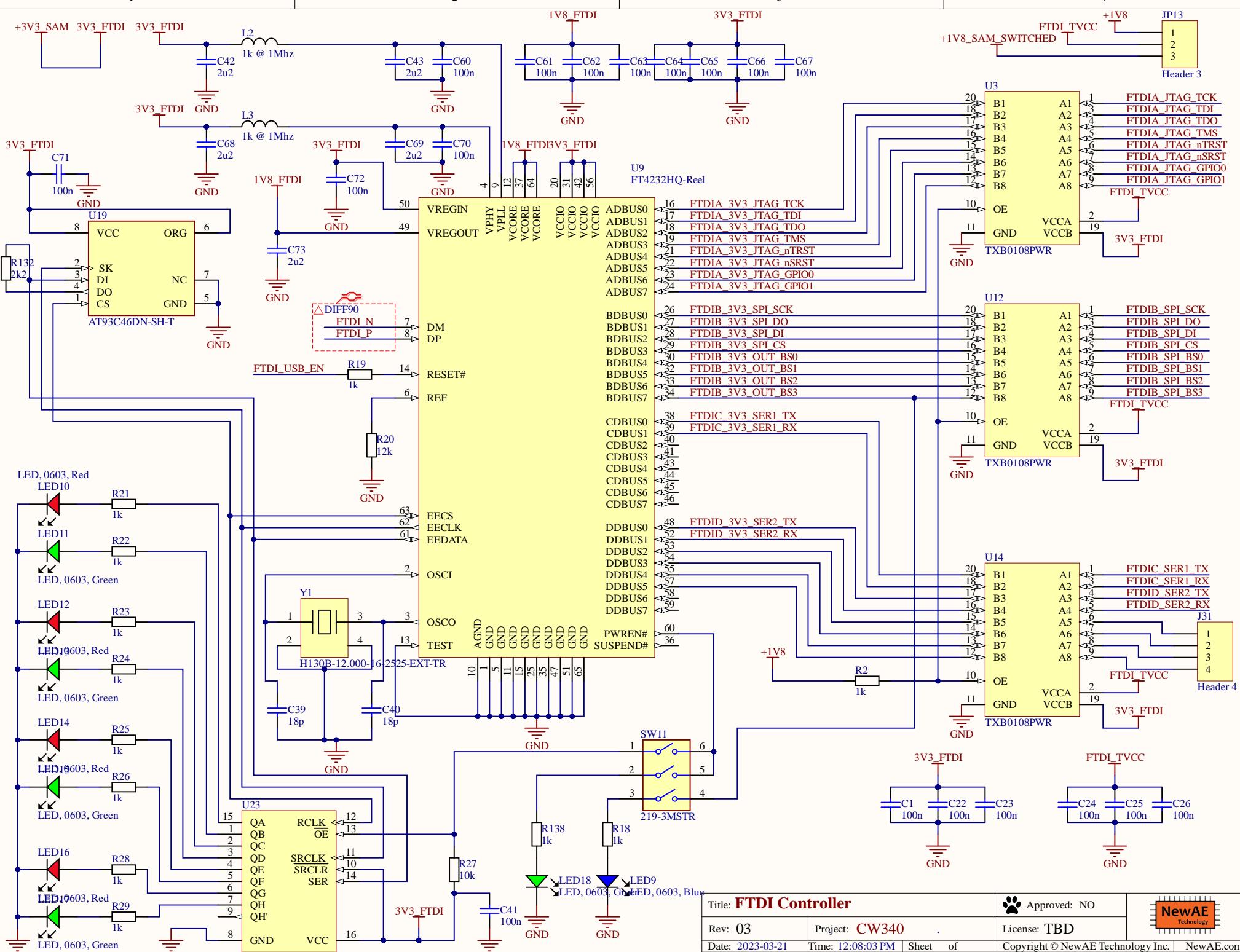
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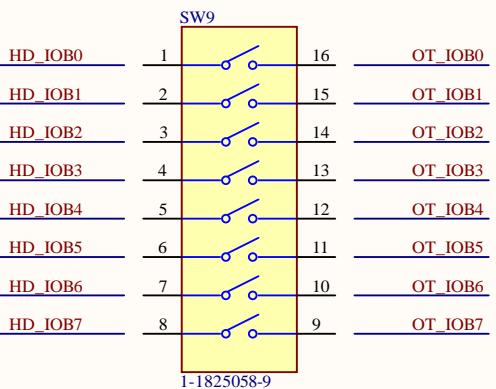
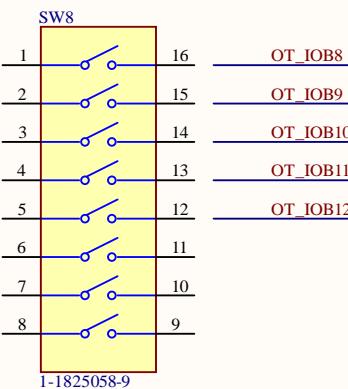


△ TODO: Should we route this too?

USR DBG NCO

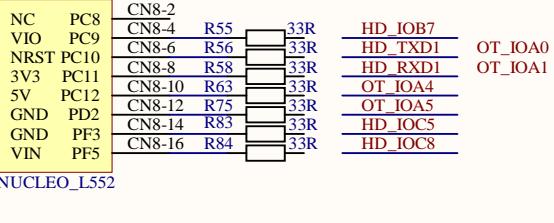
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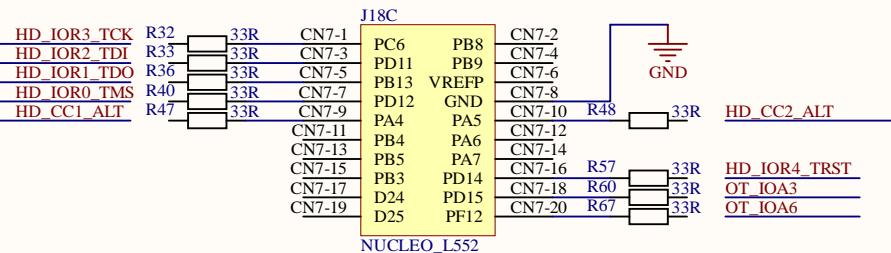
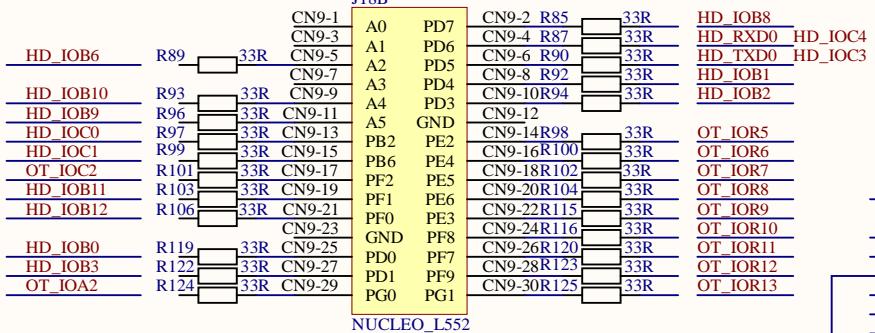


△ HD held in reset if VIO is > 1.8V.

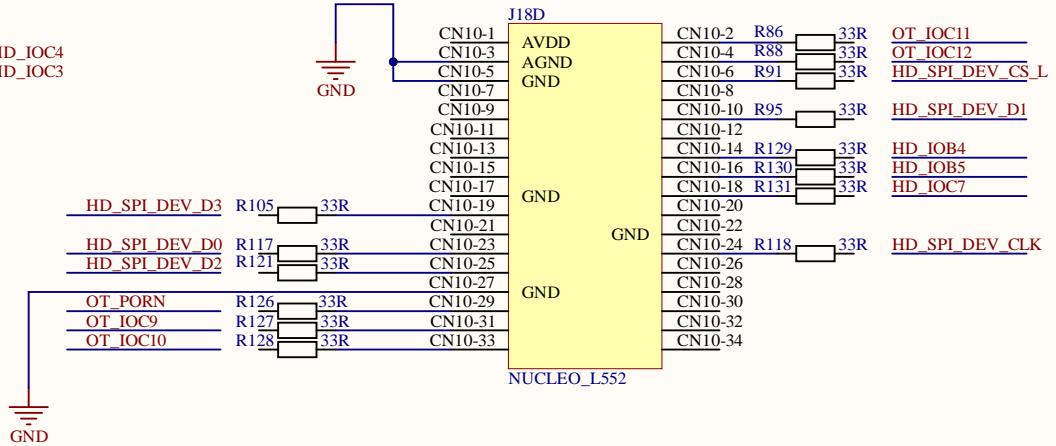
J18A



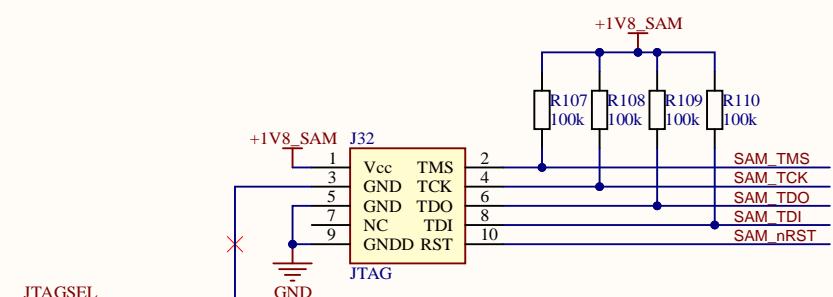
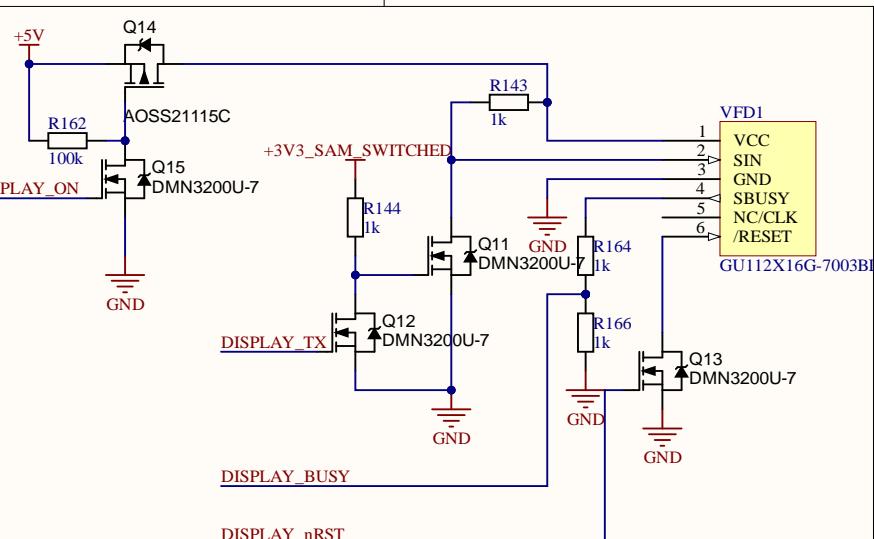
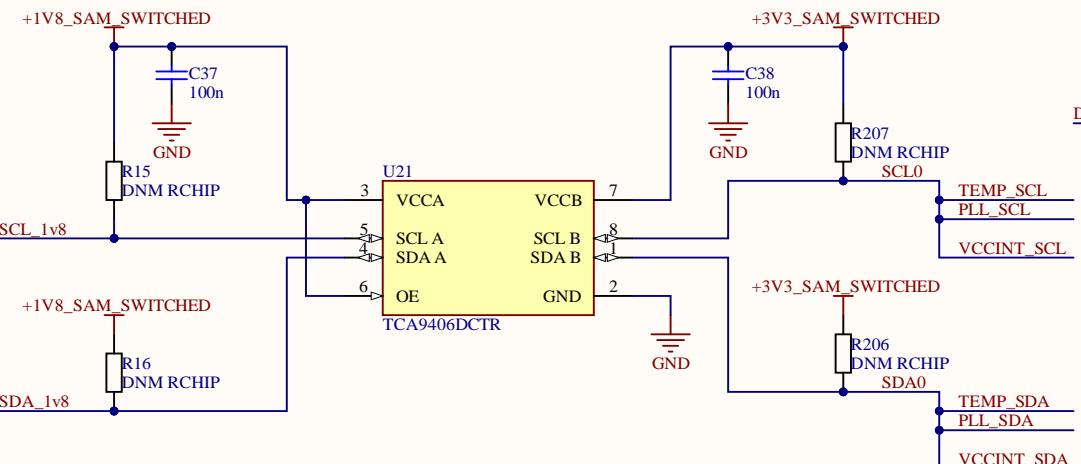
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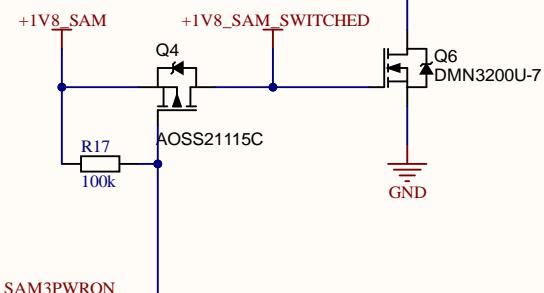
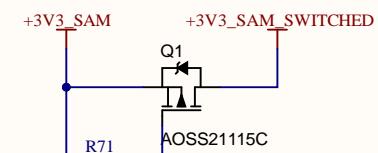
J18D



1 2 3 4



If SAM3X goes to sleep, turns off connected devices (PLL chip, etc). Also need to turn off power to pull-ups and similar.



D

Title: MCU Misc Connections			Approved: NO	NewAE Technology
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1 2 3 4

A

A

B

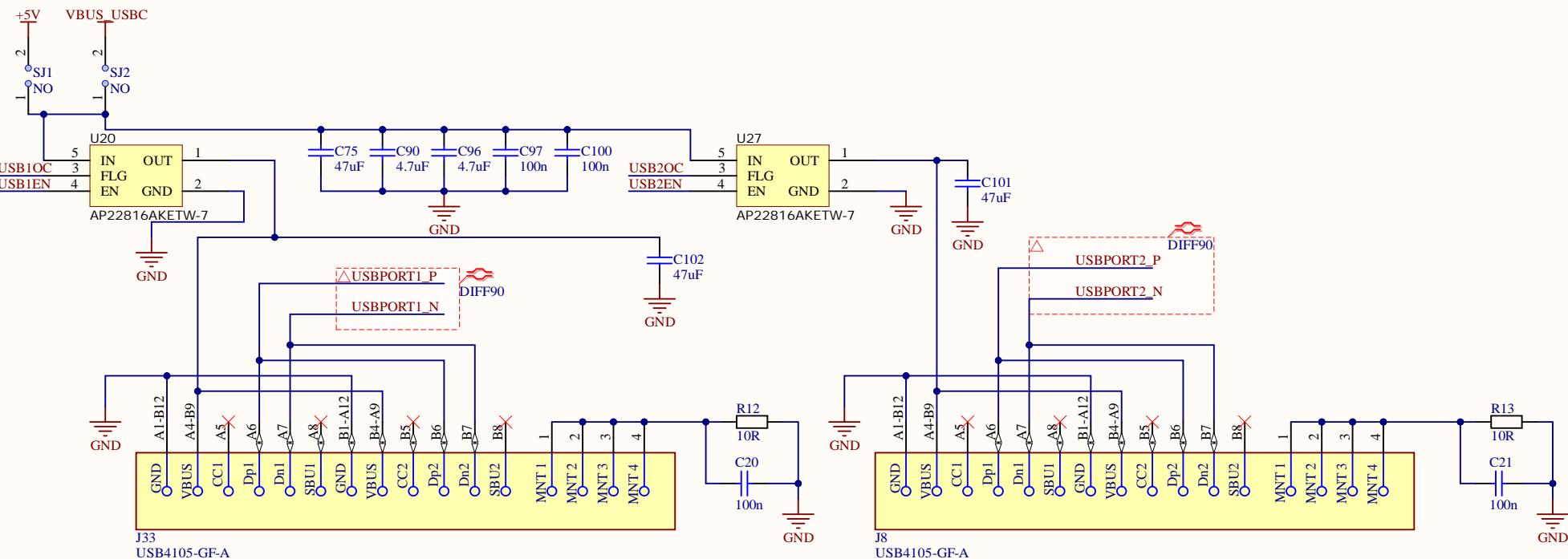
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C

C

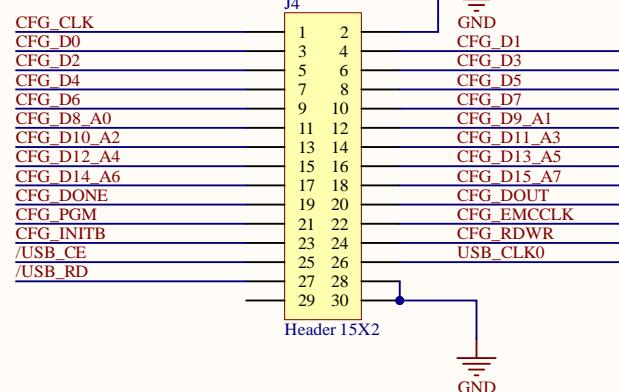
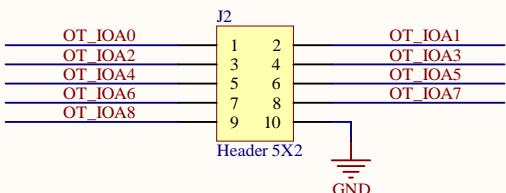
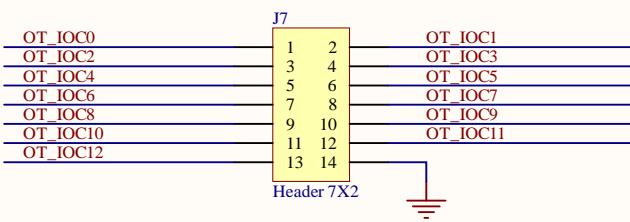
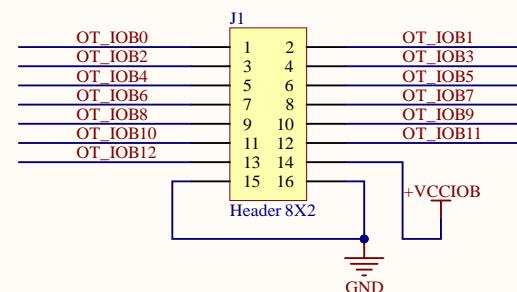
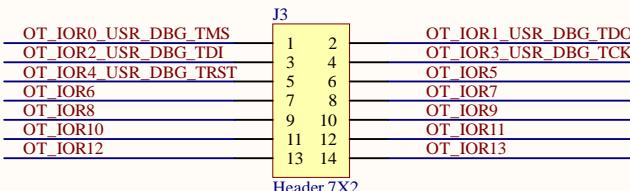
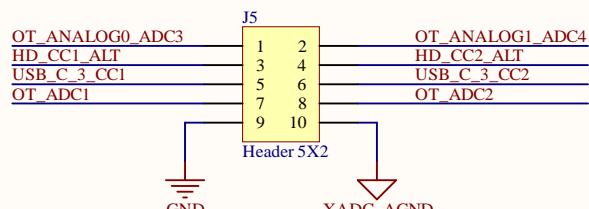
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D



Title

Size	Number	Revision
A4		
Date:	3-21-2023	Sheet of
File:	C:\Users\...\CW340_USBHUB_ExtPorts	Drawn By:



D

TODO: Consider breakouts for these signals?

OT_SPI_DEV_CLK
OT_SPI_DEV_D0
OT_SPI_DEV_D1
OT_SPI_DEV_D2
OT_SPI_DEV_D3
OT_SPI_DEV_CS_L

OT_SPI_HOST_CLK
OT_SPI_HOST_D0
OT_SPI_HOST_D1
OT_SPI_HOST_D2
OT_SPI_HOST_D3
OT_SPI_HOST_CS_L

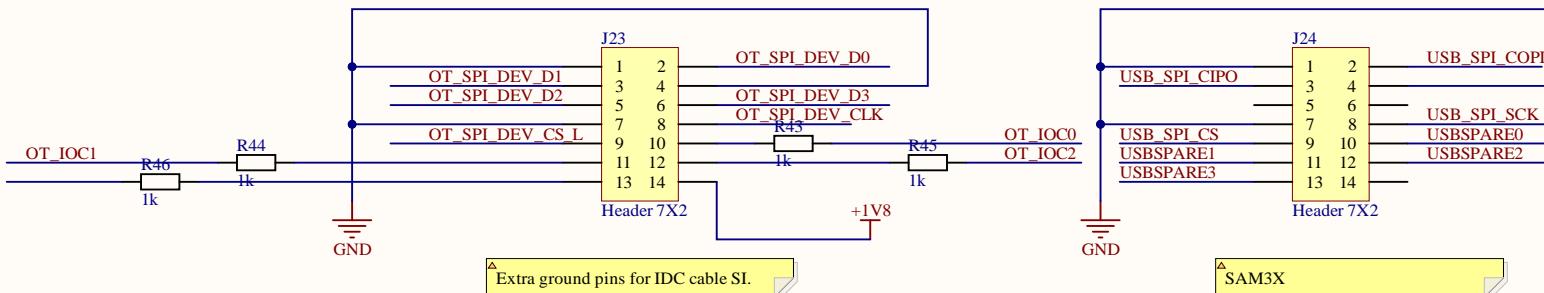
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USRUSB_VBUS_DETECT
USRUSB_VM
USRUSB_VP
USRUSB_RCV
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USRUSB_SPD
USRUSB_OE
USRUSB_SUS

PLL_CLK2
PLL_CLK1

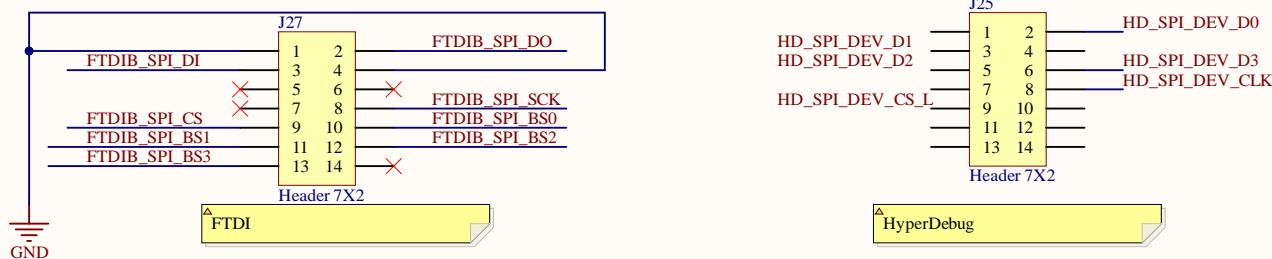
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