

ChipWhisperer CW340 "Luna Board" - Xilinx Kintex Ultrascale Target Board

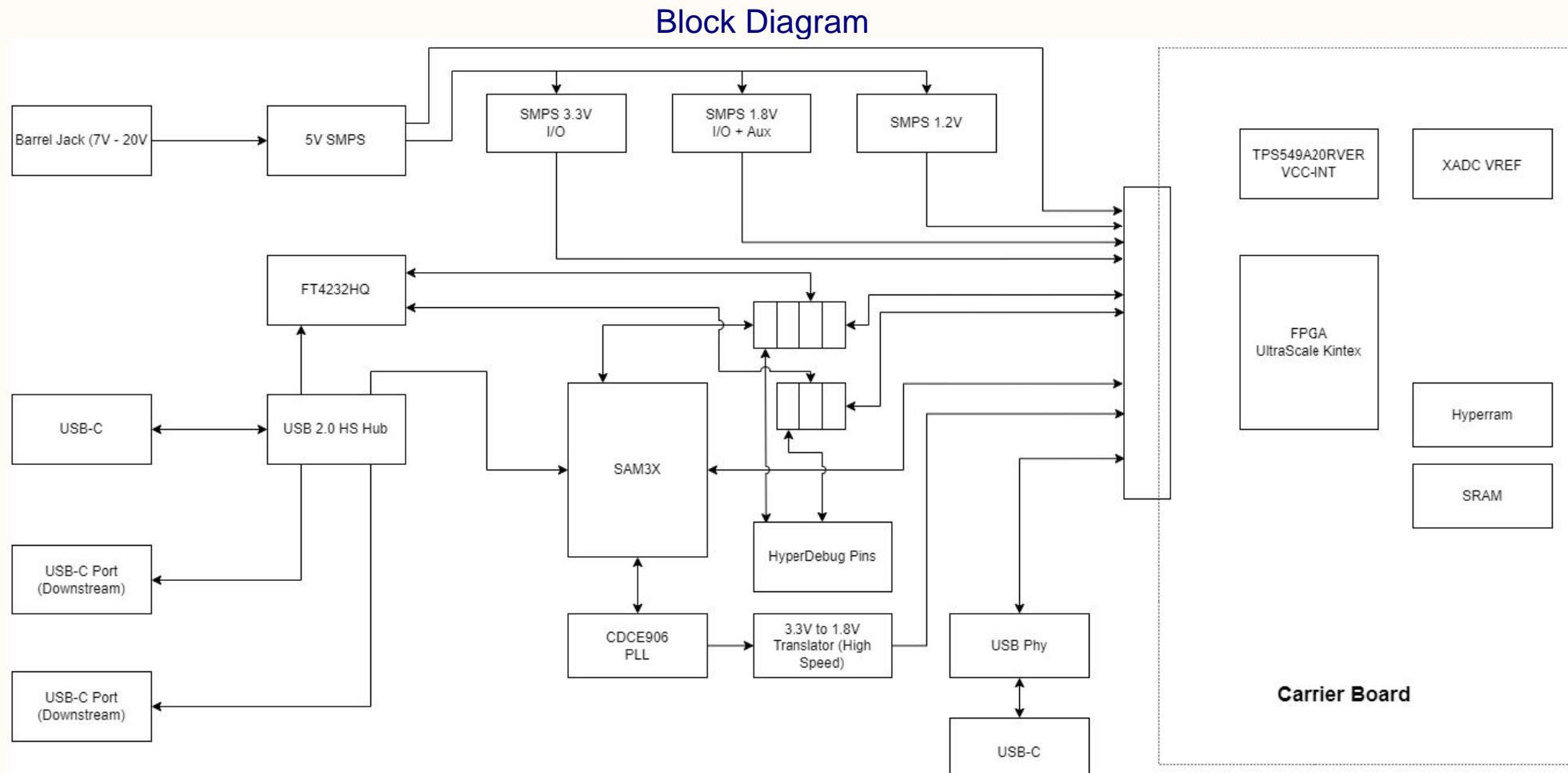
NewAE Technology Inc.

Table of Contents

Revision Summary

- 00: Ultra-alpha.
- 02: Test version.
- 03: First Beta
- 04: RC
 - * Add HD connections, including reset
 - * Fix VCCINT led
 - * Add PLL2 header & selection
- 05: Production
 - * R187 - 3.3V from HD board instead

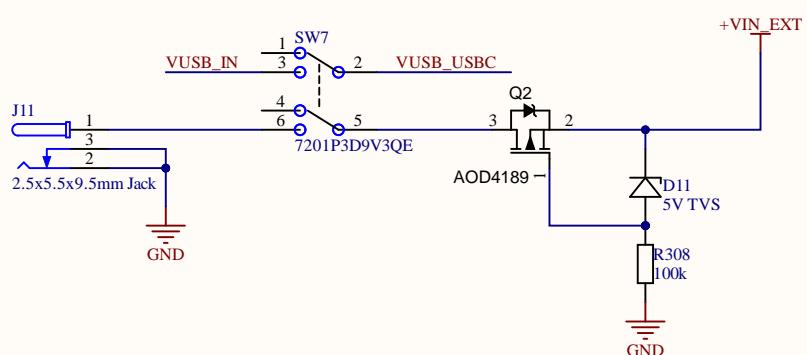
Title: Luna Board - The Cover Sheet		Approved: Yes	
Rev: 03	Project: CW340	License: TBD	
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File: CW340_Cover_Page.SchDoc			



Title: Block Diagram		Approved: *	
Rev: 03	Project: CW340 *	License: TBD	
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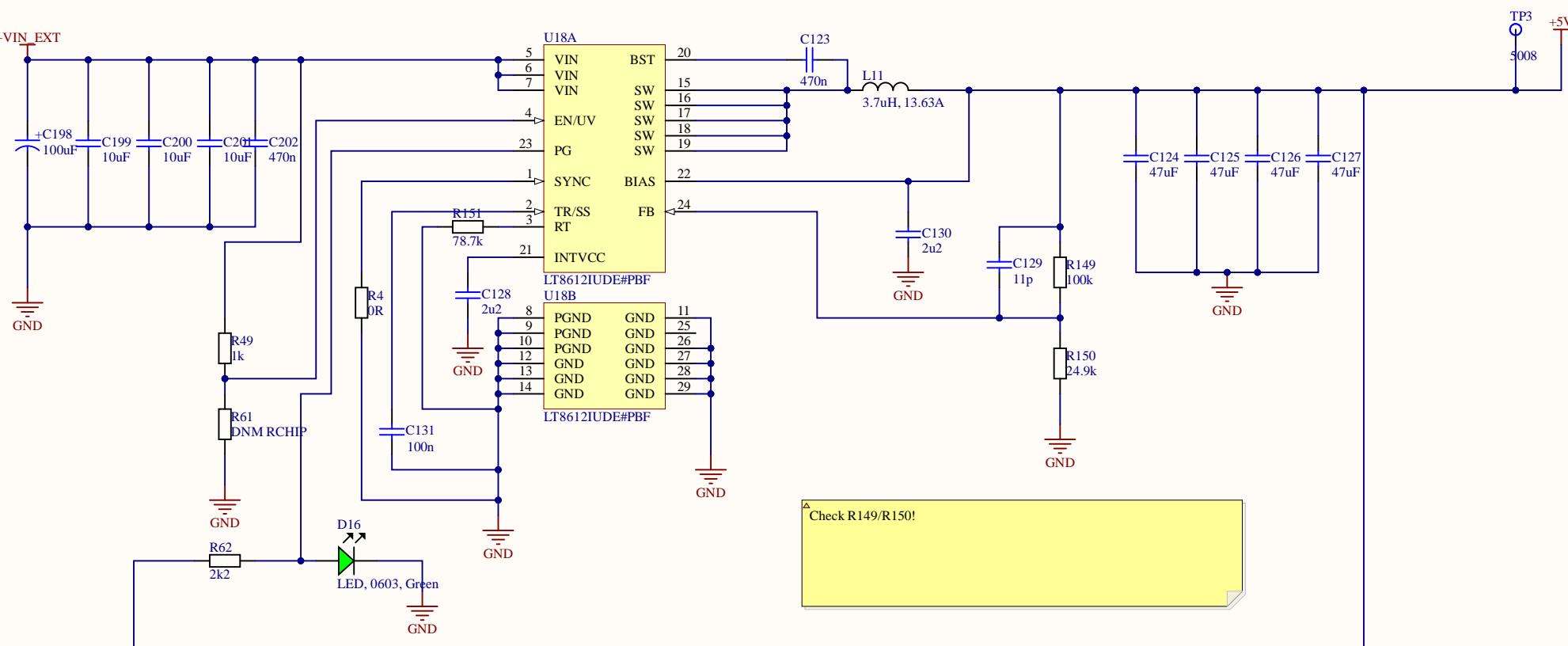
INPUT POWER

A



A

B



B

C

▲ Based on design from
<https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=9C49F428E2C4FF82>

Title: **5V Regulator**

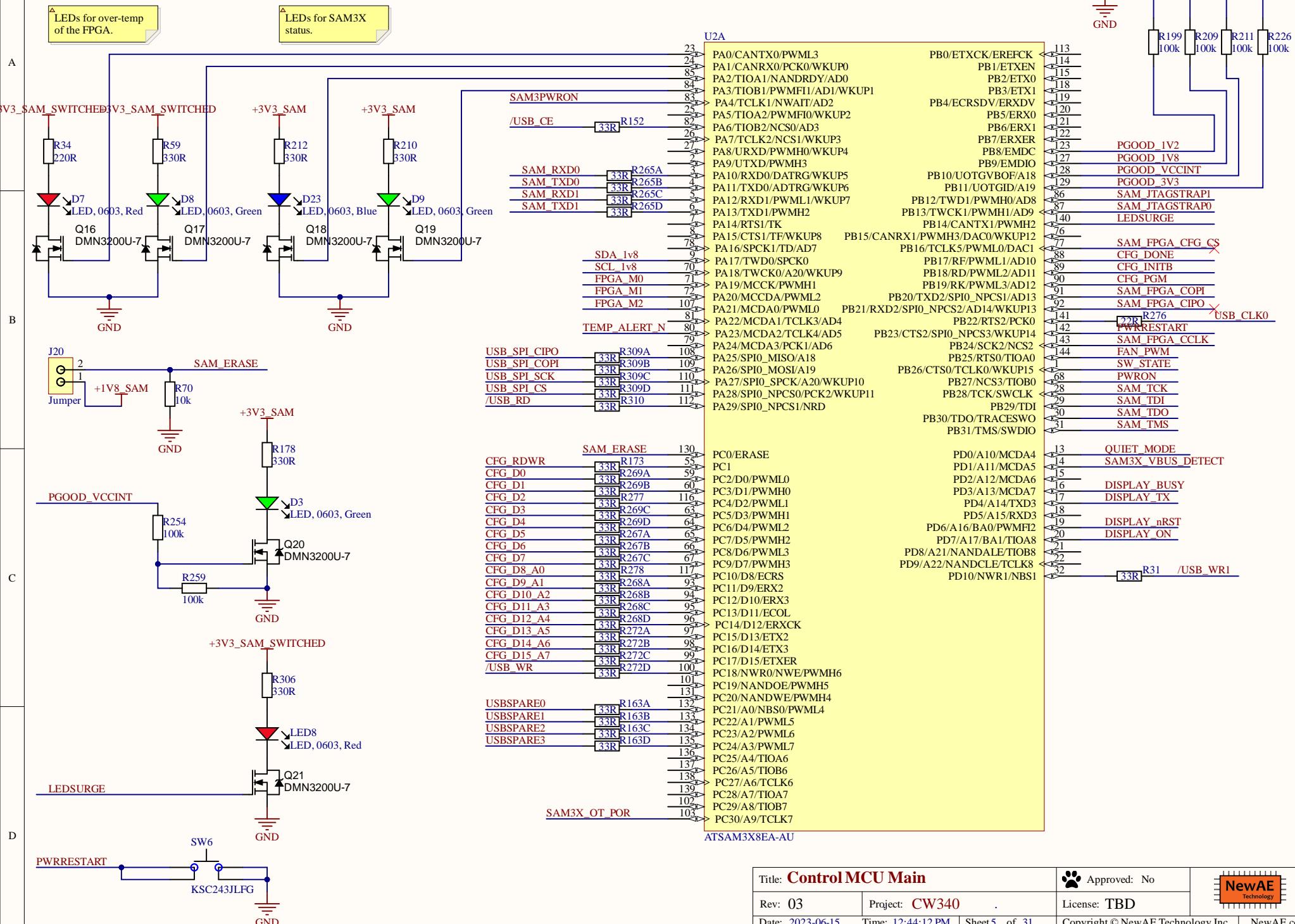
Approved: Yes

Rev: 03 Project: **CW340** License: TBD

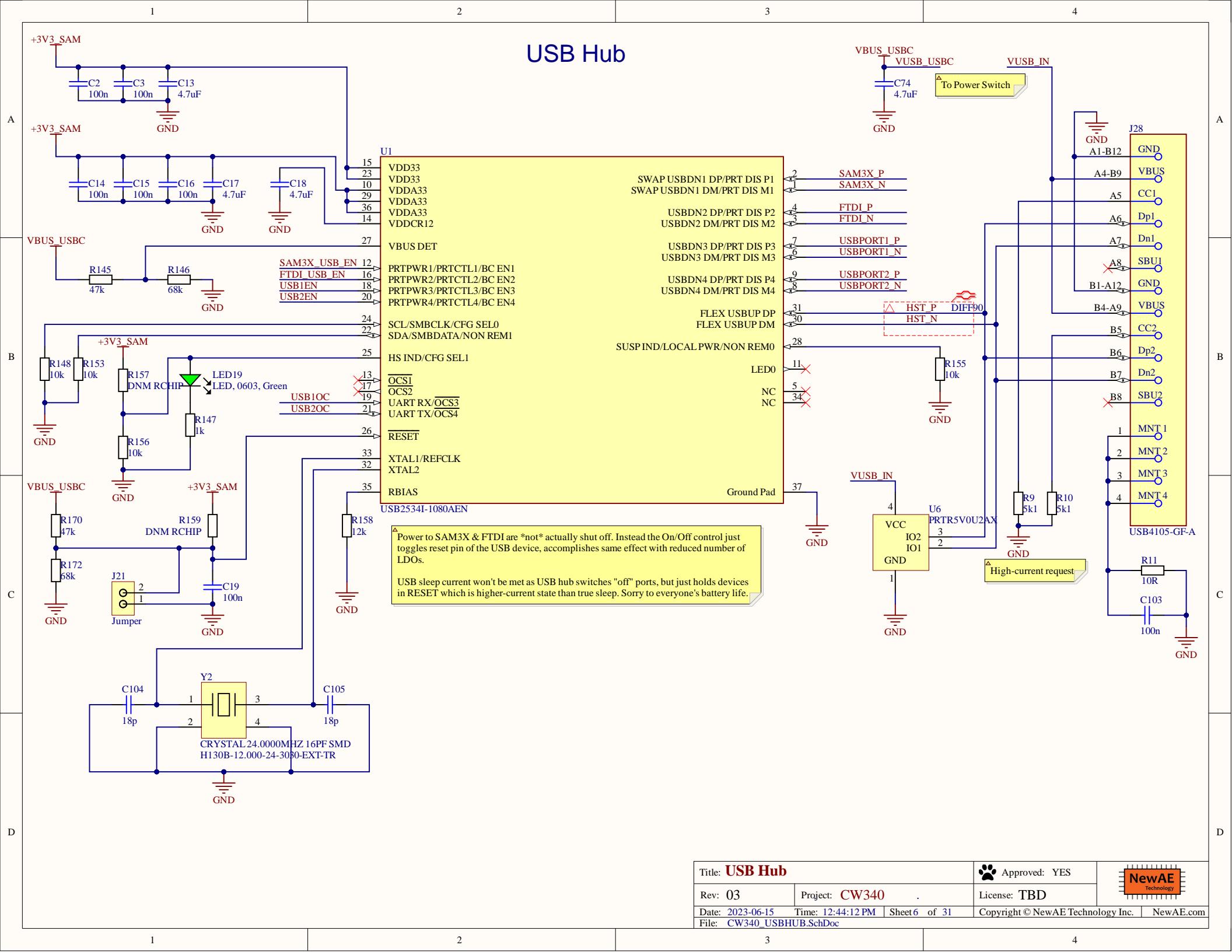
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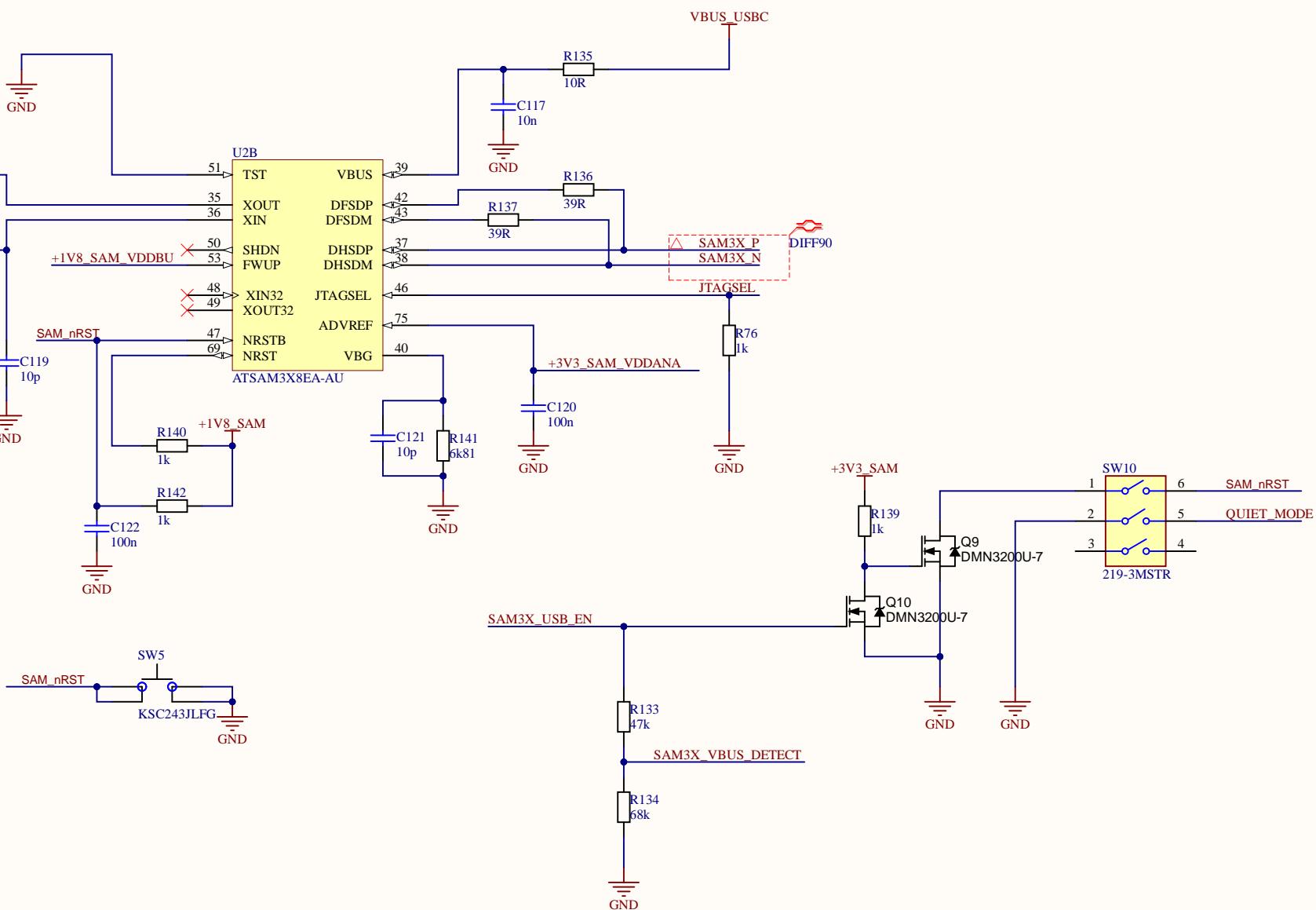
SAM3X CPU



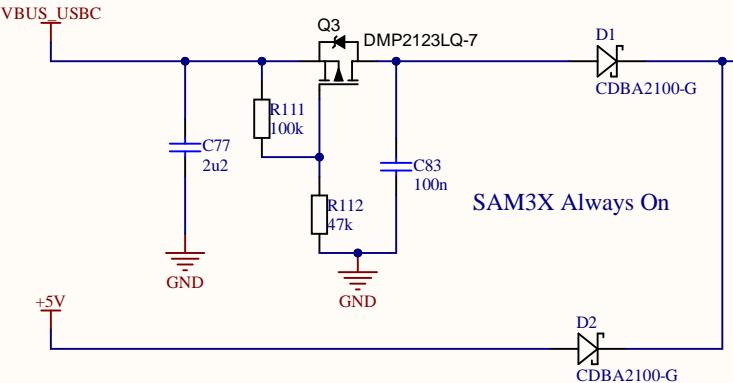
USB Hub



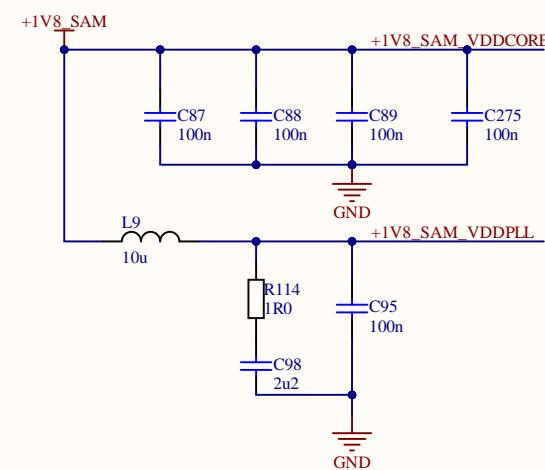
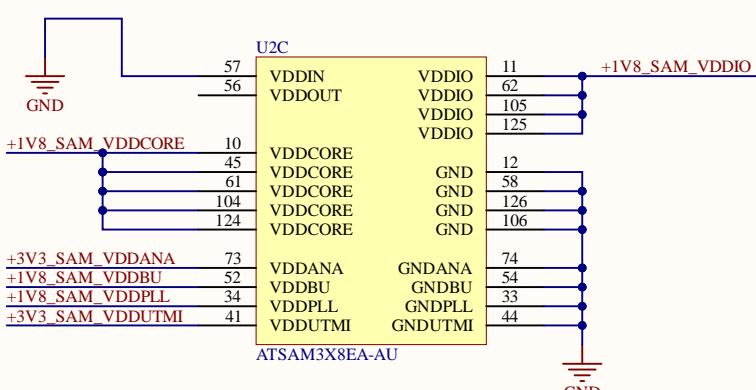
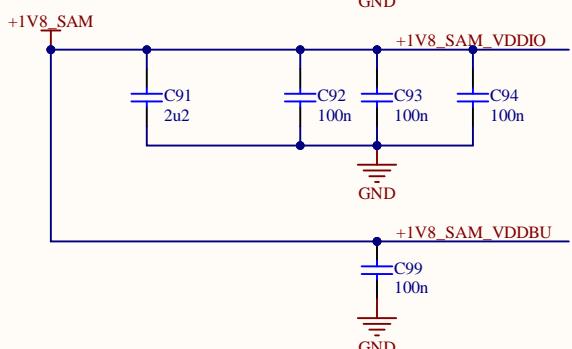
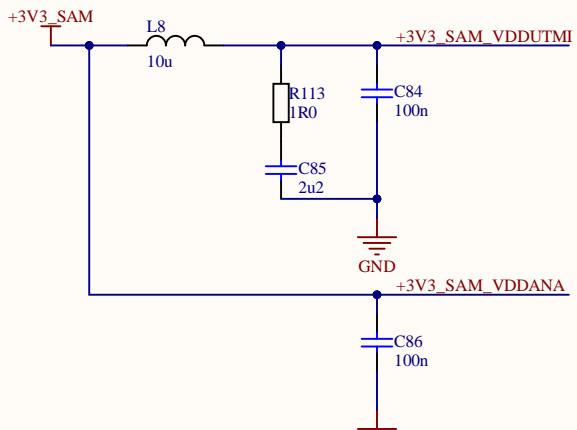
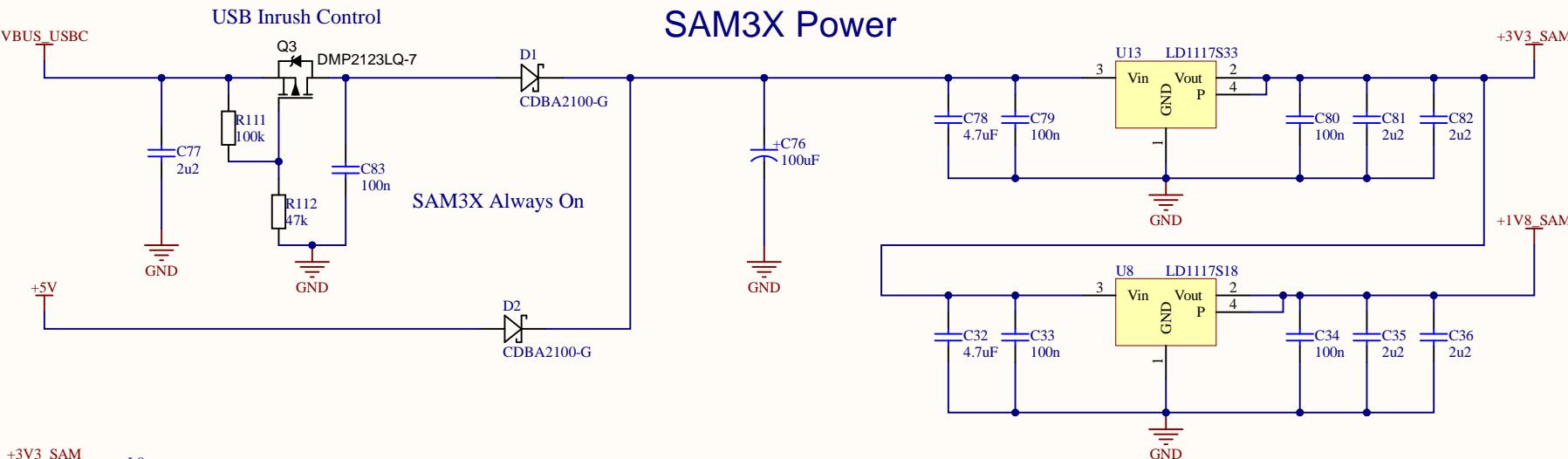
Title: USB Hub		Approved: YES	NewAE Technology
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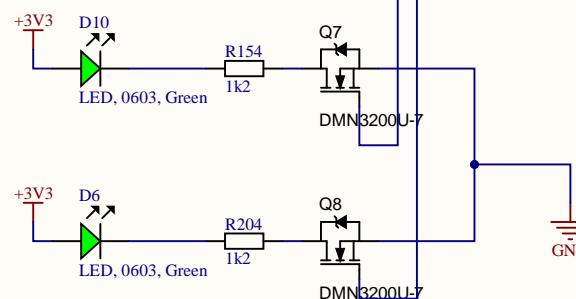
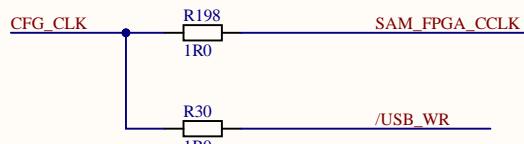
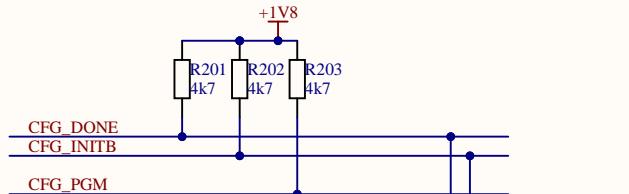
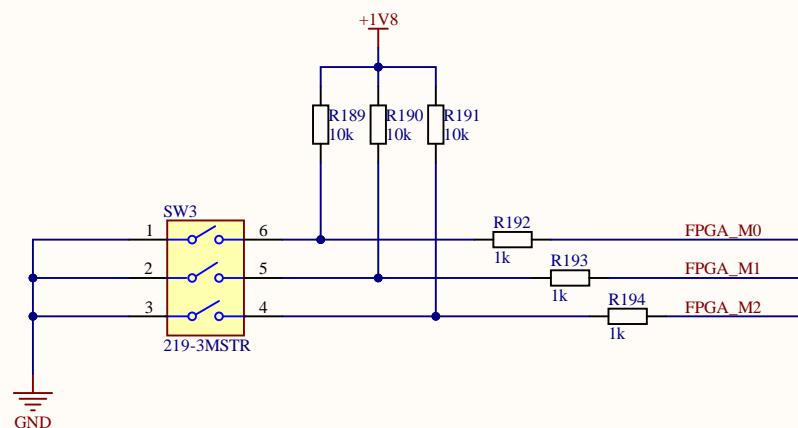
USB Inrush Control



SAM3X Power



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Configuration Routing

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A

A

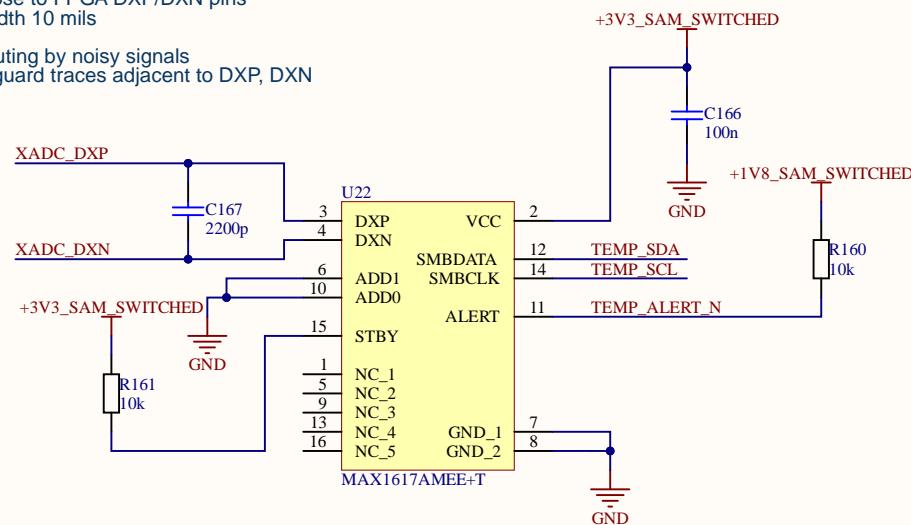
Thermal Diode Temp Sensor

B

B

Place close to FPGA DXP/DXN pins
Trace width 10 mils

Avoid routing by noisy signals
Include guard traces adjacent to DXP, DXN



I₂C Address = 0x18

Temperature diode ideality factor = 1.010

Temperature diode series resistance = 2

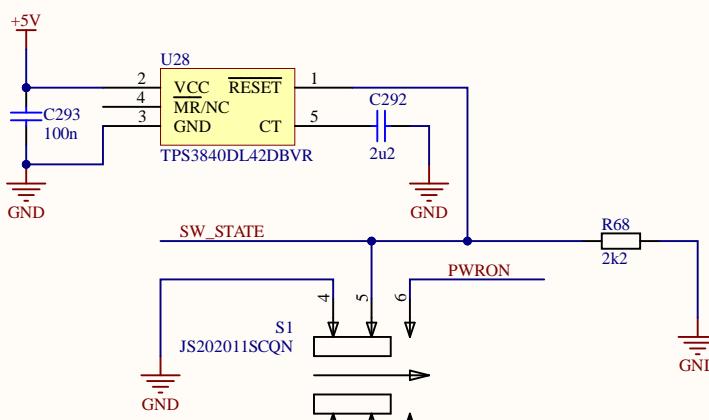
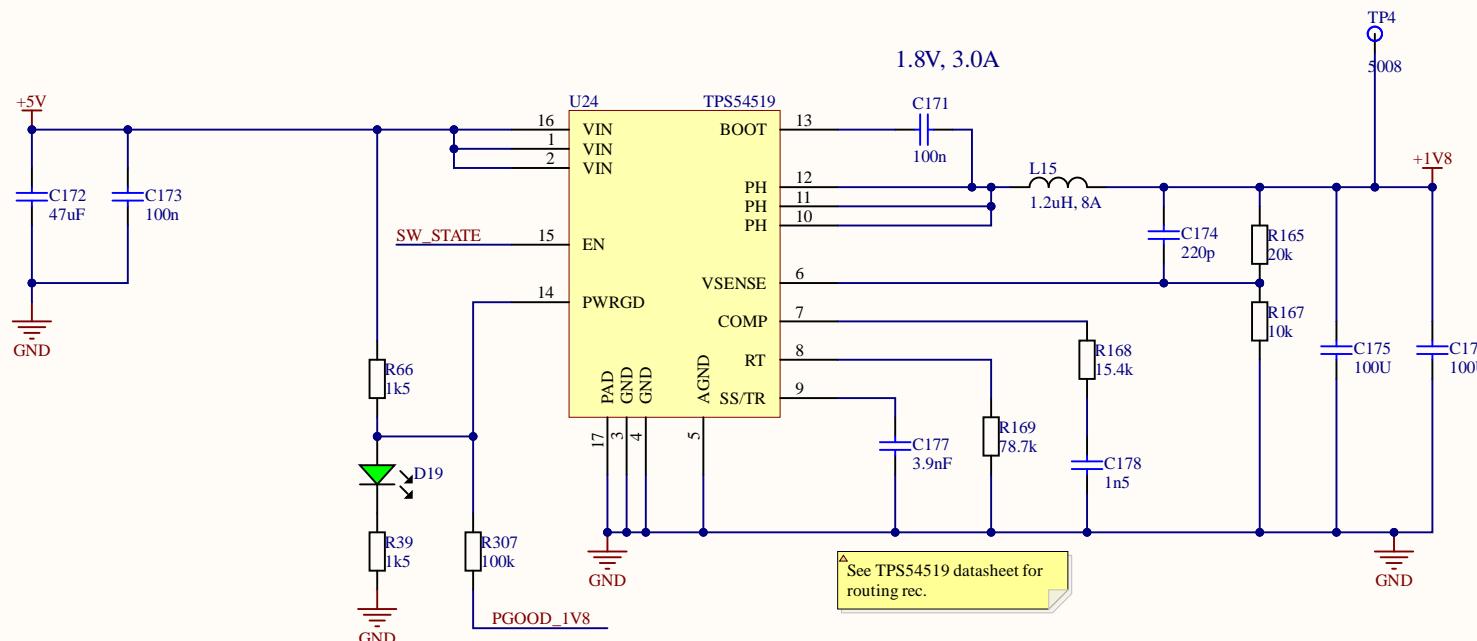
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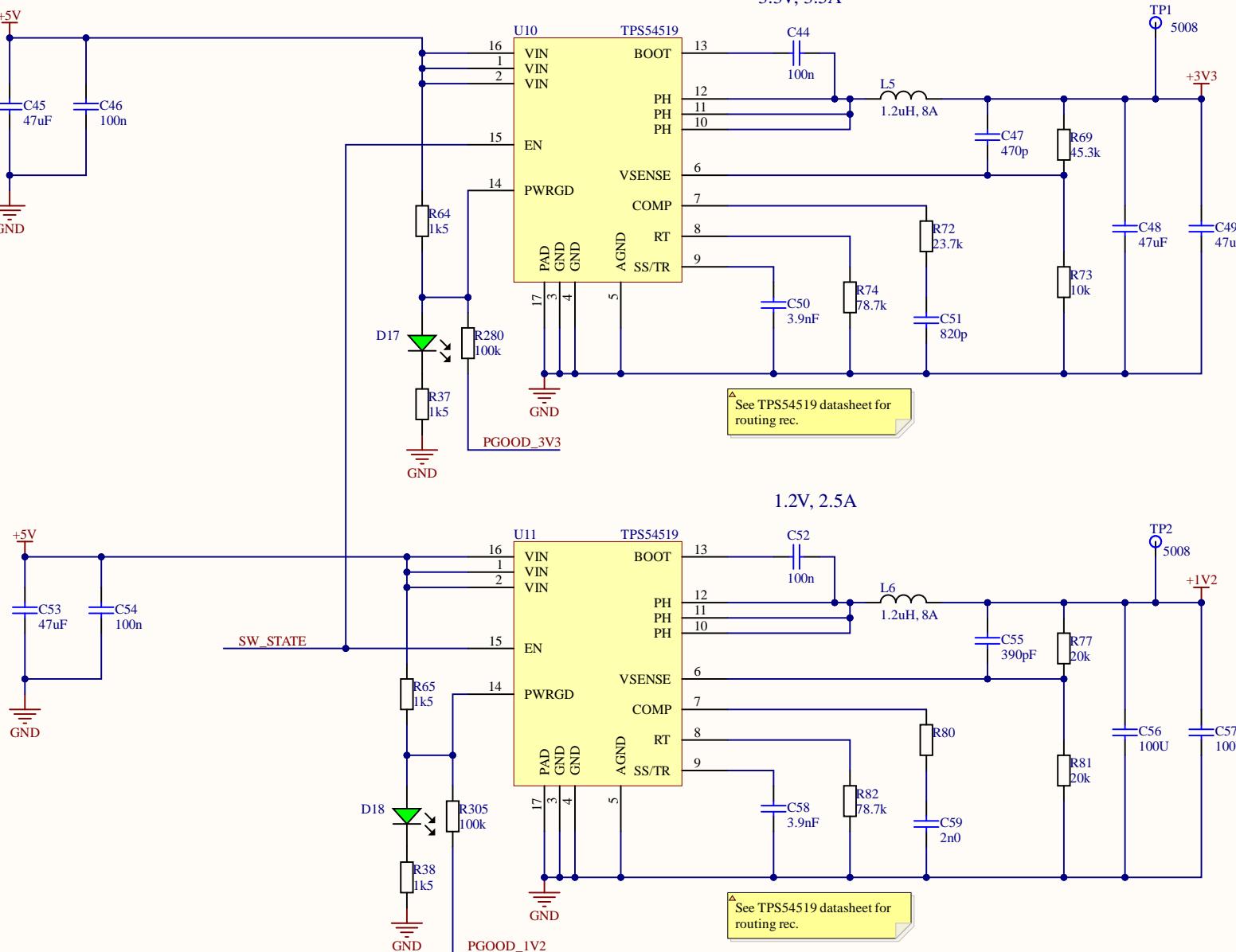
C

D

D

Title: FPGA - Thermal + XADC		Approved: Yes	
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File: CW340_FPGA_XADC.SchDoc			



Title: **VCCIO Fixed Supplies**

Approved: Yes



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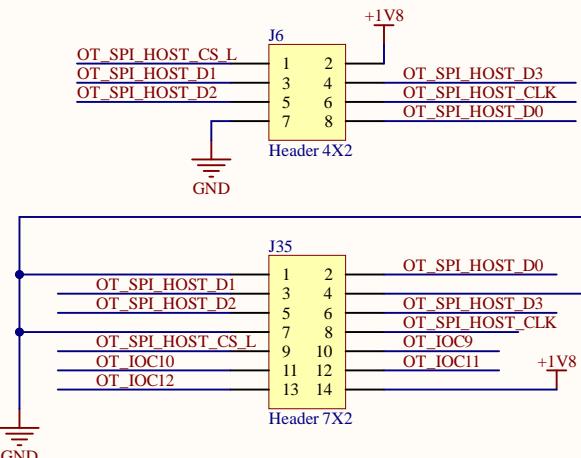
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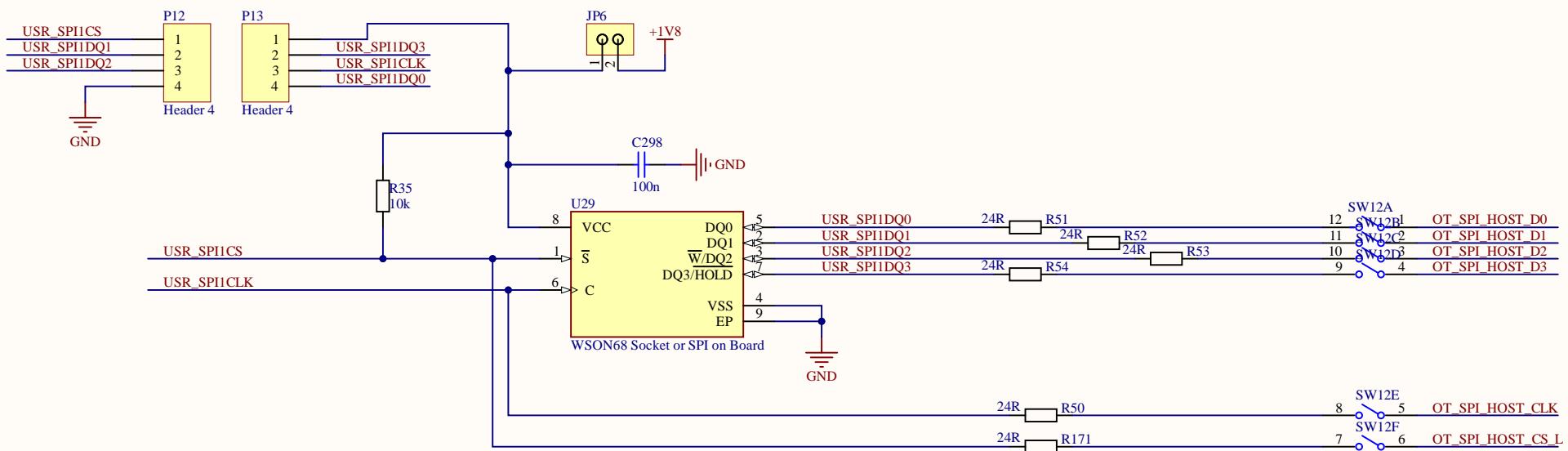
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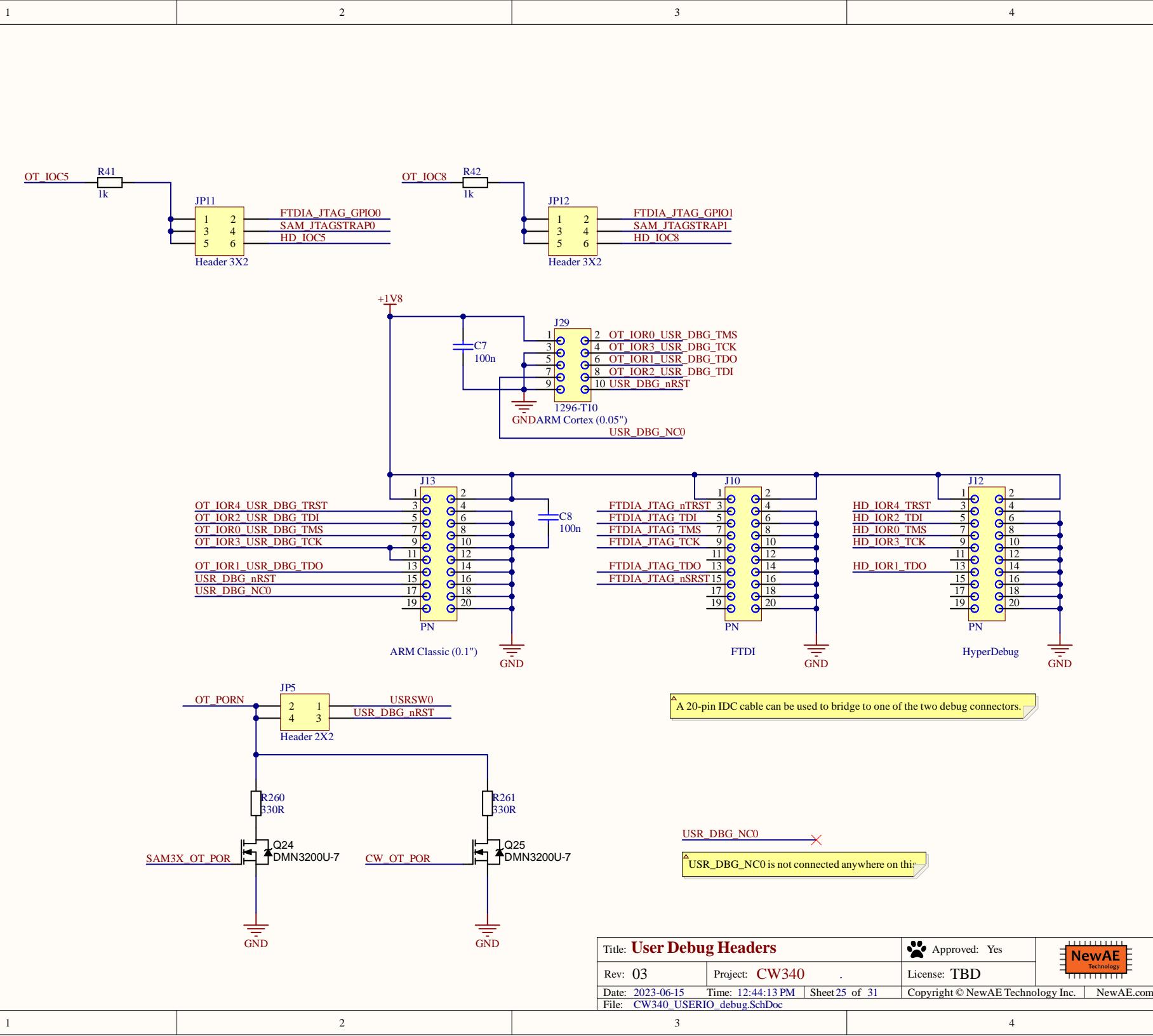
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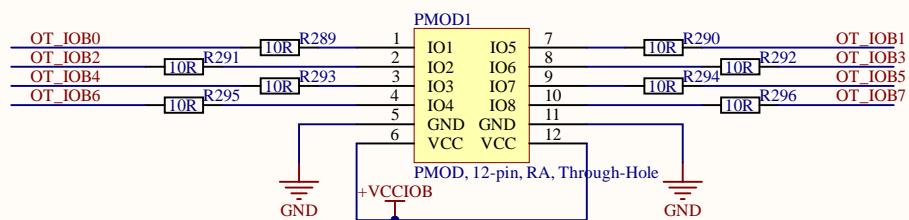
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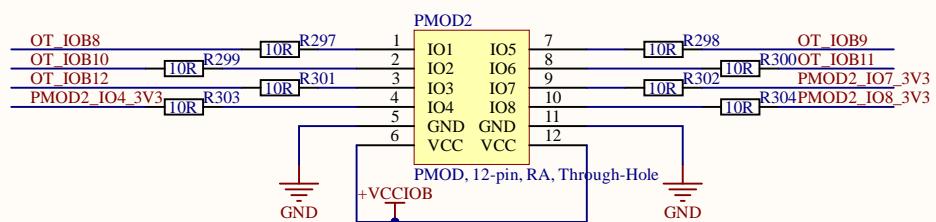
Title: SPI Flash & Breakout		Approved: NO	NewAE Technology
Rev: 03	Project: CW340	License: TBD	
Date: 2023-06-15	Time: 12:44:13 PM	Sheet 24 of 31	Copyright © NewAE Technology Inc. NewAE.com
File: CW340_SPI_flashes.SchDoc			



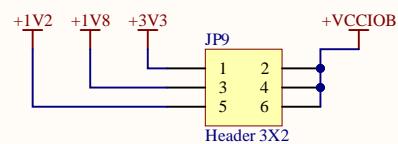
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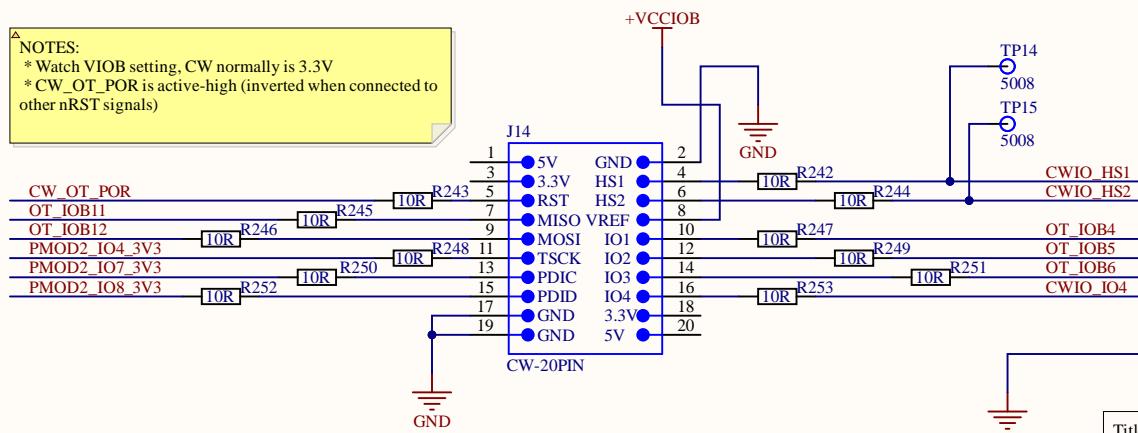
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C

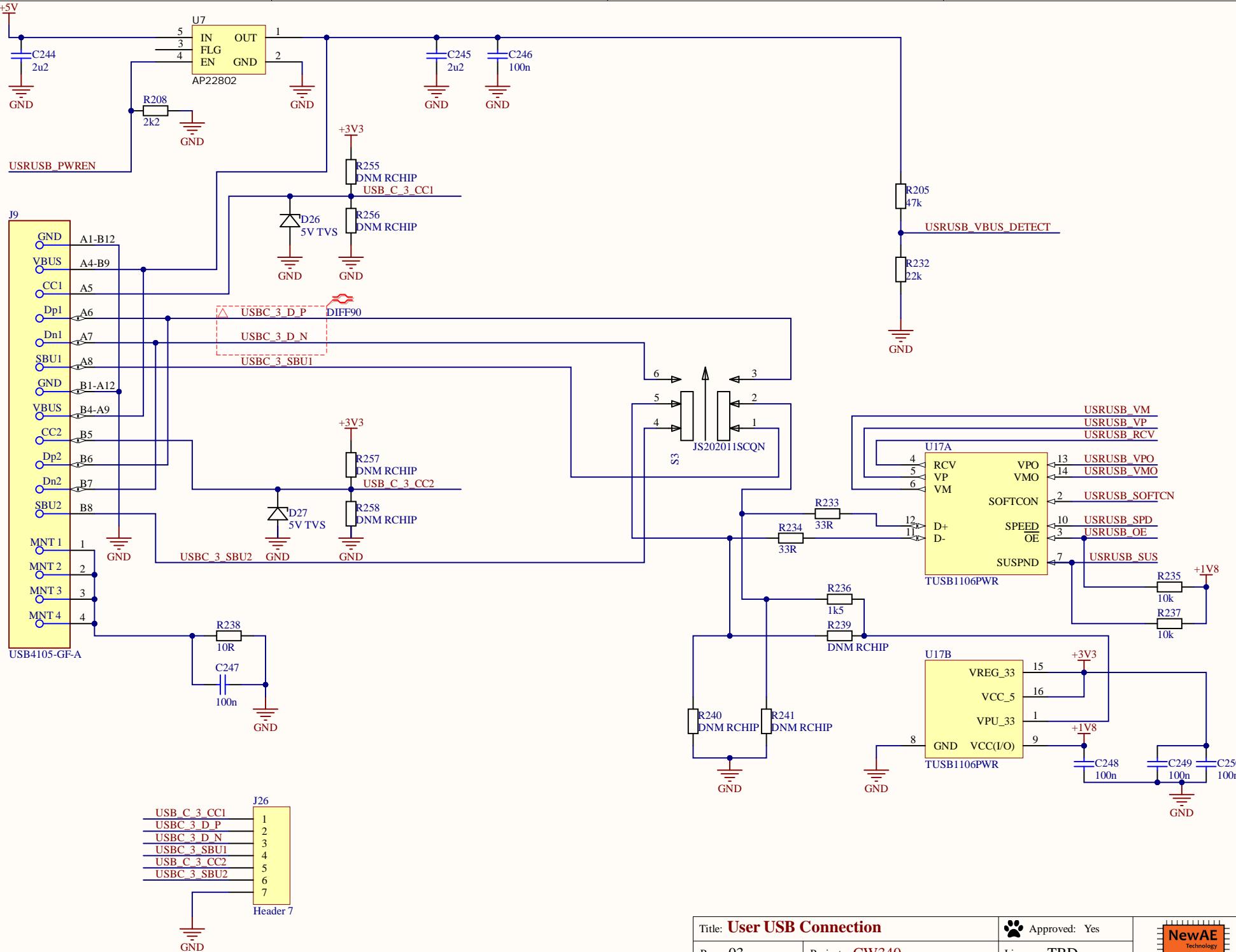


NOTES:
 * Watch VIOB setting, CW normally is 3.3V
 * CW_OT_POR is active-high (inverted when connected to other nRST signals)



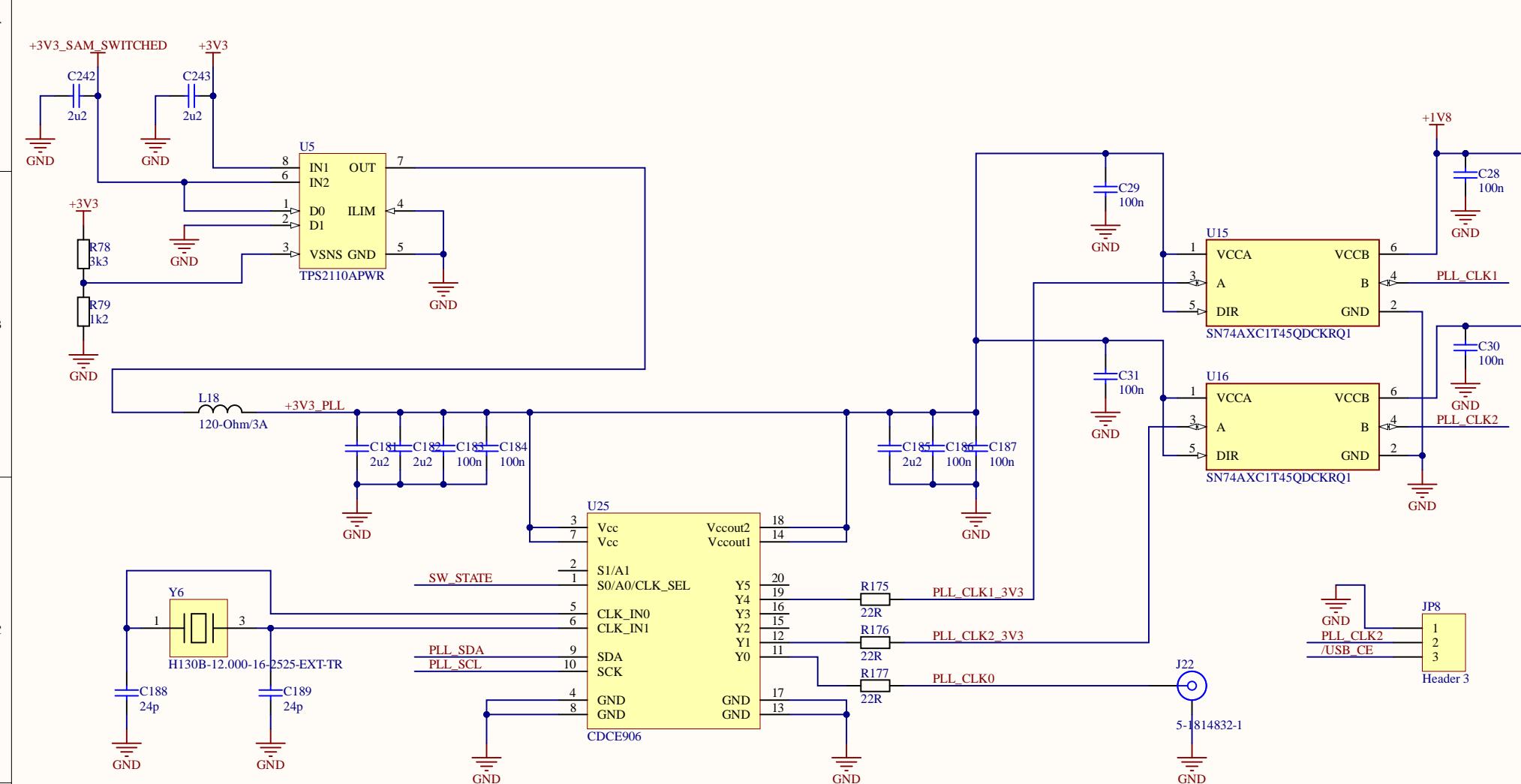
Ground

Title: User GPIO Headers			Approved: Yes	NewAE Technology
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File: CW340_USERIO_Header.SchDoc				



Title: User USB Connection		Approved: Yes	NewAE Technology
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CLOCKS



Title: PLL, Clocks for FPGA

Approved: NO



Rev: 03

Project: CW340

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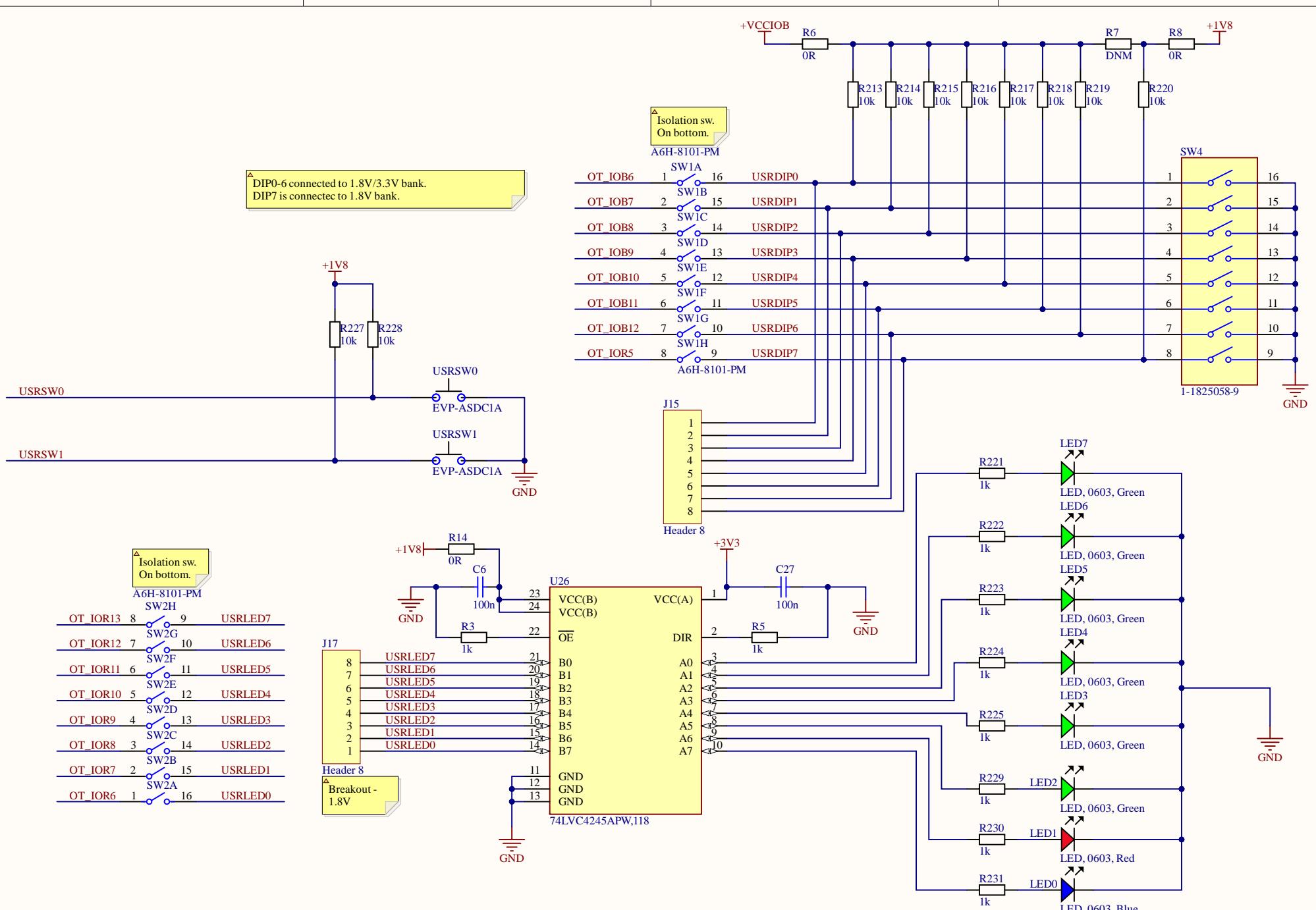
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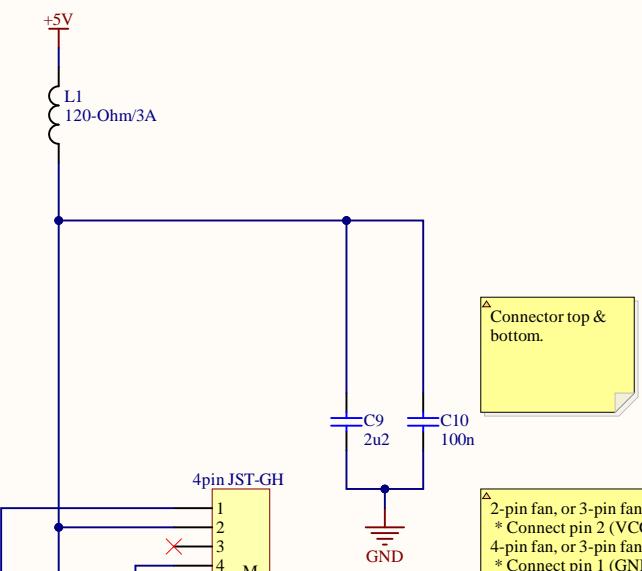
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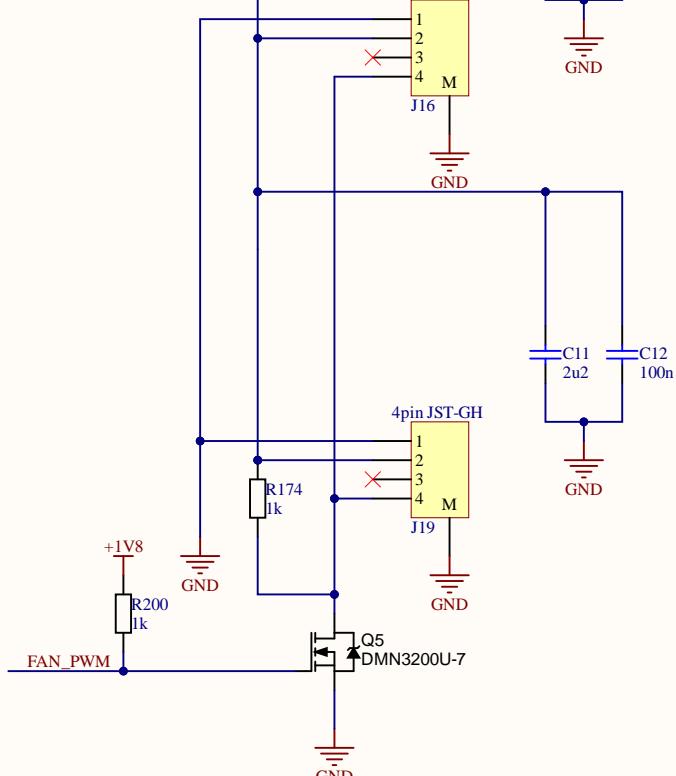
Title: **User LED / Switches** Approved: NO

 Rev: 03 Project: **CW340** License: TBD
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 File: **CW340_STATUS_LEDs.SchDoc** NewAE.com

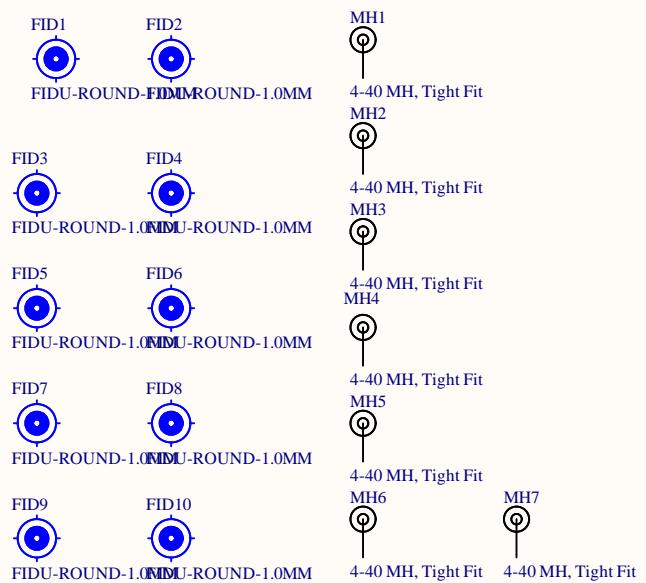
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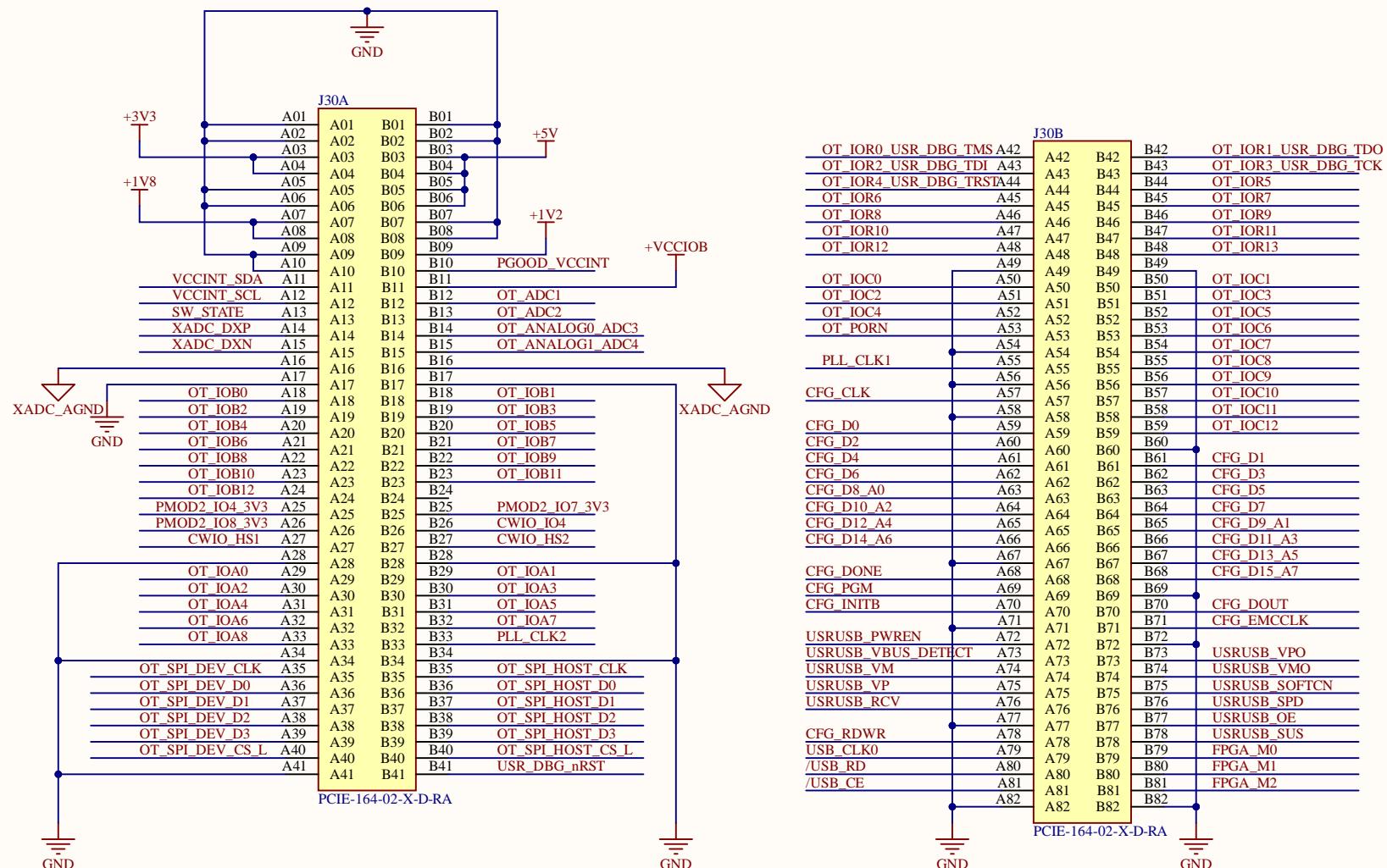
△ Connector top & bottom.
 △ 2-pin fan, or 3-pin fan with tach output:
 * Connect pin 2 (VCC), pin 4 (GND).
 4-pin fan, or 3-pin fan with control input:
 * Connect pin 1 (GND), pin 2 (VCC), pin 4 (CTRL).
 If fan has tach output, connect to pin 3 (NC) to terminate header.



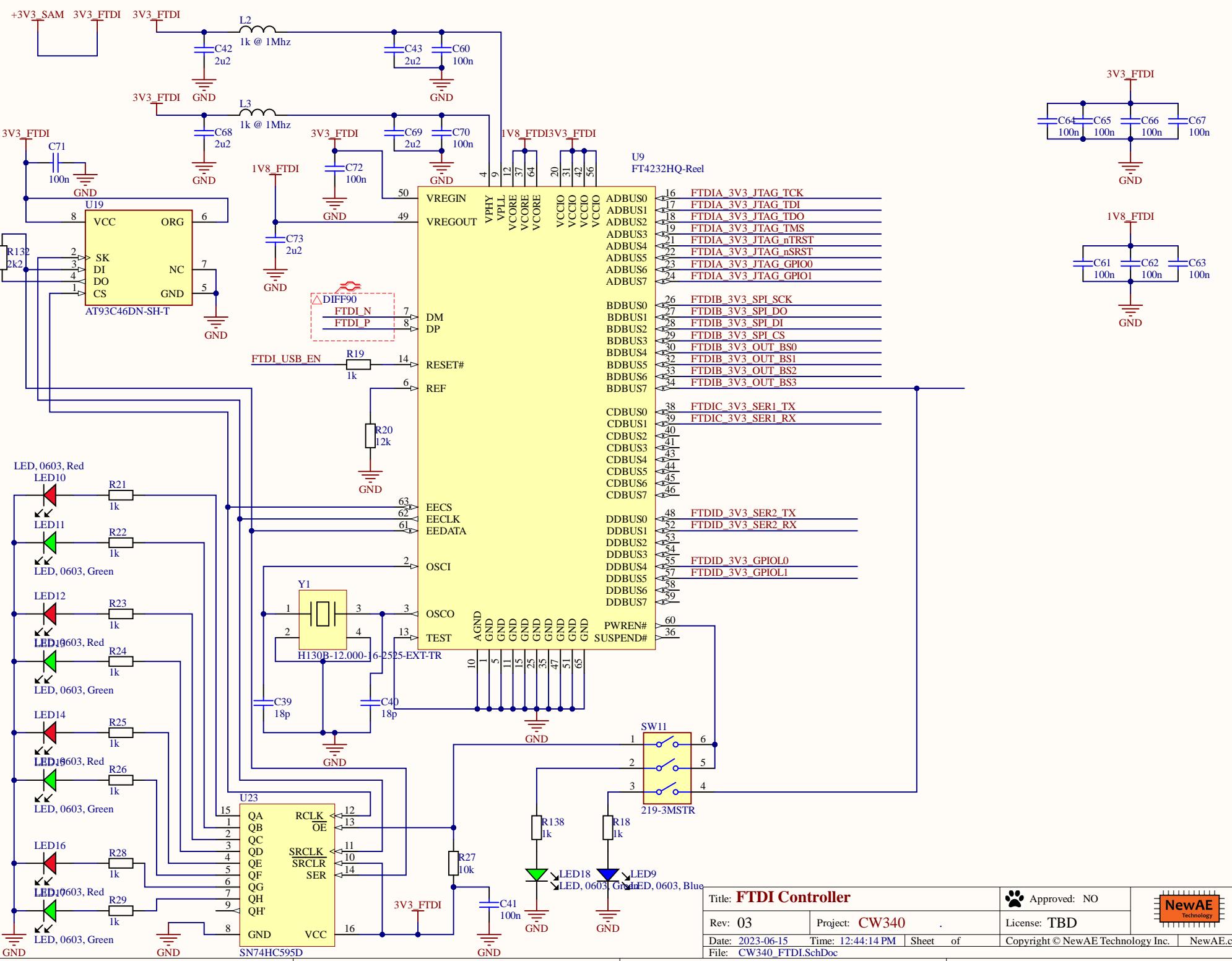
△ Mating connector:
 * Housing GHR-04V-S
 * Contacts SSHL-002T-P0.2
 * Crimp tool YRS-1590



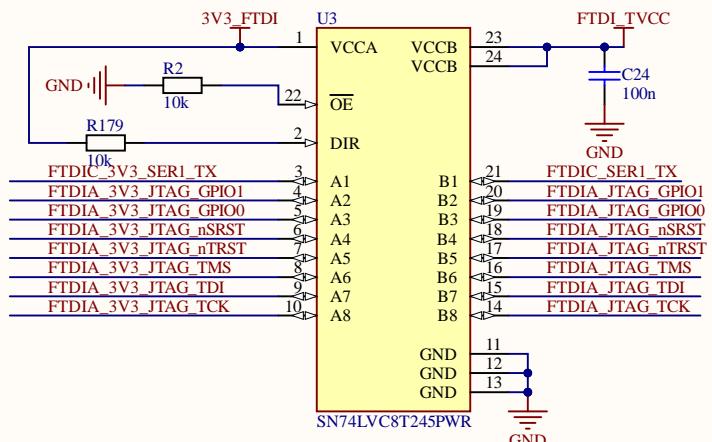
Title: FAN Headers		Approved: Yes	
Rev: 03	Project: CW340	License: TBD	
Date: 2023-06-15	Time: 12:44:14 PM	Sheet 31 of 31	Copyright © NewAE Technology Inc. NewAE.com
File: CW340 HEATSINK_FAN.SchDoc			



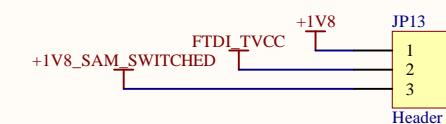
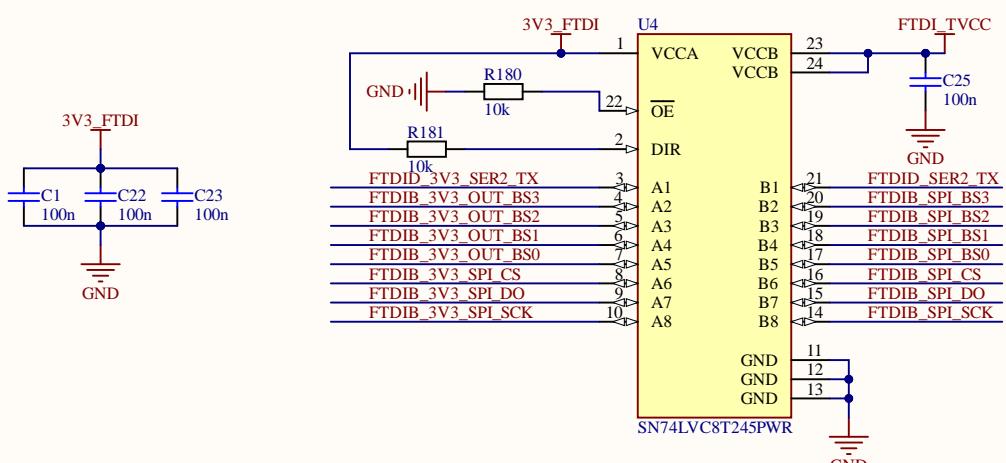
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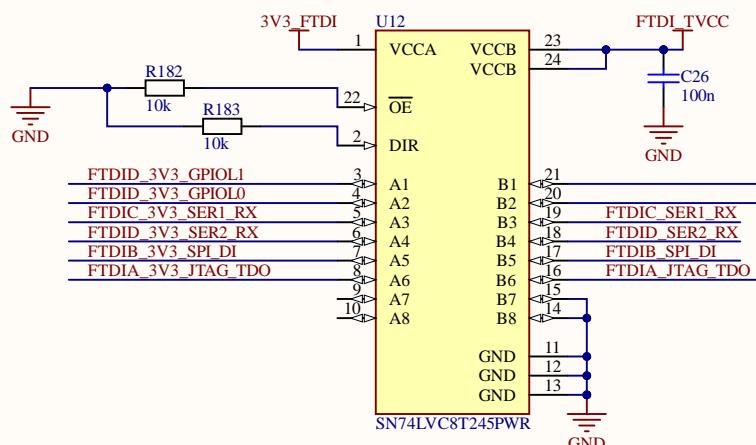
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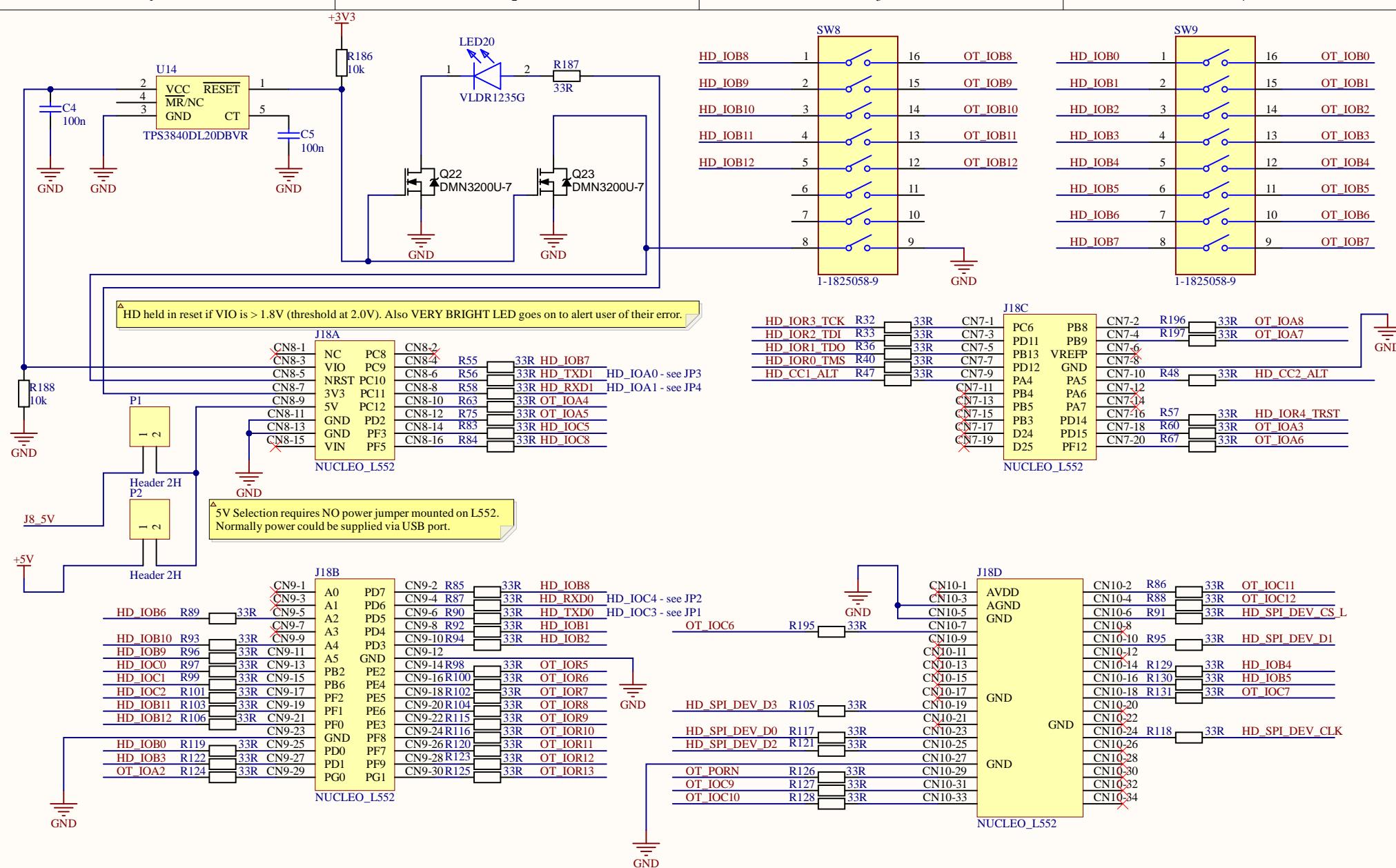
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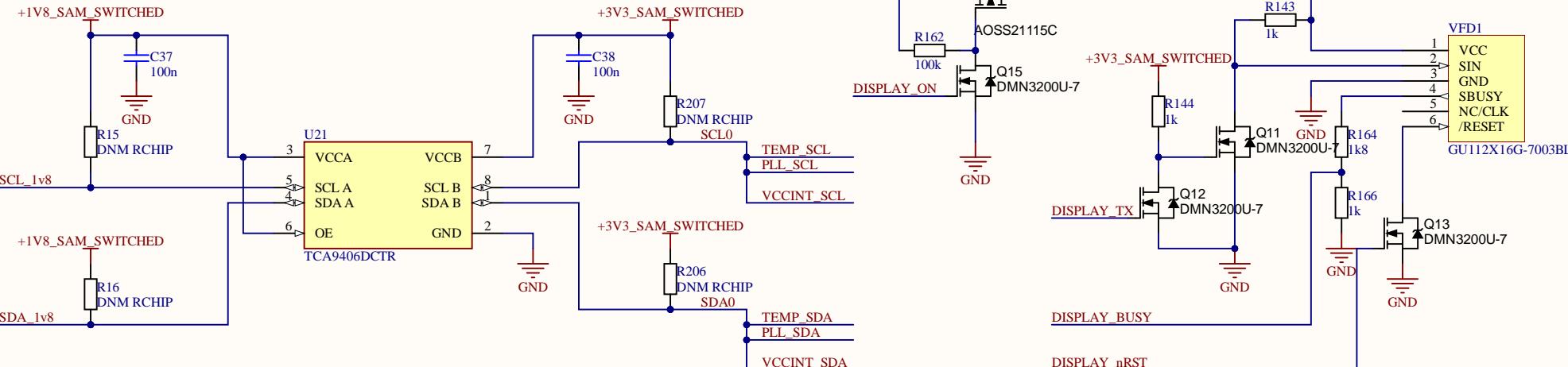


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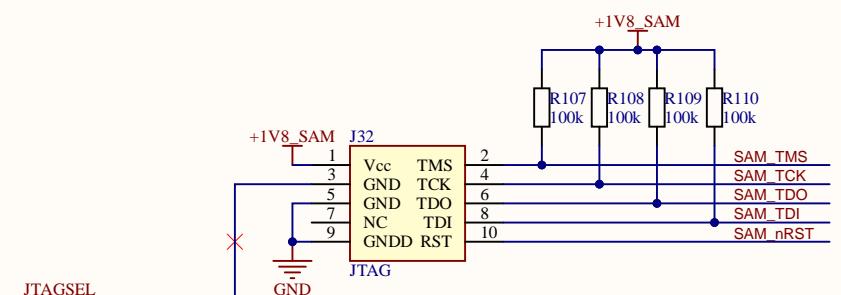


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△ If SAM3X goes to sleep, turns off connected devices (PLL chip, etc). Also need to turn off power to pull-ups and similar.



Title: MCU Misc Connections		Approved: NO	NewAE Technology
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A

A

B

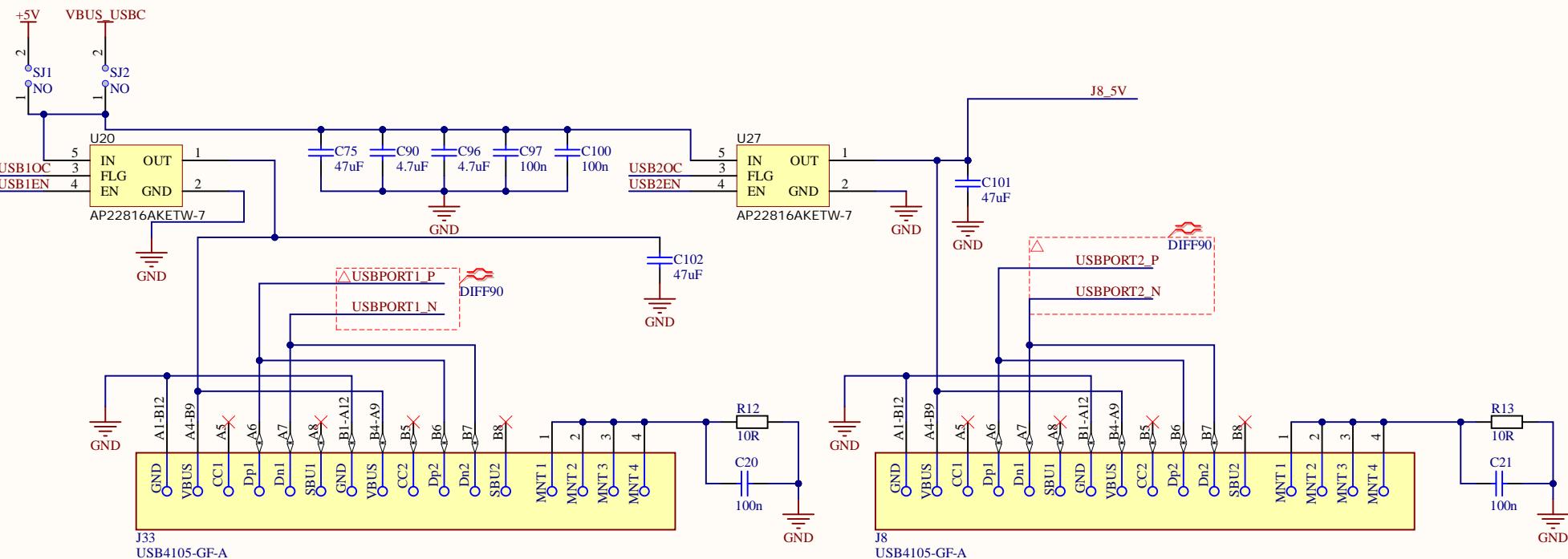
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C

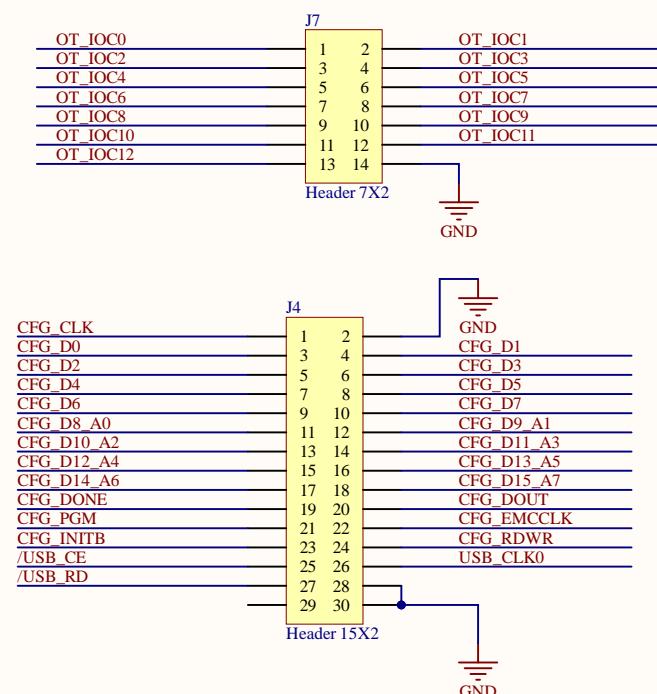
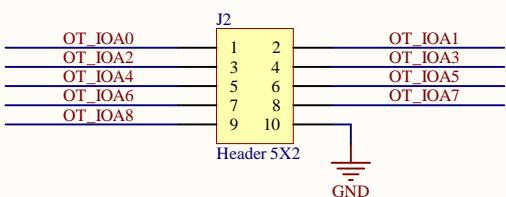
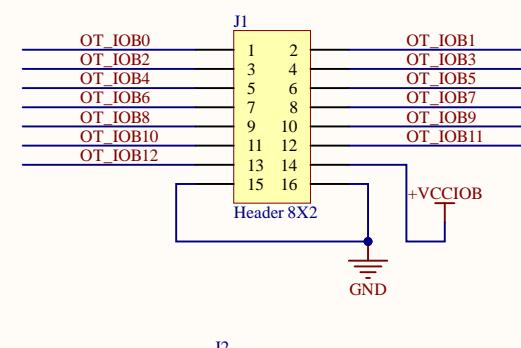
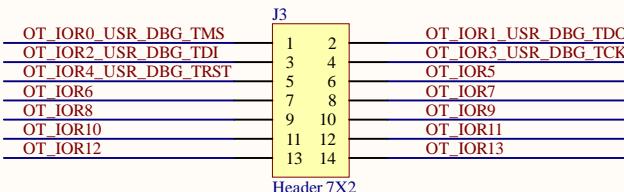
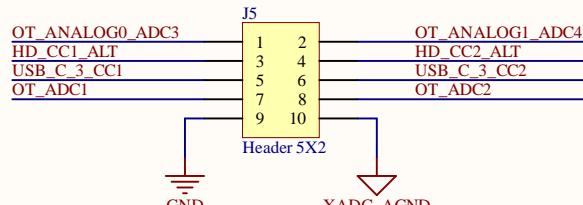
D

D



Title

Size	Number	Revision
A4		
Date:	6-15-2023	Sheet of
File:	C:\Users\...\CW340_USBHUB_ExtPorts.SchDoc	Submitted By:



Title: Breakout from Edge Connector

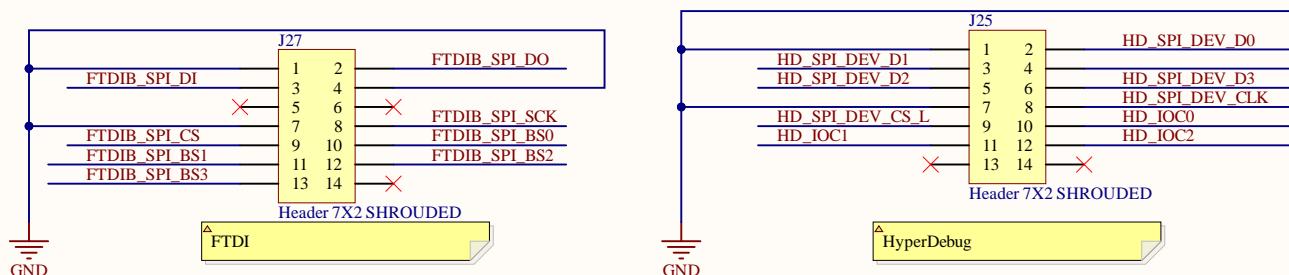
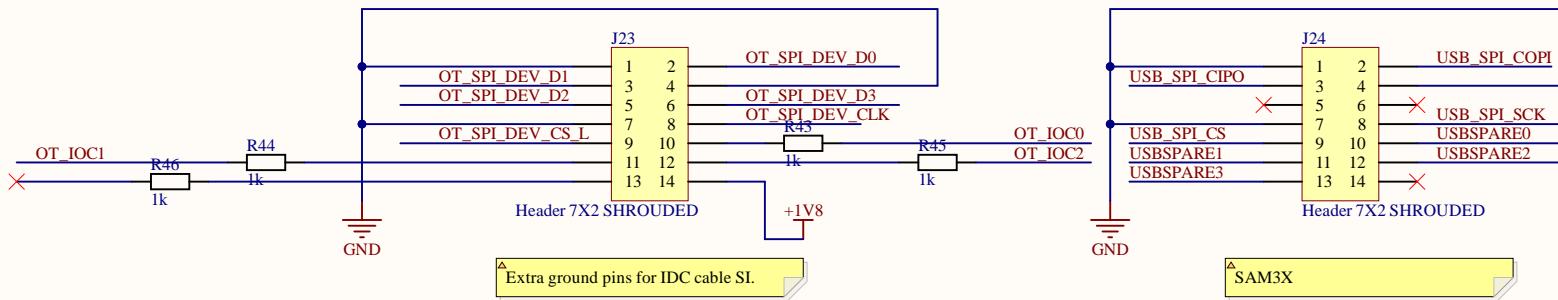
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Approved: NO



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Title: Serial Selection Jumpers		 Approved: NO	
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