

A

A

B

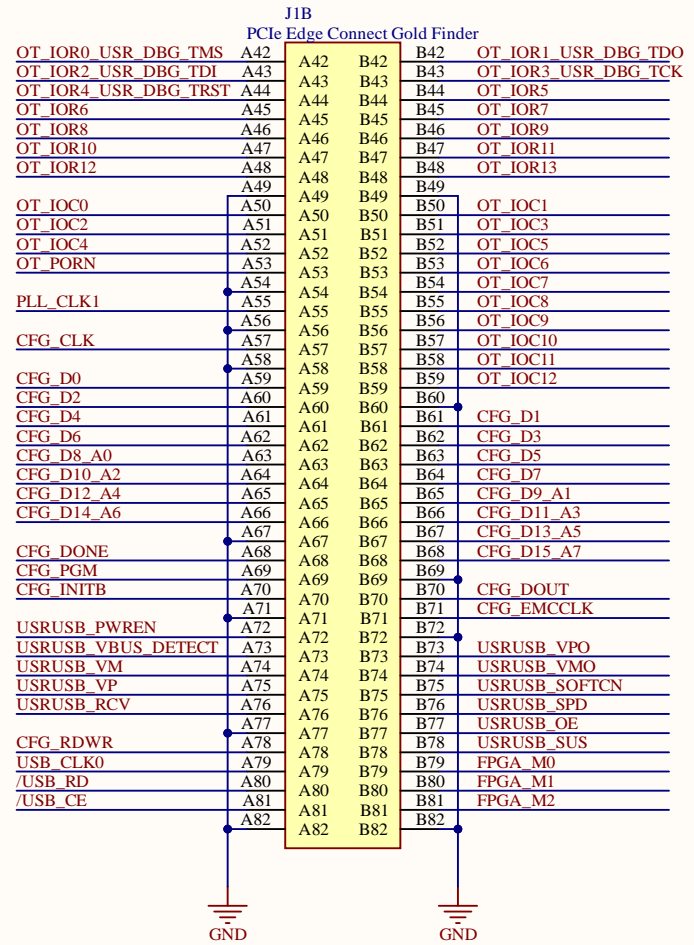
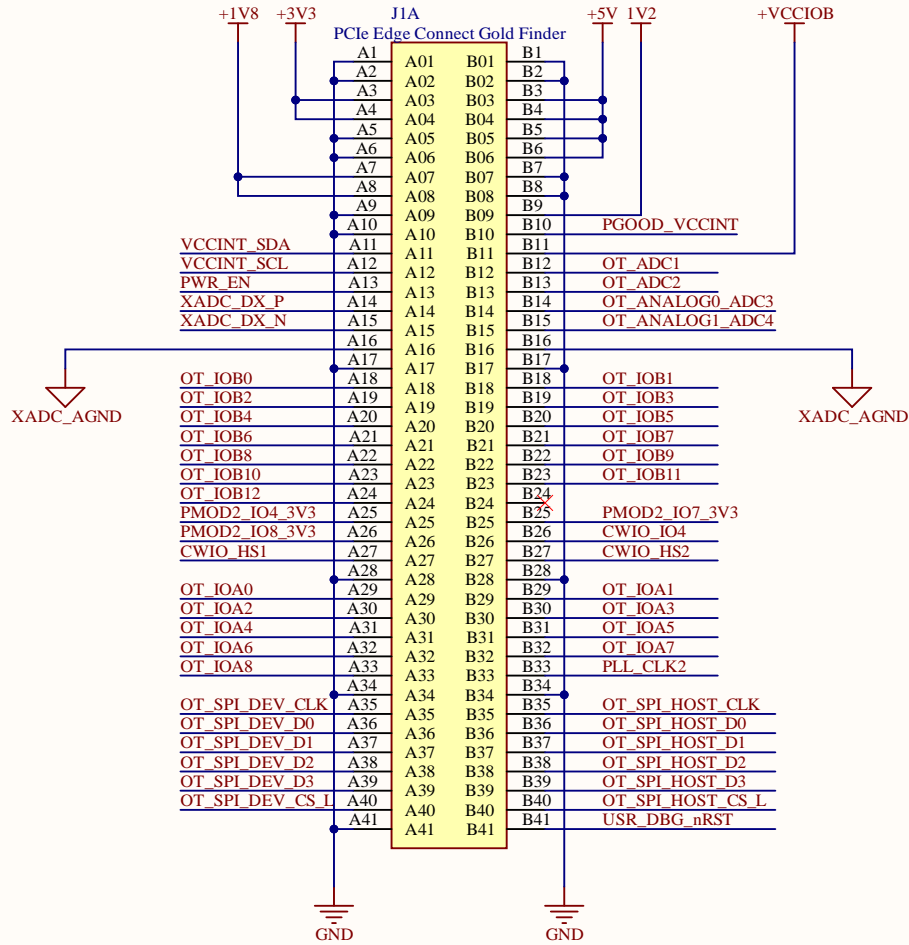
B

C

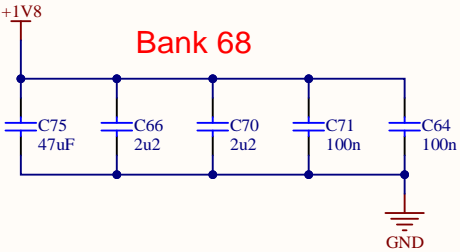
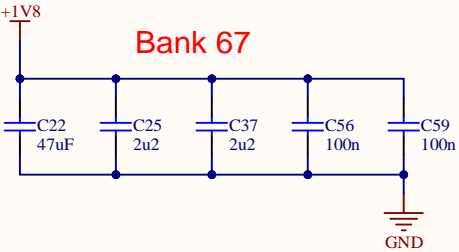
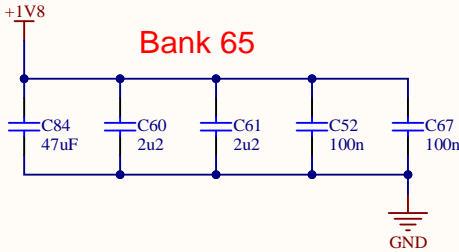
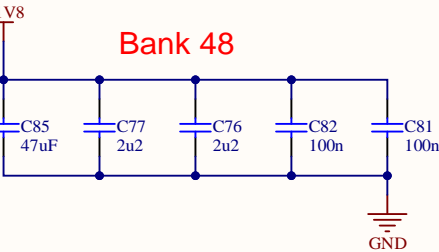
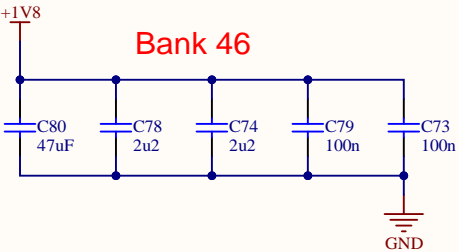
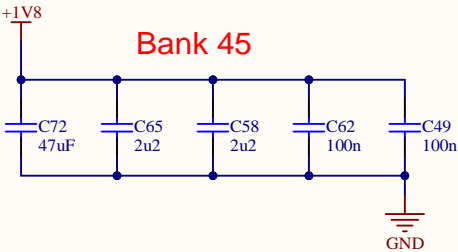
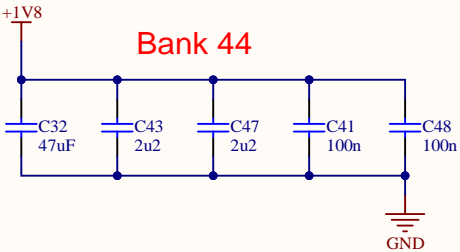
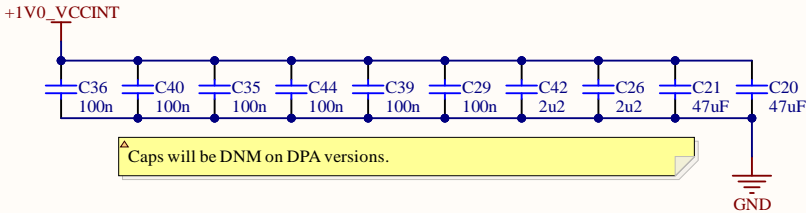
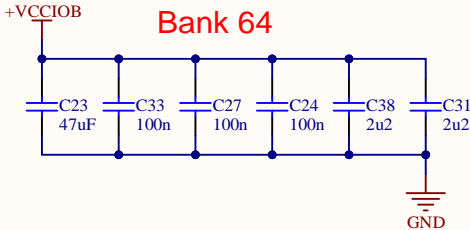
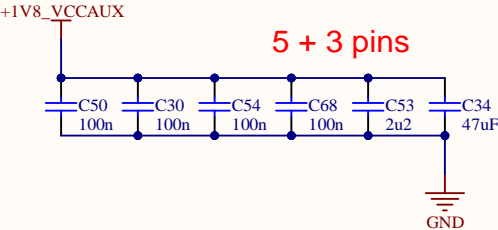
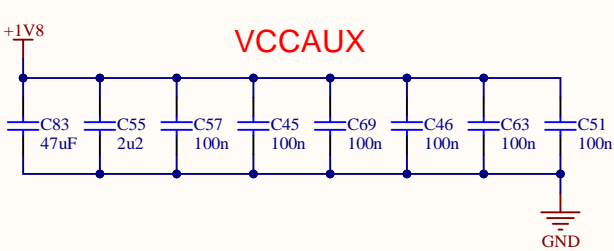
C

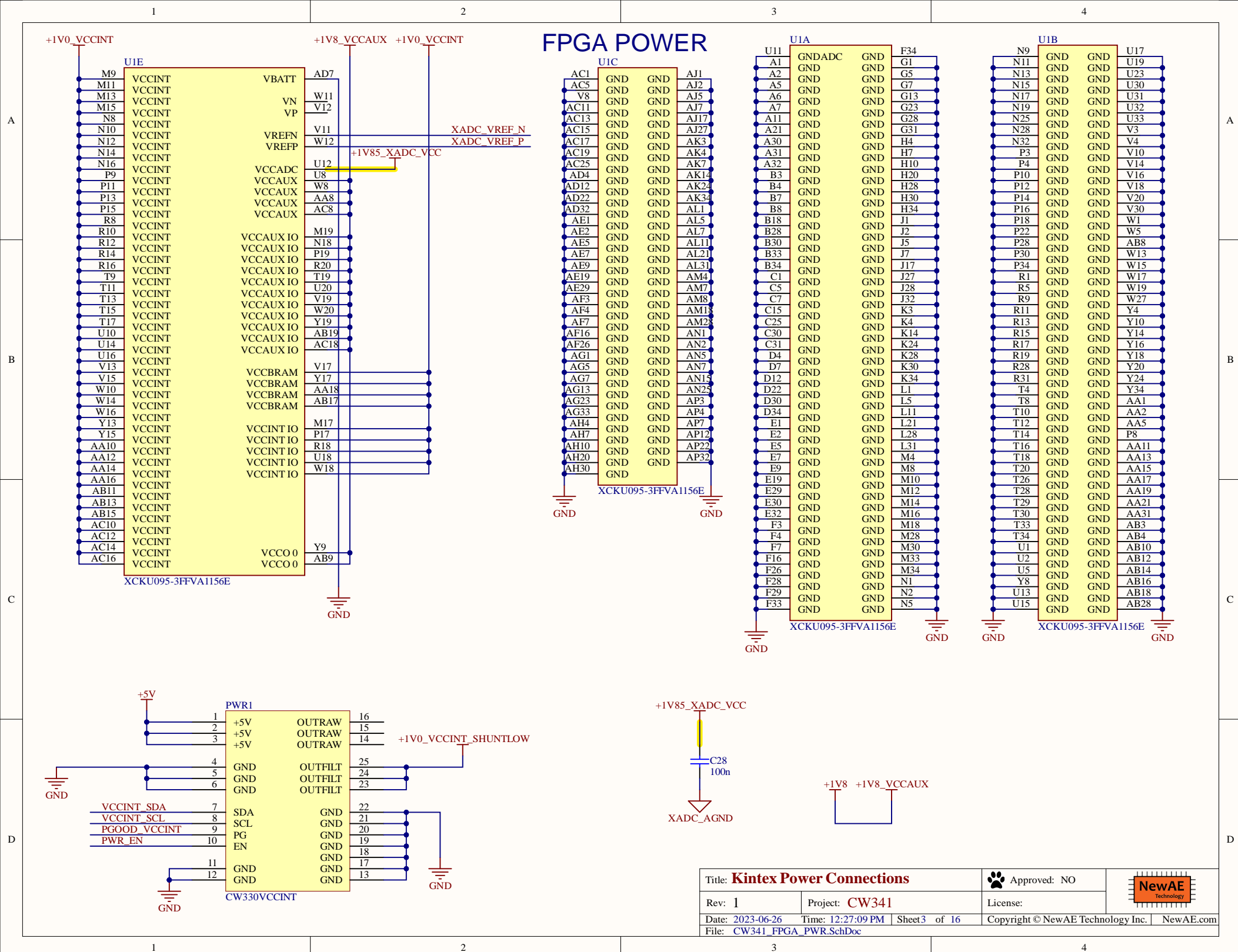
D

D

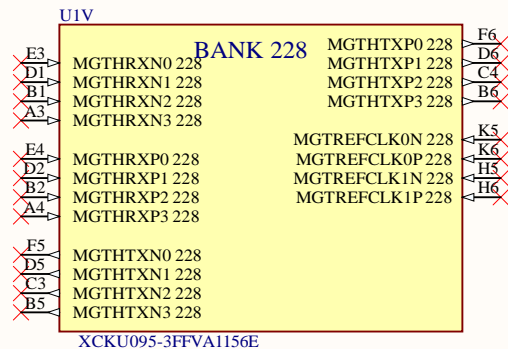
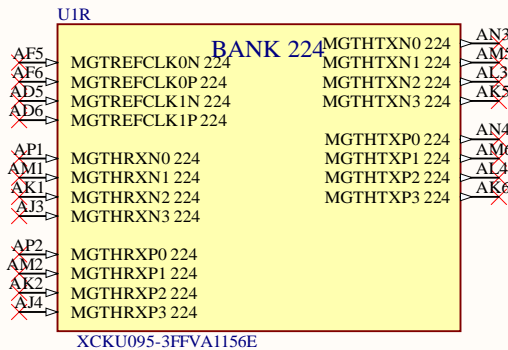
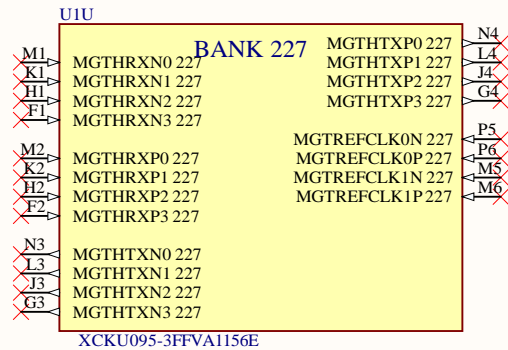
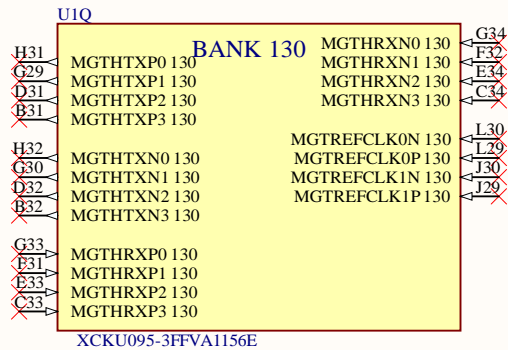
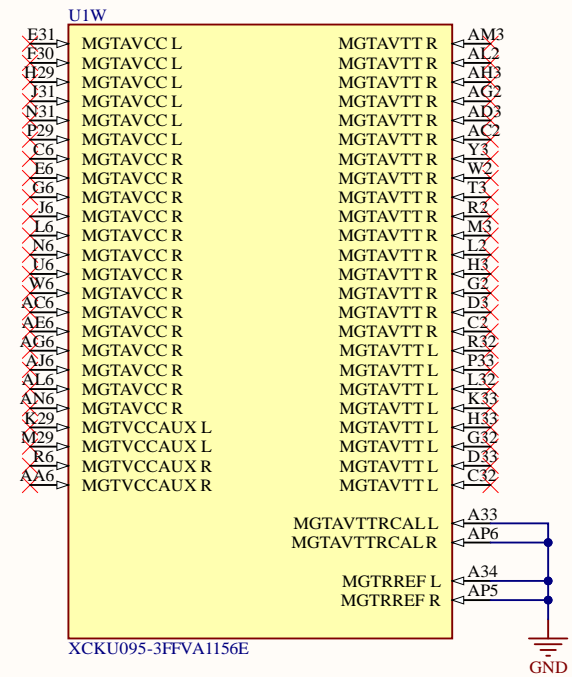
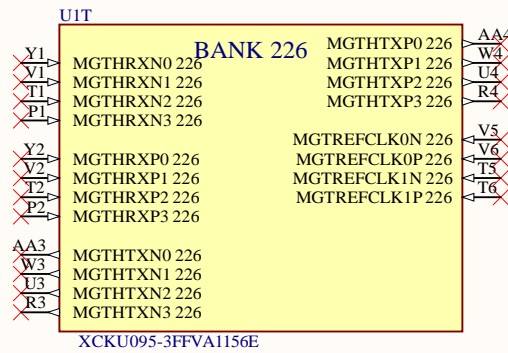
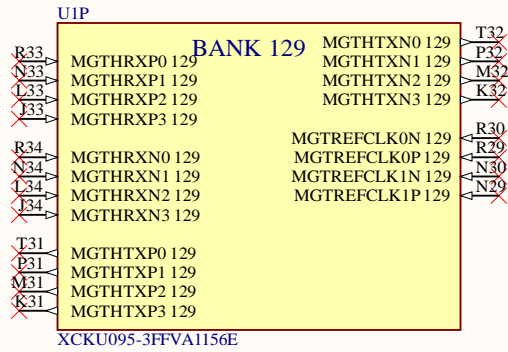


FPGA Decoupling



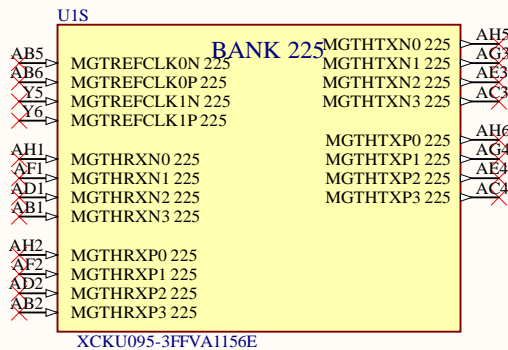


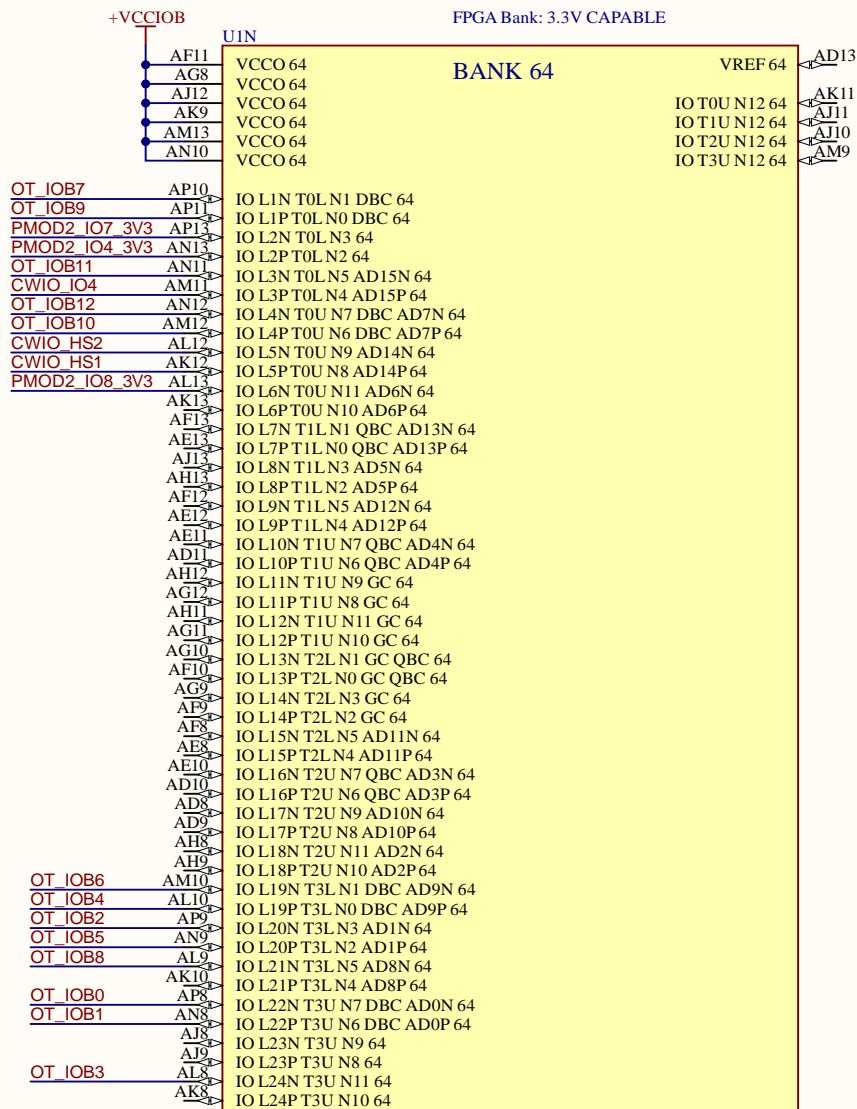
FPGA MGT Interface



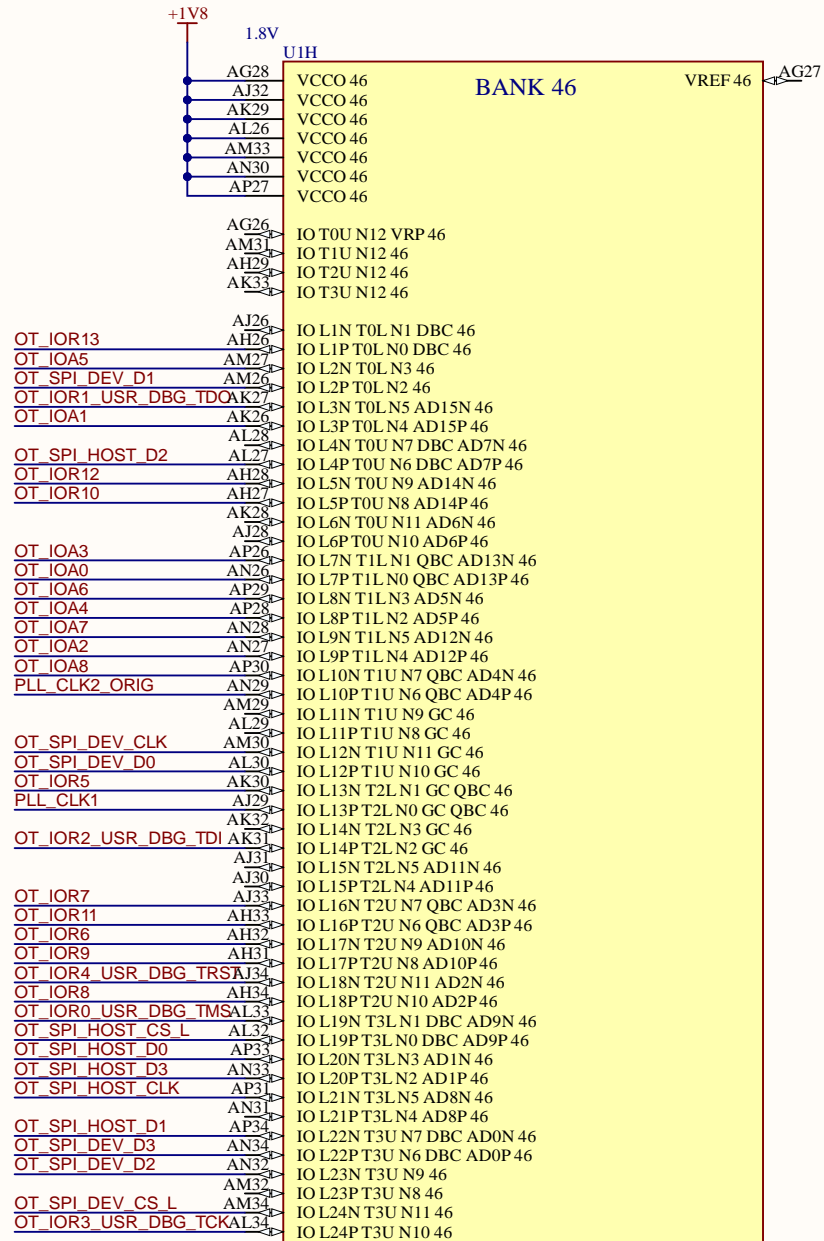
From UG576 regarding MGTAVCC, MGTAVTT, MGTVCCAUX pins:

If all of the Quads in a power supply group are not used, the associated pins can be left unconnected or tied to GND (unless the RCAL circuit is in that Quad).






XCKU095-3FFVA1156E



XCKU095-3FFVA1156E

Title: **Kintex IO Banks** Approved: No

Rev: 1

Project: **CW341**

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Time: 12:27:09 PM

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File: **CW341_FPGAIO_1.SchDoc**

A

B

C

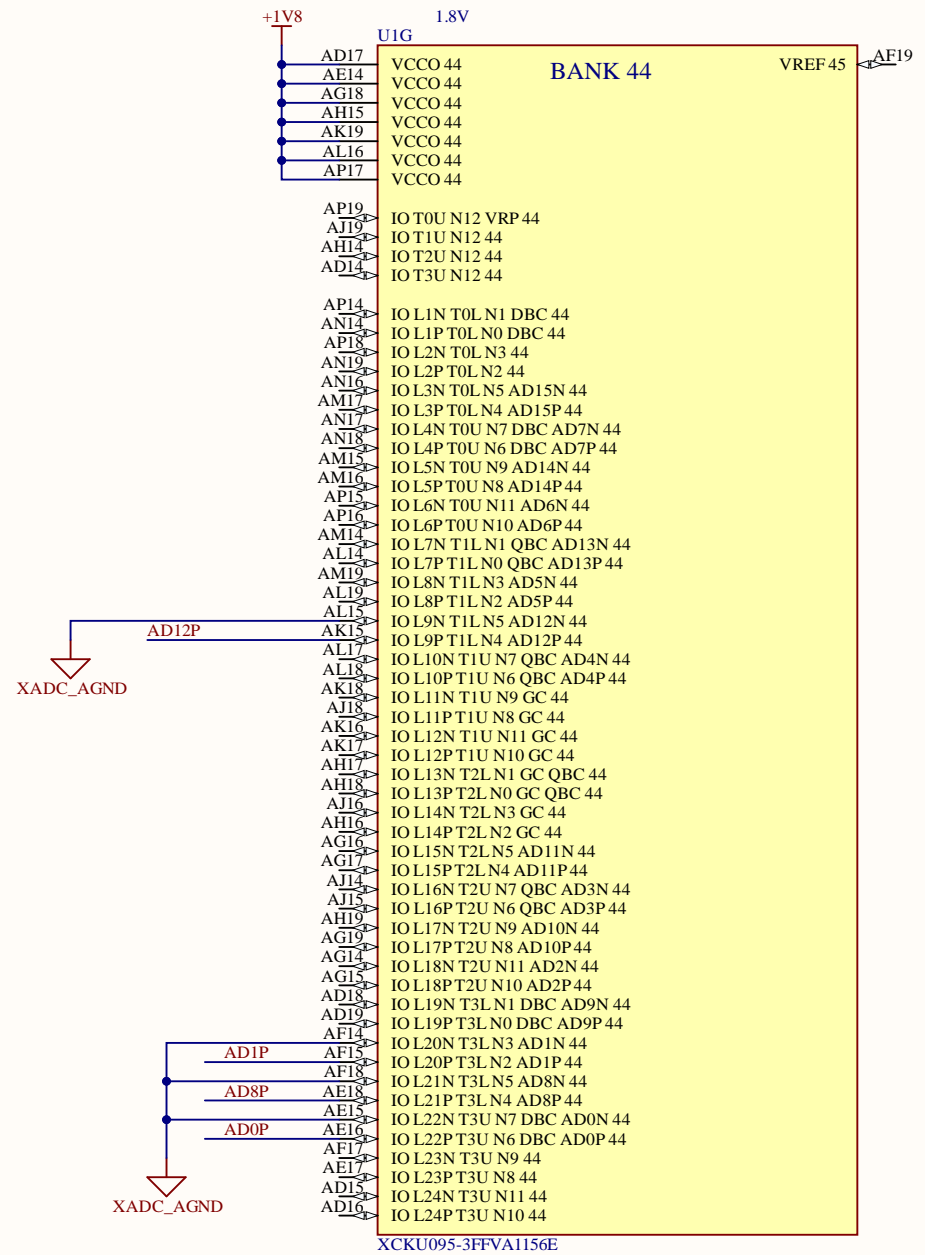
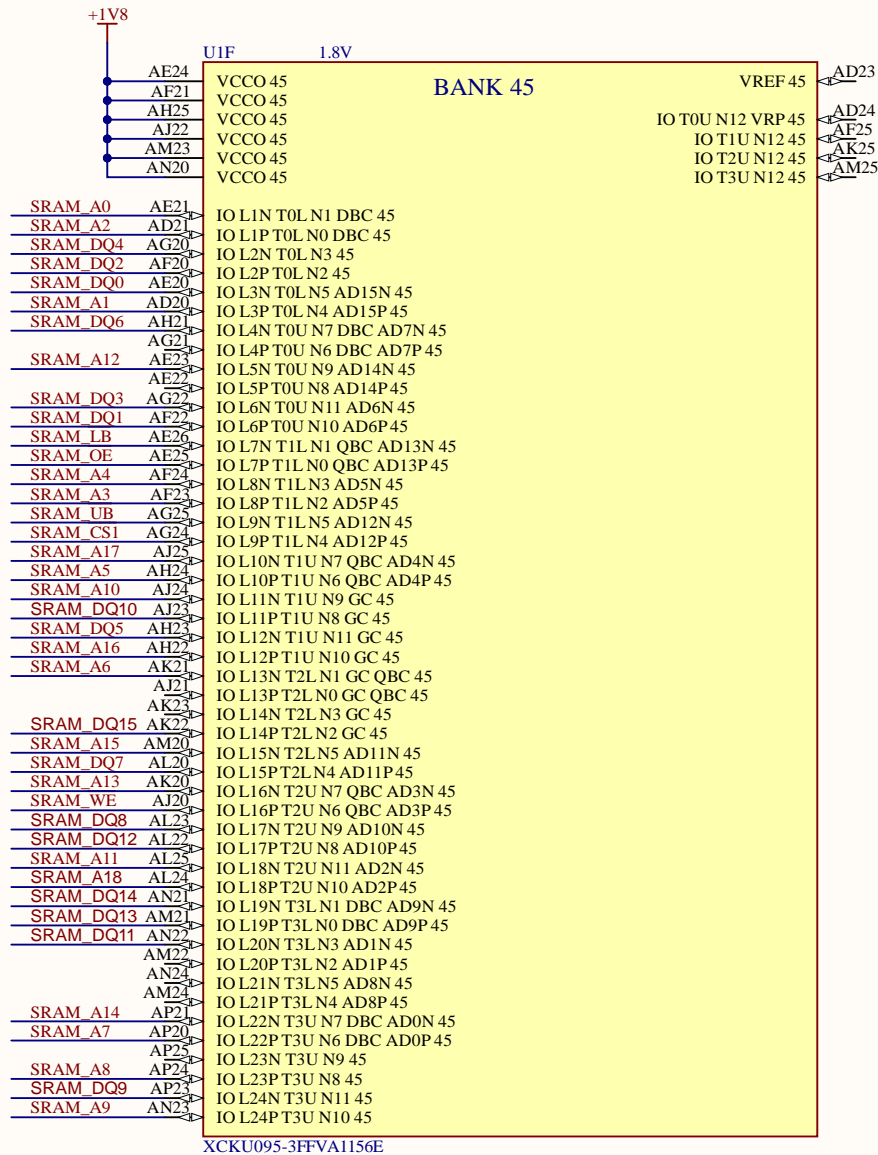
D

A

B

C

D



A

B

C

D

A

B

C

D

FPGA Bank: 1.8V (HP Bank)

U10

BANK 65

VREF 65

H25 VCCO 65
J22 VCCO 65
L26 VCCO 65
M23 VCCO 65
N20 VCCO 65
P27 VCCO 65
R24 VCCO 65

IO T0U N12 A28 65
IO T1U N12 PERSTN1 65
IO T2U N12 CSI ADV B 65
IO T3U N12 PERSTN0 65

CSI ADV_B



OT_PORN

OT_IOC9

OT_IOC12

OT_IOC10

OT_IOC11

OT_IOC6

OT_IOC7

OT_IOC8

OT_IOC5

OT_IOC4

OT_IOC3

OT_IOC2

OT_IOC1

OT_IOC0

CFG_D15_A7

CFG_D14_A6

CFG_D13_A5

CFG_D12_A4

CFG_D11_A3

CFG_D10_A2

CFG_D9_A1

CFG_D8_A0

CFG_D7

CFG_D6

CFG_D5

CFG_D4

CFG_DOUT

CFG_EMCCLK

XCKU095-3FFVA1156E

1.8V

U1L

BANK 68

VREF 68

A26 VCCO 68
B23 VCCO 68
C20 VCCO 68
D27 VCCO 68
E24 VCCO 68
F21 VCCO 68

IO T0U N12 VRP 68
IO T1U N12 68
IO T2U N12 68
IO T3U N12 68

USRUSB_SOFTCN

USRUSB_RCV

USRUSB_VM

USRUSB_VP

USRUSB_PWREN

USRUSB_VPO

USRUSB_VBUS_DETECT

USRUSB_SPD

USRUSB_VMO

USRUSB_SUS

USERIOA-40

USB_CLK0

USRUSB_OE

/USB_RD

/USB_CE

USR_DBG_nRST

PLL2_CLK_ALT

USERIOA-12

USERIOA-14

USERIOA-16

USERIOA-18

USERIOA-24

USERIOA-26

USERIOA-28

USERIOA-30

USERIOA-32

USERIOA-36

USERIOA-38

E27 IO L1N T0LN1 DBC 68
F27 IO L1PT0LN0 DBC 68
B27 IO L2N T0LN3 68
C27 IO L2PT0LN2 67
D29 IO L3N T0LN5 AD15N 68
E28 IO L3PT0LN4 AD15P 68
A29 IO L4N T0U N7 DBC AD7N 68
B29 IO L4PT0U N6 DBC AD7P 68
C28 IO L5N T0U N9 AD14N 68
D28 IO L5PT0U N8 AD14P 67
A28 IO L6N T0U N11 AD6N 68
A27 IO L6PT0U N10 AD6P 68
D26 IO L7N T1LN1 QBC AD13N 68
E26 IO L7PT1LN0 QBC AD13P 68
A25 IO L8N T1LN3 AD5N 68
B25 IO L8PT1LN2 AD5P 68
B26 IO L9N T1LN5 AD12N 68
C26 IO L9PT1LN4 AD12P 68
A24 IO L10N T1U N7 QBC AD4N 68
B24 IO L10PT1U N6 QBC AD4P 68
D25 IO L11N T1U N9 GC 68
E25 IO L11PT1U N8 GC 68
C24 IO L12N T1U N11 GC 68
D24 IO L12PT1U N10 GC 68
D23 IO L13N T2LN1 GC QBC 68
E23 IO L13PT2LN0 GC QBC 68
E22 IO L14N T2LN3 GC 68
B22 IO L14PT2LN2 GC 68
B21 IO L15N T2LN5 AD11N 68
C21 IO L15PT2LN4 AD11P 68
C20 IO L16N T2U N7 QBC AD3N 68
C20 IO L16PT2U N6 QBC AD3P 68
A20 IO L17N T2U N9 AD10N 68
F20 IO L22P T3U N6 DBC AD0P 68
E20 IO L22N T3U N7 DBC AD0N 68
B20 IO L20P T3LN2 AD1P 68
G24 IO L17PT2U N8 AD10P 68
E21 IO L19P T3LN0 DBC AD9P 68
D20 IO L20N T3LN3 AD1N 68
G23 IO L18PT2U N10 AD2P 68
D20 IO L24N T3U N11 68
E21 IO L18N T2U N11 AD2N 68
G22 IO L23P T3U N8 68
F22 IO L21P T3LN4 AD8P 68
F22 IO L23N T3U N9 68
F23 IO L21N T3LN5 AD8N 68
H21 IO L19N T3LN1 DBC AD9N 68
H21 IO L24P T3U N10 68

XCKU095-3FFVA1156E

Title: **Kintex IO Banks**

Approved: No



Rev: 1

Project: **CW341**

License:

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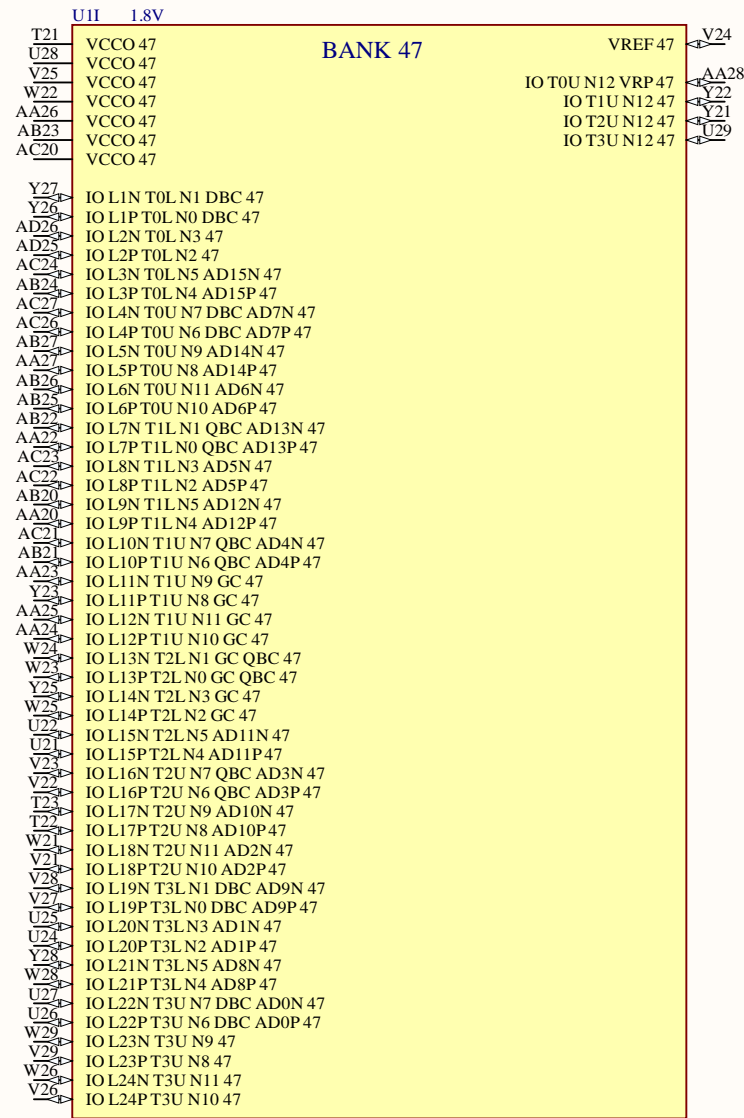
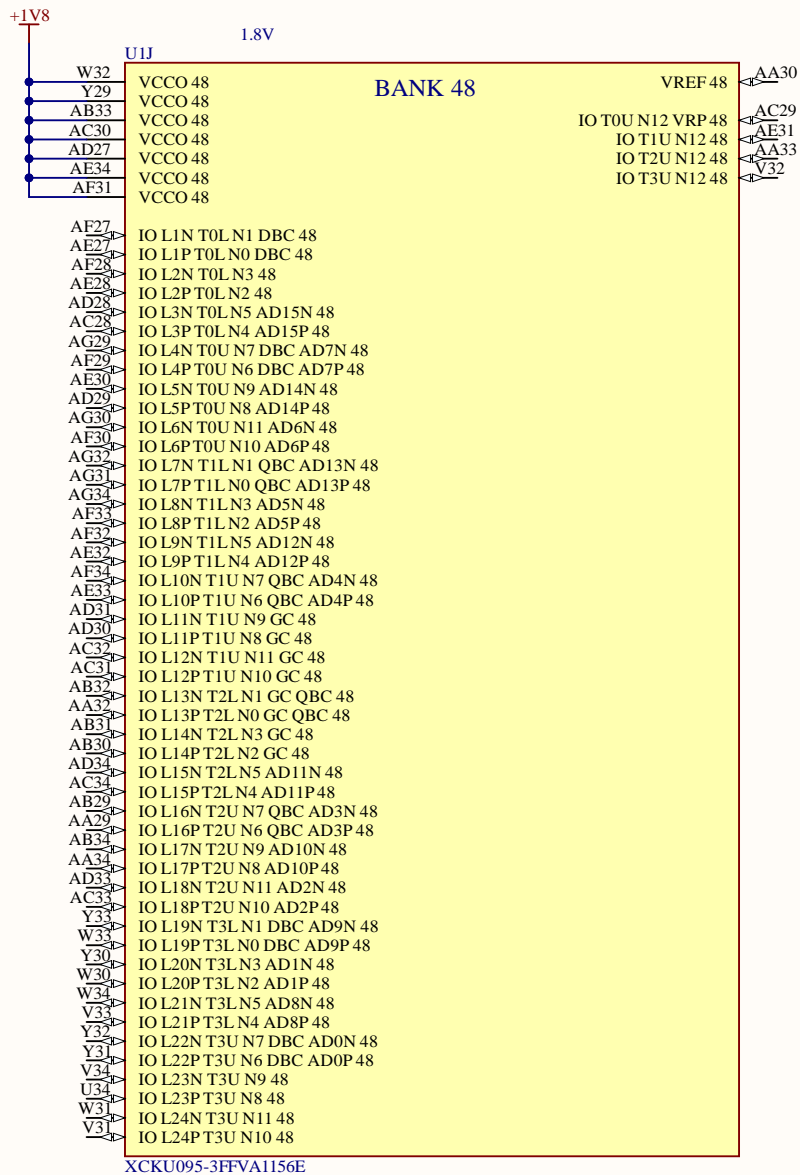
Time: 12:27:09 PM

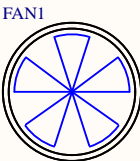
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Blower Fan, 5V, 35x35mm

⚠ Fan mounted top or bottom side of board. Blower style to pass over "open die top".



HS1
ATS-FPX035035015-56-C2-R0

⚠ Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.



MH1

4-40 MH, Tight Fit



MH2

4-40 MH, Tight Fit



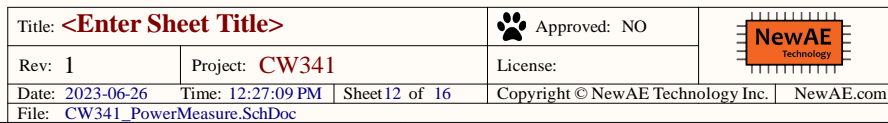
MH4

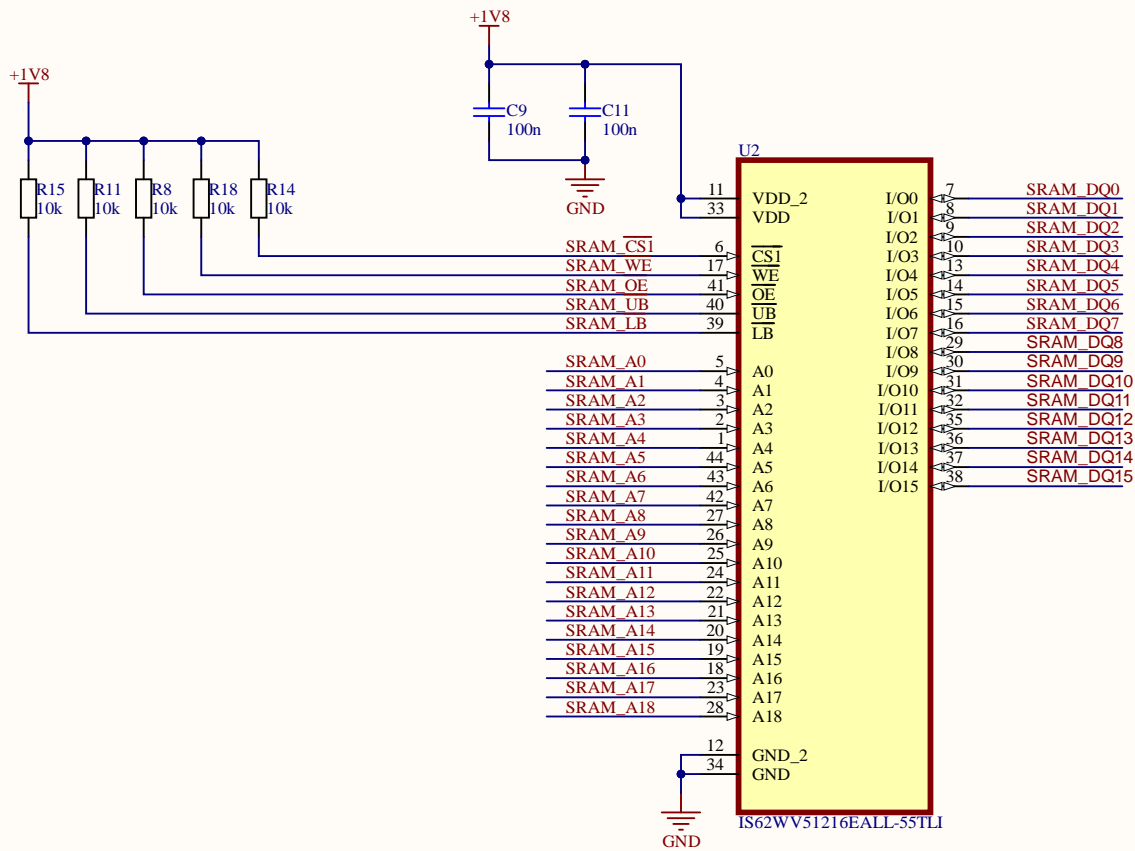
4-40 MH, Tight Fit



MH6

4-40 MH, Tight Fit





Title: **CW341 SRAM**

Approved: NO



Rev: 1

Project: **CW341**

License:

Date: 2023-06-26

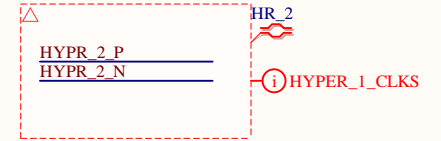
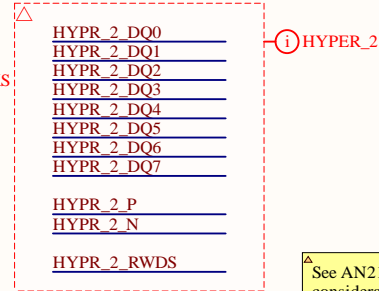
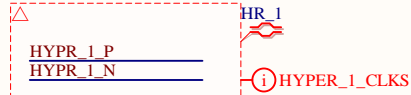
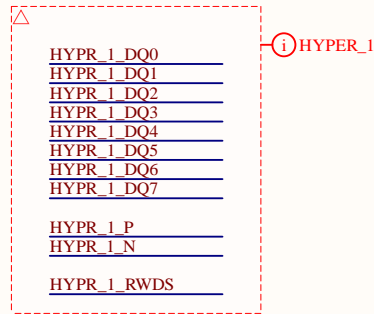
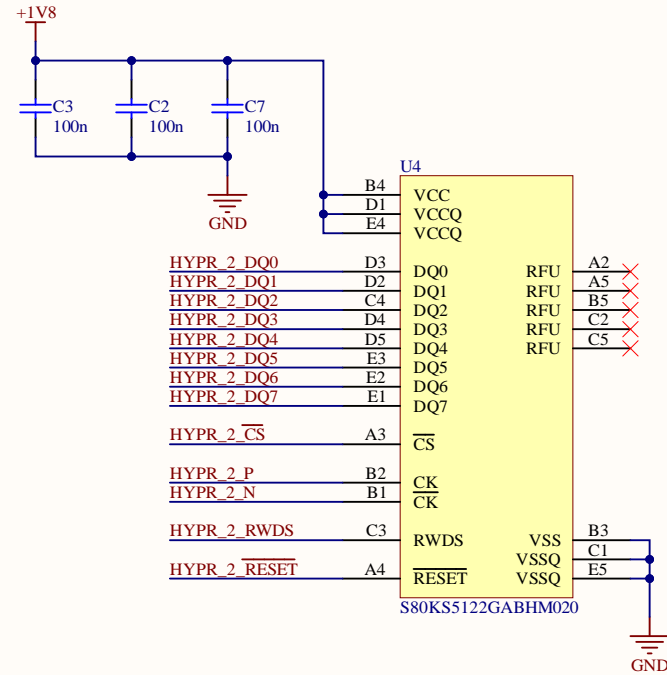
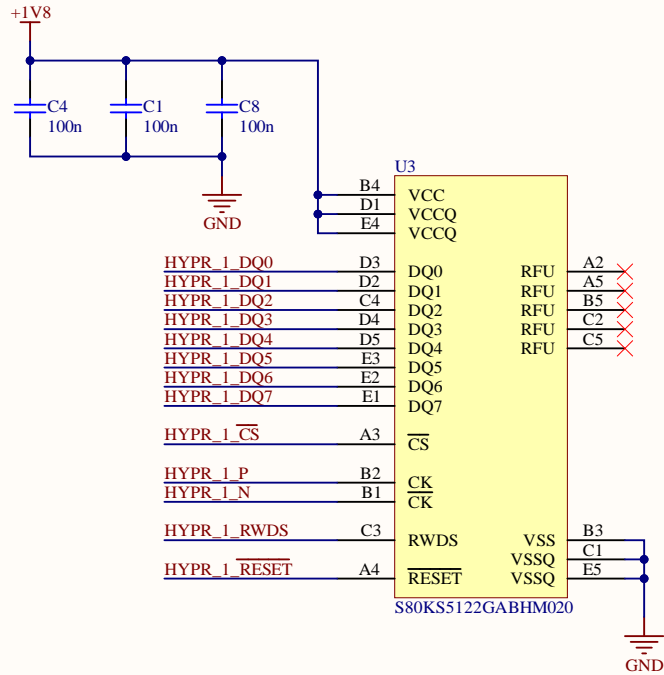
Time: 12:27:10 PM

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See AN211622 for Length Matching Rules and PCB design considerations

Title: **CW341 HyperRAM**

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Rev: 1

Project: **CW341**

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