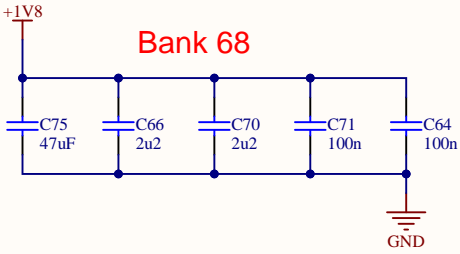
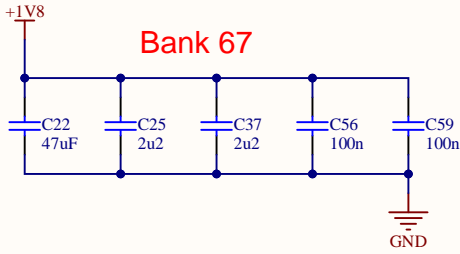
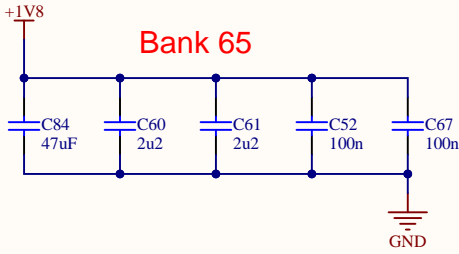
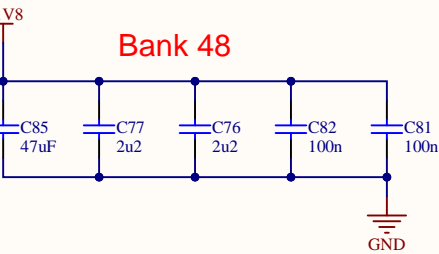
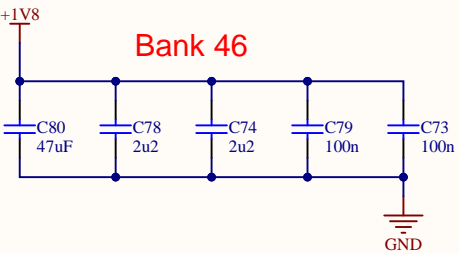
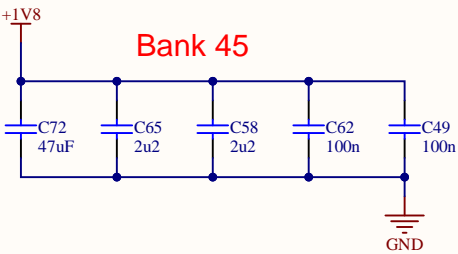
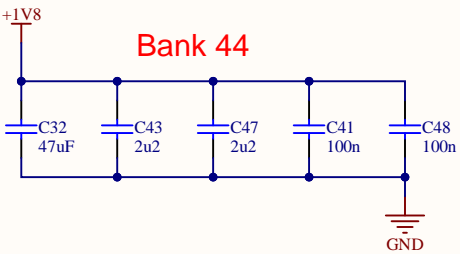
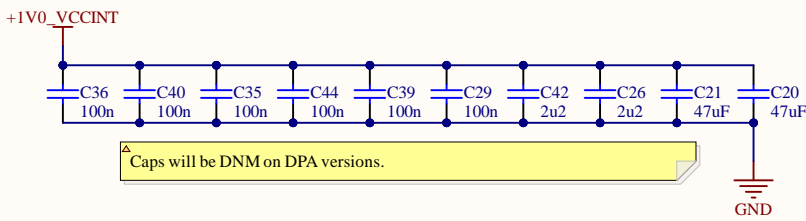
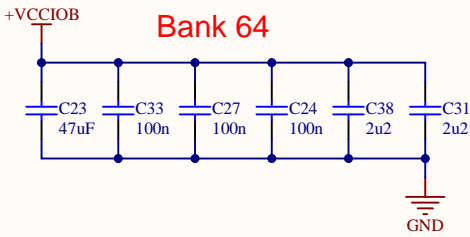
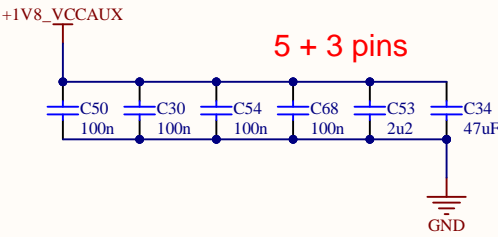
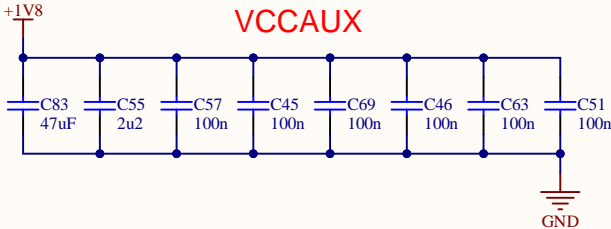
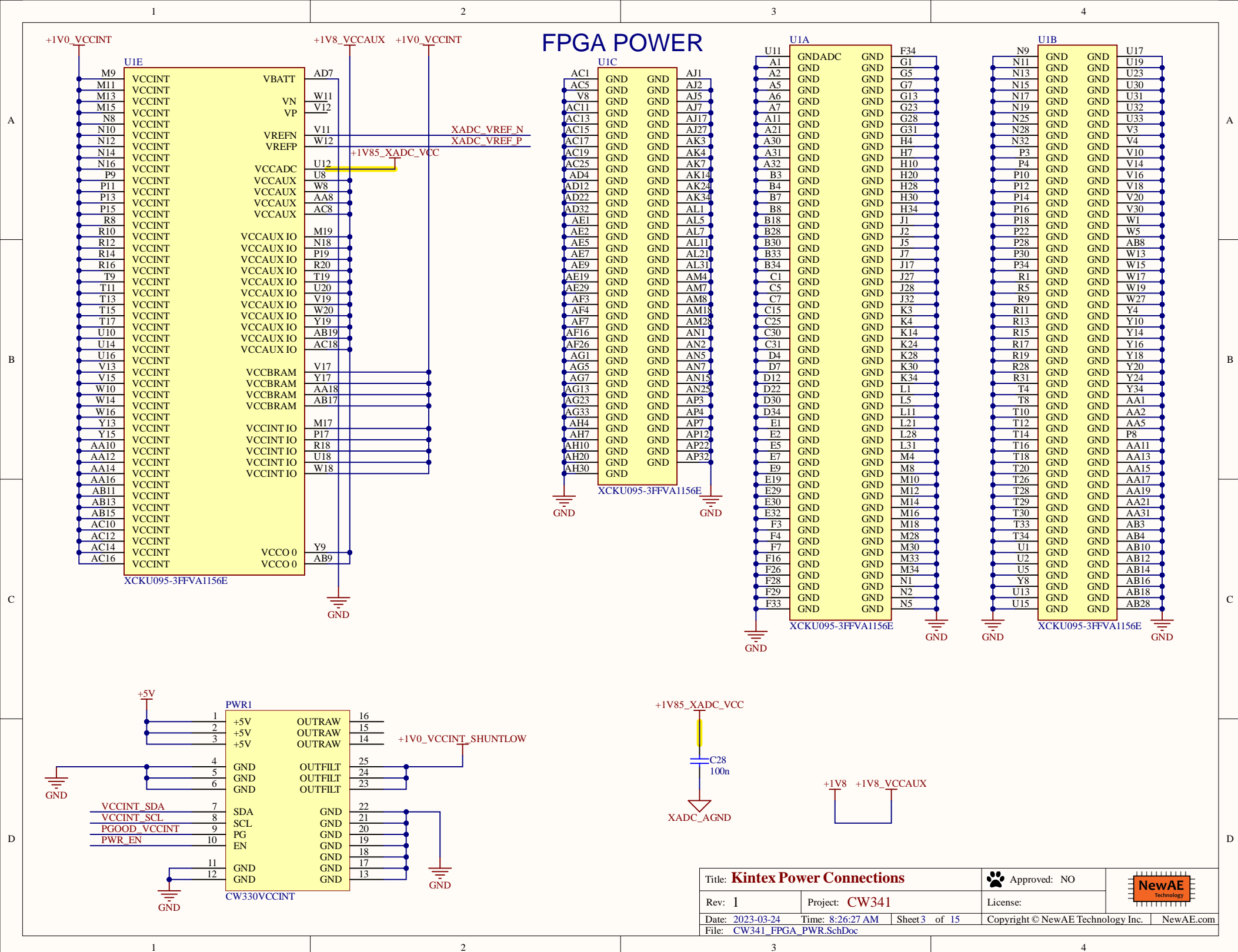
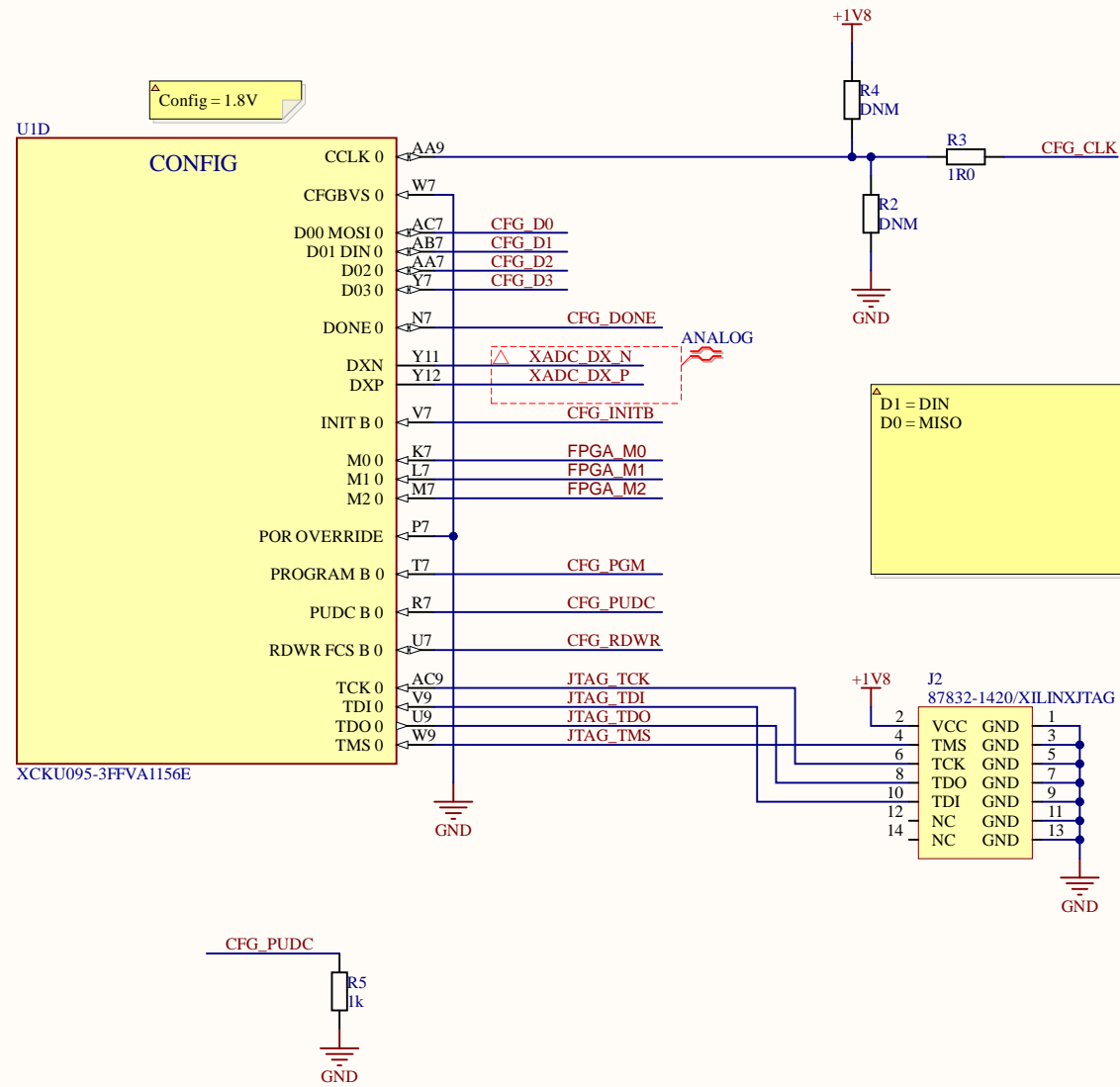


FPGA Decoupling







CFG_CLK will connect to SAM3U_NWE pin by default, possibly jumpered to a SCK pin.

Title: **Kintex CFG**

Approved: NO

Rev: 1

Project: **CW341**

License:

Date: 2023-03-24

Time: 8:26:27 AM

Sheet 4 of 15

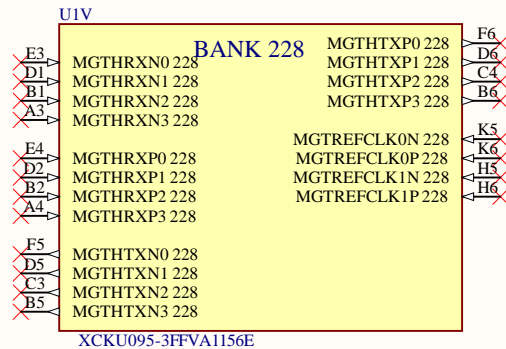
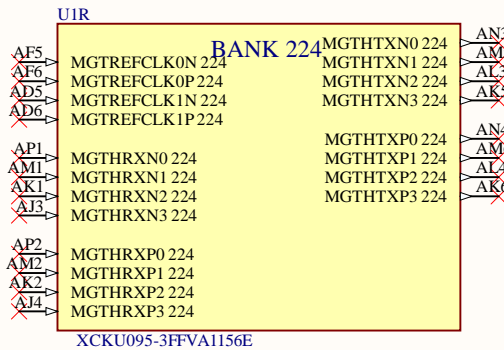
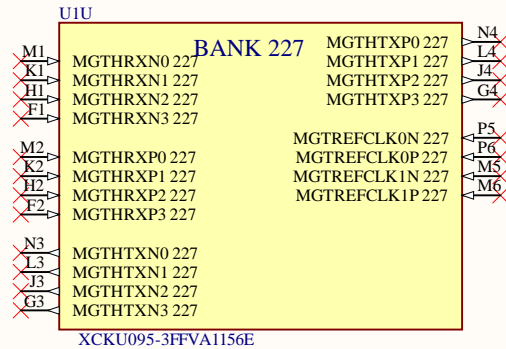
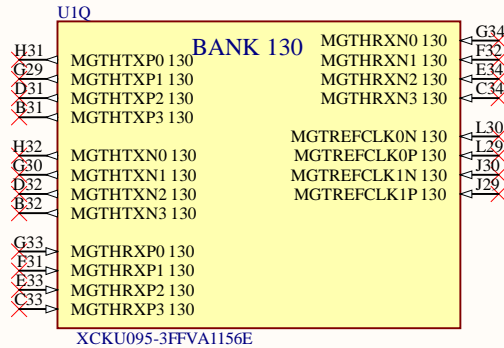
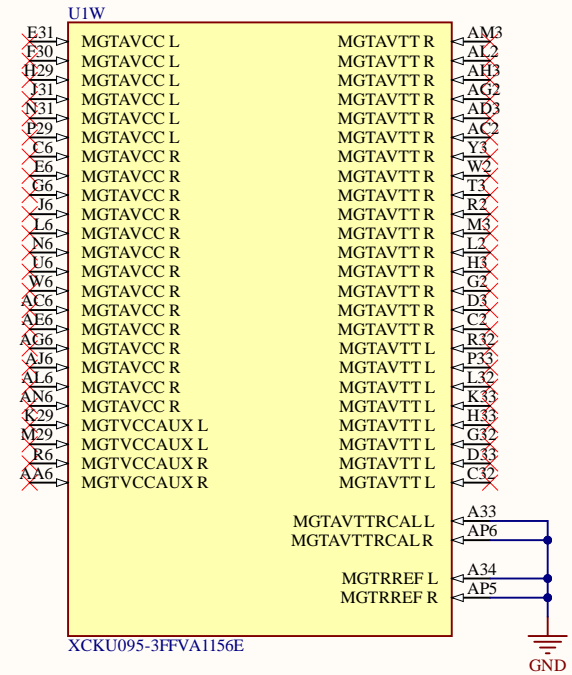
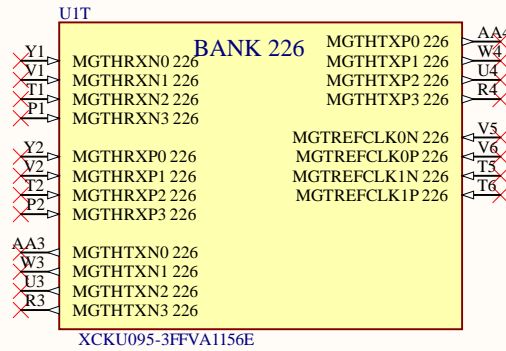
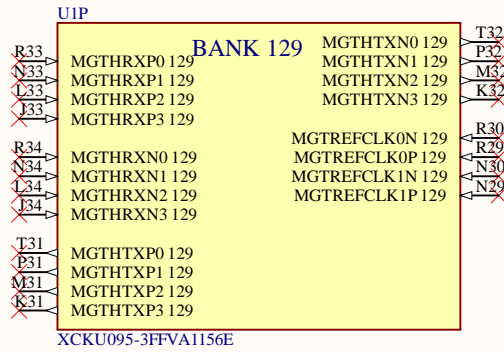
Copyright © NewAE Technology Inc.

NewAE.com

File: **CW341_FPGA_CFG.SchDoc**

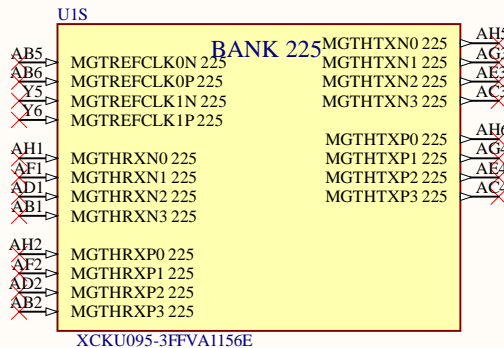


FPGA MGT Interface



From UG576 regarding MGTAVCC, MGTAVTT, MGTVCCAUX pins:

If all of the Quads in a power supply group are not used, the associated pins can be left unconnected or tied to GND (unless the RCAL circuit is in that Quad).



A

A

B

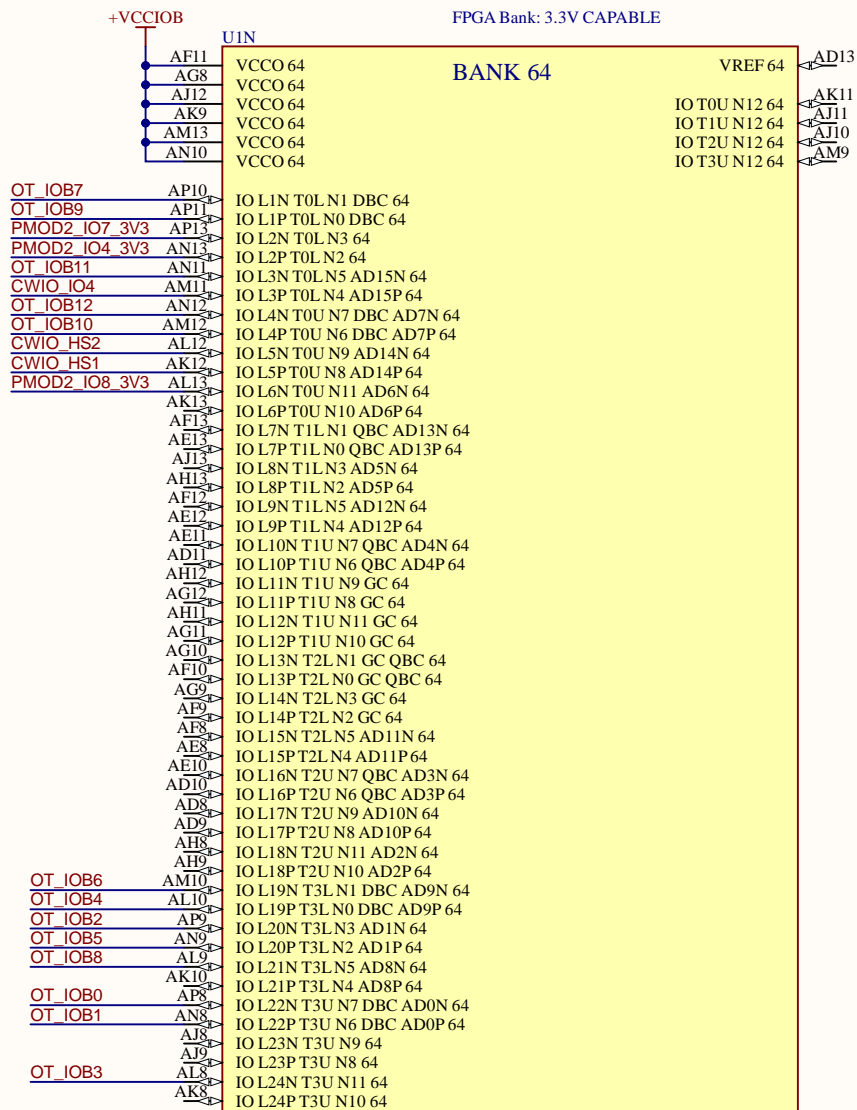
B

C

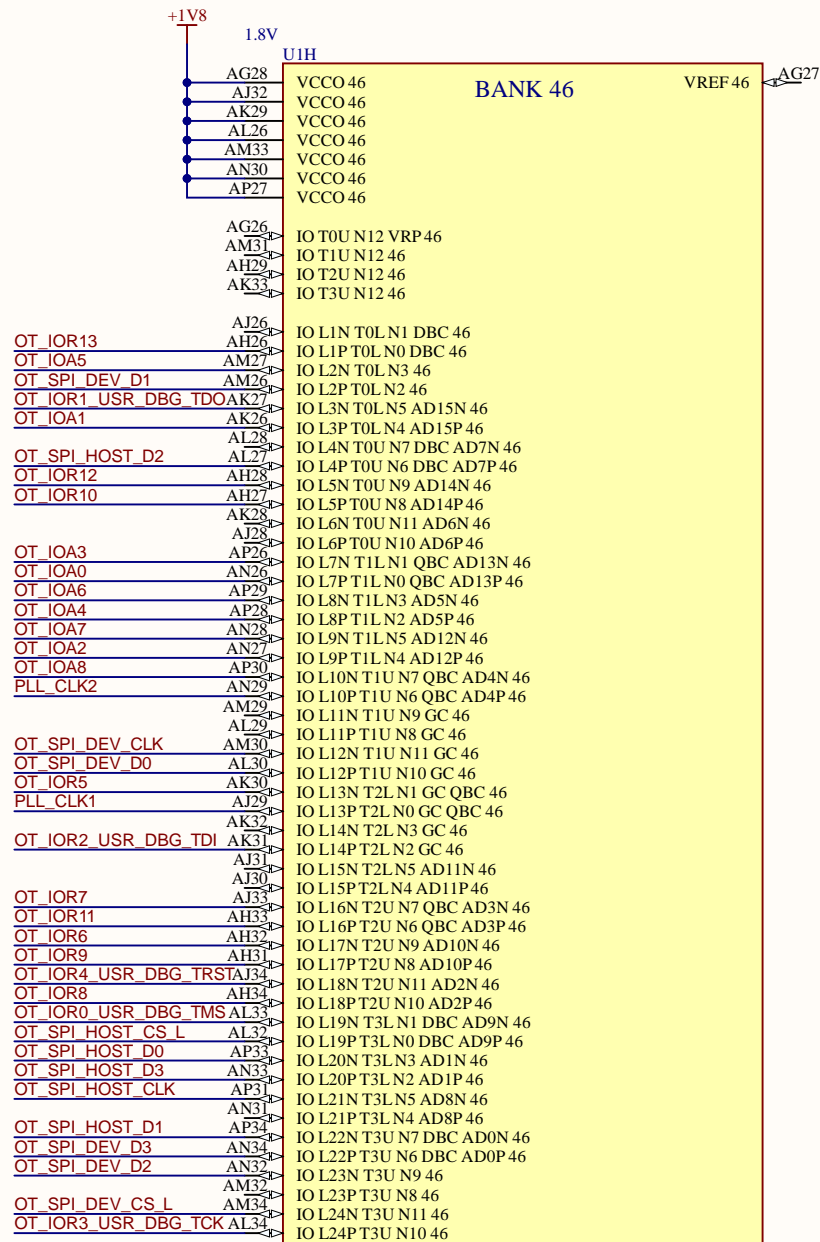
C

D

D



XCKU095-3FFVA1156E



XCKU095-3FFVA1156E

Title: **Kintex IO Banks** Approved: NoRev: **1**Project: **CW341**

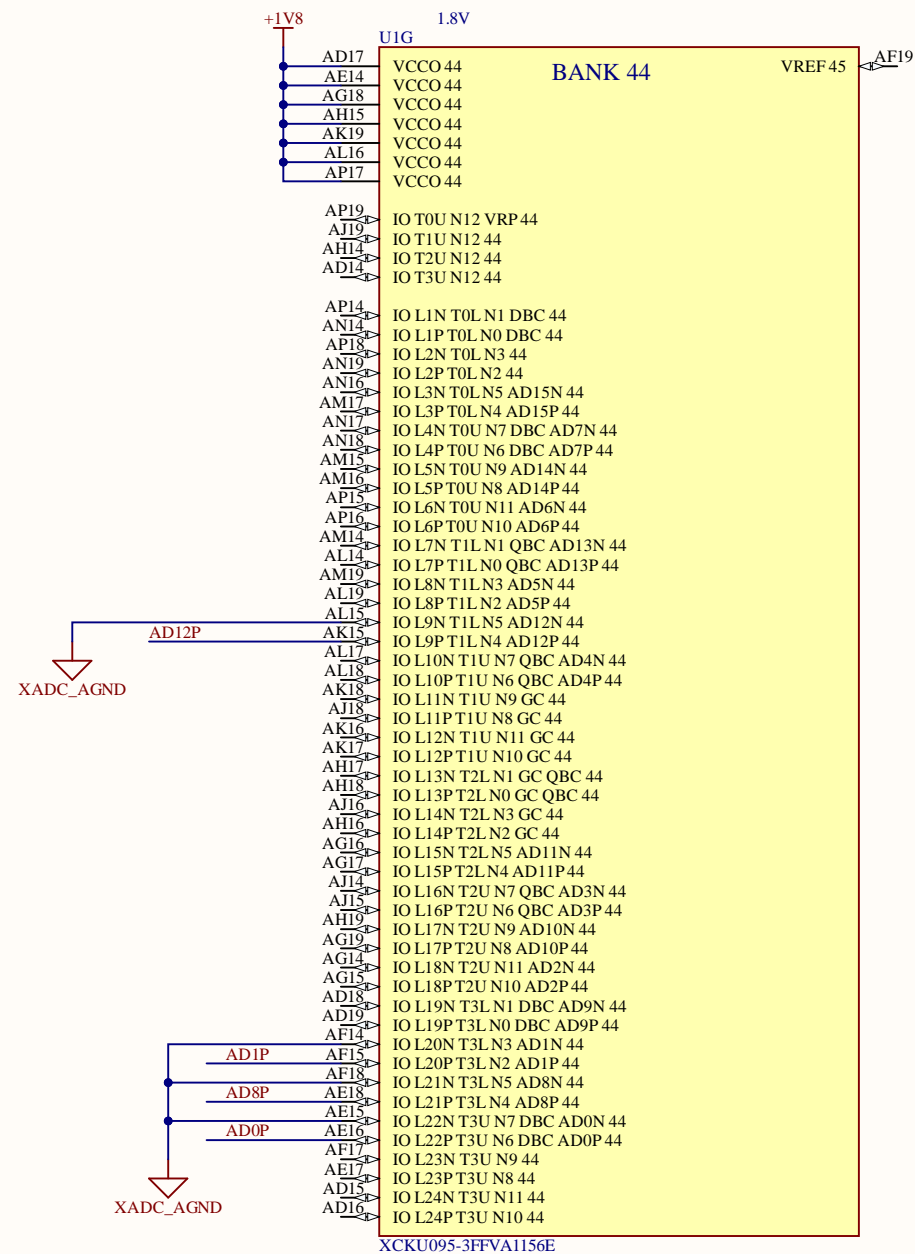
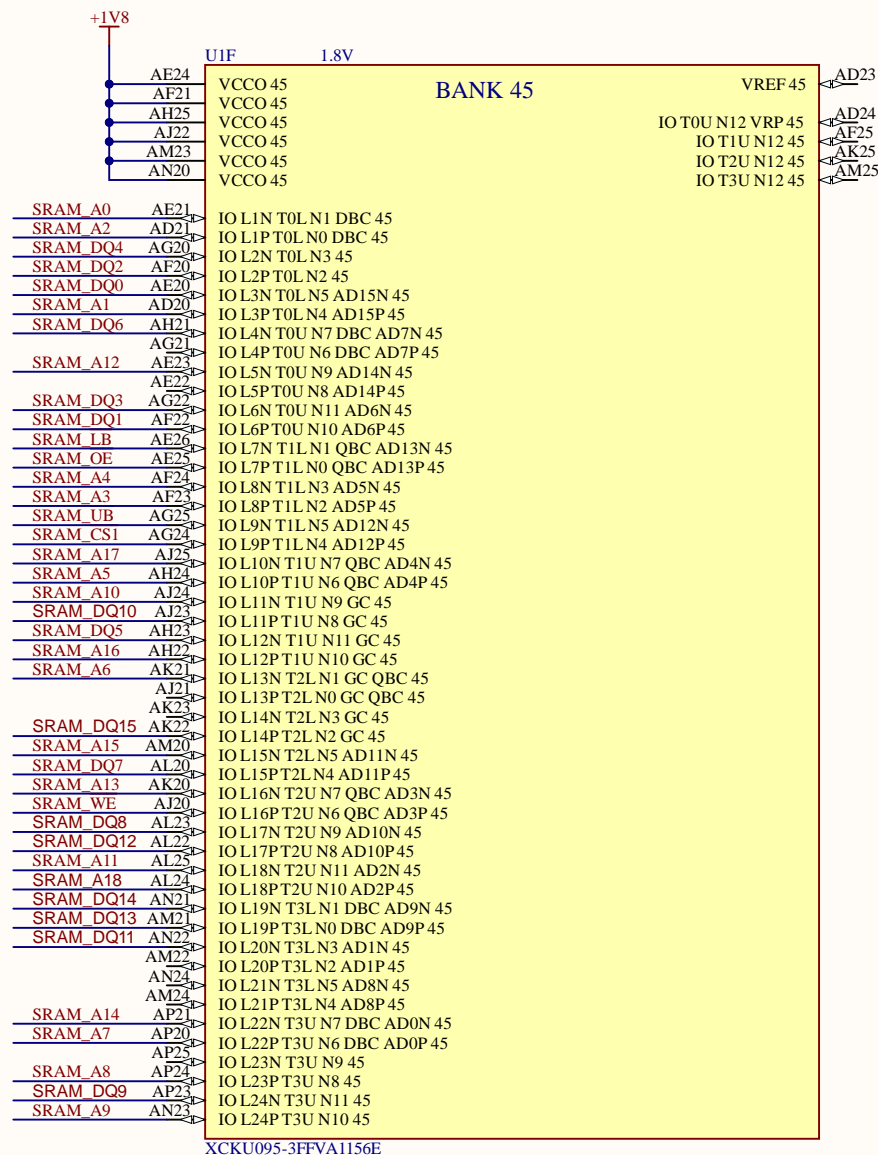
License:

Date: **2023-03-24**Time: **8:26:27 AM**Sheet **6** of **15**

Copyright © NewAE Technology Inc.

NewAE.com

File: **CW341_FPGAIO_1.SchDoc**

Title: **Kintex IO Banks**

Approved: No



Rev: 1

Project: CW341

License:

Date: 2023-03-24

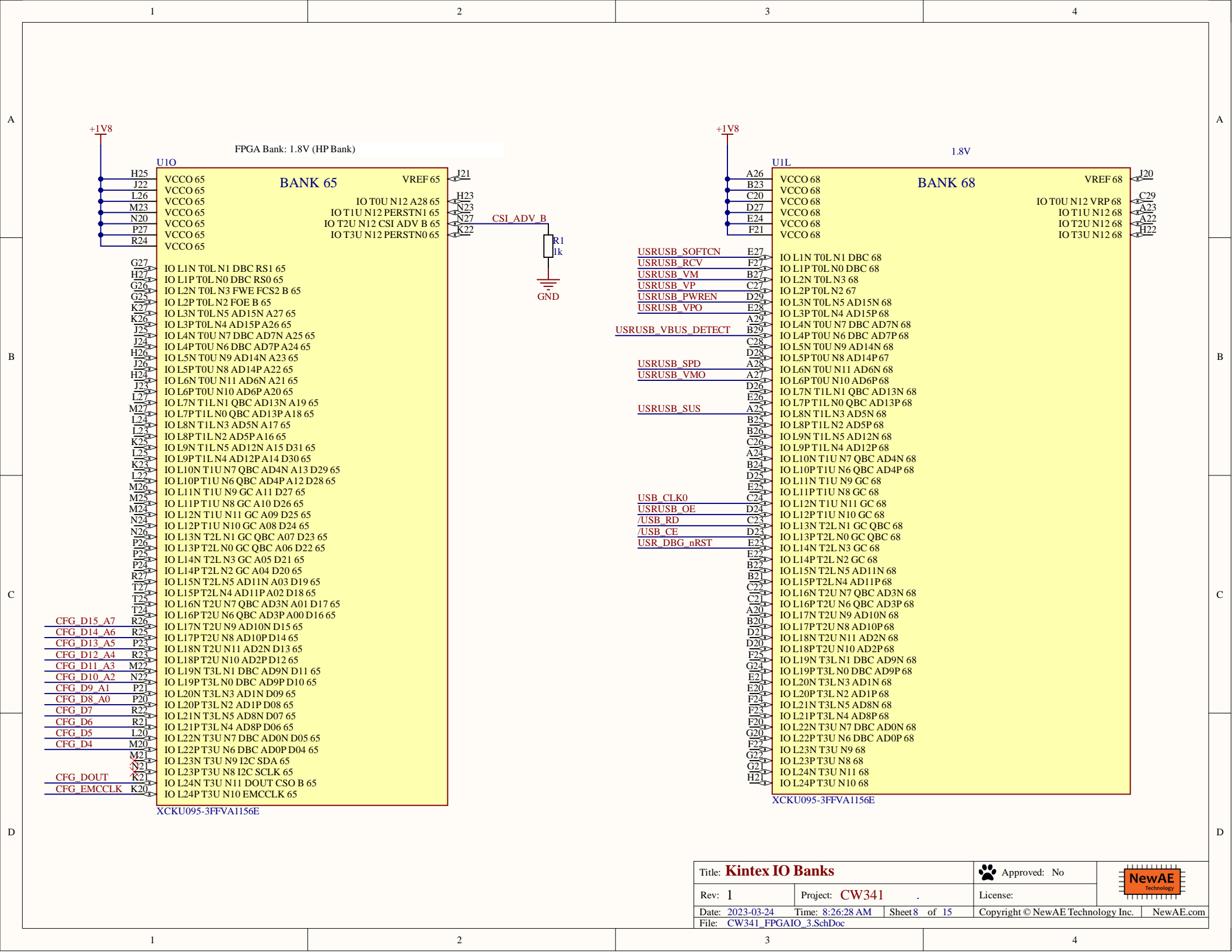
Time: 8:26:28 AM

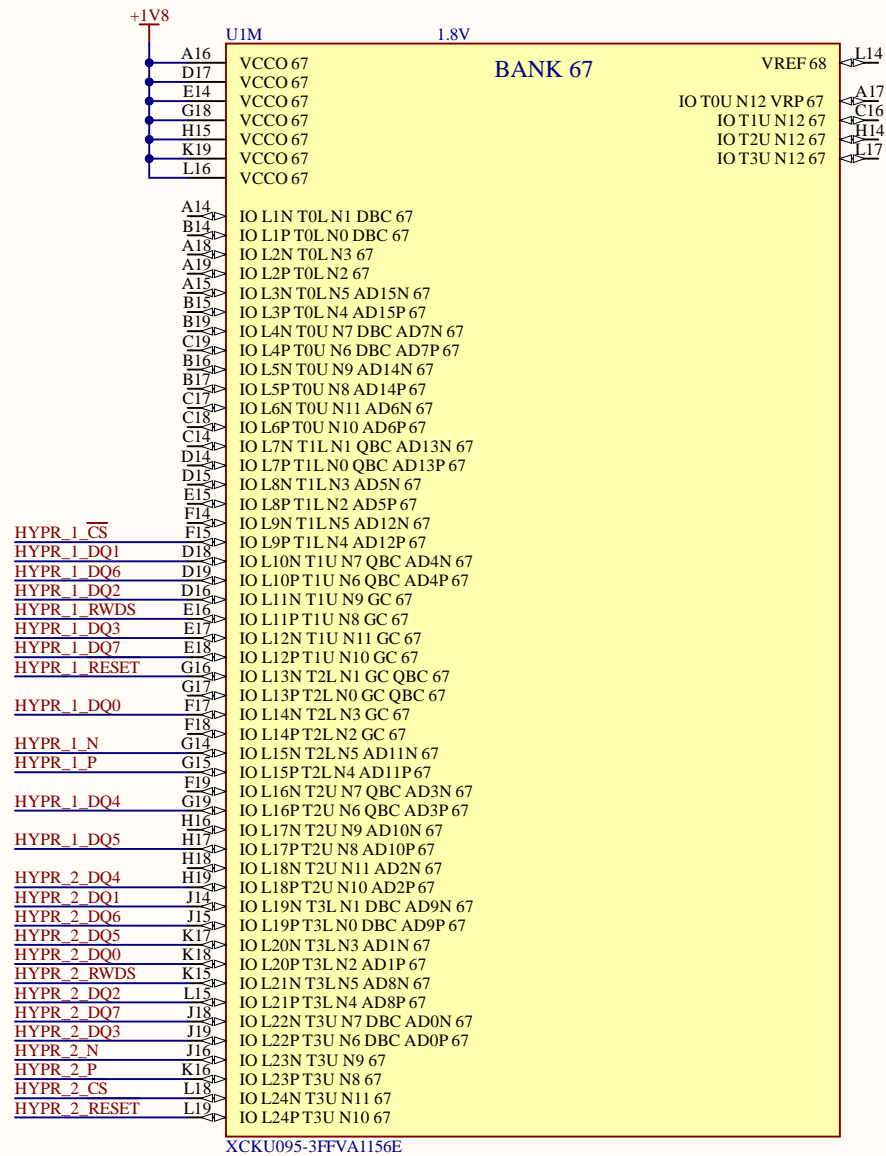
Sheet 7 of 15

Copyright © NewAE Technology Inc.

NewAE.com

File: CW341_FPGAIO_2.SchDoc



Title: **Kintex IO Banks**

Approved: NO



Rev: 1

Project: CW341

License:

Date: 2023-03-24

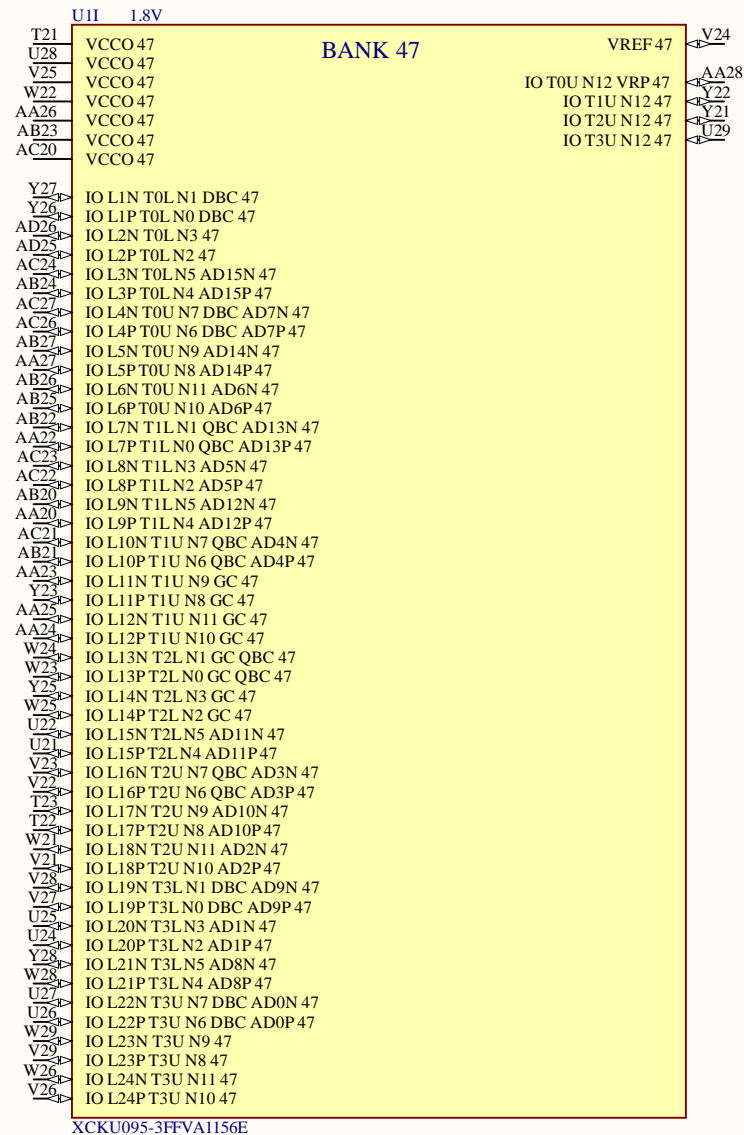
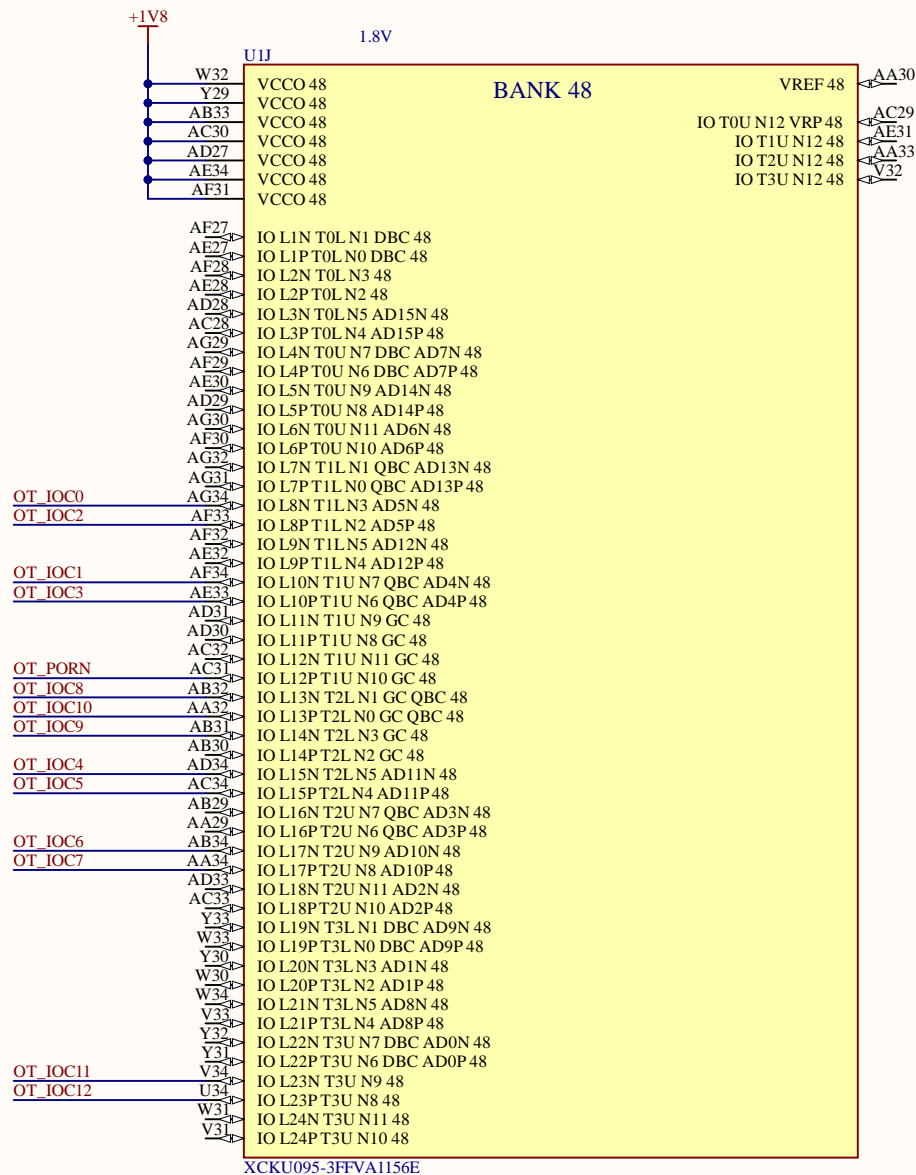
Time: 8:26:28 AM

Sheet9 of 15

Copyright © NewAE Technology Inc.

NewAE.com

File: CW341_FPGAIO_4.SchDoc

Title: **Kintex IO Banks**

Approved: NO



Rev: 1

Project: **CW341**

License:

Date: 2023-03-24

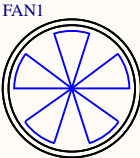
Time: 8:26:28 AM

Sheet 10 of 15

Copyright © NewAE Technology Inc.

NewAE.com

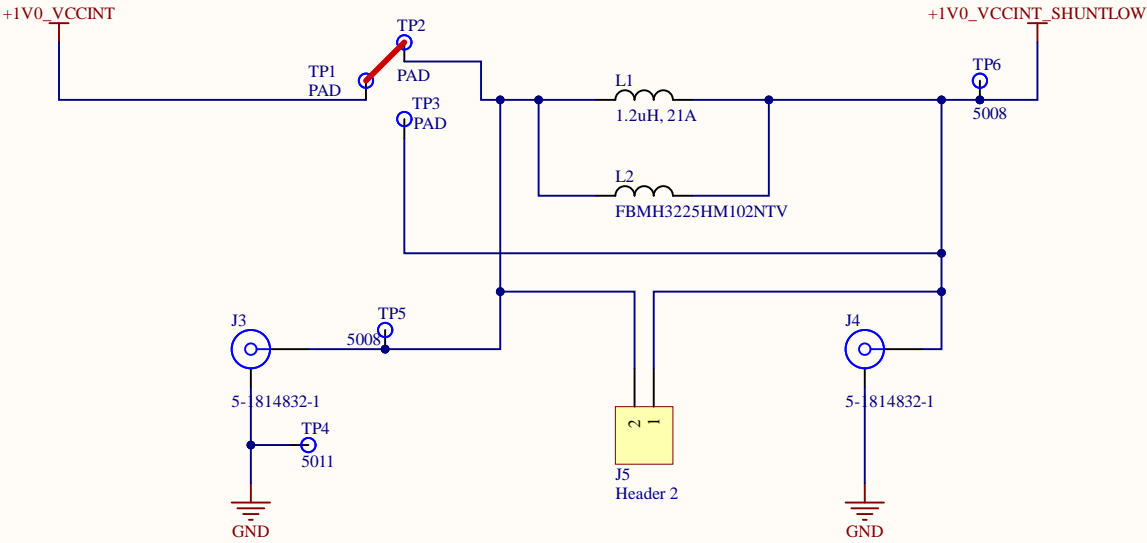
File: **CW341_FPGAIO_5.SchDoc**



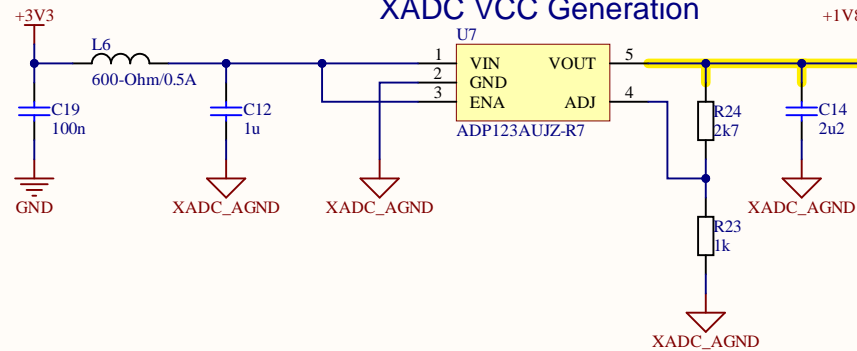
Blower Fan, 5V, 35x35mm

⚠ Fan mounted top or bottom side of board. Blower style to pass over "open die top".

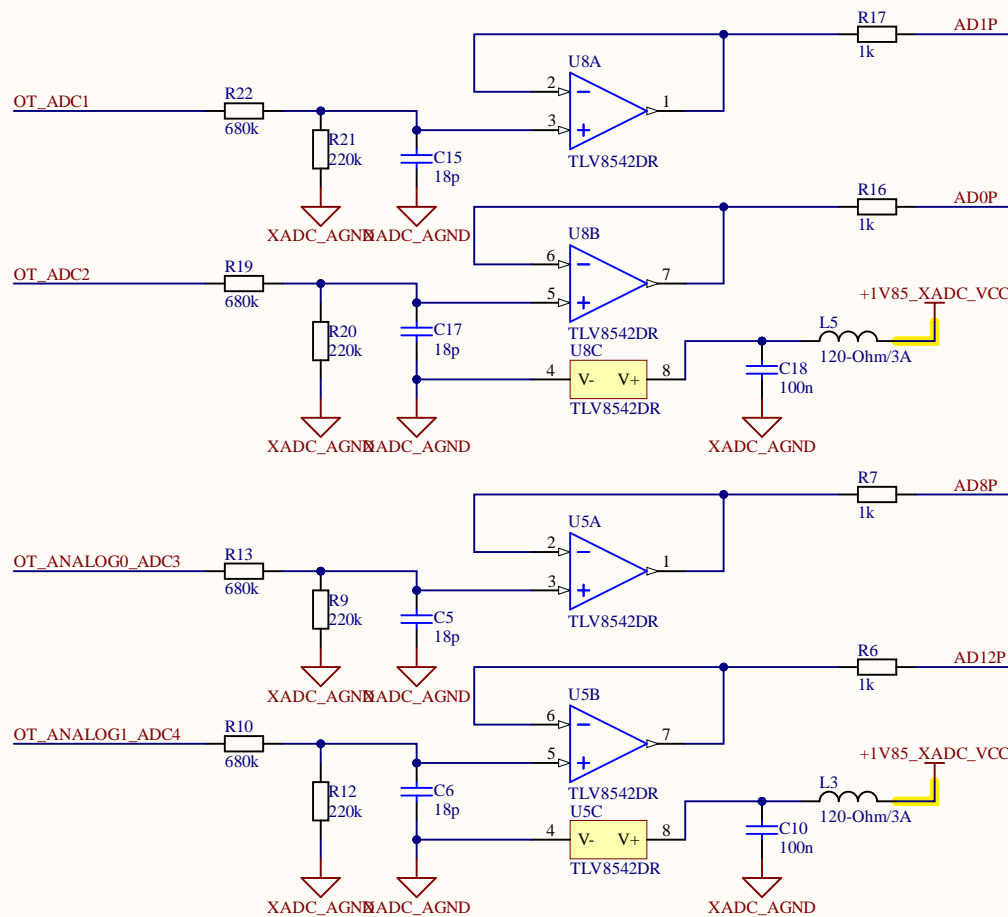
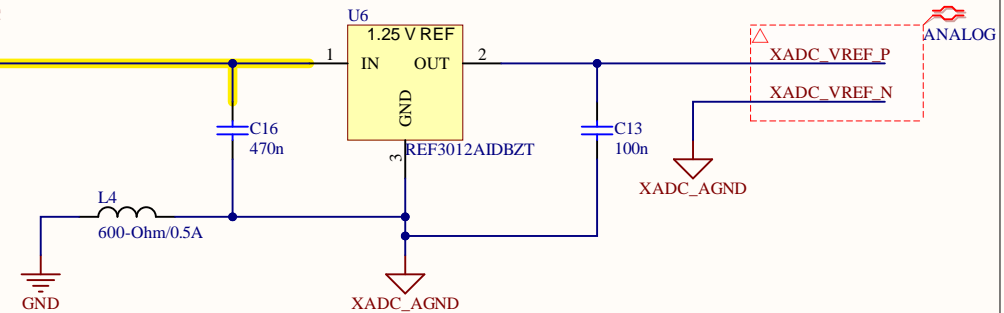
⚠ Optional heatsink-mounted fan also support - 30x30mm should screw into heatsink, otherwise mounting bracket needed.



XADC VCC Generation



XADC VREF Generation



These two net names don't look right..
outputs shared with other op amp?

Oops! Yes they should go to another
XADC input positive channel.

Title: **CW341 XADC**

Approved: NO

Rev: 1

Project: **CW341**

License:

Date: 2023-03-24

Time: 8:26:28 AM

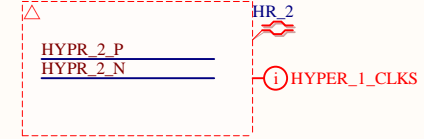
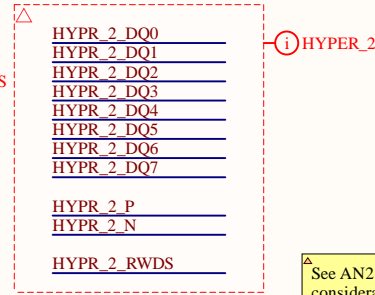
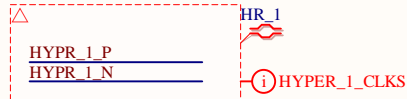
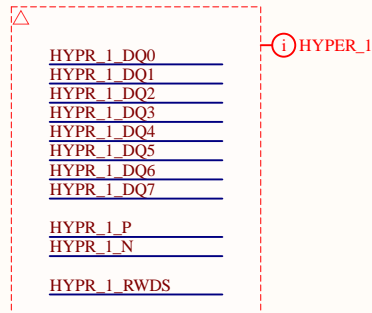
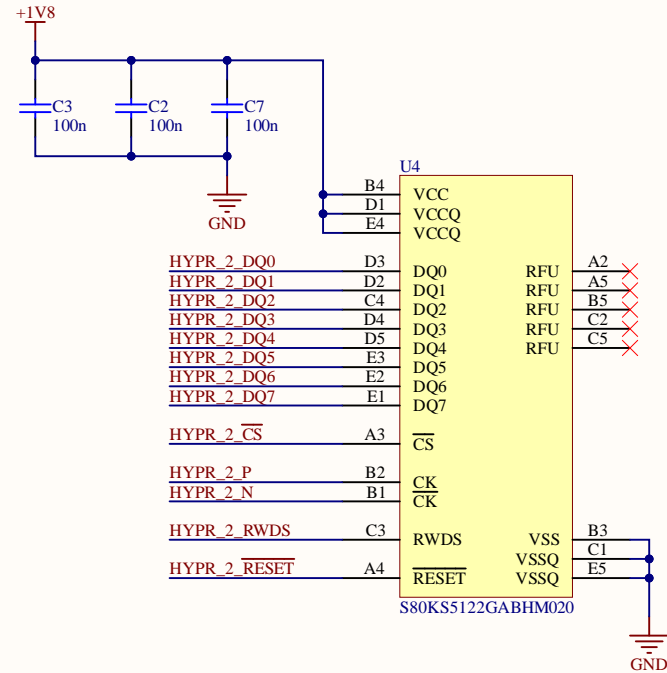
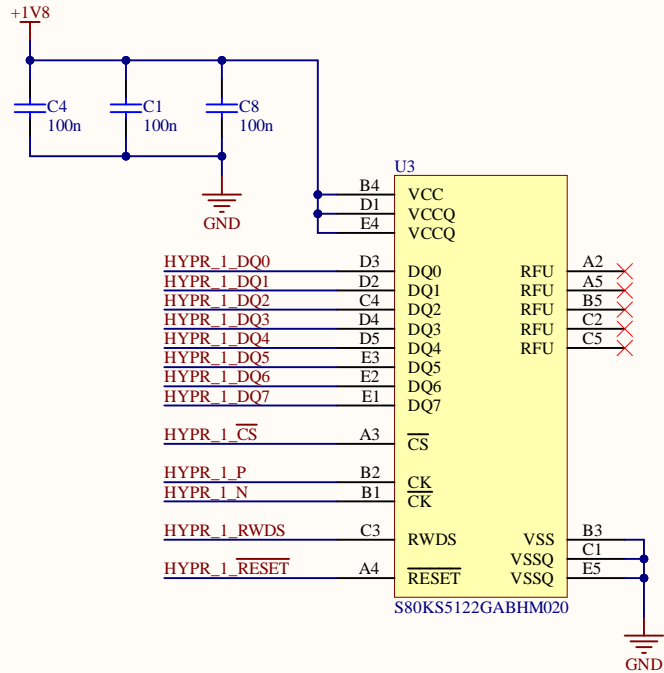
Sheet 14 of 15

Copyright © NewAE Technology Inc.

NewAE.com

File: CW341_XADC.SchDoc





See AN211622 for Length Matching Rules and PCB design considerations

Title: **CW341 HyperRAM**

Approved: NO

Rev: 1

Project: **CW341**

License:

Date: 2023-03-24

Time: 8:26:28 AM

Sheet 15 of 15

Copyright © NewAE Technology Inc.

NewAE.com

File: **CW341_HyperRam.SchDoc**

