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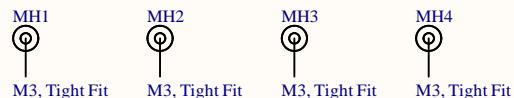
D

Changes:

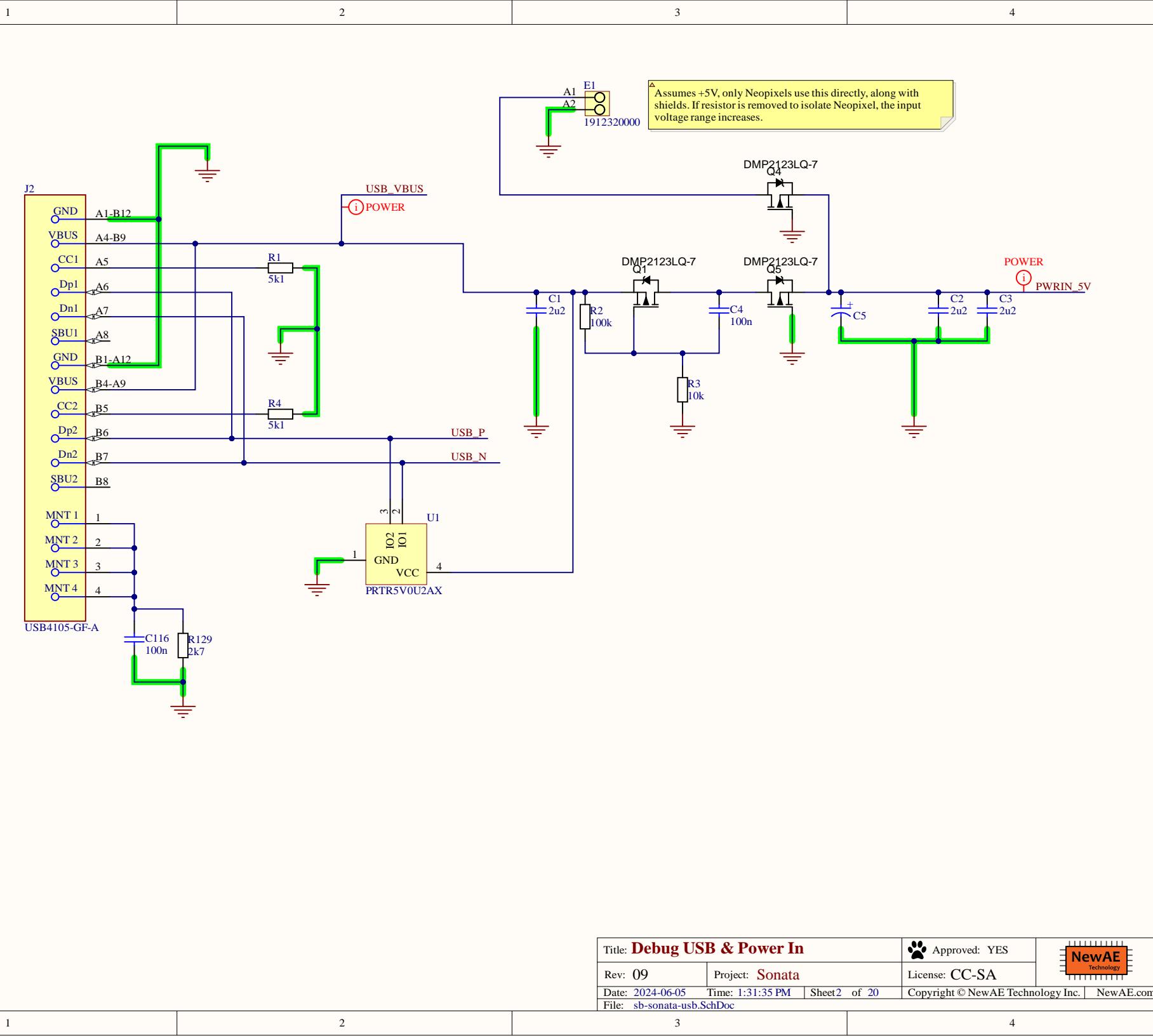
- 05:
* Fix ethernet termination
- 06:
* Add option for RGBLED pull direction
* Add I2C pull-ups on R-Pi Header
- 07:
* Add RGBLED0 driven by RP2040 option
- 08:
* Minor PCB silkscreen changes, production version
- 09:
* PUDC has pull-up resistor
* Input protection is PMOS
* Remove D1/D2

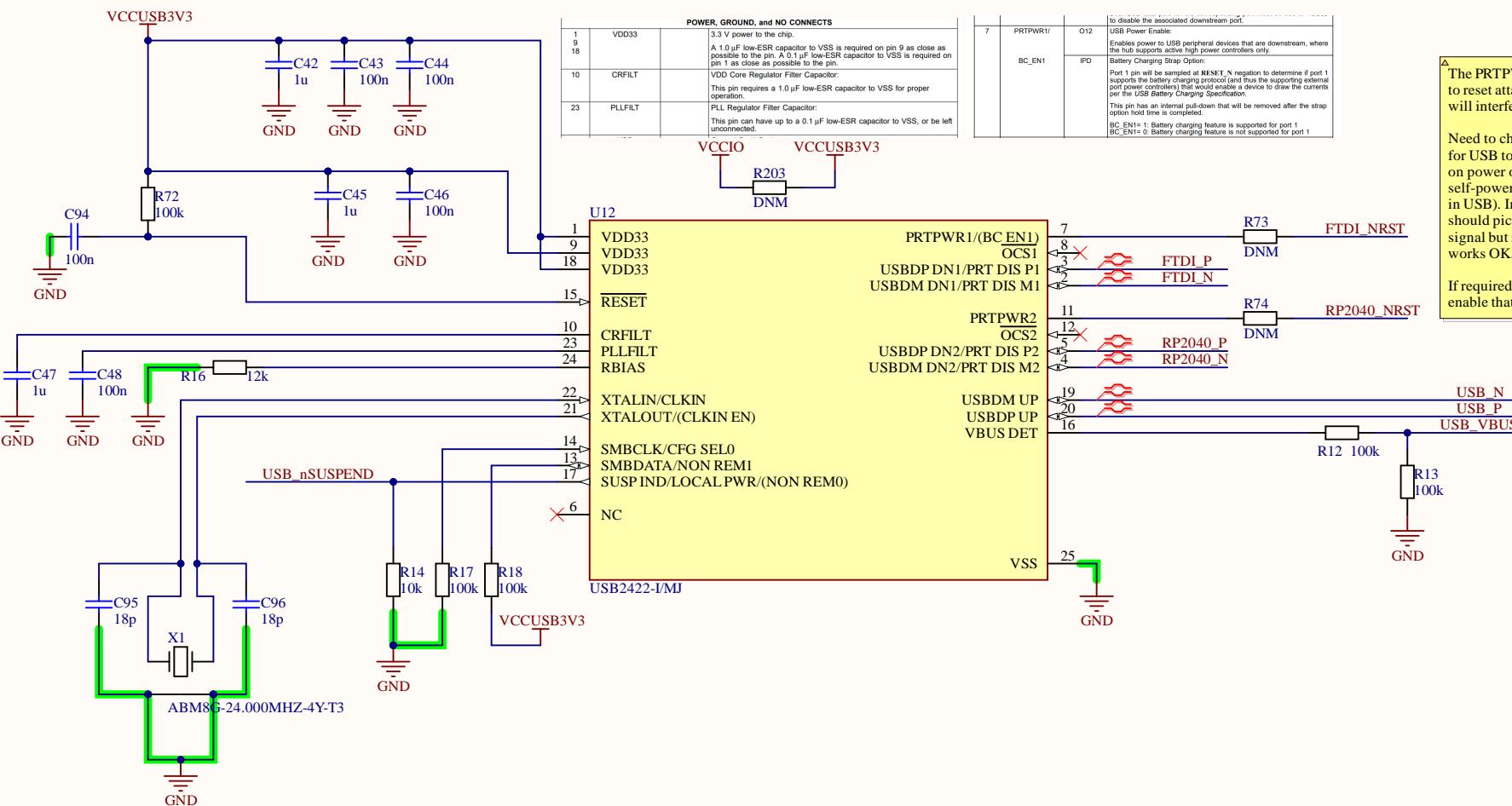
Known Issues:

- * See issues on <https://github.com/newaetech/sonata-pcb> for tracking
- 08:
* RGB leds are always powered on, which can have random or old data loaded.



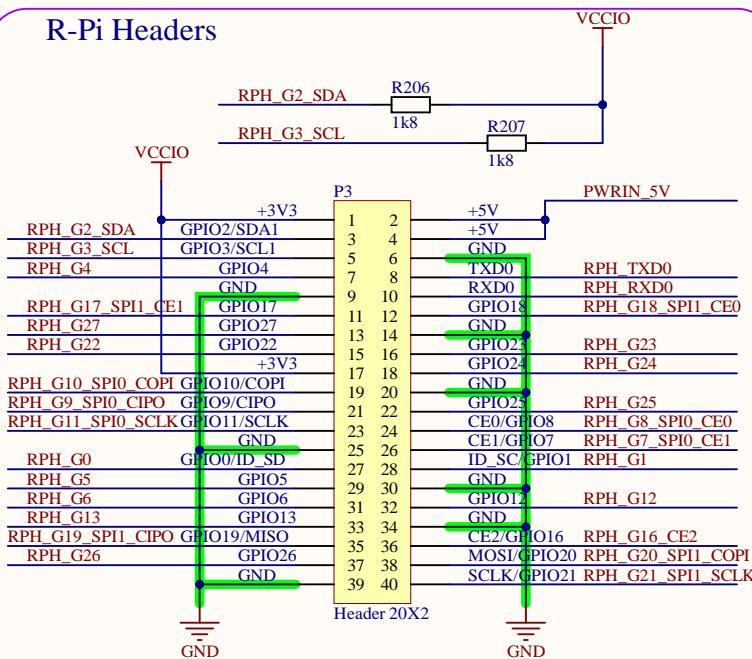
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Rev: 09	Project: Sonata	License: CC-SA	
Date: 2024-06-05	Time: 1:31:35 PM	Sheet 1 of 20	Copyright © NewAE Technology Inc. NewAE.com
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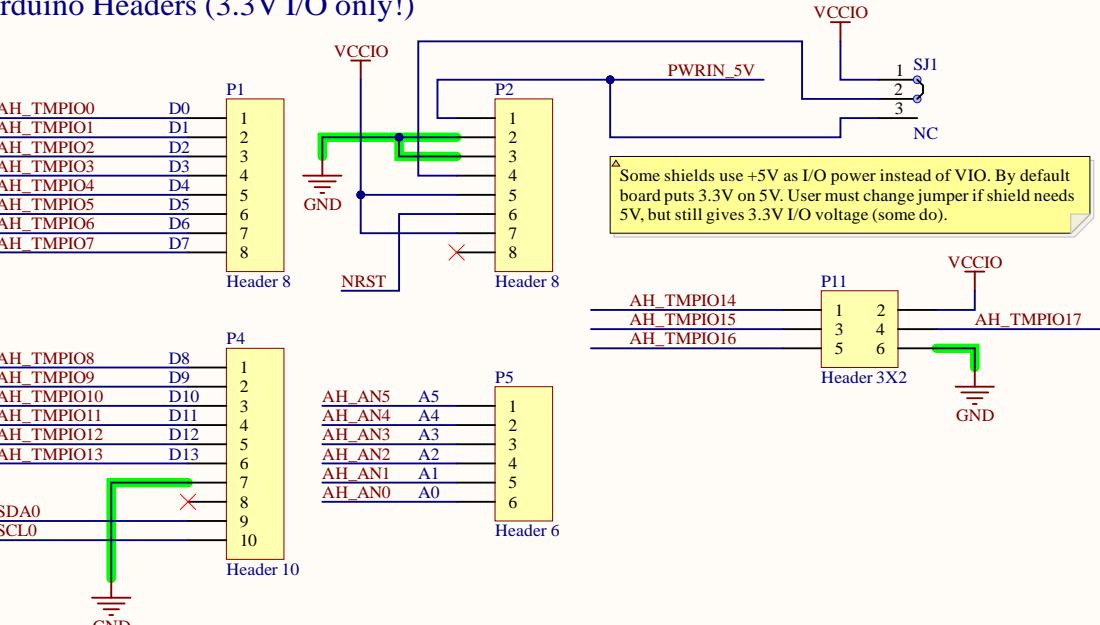


NON_Rem[1:0] = 00: all ports are removable
 NON_Rem[1:0] = 01: port 1 is non-removable
 NON_Rem[1:0] = 10: ports 1 and 2 are non-removable
 NON_Rem[1:0] = 11: reserved

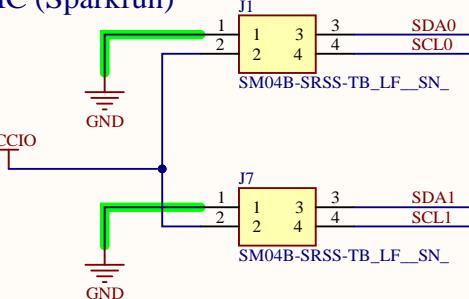
R-Pi Headers



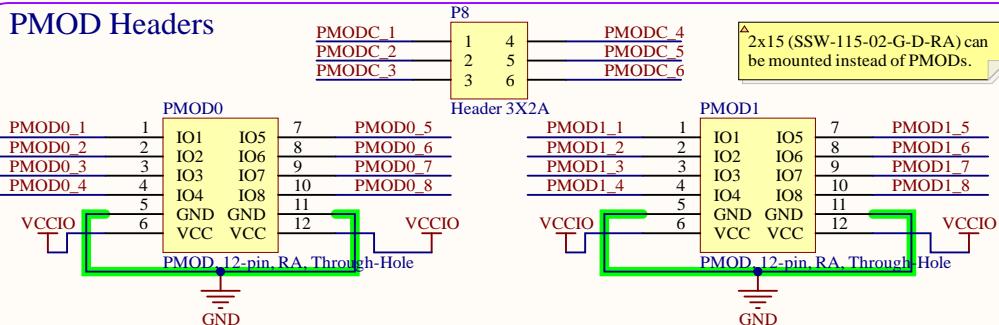
Arduino Headers (3.3V I/O only!)



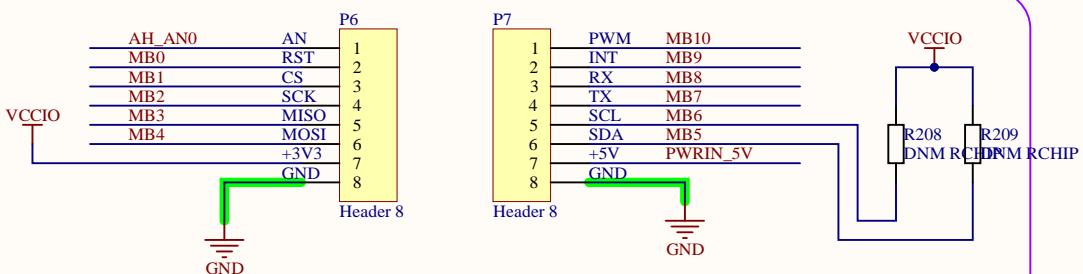
QWIIC (Sparkfun)



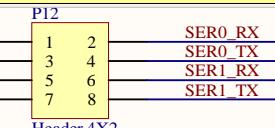
PMOD Headers



mikroBUS Click

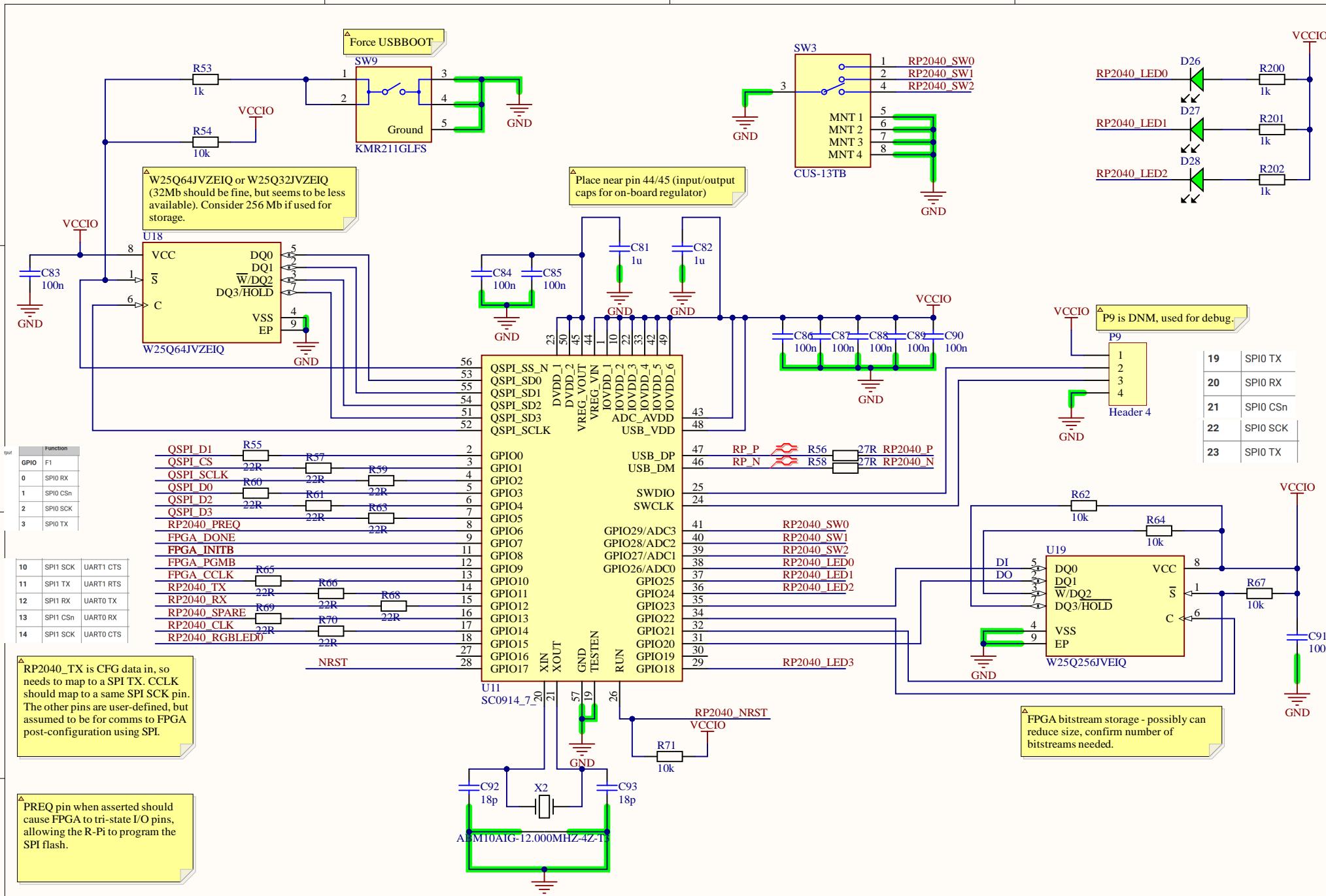


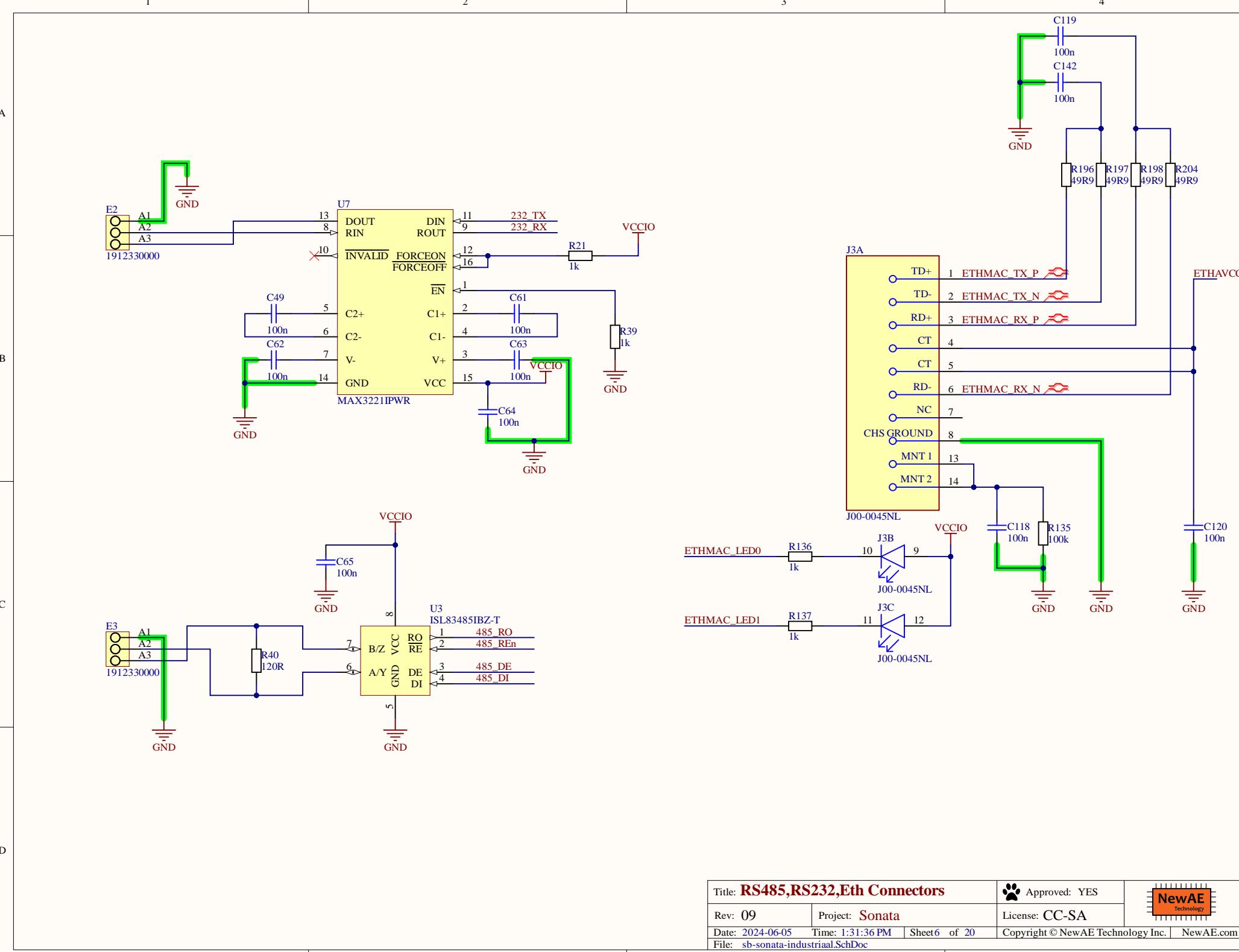
Jumpers serial to FTDI, or use to breakout extra serial.

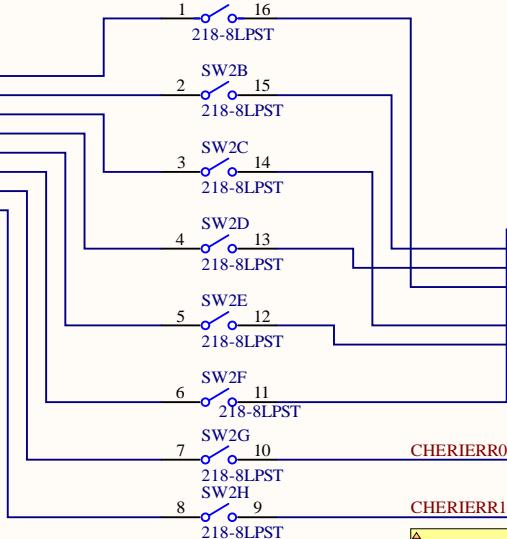
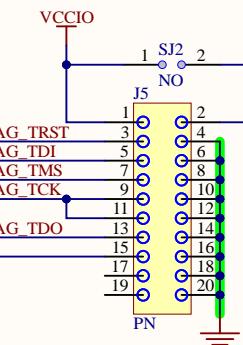
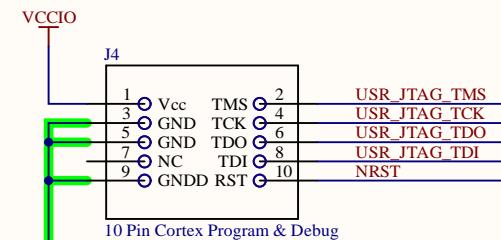
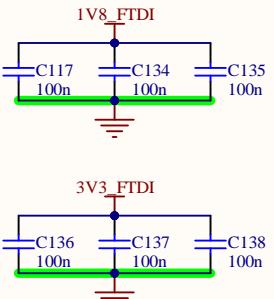
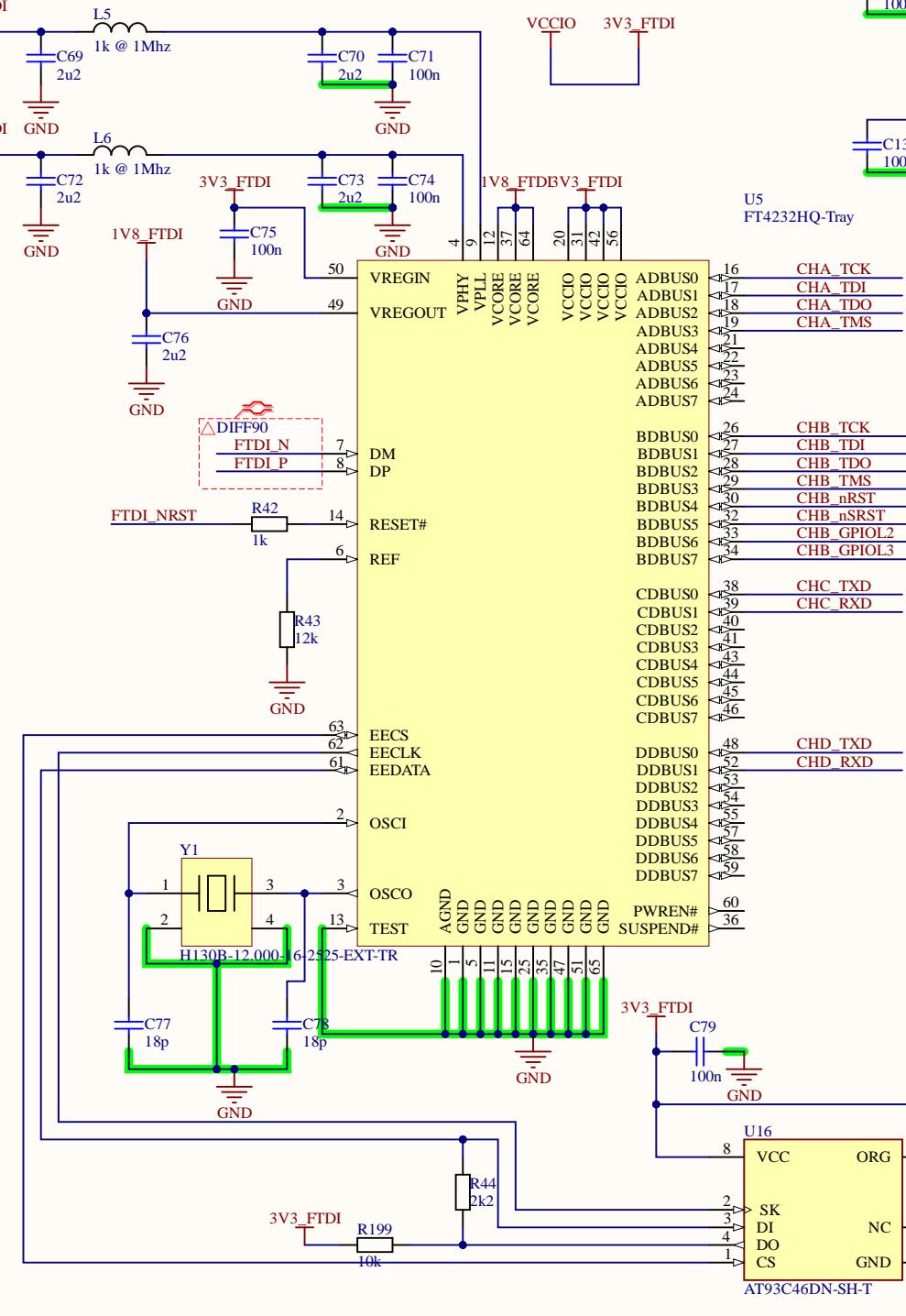


Title: Header Pins

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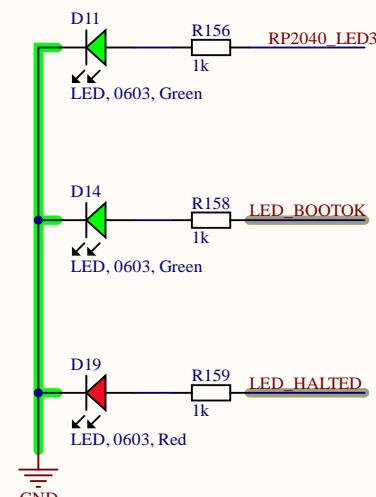
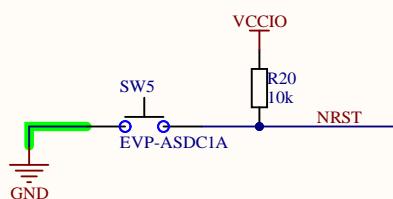
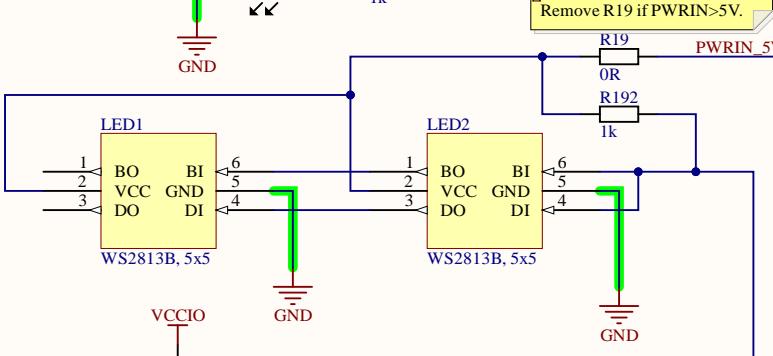
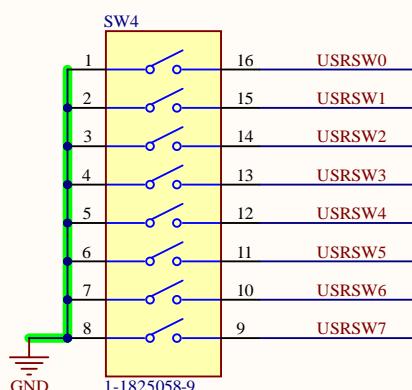
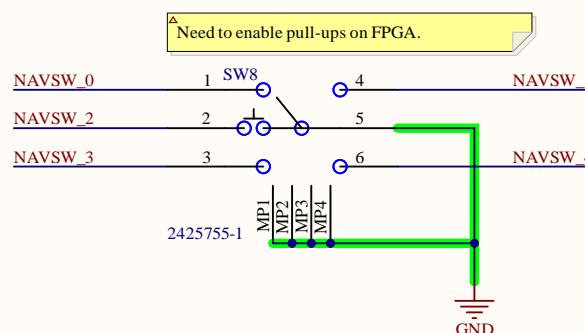
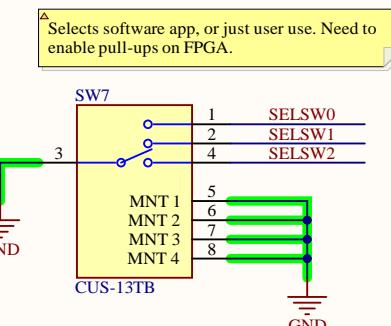
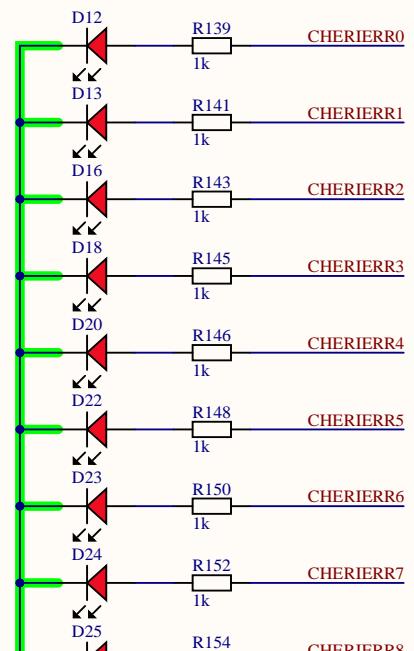
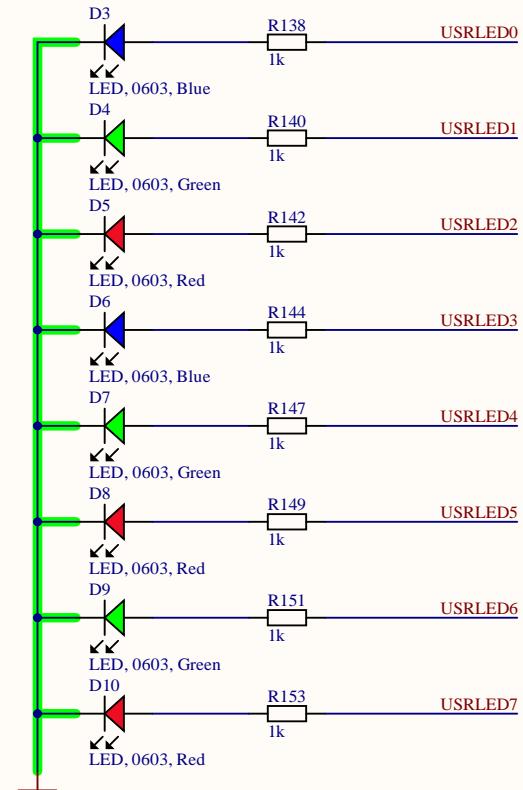
Can use these as strapping pins if needed (default - LED outputs).

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4



Title: LEDs and Switches

Rev: 09 | Project: Sonata

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File: sb-sonata-led.SchDoc

Approved: YES



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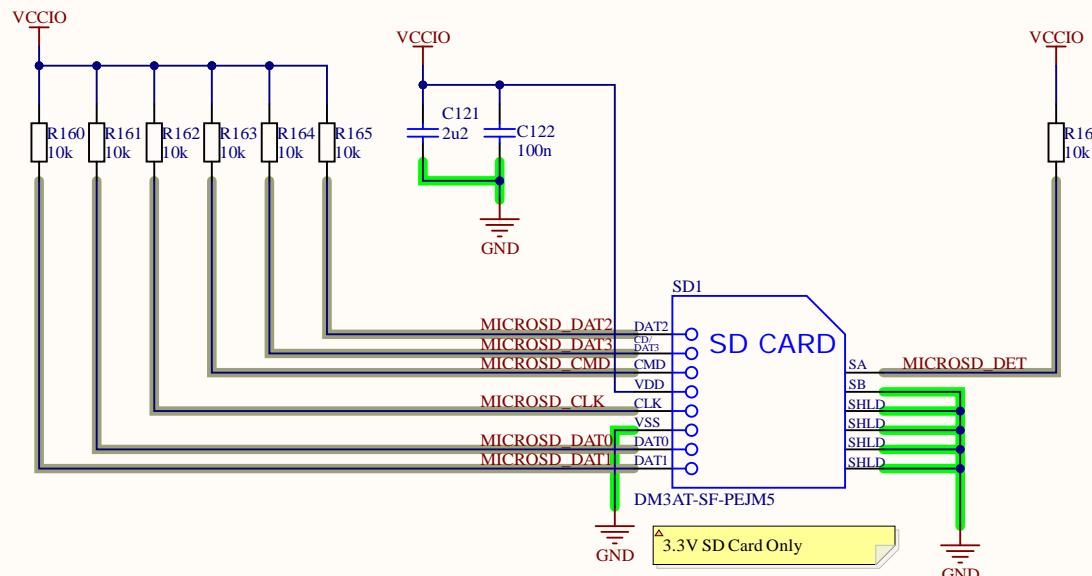
B

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Title: MicroSD Card Connector

Approved: YES



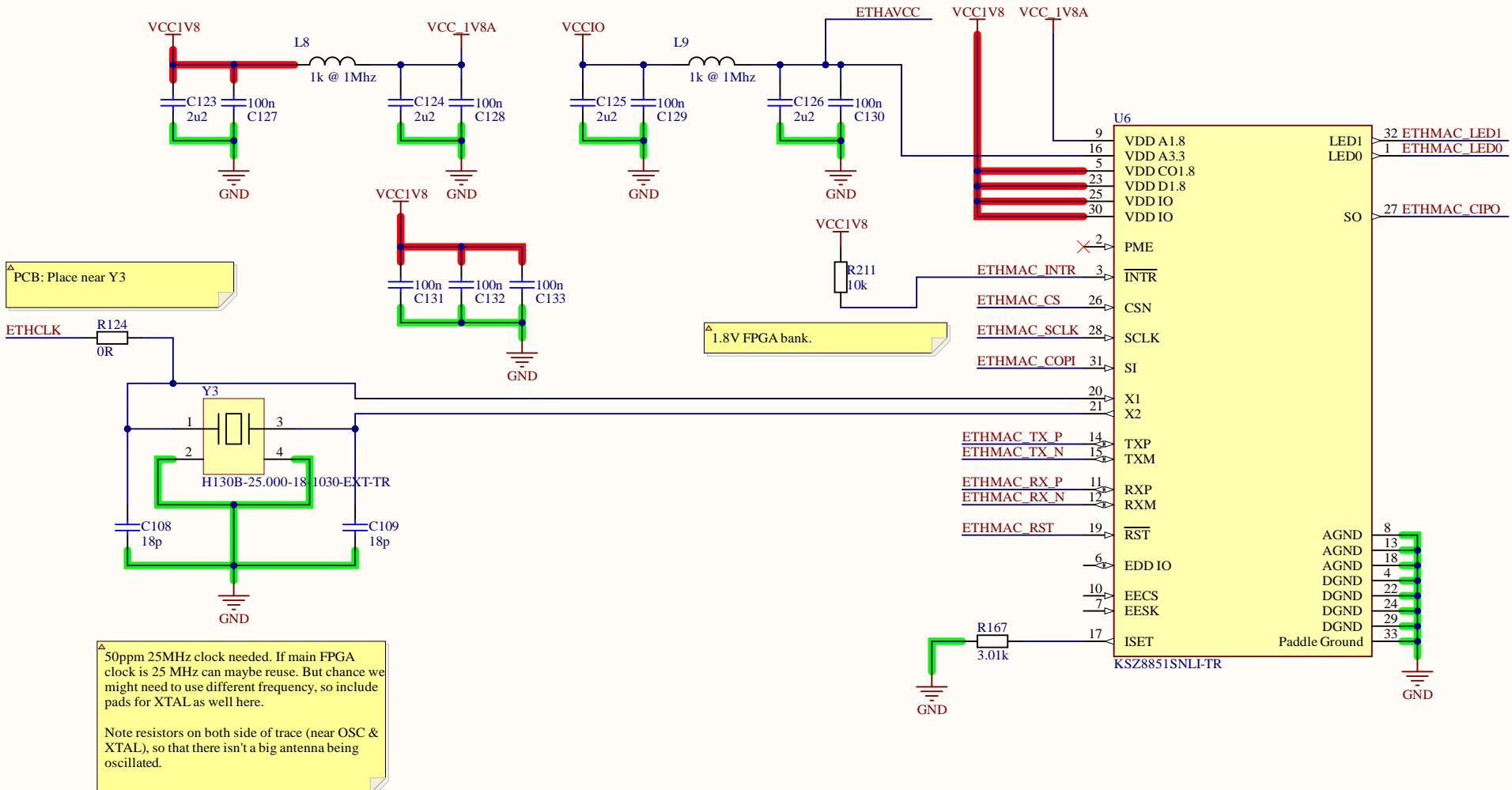
Rev: 09

Project: Sonata

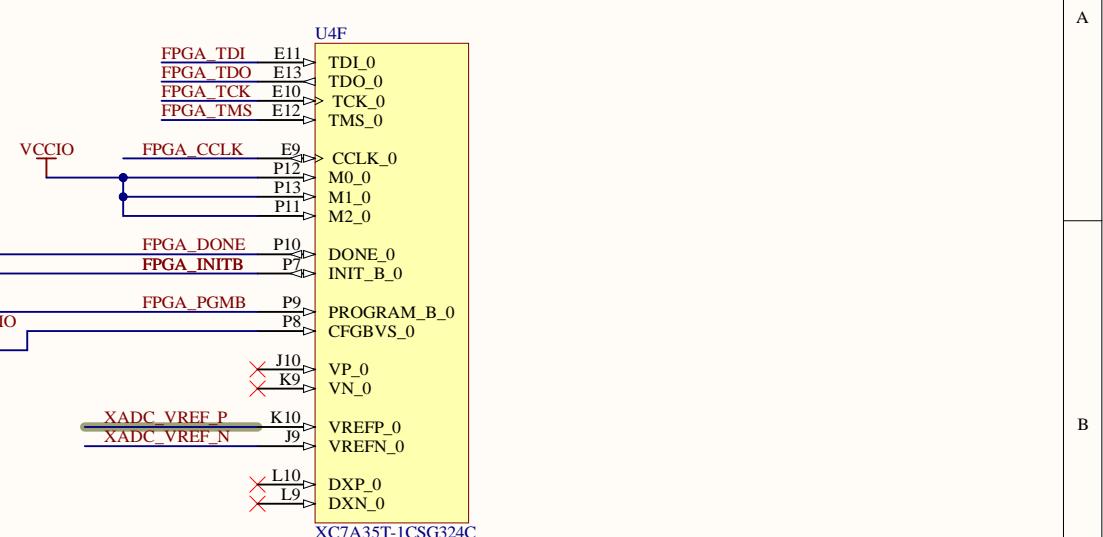
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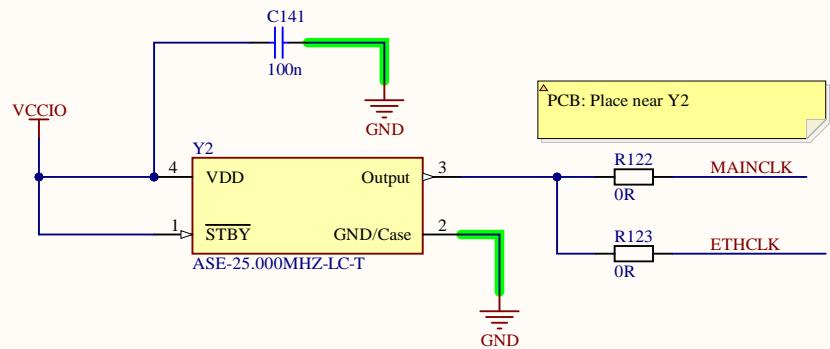
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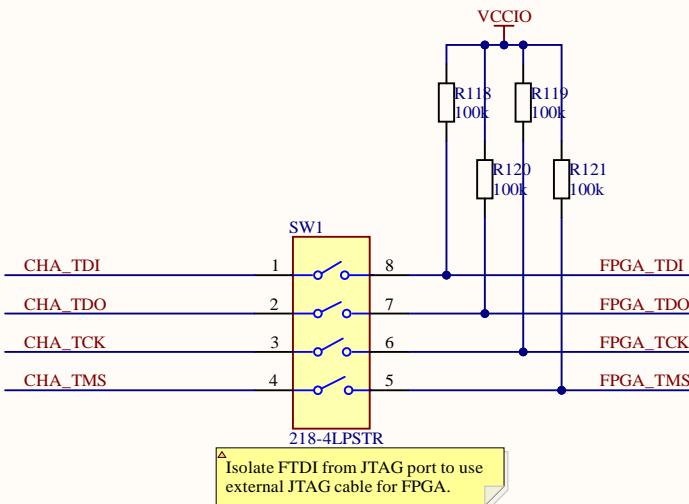
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Title: FPGA Config & Misc

Rev: 09 Project: Sonata

Date: 2024-06-05 Time: 1:31:36 PM Sheet 11 of 20

File: sb-sonata-fpga.SchDoc

Approved: YES



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U4A

IO_0_14	R11	R183C	33R	RPH_G7_SPI0_CE1
IO_L19P_T3_A10_D26_14	T11	R188A	33R	AH_TMPIO0
IO_L20P_T3_A08_D24_14	U12	R188B	33R	AH_TMPIO1
IO_L5P_T0_D06_14	R12	R188C	33R	AH_TMPIO2
IO_L23N_T3_A02_D18_14	U13	R188D	33R	AH_TMPIO3
IO_25_14	R10	R189A	33R	AH_TMPIO4
IO_L20N_T3_A07_D23_14	V12	R189B	33R	AH_TMPIO5
IO_L19N_T3_A09_D25_VREF_14	U11	R189C	33R	AH_TMPIO6
IO_L4N_T0_D05_14	M18	R189D	33R	AH_TMPIO7
IO_L17N_T2_A13_D29_14	U18	R190A	33R	AH_TMPIO8
IO_L15N_T2_DQS_DOUT_CS0_B_14	T16	R190B	33R	AH_TMPIO9
IO_L18P_T2_A12_D28_14	U16	R190C	33R	AH_TMPIO10
IO_L7N_T1_D10_14	T18	R190D	33R	AH_TMPIO11
IO_L15P_T2_DQS_RDWR_B_14	R16	R191A	33R	AH_TMPIO12
IO_L12N_T1_MRCC_14	R17	R191B	33R	AH_TMPIO13
IO_L7P_T1_D09_14	R18	R191C	33R	AH_TMPIO14
IO_L8N_T1_D12_14	P14	R191D	33R	AH_TMPIO15
IO_L9P_T1_DQS_14	N17	R168	22R	AH_TMPIO16
IO_L6N_T0_D08_VREF_14	M13	R169	22R	AH_TMPIO17
IO_L10P_T1_D14_14	M16	R175D	33R	RPH_G3_SCL
IO_L10N_T1_D15_14	M17			RP2040_RX
IO_L4P_T0_D04_14	L18	R175A	33R	RPH_RXD0
IO_L1P_T0_D00_MOSL_14	K17	R175B	33R	RPH_TXD0
IO_L6P_T0_FCS_B_14	L13	R175C	33R	RPH_G2_SDA
IO_L1N_T0_D01_DIN_14	K18	R175D	33R	RP2040_TX
IO_L13P_T2_MRCC_14	P15			MAINCLK
IO_L11P_T1_SRCC_14	N15	R177A	33R	RPH_G4
IO_L2N_T0_D03_14	M14	R177B	33R	RPH_G17_SPI1_CE1
IO_L2P_T0_D02_14	L14	R177C	33R	RPH_G27
IO_L3N_T0_DQS_EMCCCLK_14	L16	R177D	33R	RPH_G22
IO_L16N_T2_A15_D31_14	V16	R179A	33R	RPH_G10_SPI0_COPI
IO_L18N_T2_A11_D27_14	V17	R179B	33R	RPH_G9_SPI0_CIPO
IO_L12P_T1_MRCC_14	P17	R179C	33R	RPH_G11_SPI0_SCLK
IO_L17P_T2_A14_D30_14	U17	R179D	33R	RPH_G0
IO_L23P_T2_A03_D19_14	T13	R181A	33R	RPH_G5
IO_L22P_T3_A05_D21_14	U14	R181B	33R	RPH_G6
IO_L5N_T0_D07_14	R13	R181C	33R	RPH_G13
IO_L22N_T3_A04_D20_14	V14	R181D	33R	RPH_G19_SPI1_CIPO
IO_L13N_T2_MRCC_14	I15	R182A	33R	RPH_G26
IO_L9N_T1_DQS_D13_14	P18	R182B	33R	RPH_G18_SPI1_CE0
IO_L8P_T1_D11_14	N14	R182C	33R	RPH_G23
IO_L11N_T1_SRCC_14	N16	R182D	33R	RPH_G24
IO_L3P_T0_DQS_PUDC_B_14	L15	R183A	33R	RPH_G25
IO_L16P_T2_CSR_B_14	V15	R183B	33R	RPH_G8_SPI0_CE0
IO_L14P_T2_SRCC_14	T14			RP2040_CLK
IO_L14N_T2_SRCC_14	T15	R183D	33R	RPH_G1
IO_L21P_T3_DQS_14	V10	R184A	33R	RPH_G12
IO_L24P_T3_A01_D17_14	T9	R184B	33R	RPH_G16_CE2
IO_L24N_T3_A00_D16_14	T10	R185C	33R	RPH_G20_SPI1_COPI
IO_L21N_T3_DQS_A06_D22_14	V11	R185D	33R	RPH_G21_SPI1_SCLK

XC7A35T-1CSG324C

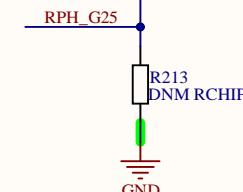
U4D

K6	IO_0_34	CHERIERR0
IO_L1P_T0_34	U1	CHERIERR1
IO_L1N_T0_34	M1	CHERIERR2
IO_L2P_T0_34	K3	CHERIERR3
IO_L2N_T0_34	L3	CHERIERR4
IO_L3P_T0_DQS_34	N2	CHERIERR5
IO_L3N_T0_DQS_34	N1	CHERIERR6
IO_L4P_T0_34	M3	CHERIERR7
IO_L4N_T0_34	M2	CHERIERR8
IO_L5P_T0_34	K5	LED_LEGACY
IO_L5N_T0_34	L4	LED_CHERI
IO_L6P_T0_34	L6	LED_HALTED
IO_L6N_T0_VREF_34	L5	LED_BOOTOK
IO_L22N_T3_34	U6	MICROSD_CLK
IO_L10N_T1_34	V4	MICROSD_DAT0
IO_L23P_T3_34	R7	MICROSD_DAT1
IO_L10P_T1_34	V5	MICROSD_DAT2
IO_L24N_T3_34	T8	MICROSD_DAT3
IO_L24P_T3_34	R8	MICROSD_CMD
IO_L22P_T3_34	U7	R170A 33R SDA0
IO_L20P_T3_34	V9	R170B 33R SCL0
IO_L21P_T3_DQS_34	V7	R170C 33R SDA1
IO_L20P_T3_DQS_34	U9	R170D 33R SCL1
IO_L12P_T1_MRCC_34	T5	NRST
IO_L12N_T1_MRCC_34	T4	FPGAIO_TURBO
IO_L13P_T2_MRCC_34	N5	LCD_BACKLIGHT
IO_L8N_T1_34	U3	R171 22R RP2040_PREQ
IO_L14P_T2_SRCC_34	P4	RP2040_SPARE
IO_L14N_T2_SRCC_34	P3	232 TX
IO_L18N_T2_34	N6	232 RX
IO_L15N_T2_DQS_34	R2	485 RO
IO_L16N_T2_34	M4	485 DE
IO_L16N_T2_34	N4	485 REn
IO_L18P_T2_34	M6	485 DI
IO_L15P_T2_DQS_34	P2	R178A 33R MB0
IO_L17P_T2_34	R1	R178B 33R MB1
IO_L17N_T2_34	T1	R178C 33R MB2
IO_L7P_T1_34	U1	R178D 33R MB3
IO_L11N_T1_SRCC_34	T3	R180A 33R MB4
IO_L7N_T1_34	V1	R180B 33R MB5
IO_L9P_T1_DQS_34	U2	R180C 33R MB6
IO_L9N_T1_DQS_34	V2	R180D 33R MB7
IO_25_34	U8	R184A 33R MB8
IO_L23N_T3_34	T6	R184B 33R MB9
IO_L20N_T3_34	V6	R184C 33R MB10
IO_L19P_T3_34	R6	LCD_RST
IO_L8P_T1_34	U4	LCD_DC
IO_L11P_T1_SRCC_34	R3	LCD_COP1
IO_L19N_T3_VREF_34	R5	LCD_CLK
IO_L13N_T2_MRCC_34	P5	LCD_CS

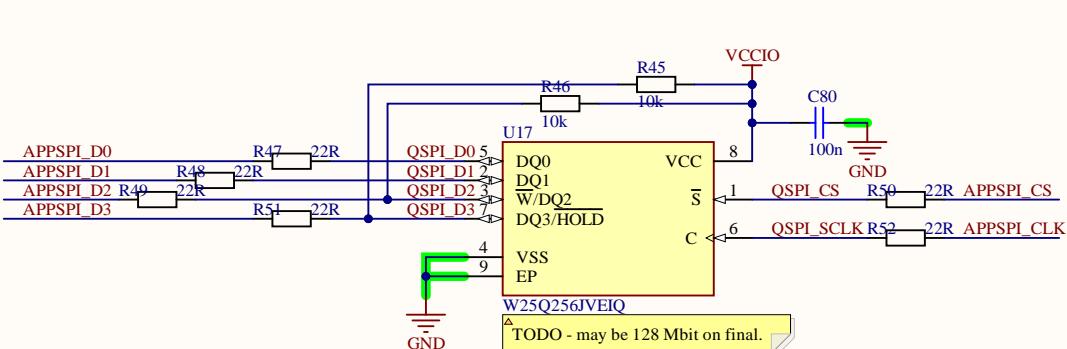
XC7A35T-1CSG324C

R184D 33R

VCCIO

R212
12kR213
DNM RCHIP

GND



Title: IO Banks 14+34 + Flash

Approved: YES



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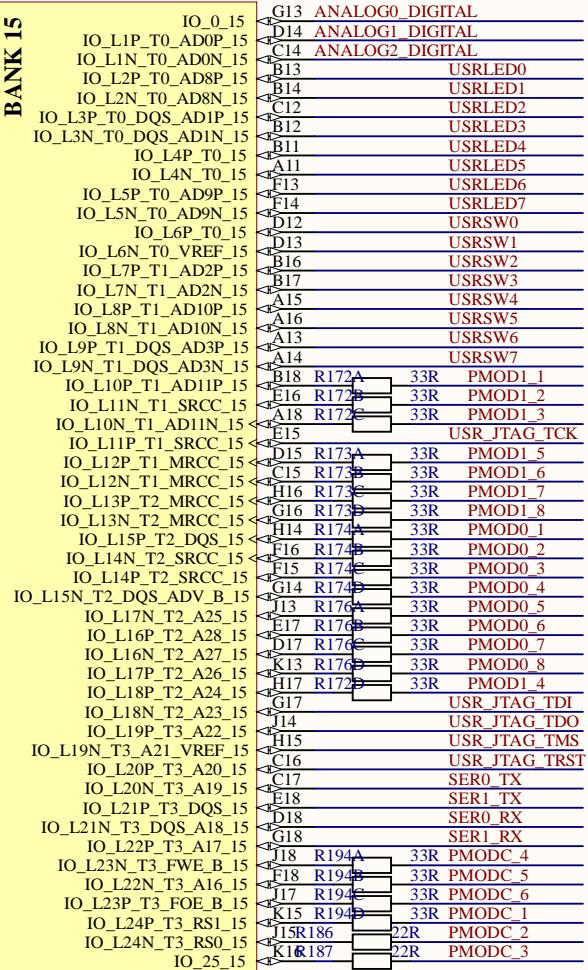
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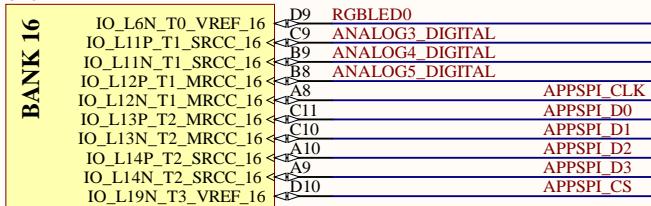
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U4B

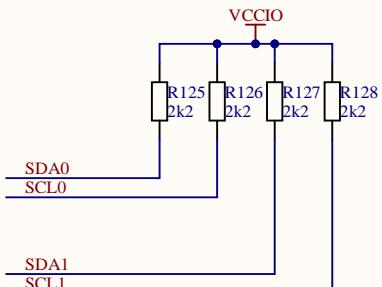


XC7A35T-1CSG324C

U4C



XC7A35T-1CSG324C



Title: IO Banks 15 + 16

Rev: 09

Project: Sonata

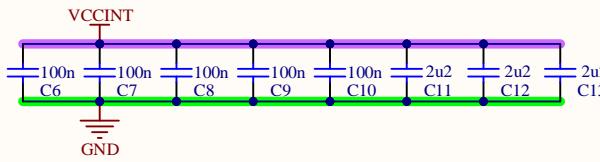
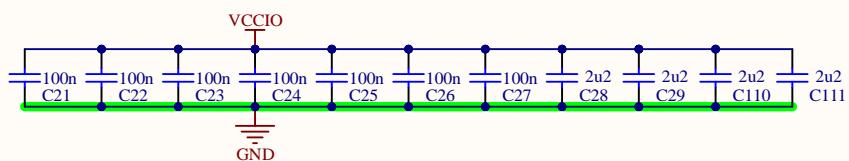
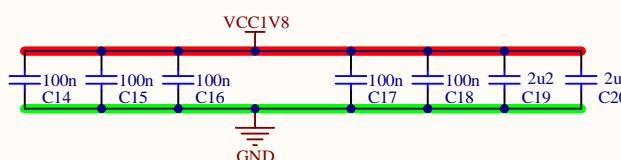
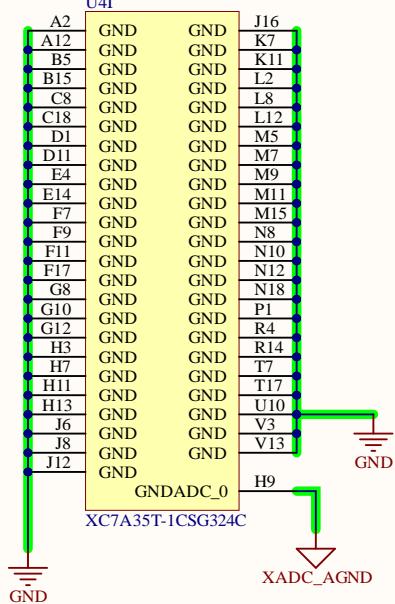
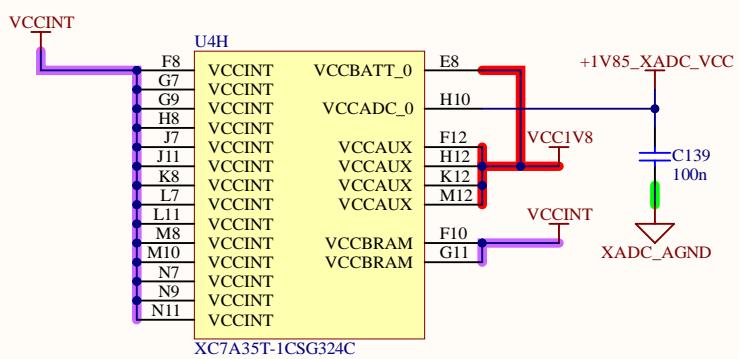
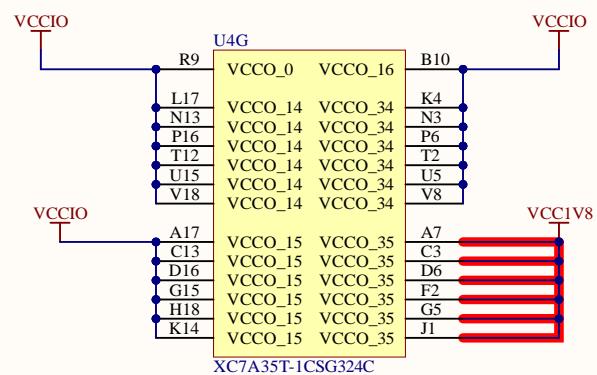
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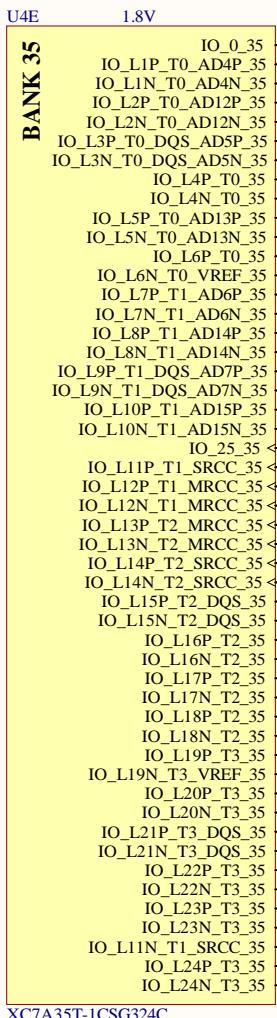
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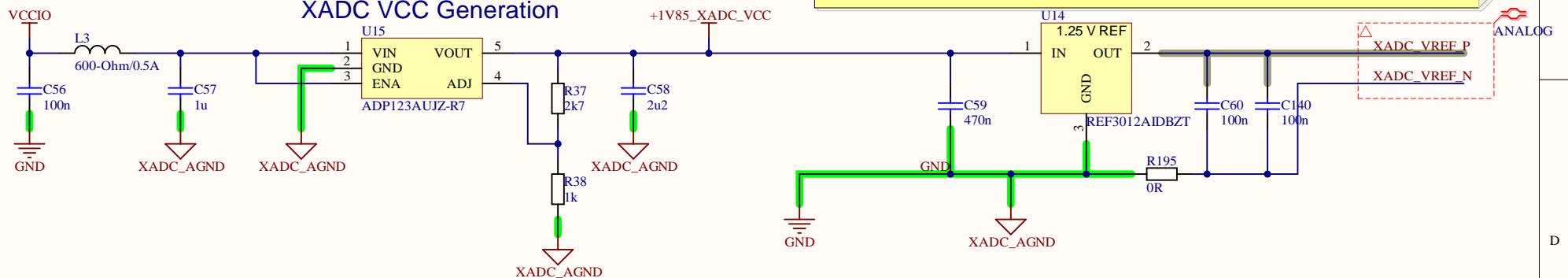
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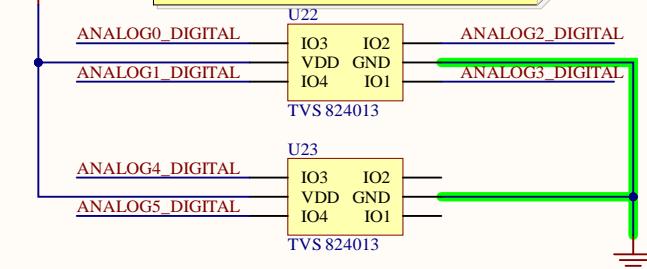




XADC VCC Generation



These are just clamps for analog input/digital pin. Can switch P/N if package isn't convient, and pinswap any of the I/O pins.

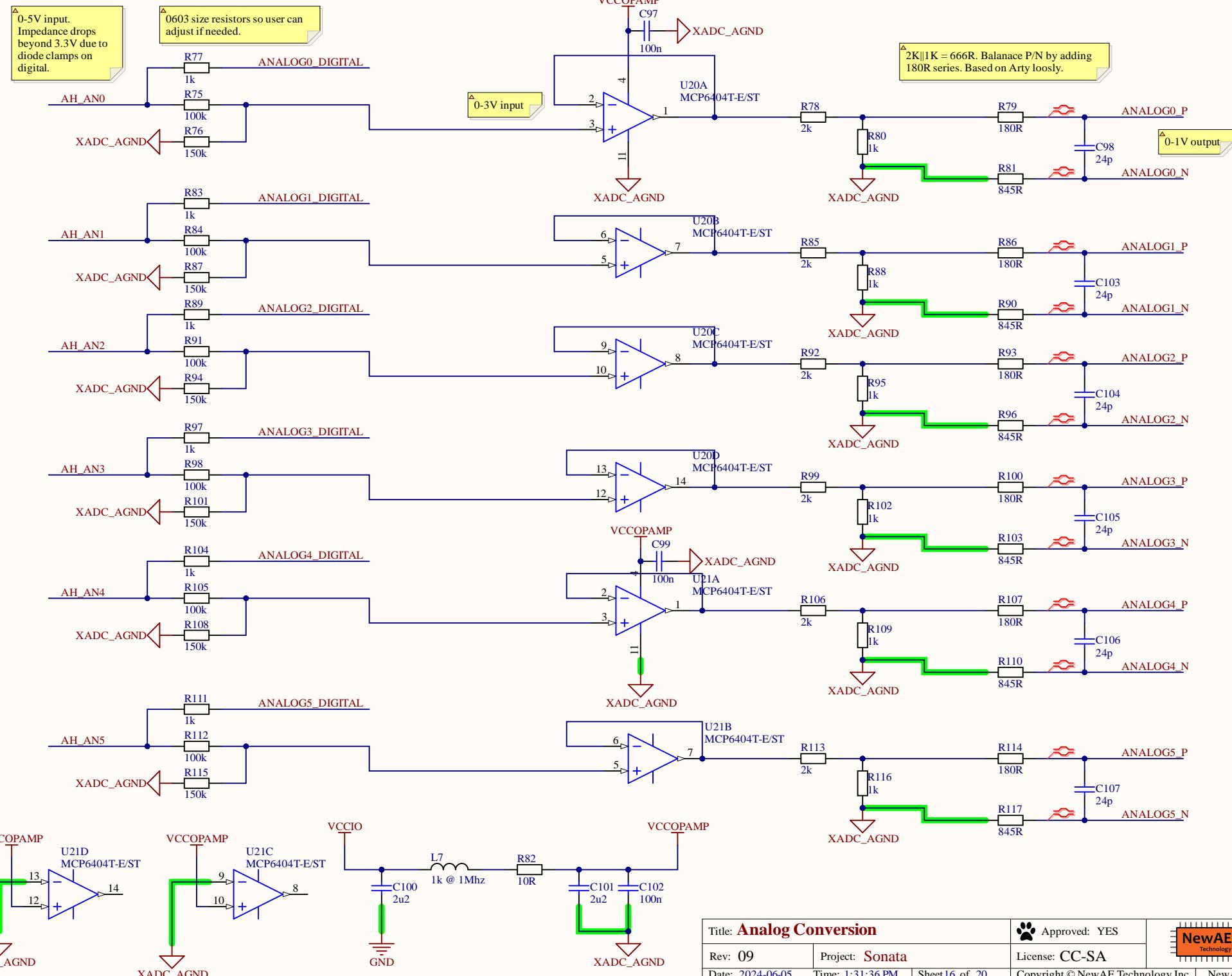


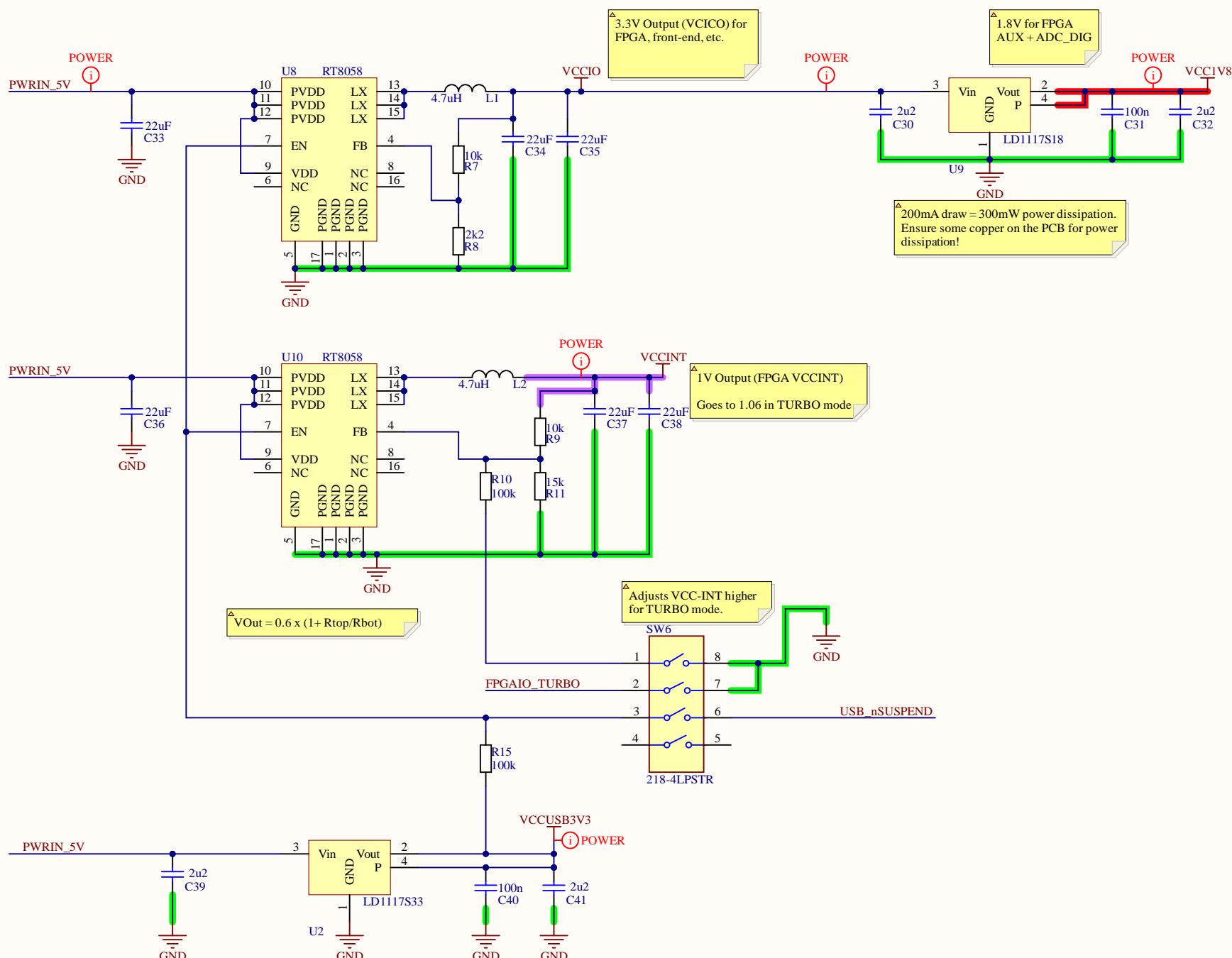
► NOTE on XADC AGND:

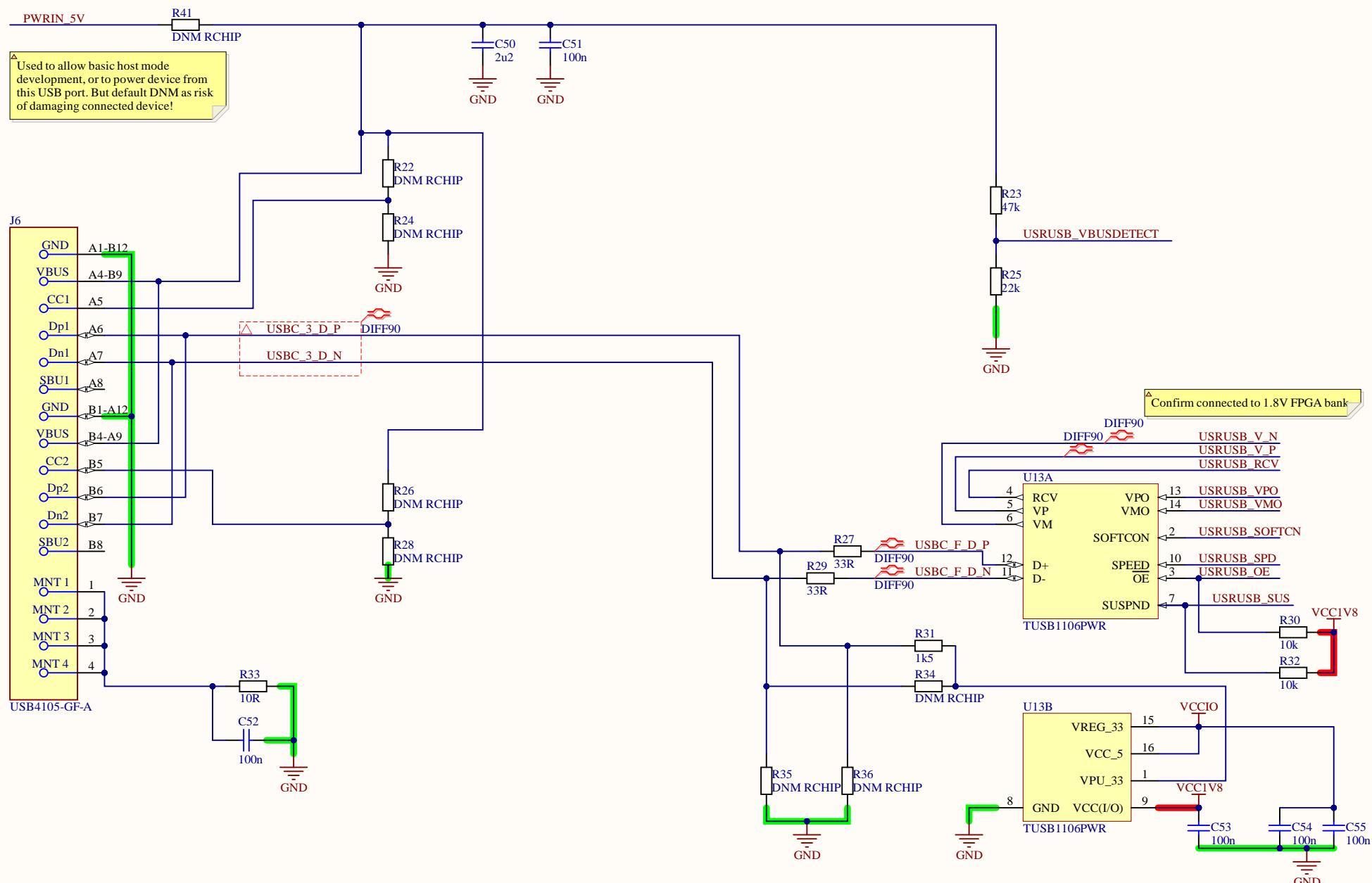
The area where XADC_AGND would live would have FPGA signals cross it. This will generate a lot of noise/issues... instead just made a single ground plane which should be better. In the future could separate GND and ADCGND if required but needs major routing changes.

Title: **FPGA Analog + 1.8V Bank** Approved: YES

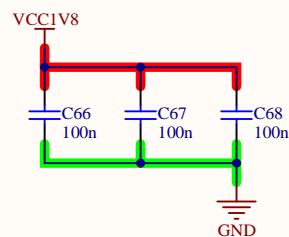
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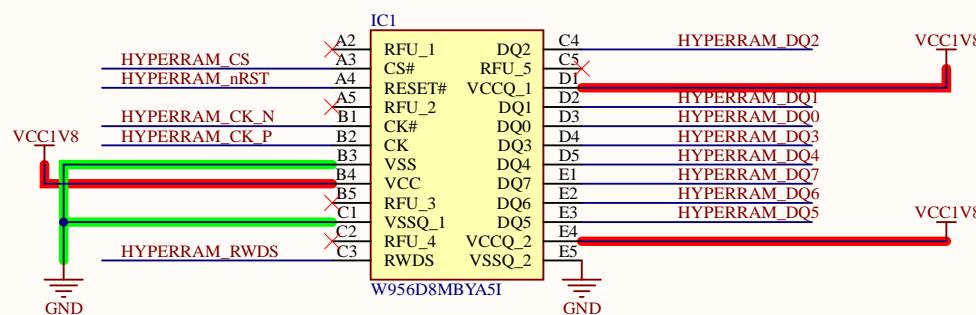




A



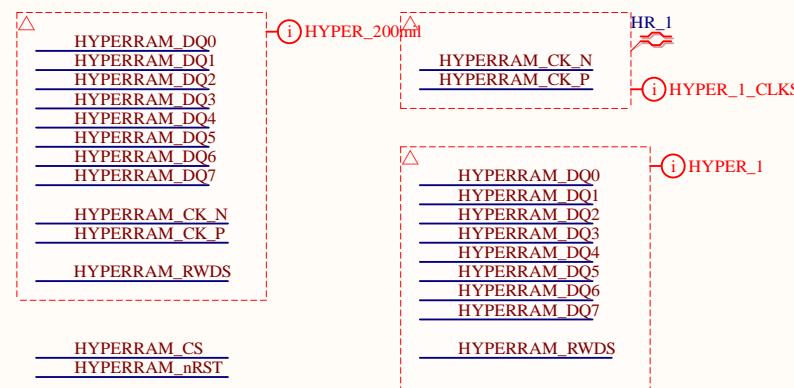
B



C

Table 5 Length matching

Signal group	Length matching tolerance
	200 MHz
CK to CK#	±10 mils
RWDS to DQ[7:0]	±15 mils
RWDS1 to DQ[15:8] ¹	±15 mils
DQx[7:0] to DQy[7:0]	±30 mils
DQx[15:8] to DQy[15:8] ¹	
CK/CK# to DQ[7:0]	±200 mils
CK/CK# to DQ[15:0] ¹	
CK/CK# to CS#	±1500 mils
CK/CK# to RWDS	±1500 mils
RESET# to RST# to CS#	±2000 mils



¹nRST is longest PCB trace, taken out of group to avoid making length matching harder as length match is +/- 2 inches so will meet that anyway...

D

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Project: Sonata

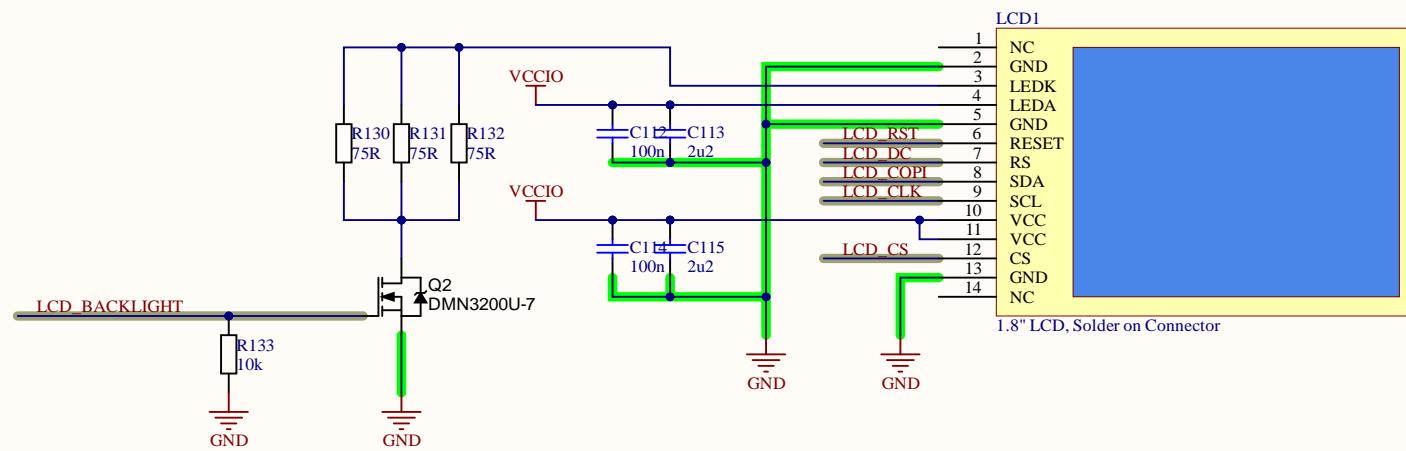
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File: sb-sonata-hyperram.SchDoc

Approved: YES



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Rev: 09	Project: Sonata	License: CC-SA	
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