

A

A

B

B

C

C

D

D

MH1
M3, Tight FitMH2
M3, Tight FitMH3
M3, Tight FitMH4
M3, Tight FitMH5
M3, Tight FitMH6
M3, Tight FitMH7
M3, Tight FitTitle: **Mechanical & Title Page**

Approved: NO



Rev: 02

Project: Sonata

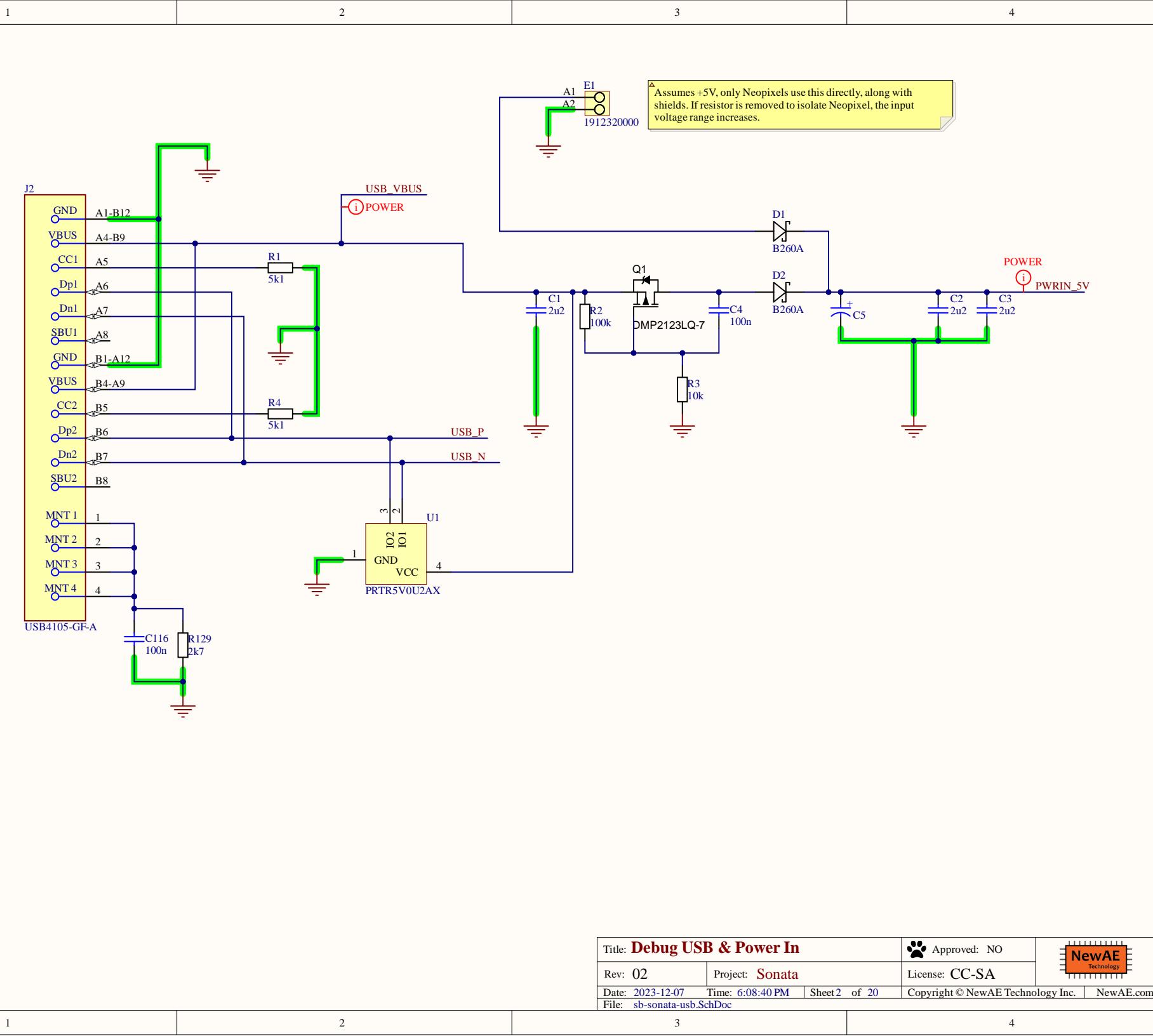
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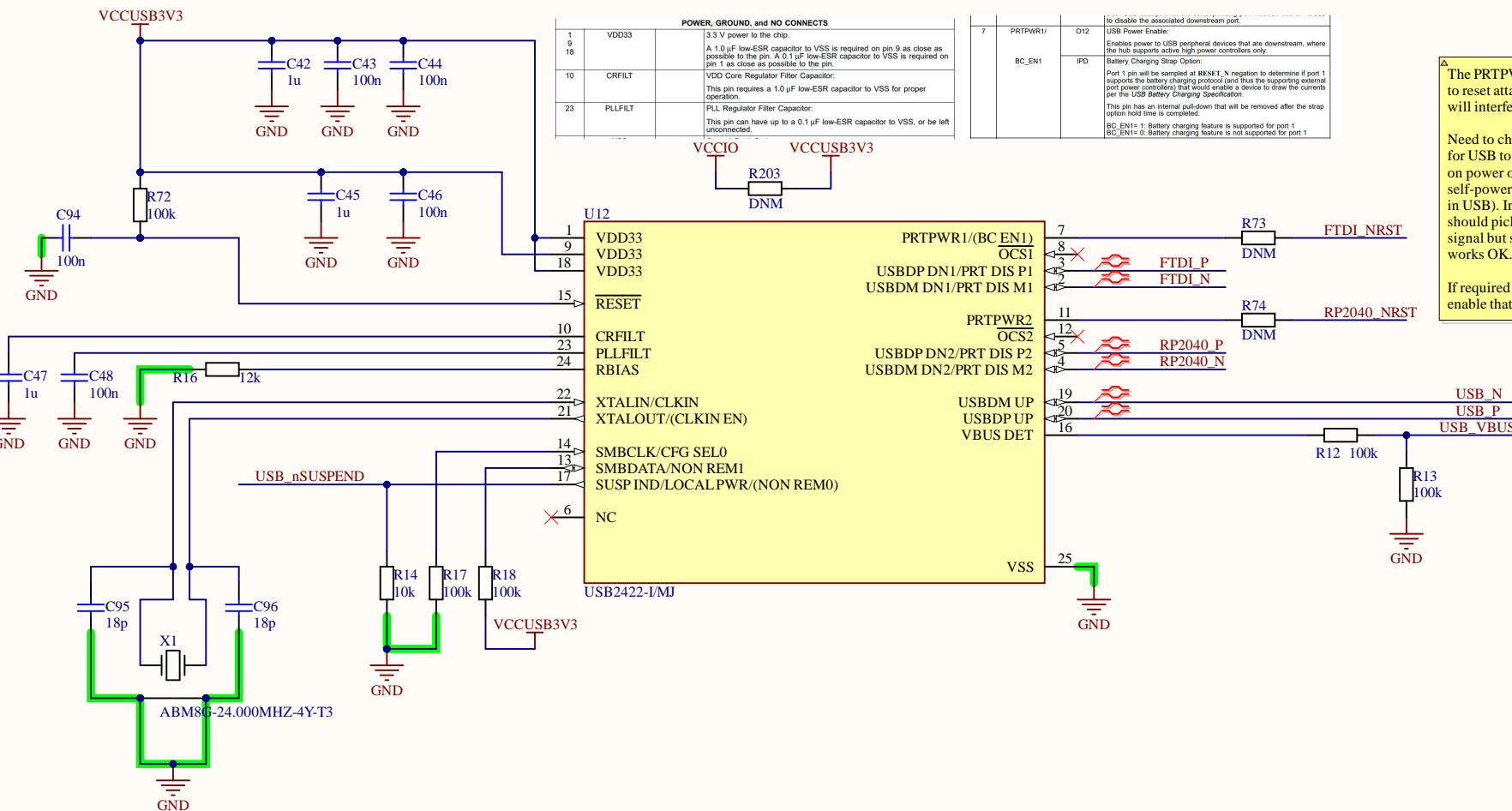
Date: 2023-12-07

Time: 6:08:40 PM

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File: sb-sonata-mech.SchDoc





The PRTPWR pins could be used to reset attached devices. But that will interfere with standalon usage.

Need to check if reset is required for USB to be picked up depending on power order (e.g. if board is self-powered, then someone plugs in USB). In theory attached devices should pick up the USB suspend signal but something to confirm works OK.

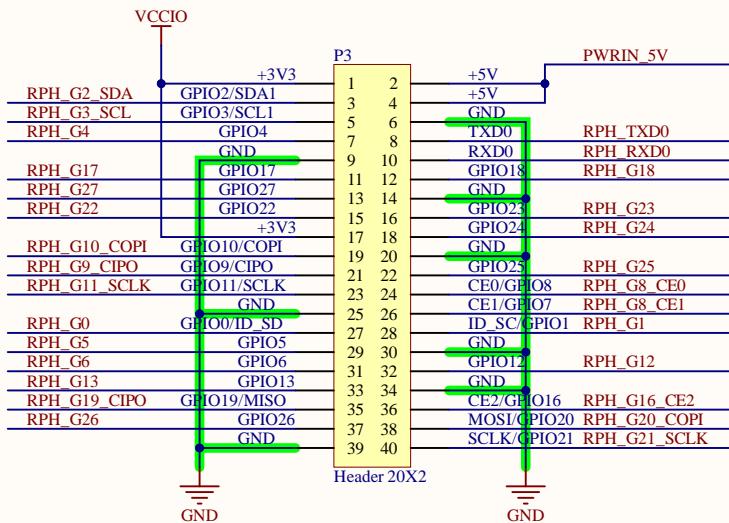
If required the series resistors will enable that for now.

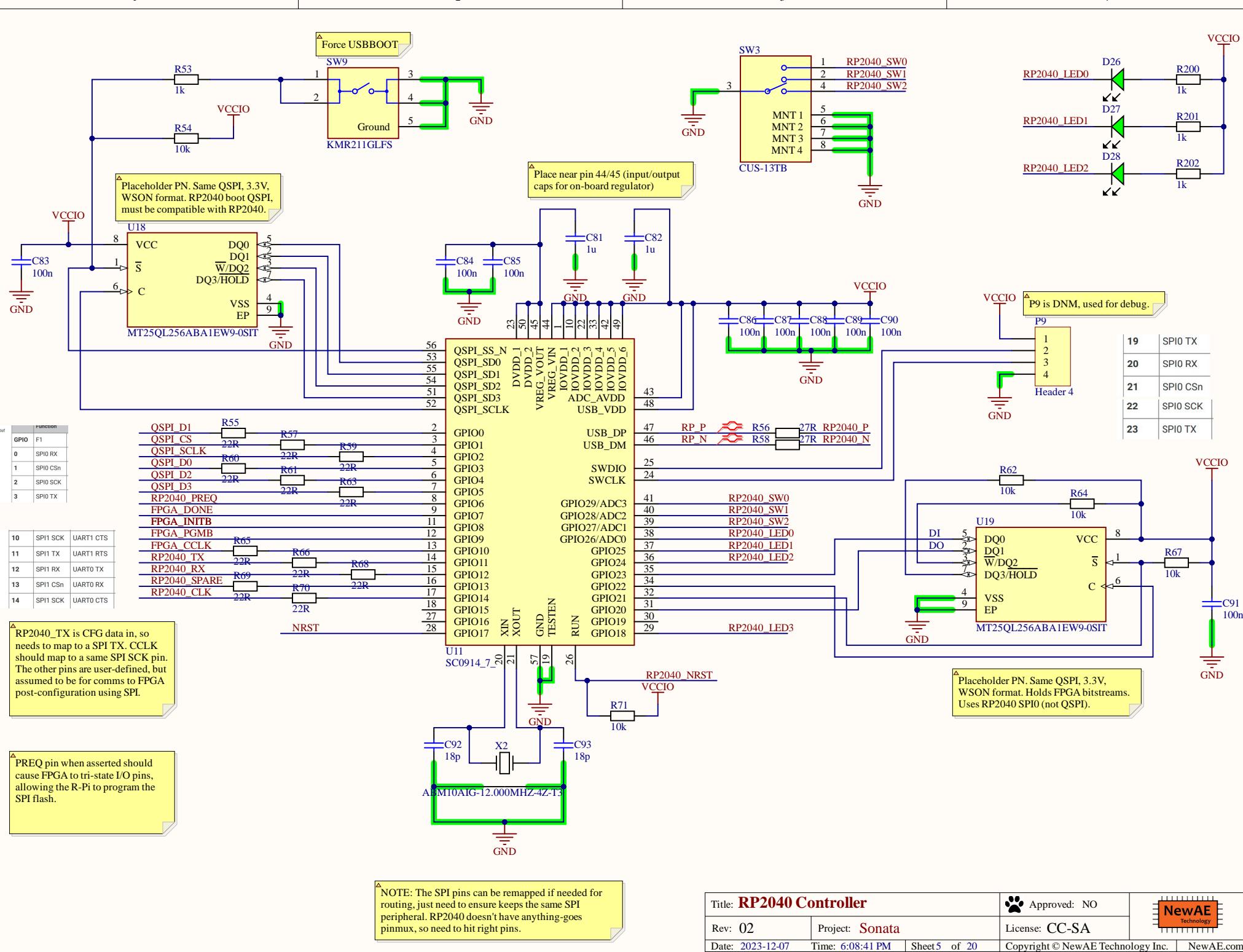
TABLE 4-1: HUB CONFIGURATION OPTIONS

CFG_SEL	Description
0	Default configuration: • Strap options enabled • Hub descriptors indicate the hub as "self-powered"
1	The hub is configured externally over SMBus (as an SMBus slave device with address 0101100b): • Strap options disabled • Self-powered or bus-powered depending on register settings • All registers configured over SMBus

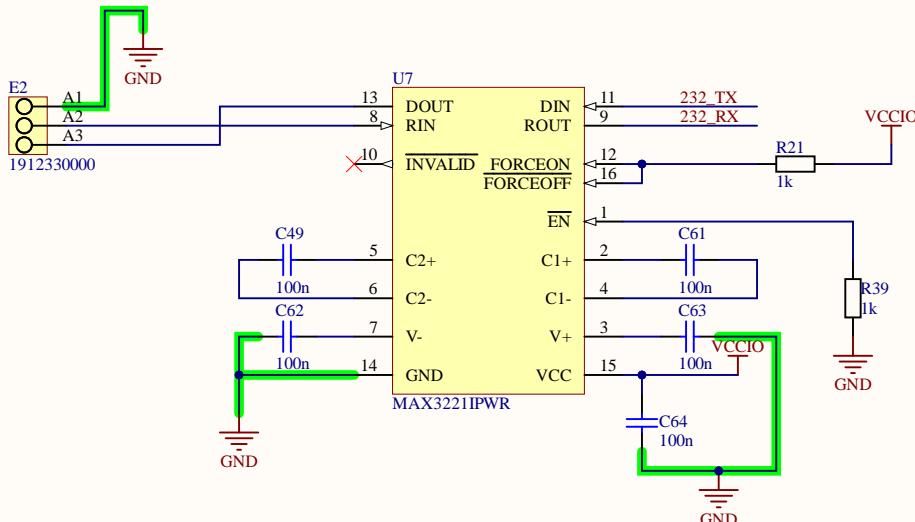
NON_Rem[1:0] = 00: all ports are removable
NON_Rem[1:0] = 01: port 1 is non-removable
NON_Rem[1:0] = 10: ports 1 and 2 are non-removable
NON_Rem[1:0] = 11: reserved

R-Pi Headers

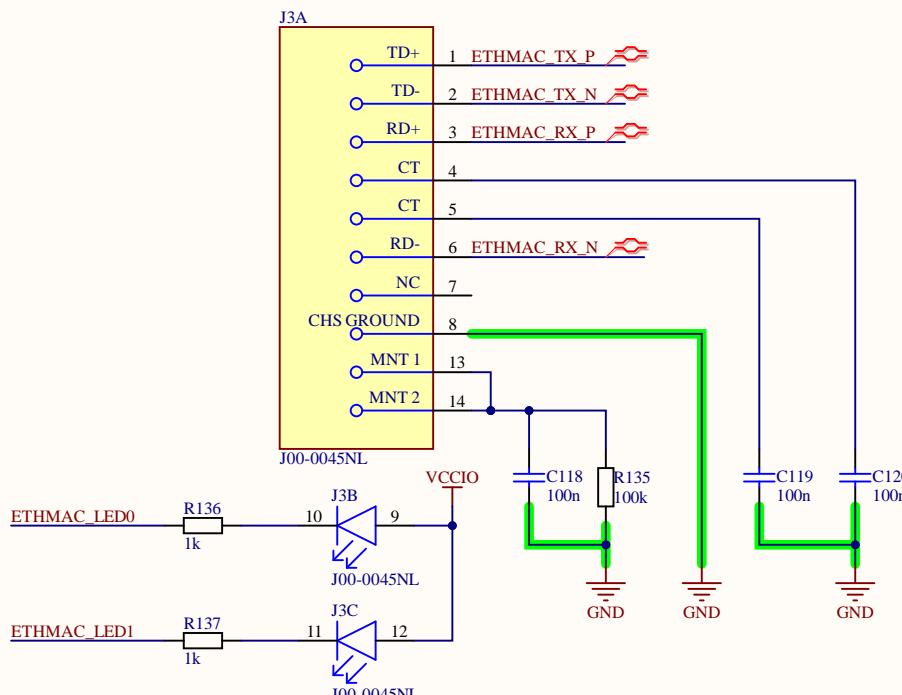




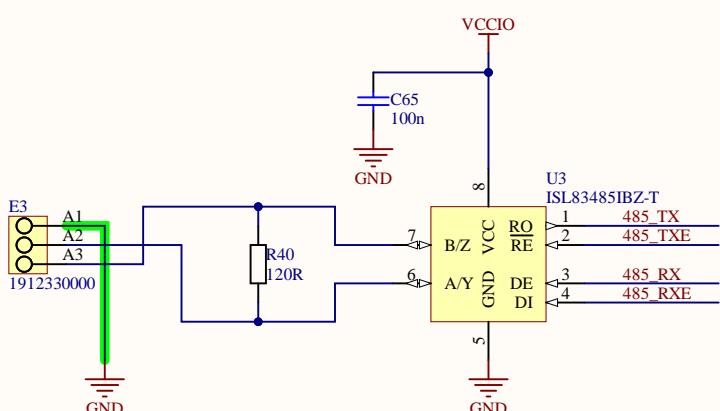
A



B

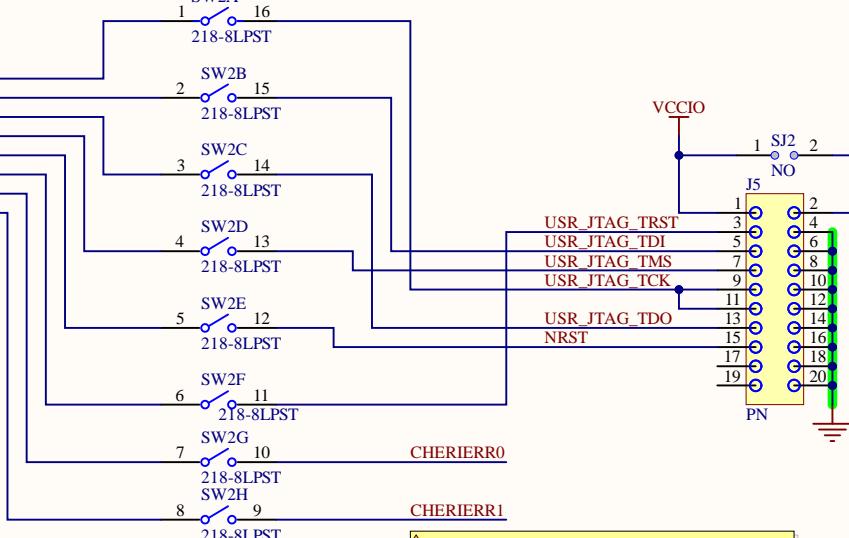
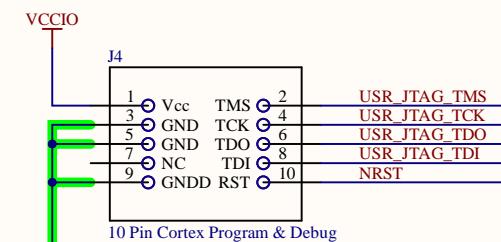
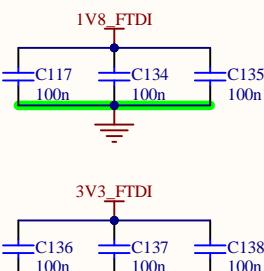
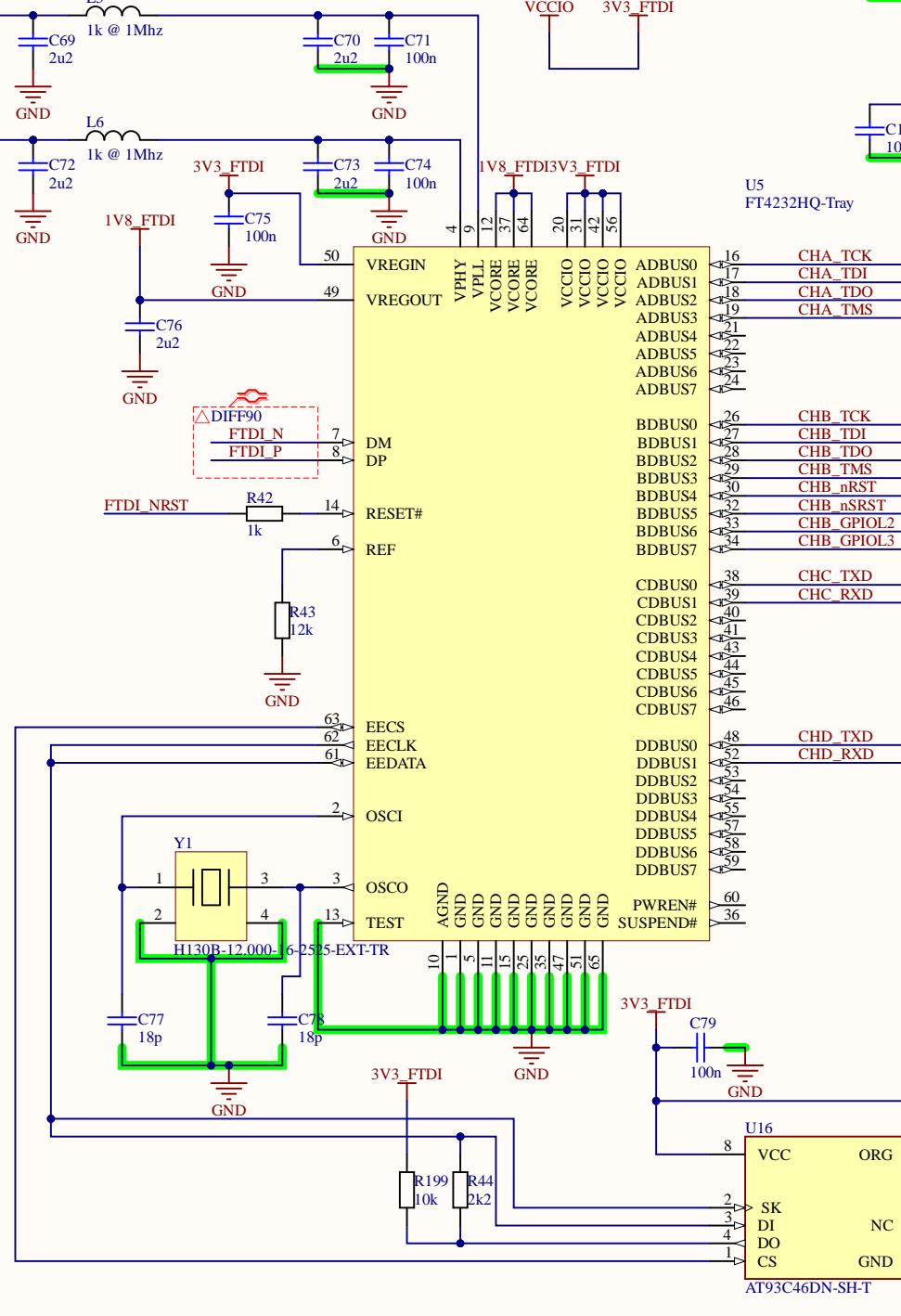


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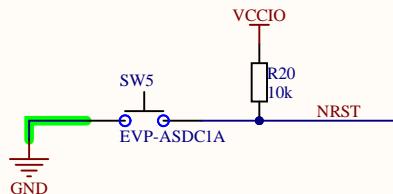
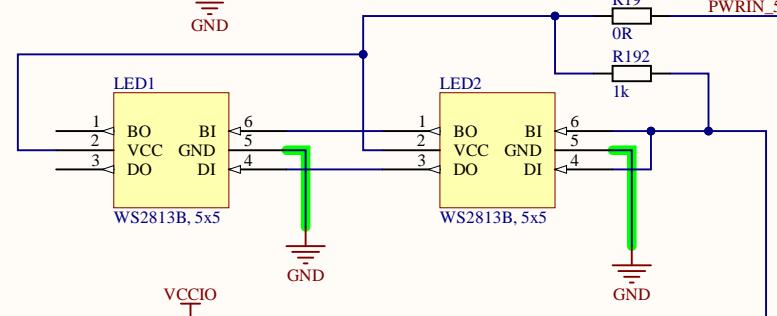
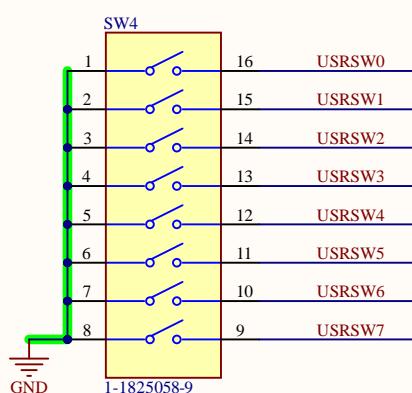
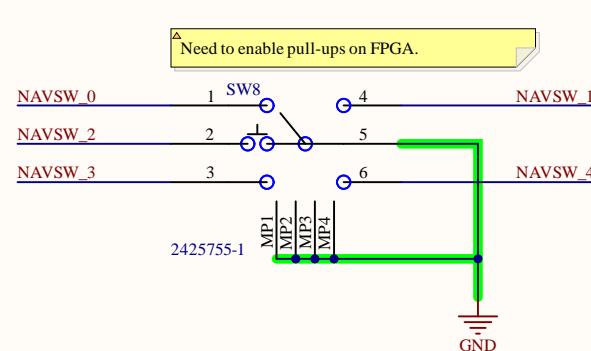
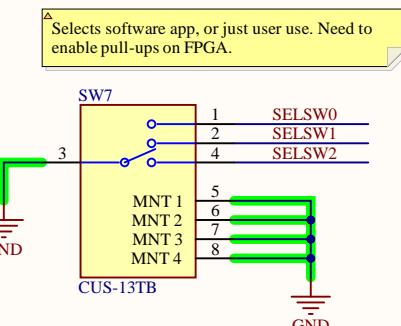
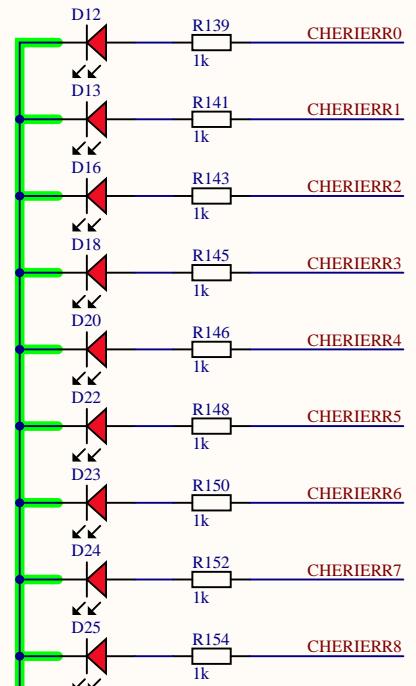
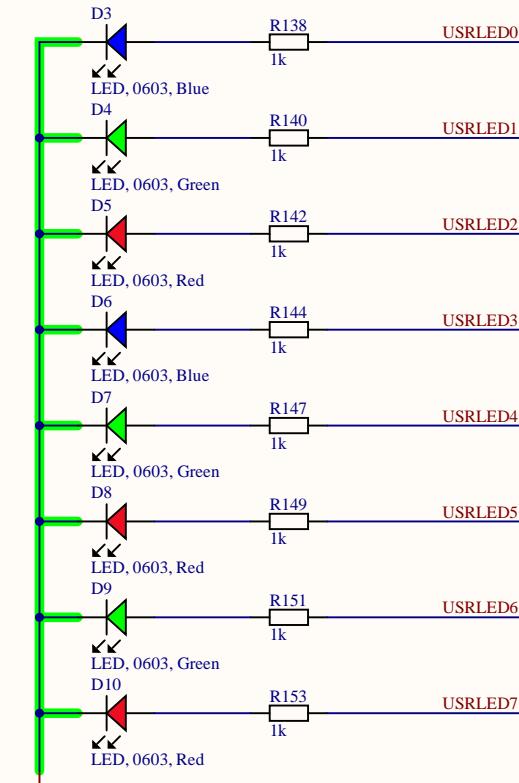


D

Title: RS485,RS232,Eth Connectors		Approved: NO	NewAE Technology
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Can use these as strapping pins if needed (default - LED outputs).



Inverted data line dealt with in FPGA

Title: LEDs and Switches

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A

A

B

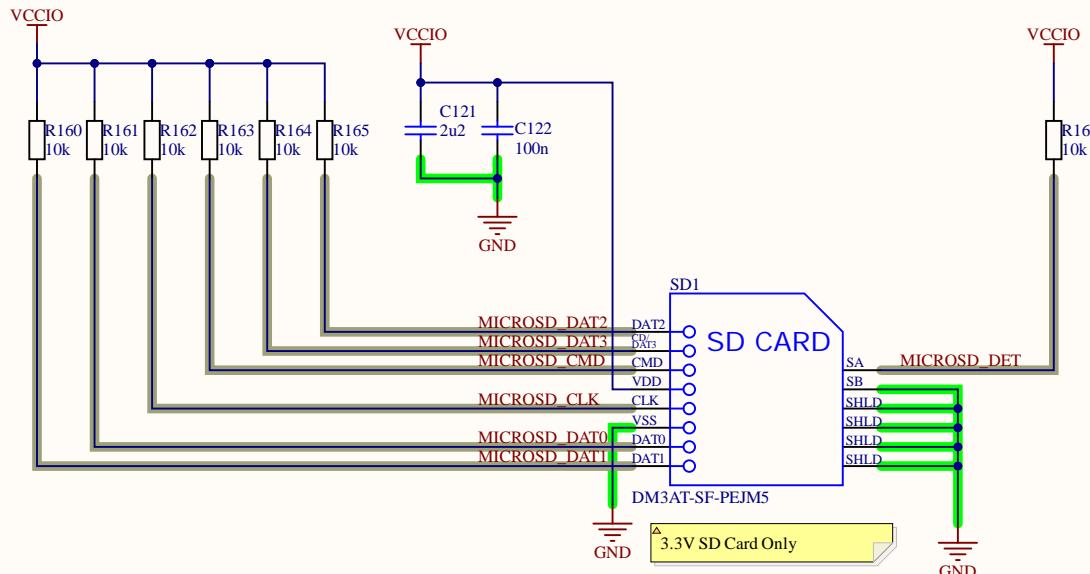
B

C

C

D

D



Title: MicroSD Card Connector

Rev: 02

Project: Sonata

Approved: NO



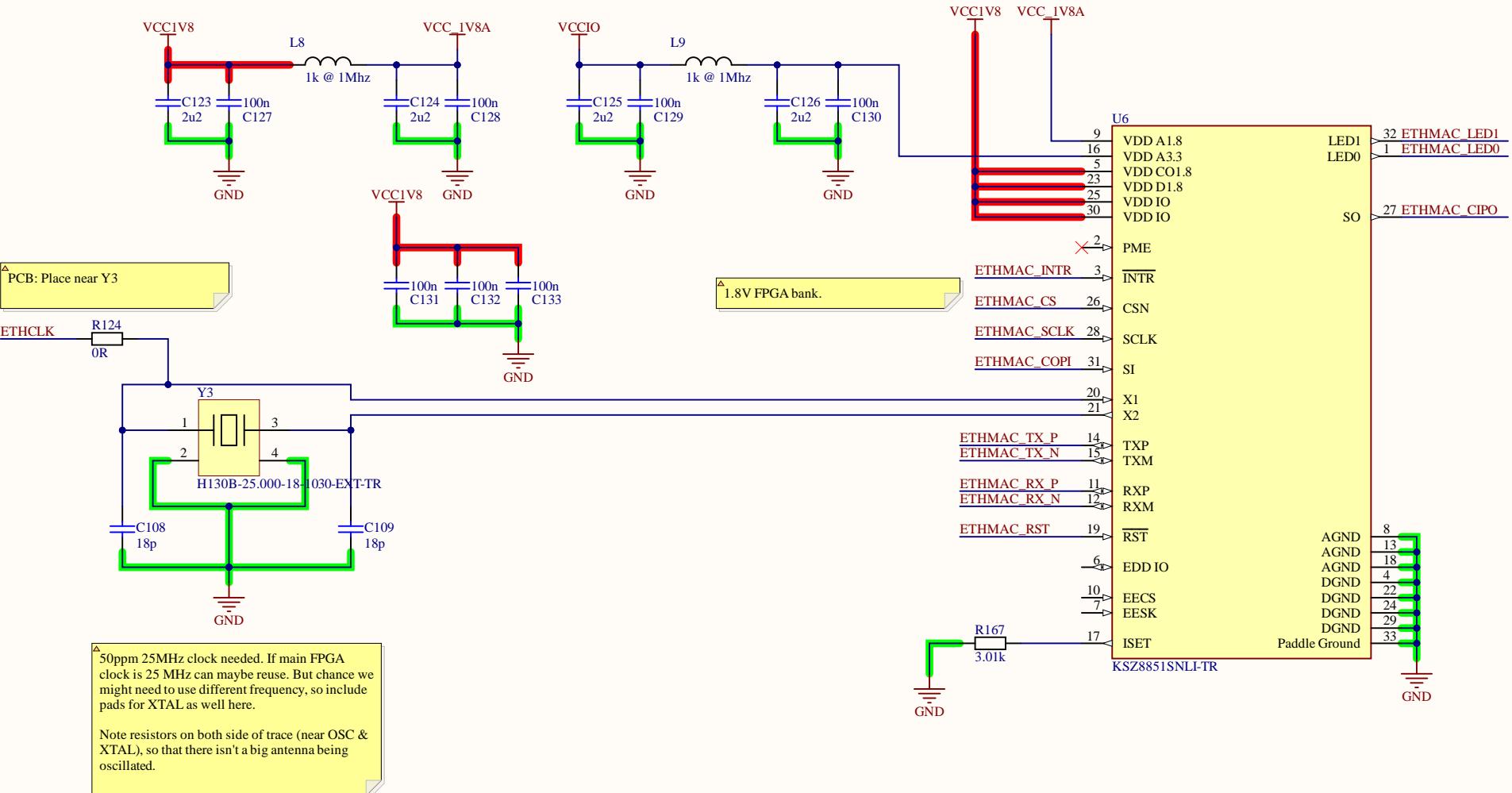
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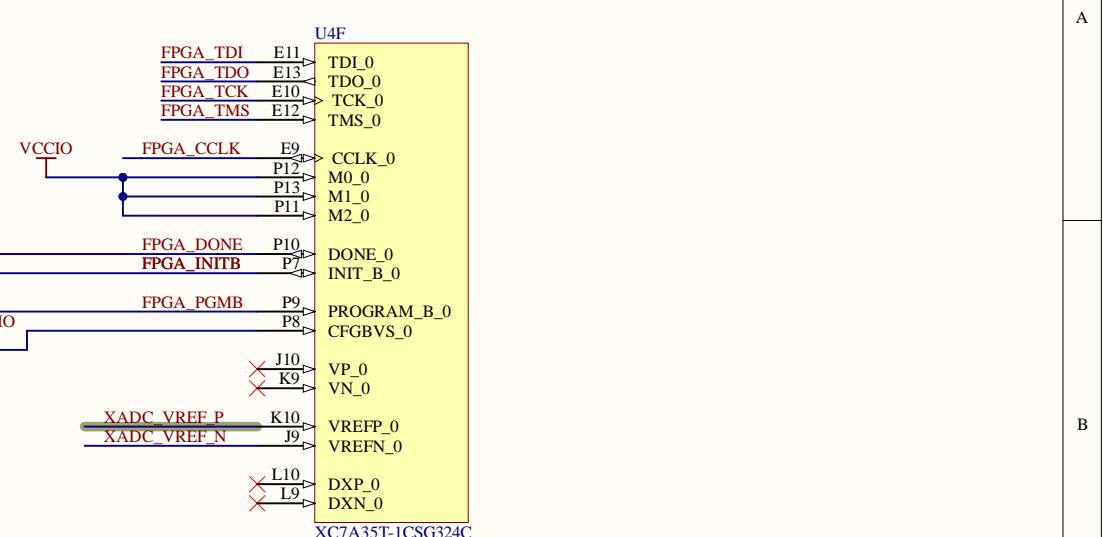
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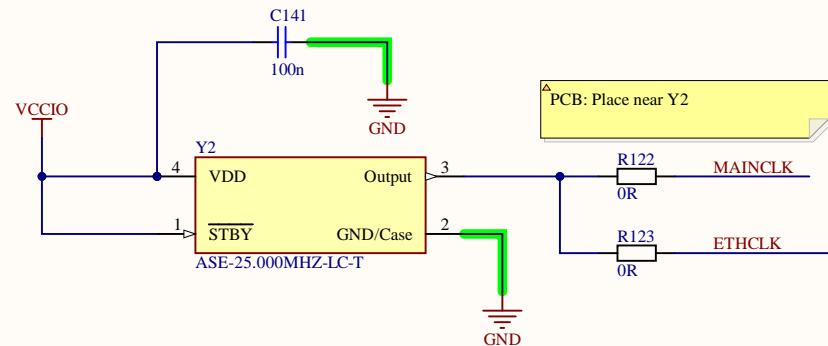
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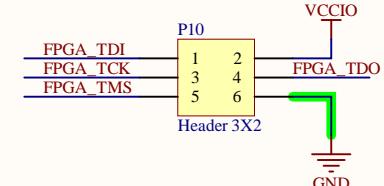
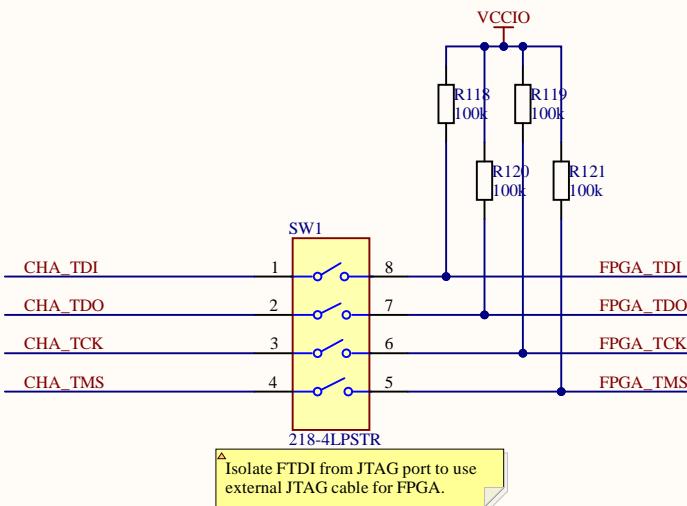
A



B



C



Non-standard. Roughly based on AVR 6-pin ISP header.

D

Title: FPGA Config & Misc

Rev: 02 Project: Sonata

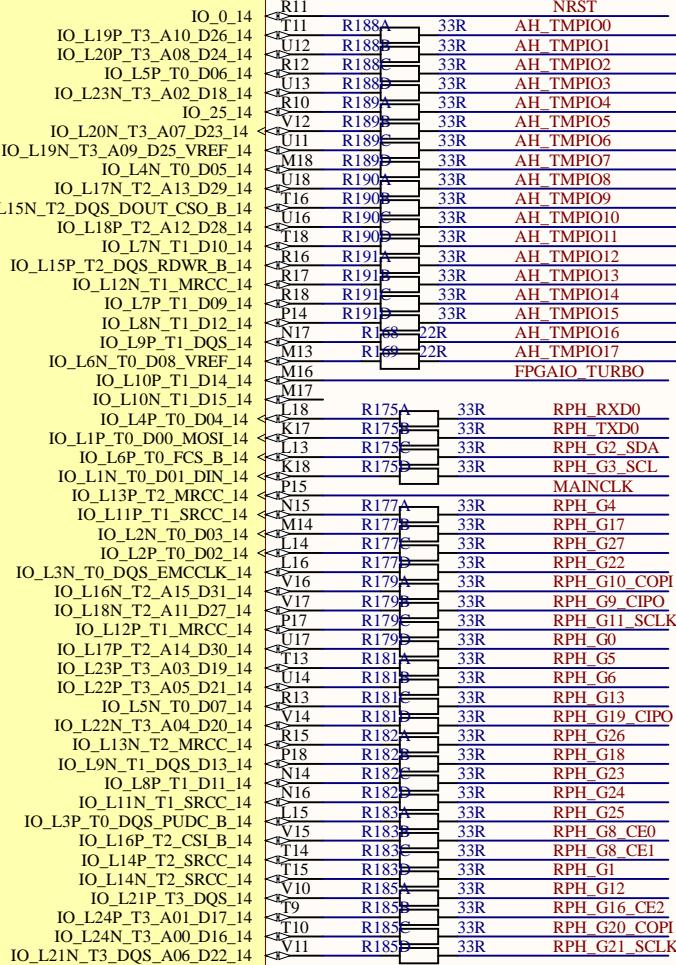
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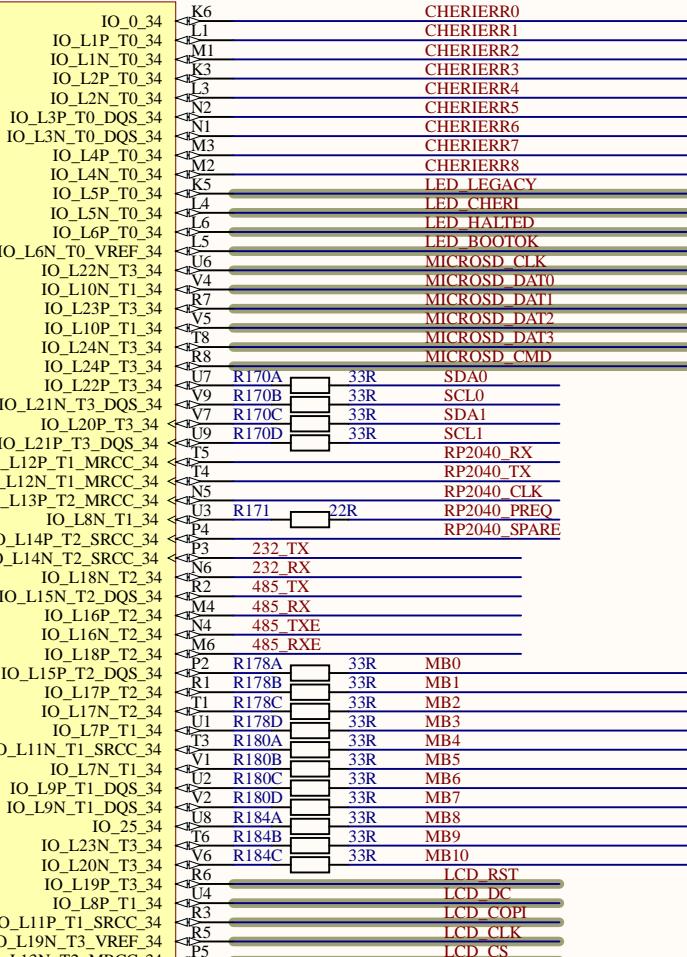
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U4A

XC7A35T-1CSG324C

BANK 34

XC7A35T-1CSG324C

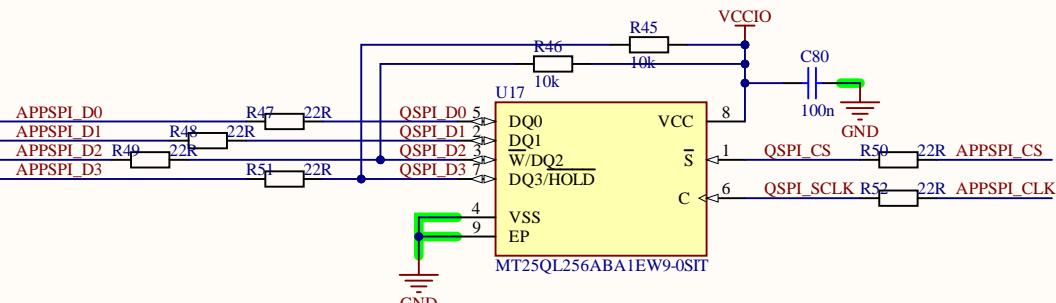
R184D 33R

A

TODO: Add series resistors, check if placement actually is possible:

Arduino: 47 ohm
RP: 22 ohm
PMOD: 22 ohm
MB Click: 10 ohm
SDA/SCL: 47 ohm

It's possible not reasonable to do it due to PCB routing though.
Have used resistor array below on some boards which helps with space.



D

This SPI flash can be driven from both the FPGA and from the RP2040. Ideally placed between them with a sort of daisy-chain style routing FPGA-->SPI-->RP2040, as short as possible.

Title: **IO Banks 14+34 + Flash**Rev: 02 Project: **Sonata**

Date: 2023-12-07 Time: 6:08:42 PM Sheet 12 of 20

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U4B

BANK 15	
IO_0_15	G13 ANALOG0_DIGITAL
IO_L1P_T0_AD0P_15	D14 ANALOG1_DIGITAL
IO_L1N_T0_AD0N_15	C14 ANALOG2_DIGITAL
IO_L2P_T0_AD8P_15	B13 USRLED0
IO_L2N_T0_AD8N_15	B14 USRLED1
IO_L3P_T0_DQS_AD1P_15	C12 USRLED2
IO_L3N_T0_DQS_AD1N_15	B12 USRLED3
IO_L4P_T0_15	B11 USRLED4
IO_L4N_T0_15	A11 USRLED5
IO_L5P_T0_AD9P_15	F13 USRLED6
IO_L5N_T0_AD9N_15	F14 USRLED7
IO_L6P_T0_15	D12 USRSW0
IO_L6N_T0_VREF_15	D13 USRSW1
IO_L7P_T1_AD2P_15	B16 USRSW2
IO_L7N_T1_AD2N_15	B17 USRSW3
IO_L8P_T1_AD10P_15	A15 USRSW4
IO_L8N_T1_AD10N_15	A16 USRSW5
IO_L9P_T1_DQS_AD3P_15	A13 USRSW6
IO_L9N_T1_DQS_AD3N_15	A14 USRSW7
IO_L10P_T1_AD11P_15	B18 R172A 33R PMOD1_1
IO_L11N_T1_SRCC_15	E16 R172B 33R PMOD1_2
IO_L10N_T1_AD11N_15	A18 R172C 33R PMOD1_3
IO_L11P_T1_SRCC_15	E15 R172D 33R PMOD1_4
IO_L12P_T1_MRCC_15	D15 R173A 33R PMOD1_5
IO_L12N_T1_MRCC_15	C15 R173B 33R PMOD1_6
IO_L13P_T2_MRCC_15	H16 R173C 33R PMOD1_7
IO_L13N_T2_MRCC_15	G16 R173D 33R PMOD1_8
IO_L15P_T2_DQS_15	H14 R174A 33R PMOD0_1
IO_L14N_T2_SRCC_15	F16 R174B 33R PMOD0_2
IO_L14P_T2_SRCC_15	F15 R174C 33R PMOD0_3
IO_L15N_T2_DQS_ADV_B_15	G14 R174D 33R PMOD0_4
IO_L17N_T2_A25_15	J13 R176A 33R PMOD0_5
IO_L16P_T2_A28_15	E17 R176B 33R PMOD0_6
IO_L16N_T2_A27_15	D17 R176C 33R PMOD0_7
IO_L17P_T2_A26_15	K13 R176D 33R PMOD0_8
IO_L18P_T2_A24_15	H17 USR_JTAG_TCK
IO_L18N_T2_A23_15	G17 USR_JTAG_TDI
IO_L19P_T3_A22_15	J14 USR_JTAG_TDO
IO_L19N_T3_A21_VREF_15	H15 USR_JTAG_TMS
IO_L20P_T3_A20_15	C16 USR_JTAG_TRST
IO_L20N_T3_A19_15	C17 SER0_TX
IO_L21P_T3_DQS_15	E18 SER1_RX
IO_L21N_T3_DQS_A18_15	D18 SER0_RX
IO_L22P_T3_A17_15	G18 SER1_RX
IO_L23N_T3_FWE_B_15	J18 R194A 33R PMODC_4
IO_L22N_T3_A16_15	F18 R194B 33R PMODC_5
IO_L23P_T3_FOE_B_15	J17 R194C 33R PMODC_6
IO_L24P_T3_RS1_15	K15 R194D 33R PMODC_1
IO_L24N_T3_RS0_15	J15R186 22R PMODC_2
IO_25_15	K16R187 22R PMODC_3

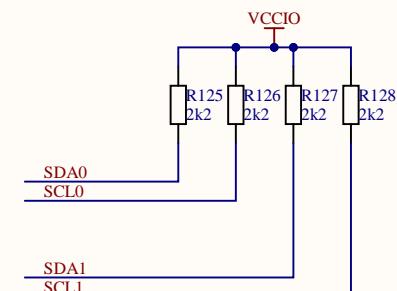
XC7A35T-1CSG324C

G13 ANALOG0_DIGITAL
D14 ANALOG1_DIGITAL
C14 ANALOG2_DIGITAL
B13 USRLED0
B14 USRLED1
C12 USRLED2
B12 USRLED3
B11 USRLED4
A11 USRLED5
F13 USRLED6
F14 USRLED7
D12 USRSW0
D13 USRSW1
B16 USRSW2
B17 USRSW3
A15 USRSW4
A16 USRSW5
A13 USRSW6
A14 USRSW7

U4C

BANK 16	
IO_L6N_T0_VREF_16	D9 RGBLED0
IO_L11P_T1_SRCC_16	C9 ANALOG3_DIGITAL
IO_L11N_T1_SRCC_16	B9 ANALOG4_DIGITAL
IO_L12P_T1_MRCC_16	B8 ANALOG5_DIGITAL
IO_L12N_T1_MRCC_16	A8 APPSPI_CLK
IO_L13P_T2_MRCC_16	C11 APPSPI_D0
IO_L13N_T2_MRCC_16	E10 APPSPI_D1
IO_L14P_T2_SRCC_16	IO_L14P_T2_SRCC_16 APPSPI_D2
IO_L14N_T2_SRCC_16	IO_L14N_T2_SRCC_16 APPSPI_D3
IO_L19N_T3_VREF_16	D10 APPSPI_CS

XC7A35T-1CSG324C



Title: IO Banks 15 + 16

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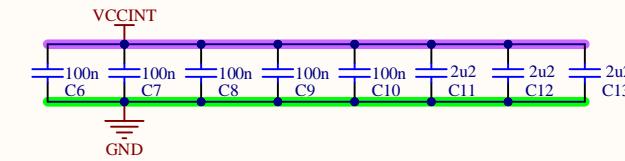
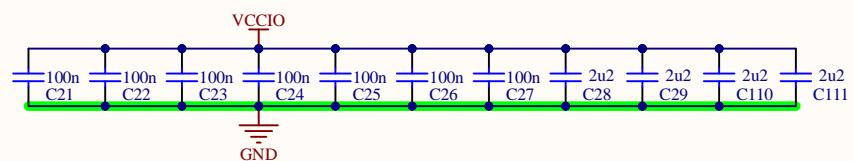
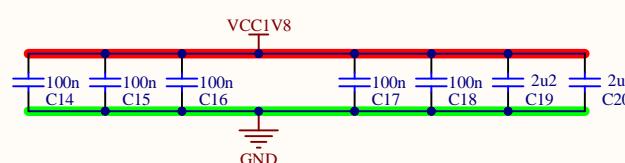
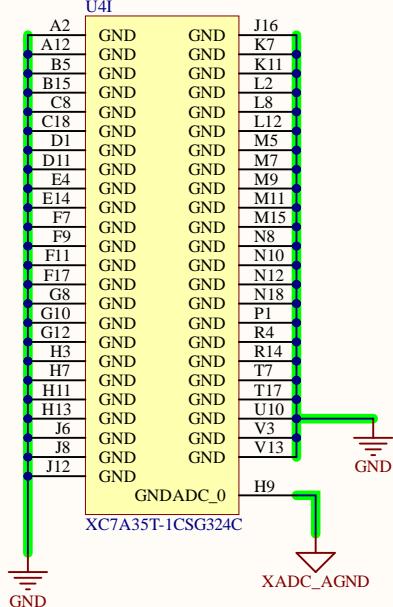
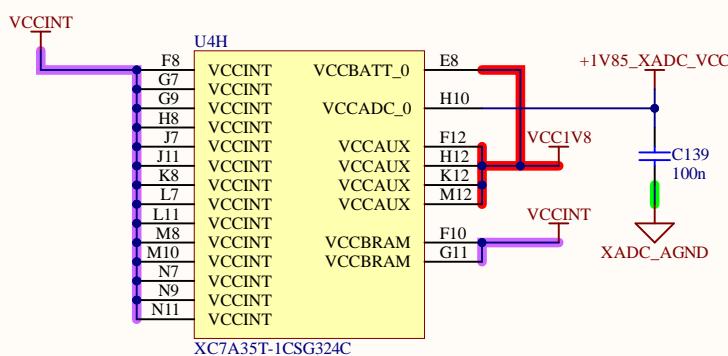
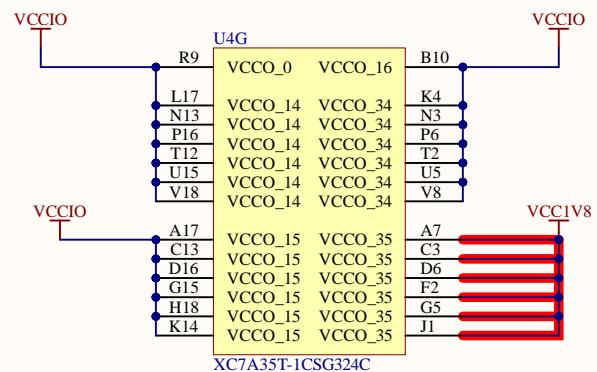
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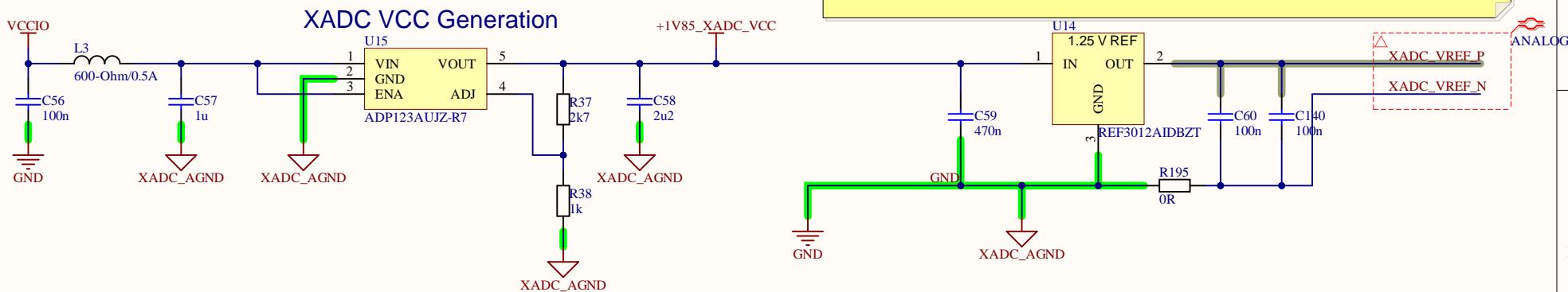
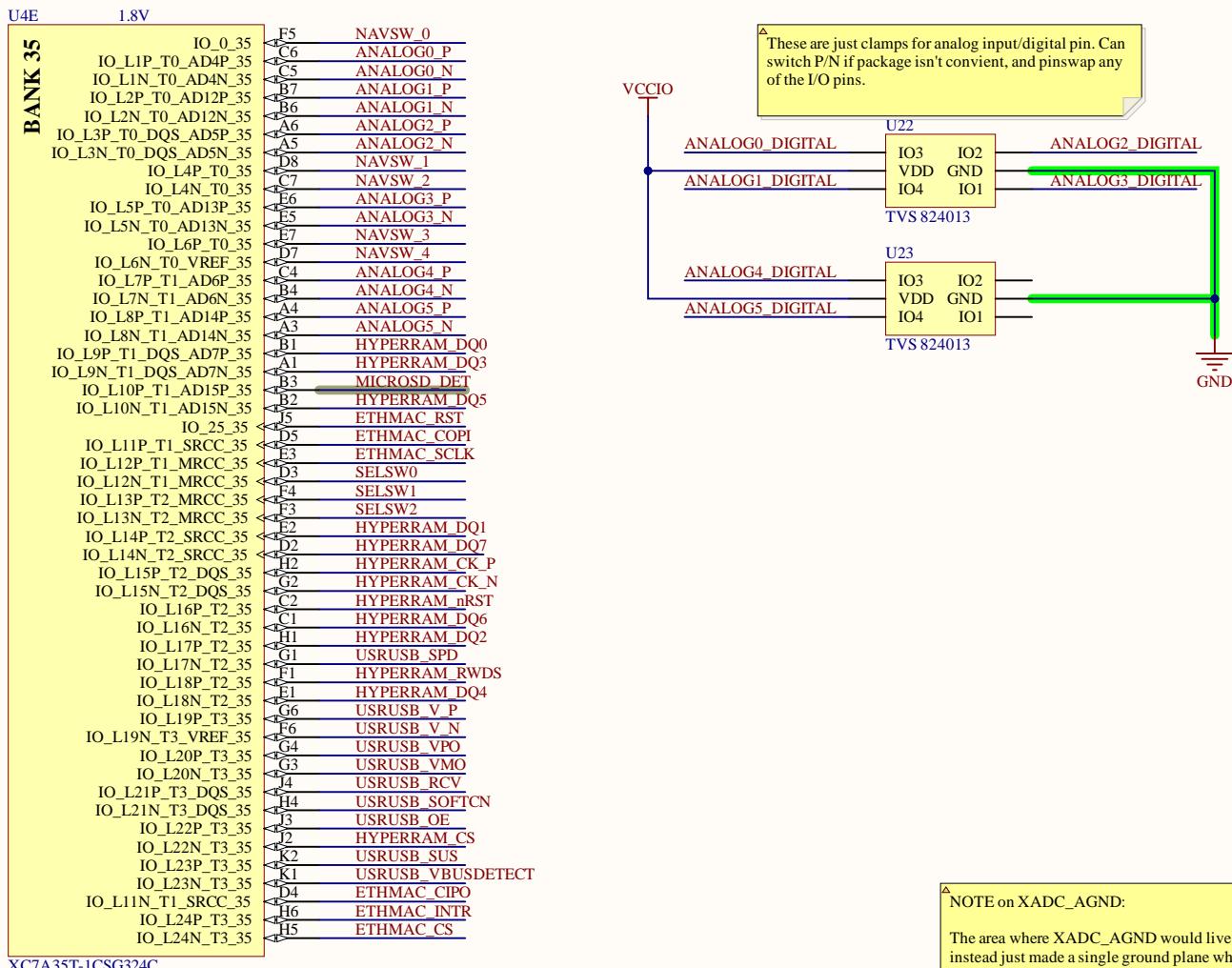
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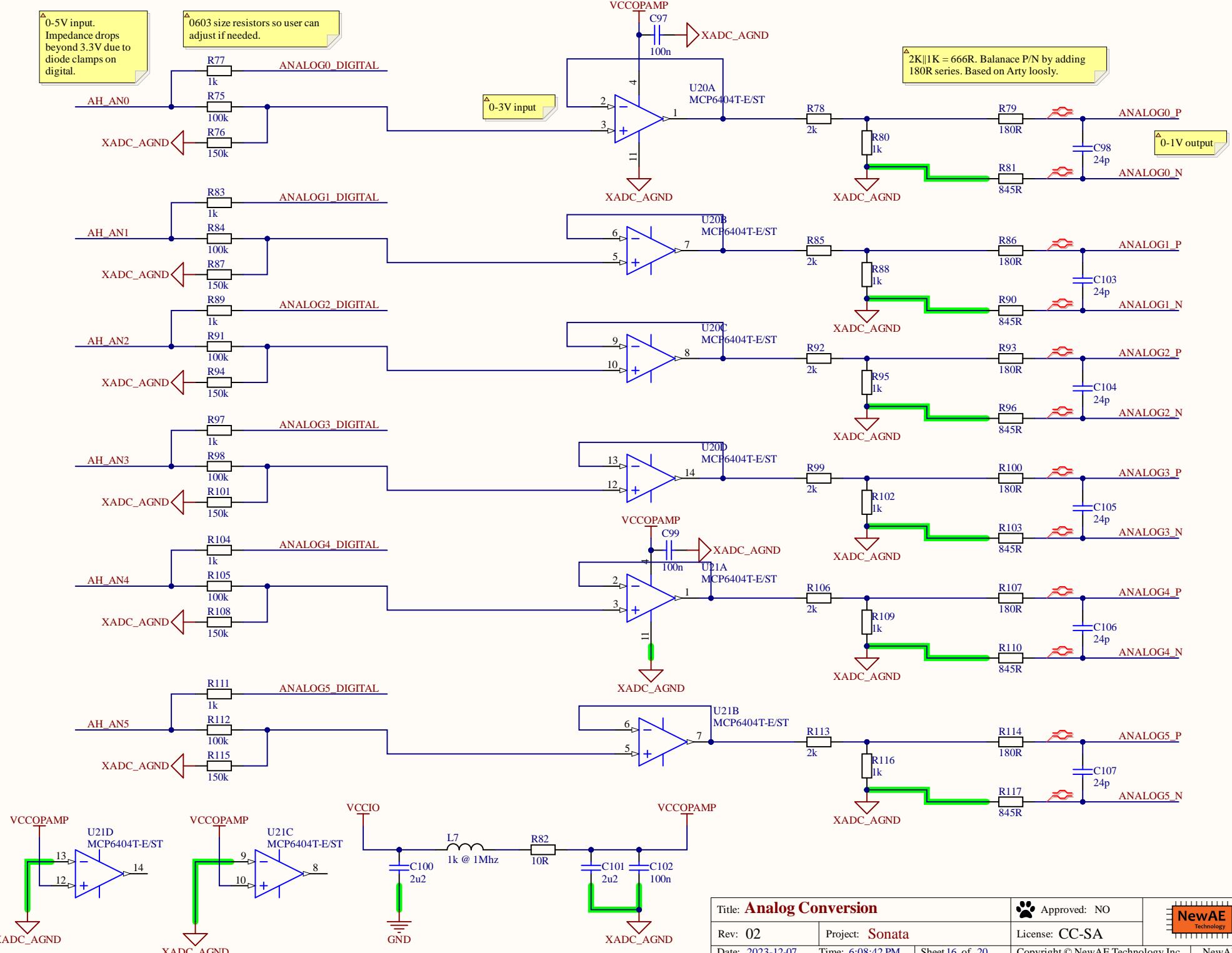
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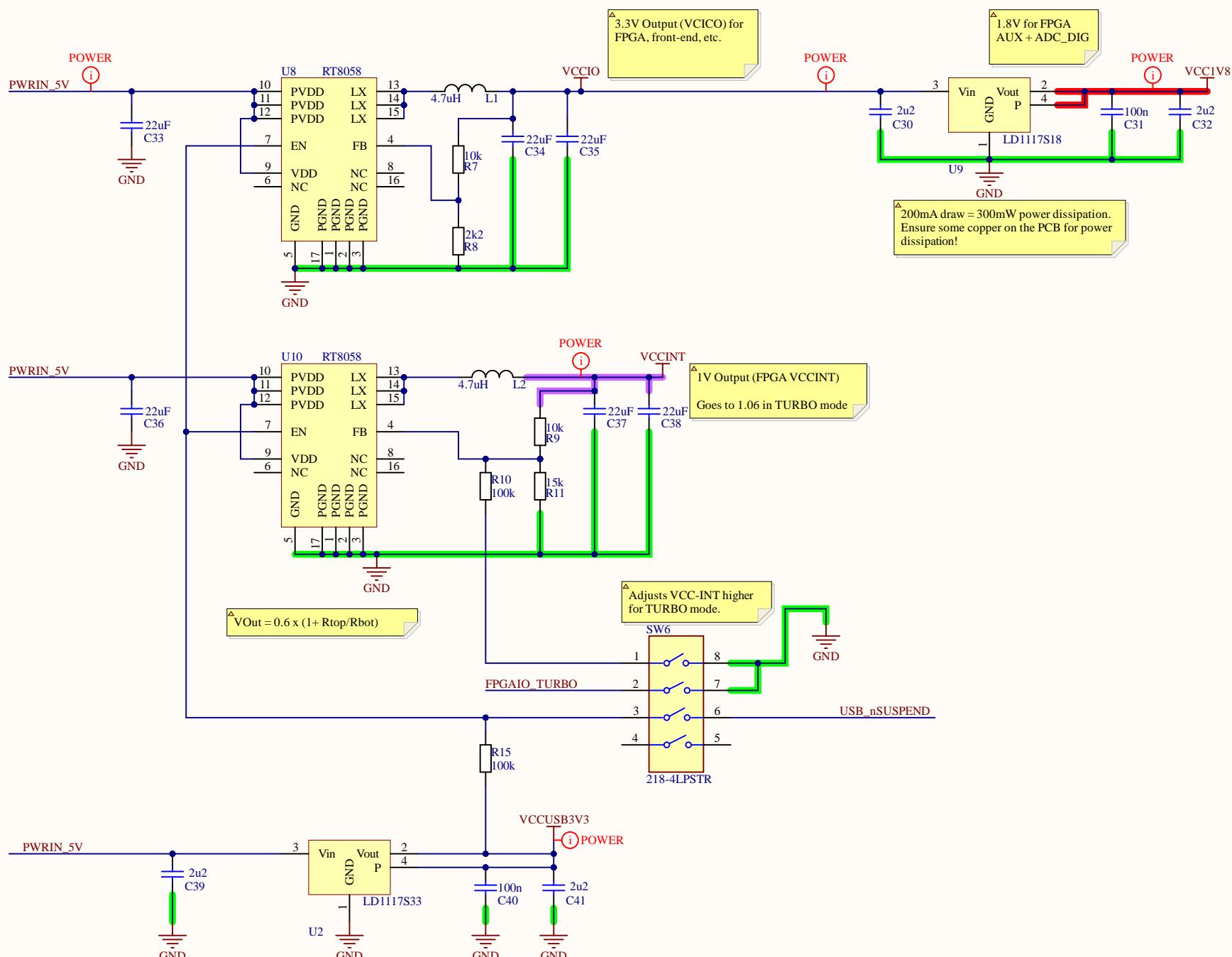


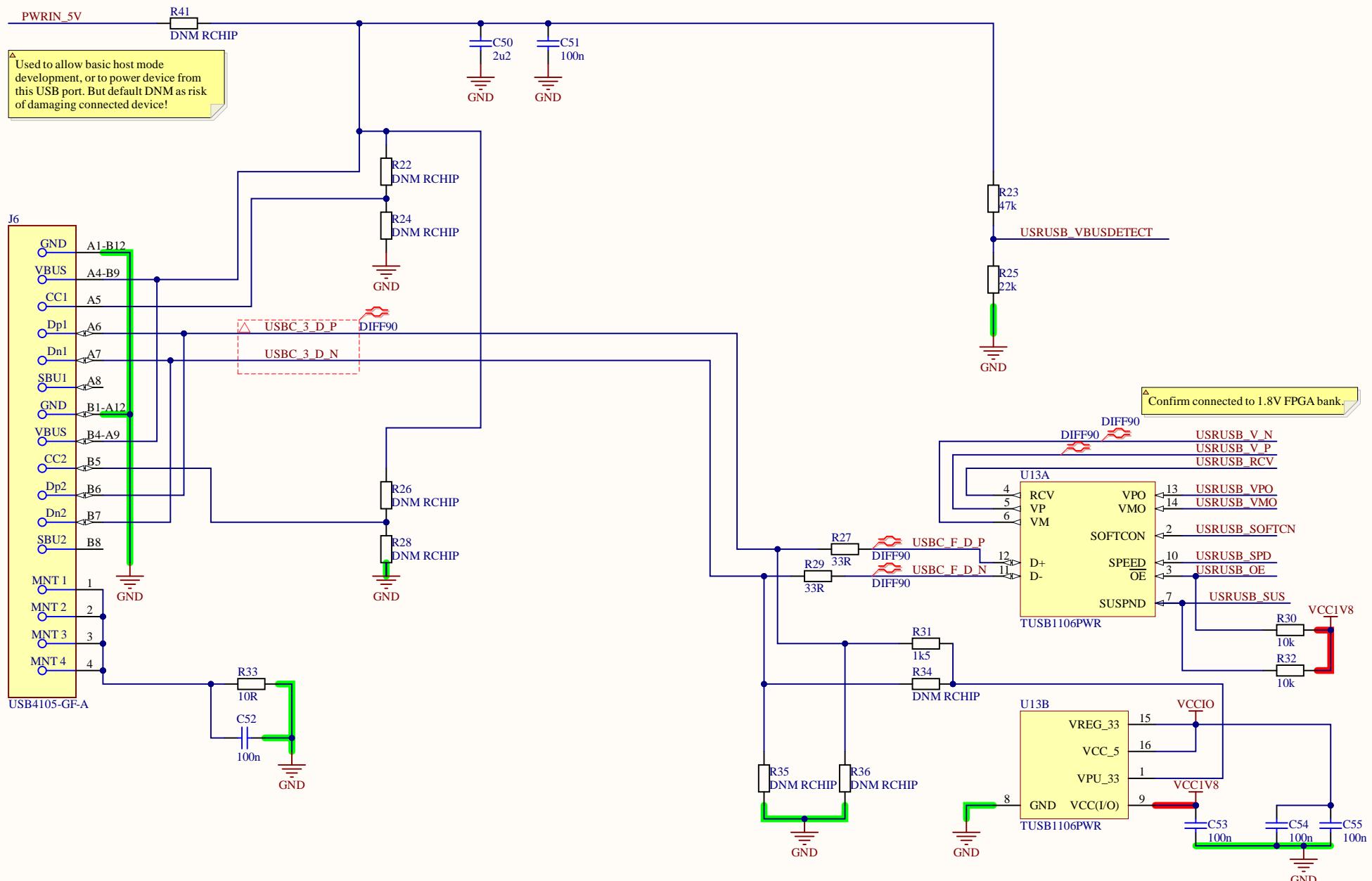


Title: FPGA Analog + 1.8V Bank		 Approved: NO	
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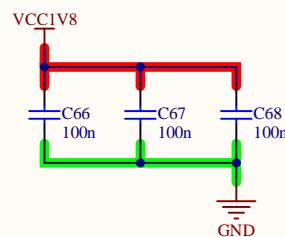
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File: sb-sonata-analoginput.SchDoc			



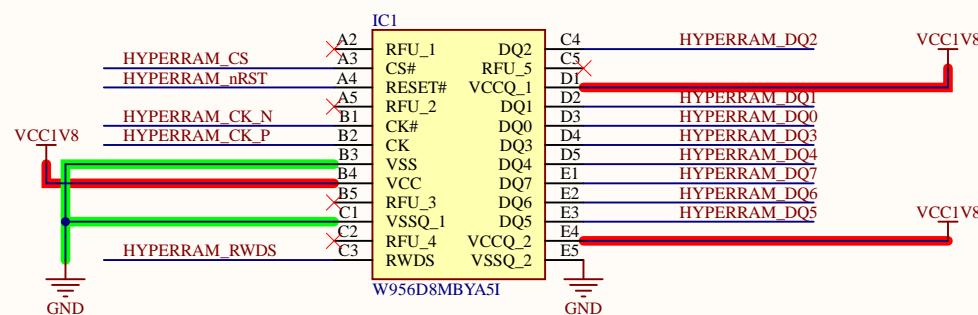


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A



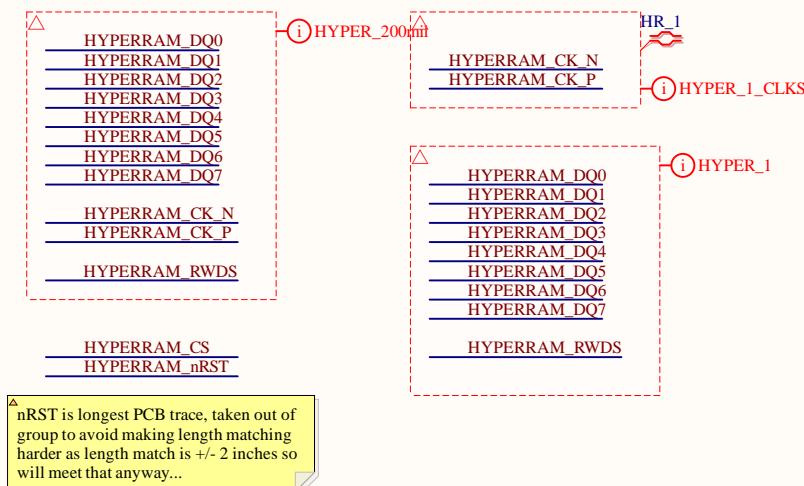
B



C

Table 5 Length matching

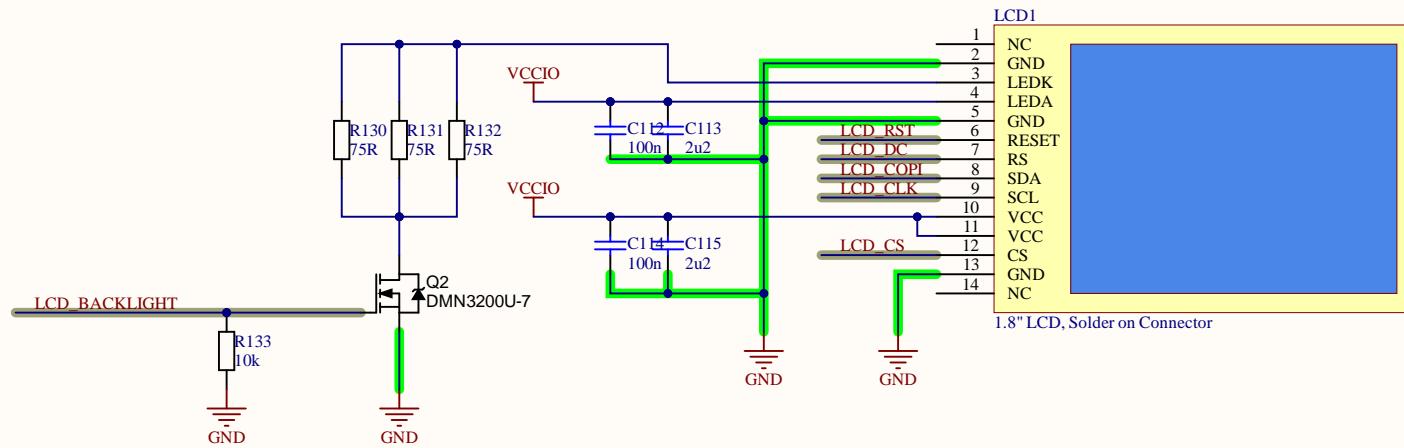
Signal group	Length matching tolerance
	200 MHz
CK to CK#	±10 mils
RWDS to DQ[7:0]	±15 mils
RWDS1 to DQ[15:8] ¹	±15 mils
DQx[7:0] to DQy [7:0]	±30 mils
DQx[15:8] to DQy [15:8] ¹	
CK/CK# to DQ[7:0]	±200 mils
CK/CK# to DQ[15:0] ¹	
CK/CK# to CS#	±1500 mils
CK/CK# to RWDS	±1500 mils
RESET# to RST0# to CS#	±2000 mils



D

A

A



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