Lecture-6

Memory Organization

In general, an N x m memory chip can store N words, each word of m-bits. To access N words, 'k' address lines are required representing k-bit address A_{k-1}……A_0 and m-data lines representing m-bit data D_{m-1}….D_0. The symbolic diagram of a static memory is shown below:

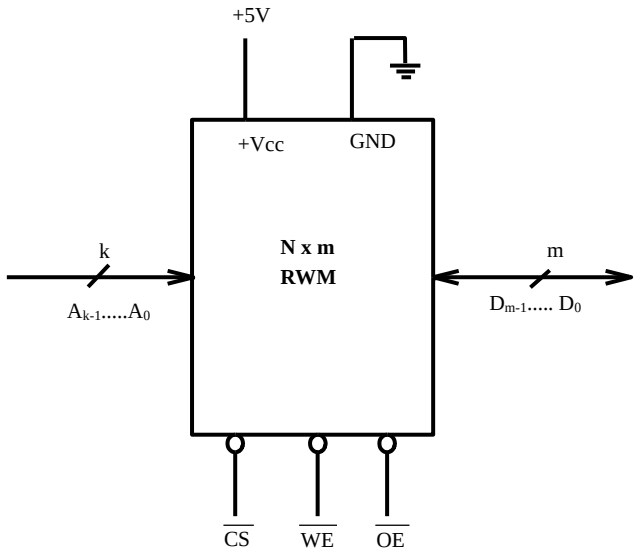

Fig.2.13 Schematic Diagram of N x m Read Write Memory

The chip has following three control inputs:

a. $\overline{CS}$ = Chip select or chip enable signal

b. $\overline{OE}$ = output enable signal

c. $\overline{WE}$ = write enable signal

All the control signals are active LOW, in general. These are representative signal. These signals may be active LOW or HIGH for other memory chips. When the chip is selected then only read/write

operation can be performed from the addressed memory location. For memory READ operation, first address is placed on address lines and then make $\overline{OE}$ is made LOW, the output is available provided $\overline{CS}$ is LOW. Under memory WRITE operation, first the address is place on address lines and data is place on data lines and $\overline{WE}$ is made LOW. The data is written into addressed memory location provided $\overline{CS}$ is LOW.

The symbolic diagram of N x m Read Only Memory (ROM) is shown below:

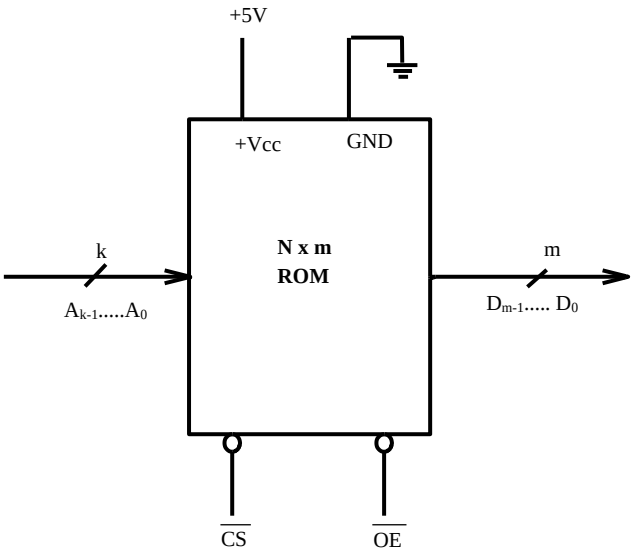

Fig.2.14 Schematic Diagram of N x m Read Only Memory

The chip is identical to RWM except that user cannot write any data into it. Therefore, the chip has two control signals- chip selection signal and output enable signal.

Two Level Decoding:

As discussed in previous lecture, the address put on address lines is decoded internally using decoder to select an internal register for memory read and write operation. This method of selection of an internal register is called linear selection. Conceptually the memory can be considered as words organized in the form of an array. The memory array in such a organization has a column length equal to the number of words, W, and a row length equal to the number of bits per word, B as shown in fig.2.15.

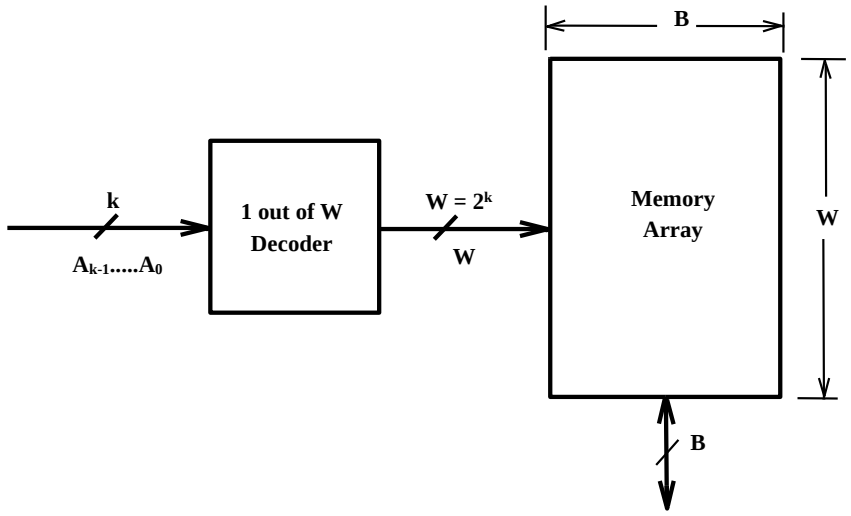

Fig.2.15 Schematic Diagram of Memory Organization using Linear Selection

The selection of a word requires a decoder, 1-out-of-W; a decoder with a mutually exclusive output for each word in the memory, as discussed earlier. The address inputs to the decoder select one, and only one, of the decoder's output- thus selecting one word in the memory array. If the size of the memory increases, the linear selection method requires a large size decoder, which increases the cost of chip.

Address decoder size is substantially reduced by organizing the memory array and the word selection logic to allow two-level decoding.

In two-level decoding, one level corresponds to a physical word and one to a logical word. A physical word consists of the number of bits in a row of the memory array. A logical word consists of the number of bits of a physical word that are selected and sent to the output at one time. The physical word is formed by combining the bits of multiple words. For example, if 256 x 4 memory is to be built then there are 256 words of 4 bits each. If these 256 words are stored in an array then a decoder of size 1 out of 256 or 8 lines x 256 lines decoder is required. Instead, if 4 words are combined to form a physical word, then only 64 physical words are to be stored in an array. Each physical word consists of 16 bits, 4-bits of each of the 4 words combined.

Two-level decoding requires two decoders: a row decoder that selects a physical word and a column decoder that selects the logical word from the selected physical word. In fact, the k bit address is divided in to two parts: one part of the address is decoded in row decoder, similar to linear selection method, and selects one physical word. The other part of the address is used in column decoder to select the desired bits of the selected physical word to form the logical word. In fact, the column decoder consists of multiple multiplexers that select one logical word from the selected physical word. In the above example of 256 x 8 memory, 6 address lines are used to select one physical word using 6 lines to 64 lines decoder. The remaining 2 address lines are used to select 4-bits of the logical word using eight 4 x1 multiplexers.

In other words, a physical word is divided into S segments (logical words); the row decoder is 1-out-of-P decoder, where P is the number of physical words and equal to W/S; and the column decoder consists of B, 1-out-of-S multiplexers. This is shown in fig.2.16.

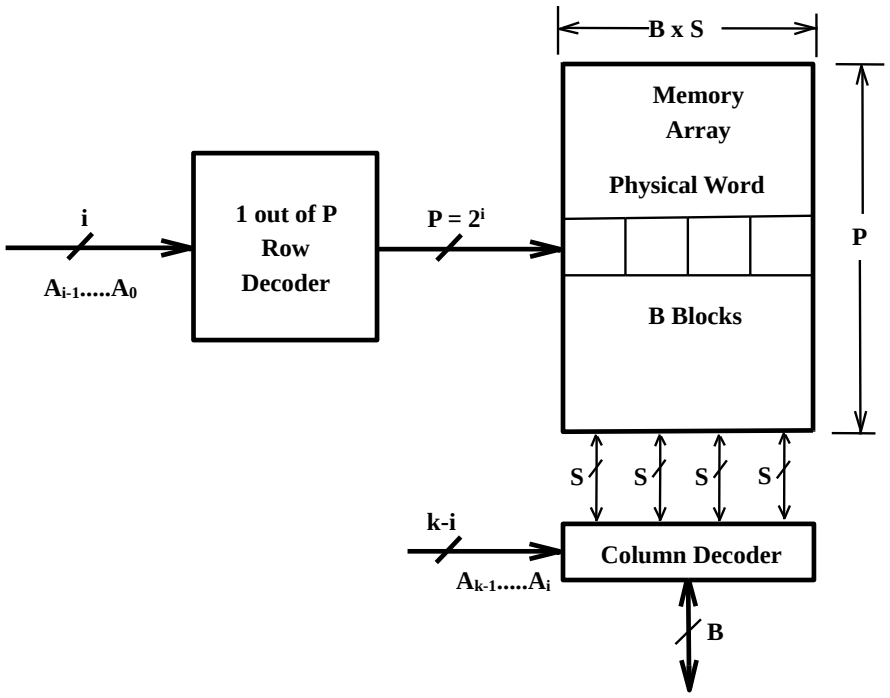

Fig.2.16 Schematic Diagram of Memory Organization using Two-level Decoding

The block diagram of 2k x 8 memory organized with two-level decoding is shown in fig.2.17. The memory array is 128 x 128 bits; thus it contains 128 physical words. A physical word is selected using the seven address bits A_6-A_0. Thus the row decoder is 1-out-of-128 decoder. Segmentation is done by dividing the physical word into eight blocks of 16 bits each. The first block contains the most significant bits of each of the 16 logical words; the next block contains the next most significant bits of each of the 16 logical words etc. The last block contains the least significant bits of each of the 16 logical words. Thus each physical word is segmented into 16 logical words, and therefore, S equals 16. Column decoding requires eight 1-out-of-16 multiplexers to provide an 8-bit logical word. The remaining 4 address bits A_{10}-A_7 are used to select one bit from each of the multiplexers to form the logical word.

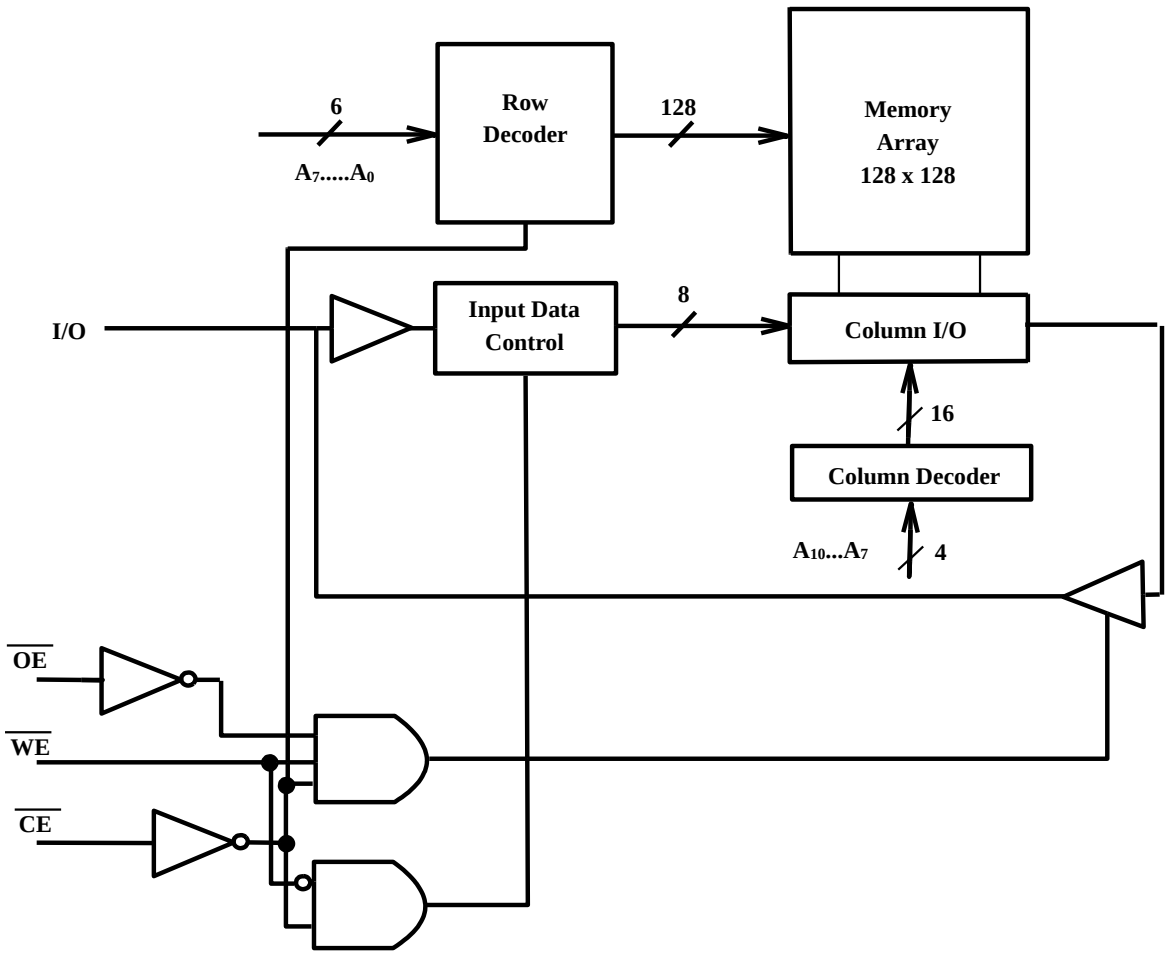

Fig.2.17 Schematic Diagram of 6116 2K x 8 SRAM using Two-level Decoding