Lecture-5

m- Bit register:

Let us see how a memory is developed and how the data can be written into and read from it. As discussed in previous lecture, memory is storage device and it is used to store both instructions and data. The smallest unit of information a digital system can store is a binary digit (Bit) which has a logic value of '0' and '1'. A bit of data is stored in a flip-flop. It is a general memory cell and has two states in which it can remain indefinitely as long as power is not interrupted. The output can be changed only if the input signals allow for it.

D flip-flop is the simplest flip-flop to store one bit of information. The input data (bit) is stored at the active edge of the clock. To store several bits of data simultaneously, the clock inputs of several D flip-flops are connected in parallel to form an m-bit register ('m' may be 4, 6 or 8) as shown in fig.2.7. Such registers store m-bits of data D_0 to D_{m-1} under the control of the clock and provide m-bits of data output Q_0 to Q_{m-1}.

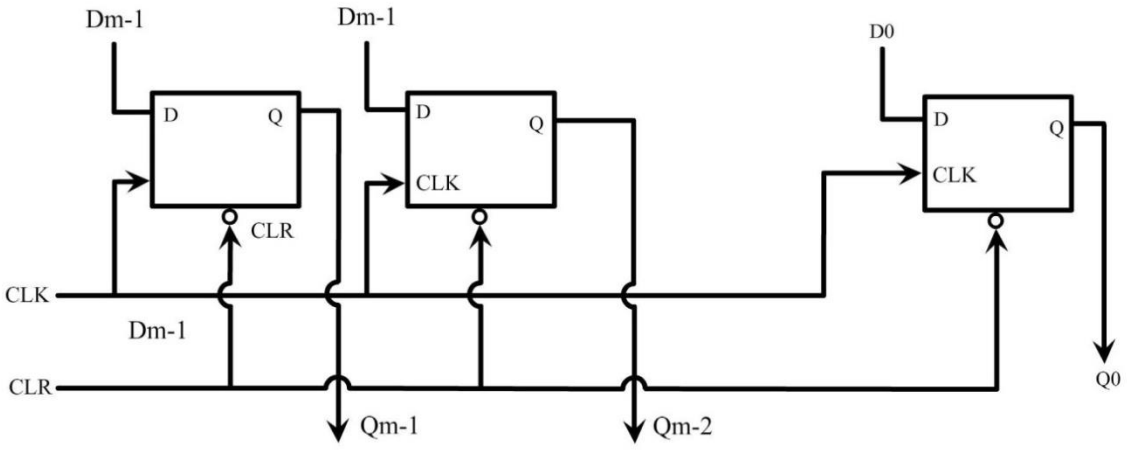

Fig.2.7 Basic Structure of m-bit Register

The act of storing data in a register is a write operation. Determining the value of the content of a register is a read operation. The m-bits of data stored in a register make up a word. A word is simply a number of contiguous bits operated upon or considered by the hardware of microprocessor as a group. The number of bits in the word ‘m’ is a word length. The ‘m’ inputs to the register are provided by an m-bit input data bus and the ‘m’ outputs by an m-bit output data bus. A bus is a number of signal lines grouped together because of similarity of function, which connect two or more systems or subsystem. 8-bit registers are often called octal registers.

Several equal length registers can be incorporated in a single IC and share a common set of inputs, a common set of inputs and a single clock such a circuit is referred to as a memory. Each register occupies a distinct location, which has a unique numerical address. Thus, memory can be thought of as a collection of addressable registers. Logic is necessary to decode address inputs to ensure that only a single register outputs its contents when data is being read from the memory, and only a single register stores the data in it when the data is being written into the memory.

Development of Memory Chip

Let us consider a memory of 16 words, each of 8 bits is to be developed. 16 words can be stored in 16 memory locations, each having a unique address and each location being capable of containing 8 bits of data. To address 16 memory locations, 16 unique

addresses are required which need 4 address lines $A_3A_2A_1A_0$. The address varies from $(0000)_2$ to $(1111)_2$.

To set up this memory system using ICs, 16 8-bit D-flip-flop registers are required. The 74LS374s are octal D flip flops with three state of outputs. To store data in them, 8 bits of data are put on the D_0 to D_7 data inputs via the data bus. Then the low to high transition on the clock input will cause the 8-bit data D_0 to D_7 to be latched into each flip-flop. The stored value in the D-flip-flops is observed at the outputs Q_0 to Q_7 by making the output enable $\overline{OE}$ pin low. Fig.2.8 shows the circuit used to implement the memory system.

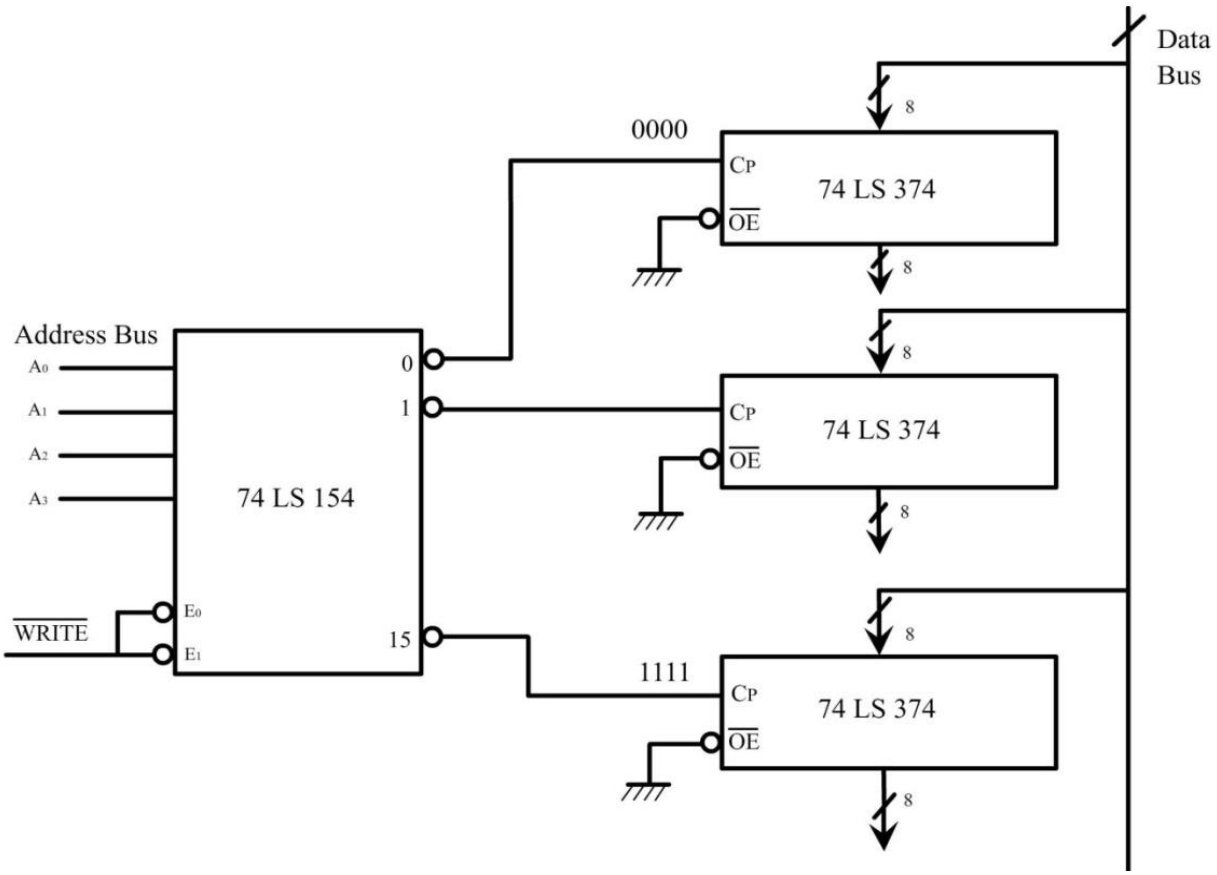

Fig.2.8 Development of 16x8 Memory for Storing Data

To select the appropriate memory location, a 4 line to16 line decoder can be used to decode the 4-bit location address to select the appropriate data register (1 out of 16) for read or write operation. IC 74LS154 is a 4-line to 16-line decoder, which decodes the address put on its input lines and outputs a low pulse on one of the output lines when the $\overline{\text{WRITE}}$ signal is pulsed low to enable the decoder. The $\overline{\text{WRITE}}$ signal is connected to both the enable inputs of the decoder. When the $\overline{\text{WRITE}}$ signal is active, one of the outputs of the decoder will be low and when this signal becomes inactive, all the outputs become high. This internally produces one rising edge at the clock input of one of the internal registers and the data available at the input data bus will be written into the selected register. The timing of setting up the address bus, data bus and pulsing the $\overline{\text{WRITE}}$ signal is critical. The standard timing diagram is shown in fig.2.9 to illustrate timing parameters for bus driven devices.

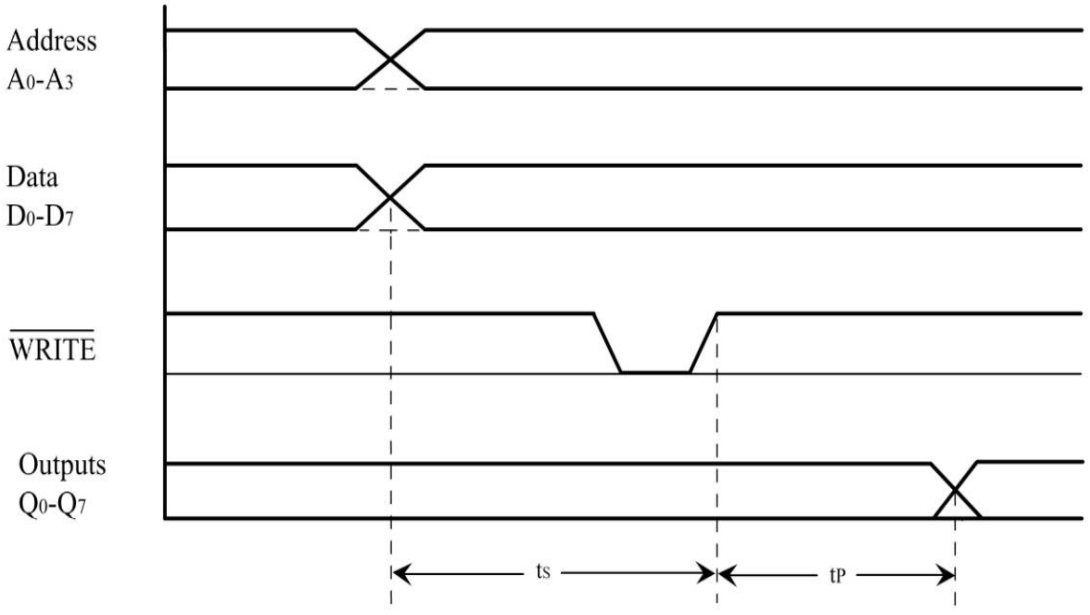

Fig.2.9 Timing Diagram for Memory Write Operation

Rather than showing all address lines and all data lines, they are grouped and ‘X’ is used to show where any or all of the lines are allowed to change digital levels.

The address and the data lines must be set up some time (t_s) before the low to high edge of $\overline{\text{WRITE}}$. In other words the address and the data lines must be valid some period of time (t_s) before the low to high edge of $\overline{\text{WRITE}}$ in order for the 74LS374 to interpret them correctly.

When the $\overline{\text{WRITE}}$ line is pulsed, the decoder outputs a low pulse on one of its 16 outputs which clocks the appropriate memory location to receive data from the data bus. After the propagation delay, (t_p) the data output at Q_0 to Q_7 will be the new data just entered into the D flip-flop. Then the t_p will include the propagation delay of decoder and of the D flip-flop.

In the figure the outputs of all the registers are continuously enabled so that their Q outputs are always active. To reduce the number of output lines the 8 outputs Q_0 to Q_7 of all 16 registers are combined to make output data bus as shown in fig.2.10. The $\overline{\text{OE}}$ enables of the 16 memory locations have to be individually selected at the appropriate time to avoid a conflict on the output data bus, called bus contention. Bus contention occurs when two or more devices are trying to send their digital levels to the shared data bus at the same time. To individually select the output of one of the registers, the grounds on the $\overline{\text{OE}}$ inputs would be removed and instead be connected to the outputs of another 1of 16 decoder 74LS154.

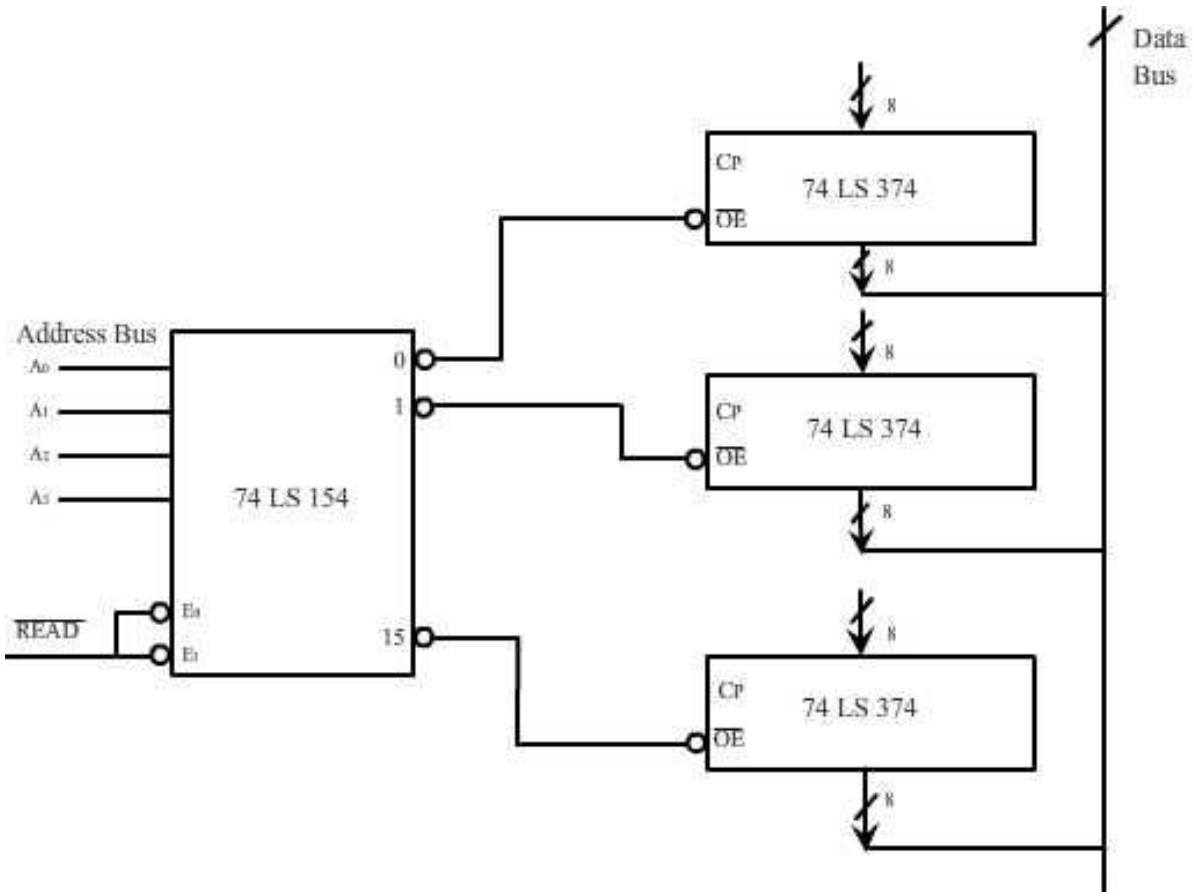

Fig.2.10 Development of 16 x 8 memory for Reading Store Data

Similar to write operation, decoder decodes the 4-bit address put on its input lines and produces a low pulse at one of its outputs when enabled. However, the decoder is now enabled by $\overline{\text{READ}}$ signal instead of $\overline{\text{WRITE}}$ signal and the $\overline{\text{READ}}$ signal is connected to both the enable inputs of the decoder. During the period $\overline{\text{READ}}$ signal is low, the data from the selected register will be available at the output data bus. When $\overline{\text{READ}}$ signal becomes high, the output data bus again goes into high-Z state. This is shown in fig.2.11.

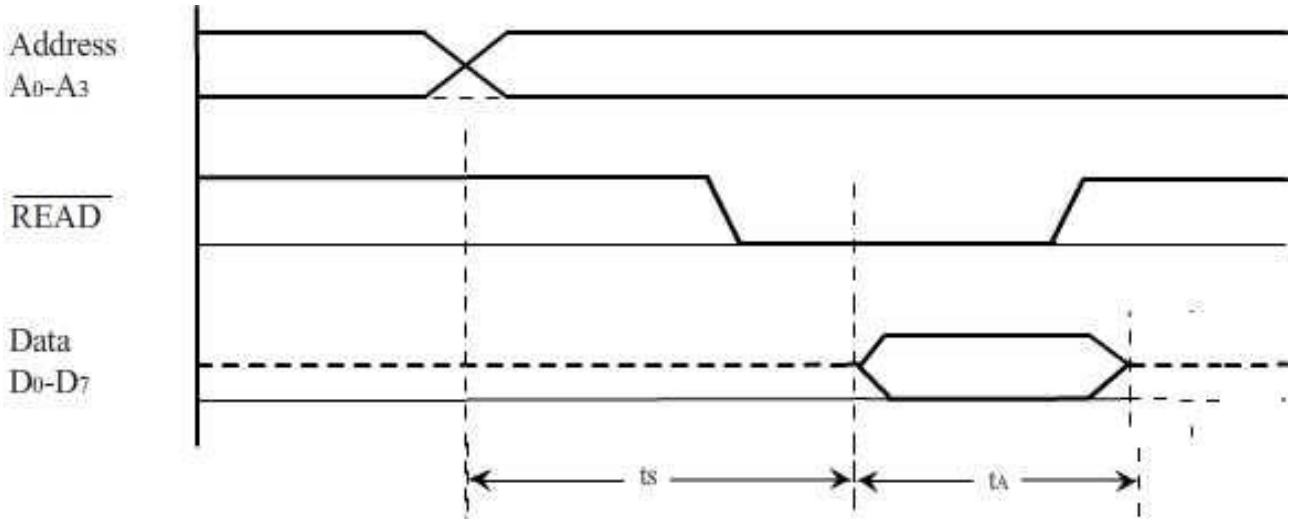

Fig.2.11 Timing Diagram for Memory Read Operation

Instead of having separate input and output data bus, these buses are internally combined and a common bidirectional data bus is formed. It is possible because at any instant either the data is written into the selected memory register (location) or the data is read from the selected memory register. For write operation $\overline{\text{WRITE}}$ signal is activated and for read operation $\overline{\text{READ}}$ signal is made active. The address lines are common to both the decoders. In a processor based system, there are multiple memory chips and at any time only one chip is selected for read or write operation. To provide this feature, the two enable inputs of the decoders are separated and one enable inputs of both the decoders are made common and it is referred to as $\overline{\text{CE}}$ chip enable input. The complete schematic diagram of the read-write memory chip is shown in fig.2.12. Commercially available memory chips combine all the decoding and the storage elements in a single package.

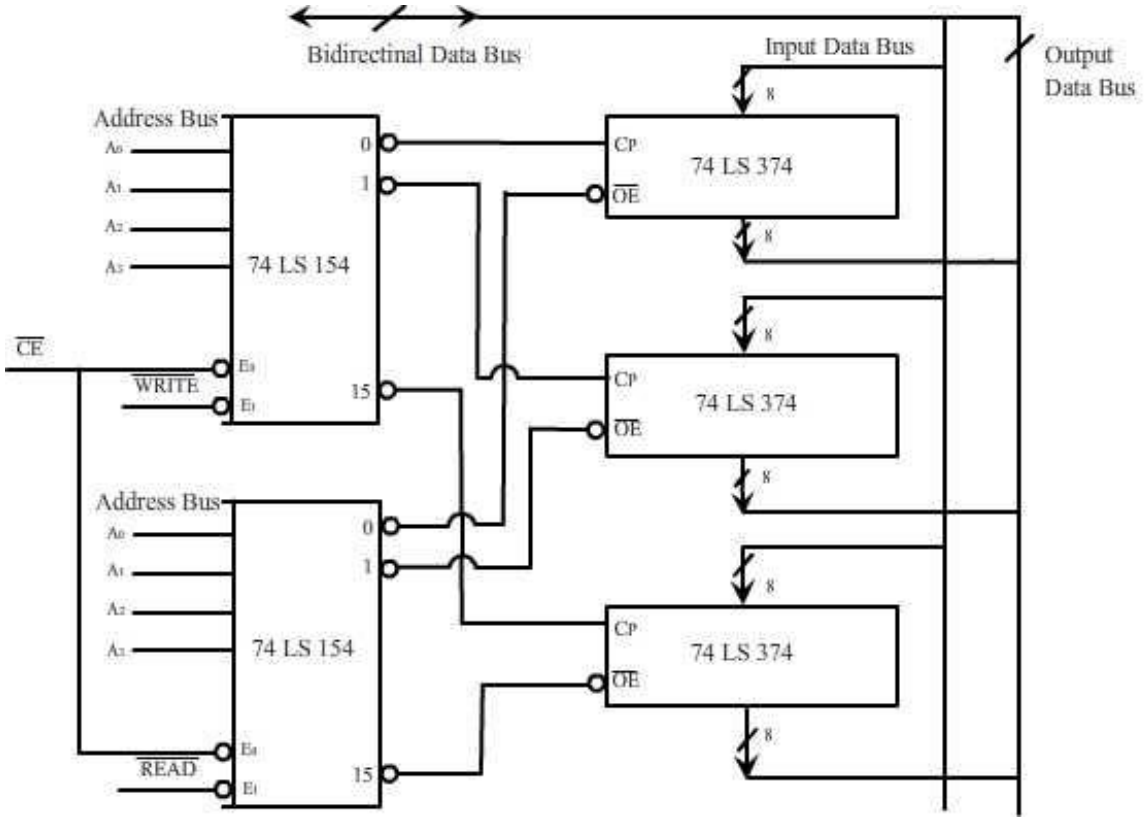

Fig.2.12 Schematic Diagram of 16 x 8 Read Write Memory

To write a data in a particular register, the address of the register is put on the address bus, the data is put on the bidirectional data bus and the $\overline{\text{WRITE}}$ signal is made active low alongwith $\overline{\text{CE}}$ signal. The data is available on output data bus also but it does not affect the registers as the output buffer of each register is disabled. On the rising edge of $\overline{\text{WRITE}}$ signal the data is written to selected memory location as discussed earlier. Similarly, to read the data from any register the address of the register is put on the address lines and $\overline{\text{READ}}$ signal is made active alongwith $\overline{\text{CE}}$ signal. The selected internal register puts the data on the data bus. It will also be available on input data bus but it does not affect the stored data as no clock will be generated. It is for the user to ensure that at any time, either the data is to be stored or the data is to be read.