HW2 - Numair Ahmed

3. analog input, comparator input, a change in notification input, digital IO. Not 5V tolerant

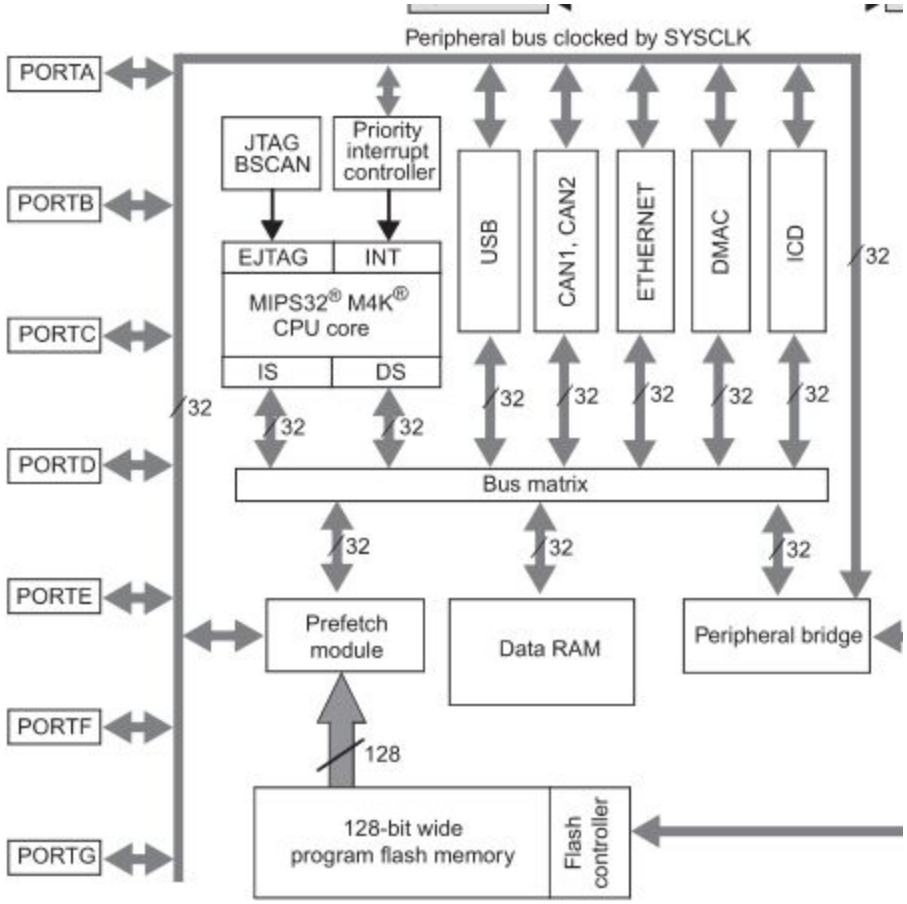
4.

Virtual Addr (BF88_)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—

5.

6. SYSCLK: clocks the CPU at max of 80MHz, down to 0Hz. Higher frequency means more calculations but more power usage.
PBCLK: clock used by many peripherals and is set to SYSCLK's frequency divided by 1,2,3,4, or 8.
PORTA to PORTG: PORTA is analog, PORTB to PORTG are digital I/O
Timer1 to TImer5: counts the number of pulses of a signal. If the pulses occur at a regular frequency, the count can be a customized timer.
10-bit ADC: analog to digital converter for converting a 0-5V analog signal into a 0 or 1 digital bit.
PWM OCI-5: generate continuous pulse signal to control motors
RAM and Program Flash Memory: your program is stored in flash memory and temporary data is stored in RAM
Prefetch Cache Module: stores recently executed program instructions, which are likely to be executed again soon.

7. the image below shows which peripherals are not clocked by PBCLK, but by SYSCLK instead.



8.

9. total 32 bytes on two cache lines. Snippet from datasheet shown below

- Two cache lines with address mask to hold repeated instructions

10. the flash memory runs slower than the CPU's 80MHz frequency. So the prefetch cache listens to flash to store the next steps in the instructions coming from flash, before the CPU asks for it.

11.

12.

13. **(a)** you set bit 13-12 to value 01 as shown below

REGISTER 29-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits
11 = PBCLK is SYSCLK divided by 8
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1

(b) bit 23 as shown below

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = The WDT is enabled and cannot be disabled by software
0 = The WDT is not enabled; it can be enabled in software

(c) to set the postscale time interval use bits 20-16 as shown:

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 14-12 are configuration bits for the primary oscilator and turn on the PLL module

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
110 = Internal Fast RC (FRC) Oscillator divided by 16
101 = Internal Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (POSC) with PLL module (XTPLL, HSPLL or ECPLL)
010 = Primary Oscillator (POSC) (XT, HS or EC)
001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
000 = Internal Fast RC (FRC) Oscillator